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(54) **CIRCUITS AND METHODS OF A
SELF-TIMED HIGH SPEED SRAM**

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(57) **ABSTRACT**

Circuits and methods for precisely self-timed SRAM
memory are disclosed to track the wordline and/or bitline/
bitline bar (BL/BLB) propagation delays. At least one refer-
ence cell can be placed near the far end of a driver to drive a
selected wordline or a reference wordline. When a wordline
and/or a reference wordline is turned on, the reference cell can
be selected not earlier than any selected SRAM cells and can
activate a reference bitline (RBL) not later than any selected
SRAM cells activating the BL or BLB. The activation of the
RBL can be used to trigger at least one sense amplifier. The
RBL can also be used to de-select wordline or reference
wordline after the sense amplifier operation is complete to
save power.

20 Claims, 10 Drawing Sheets
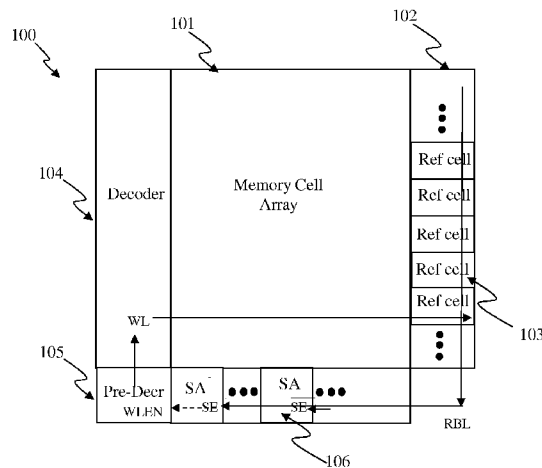
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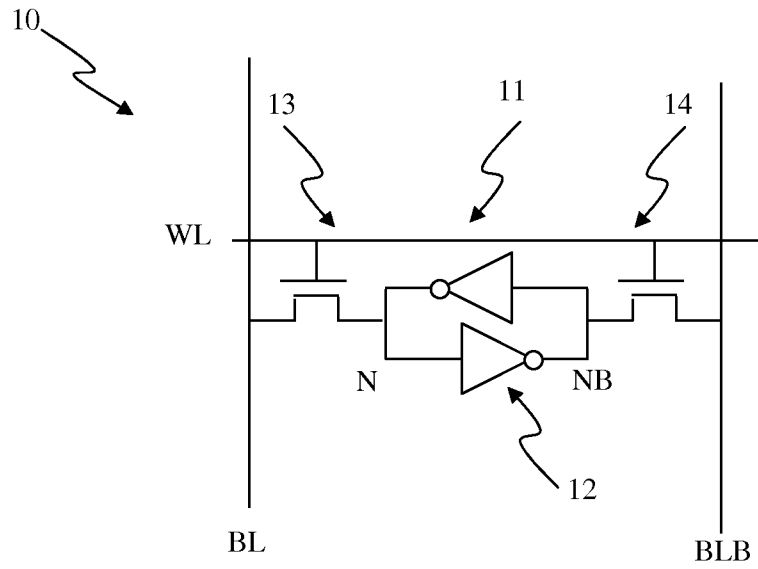
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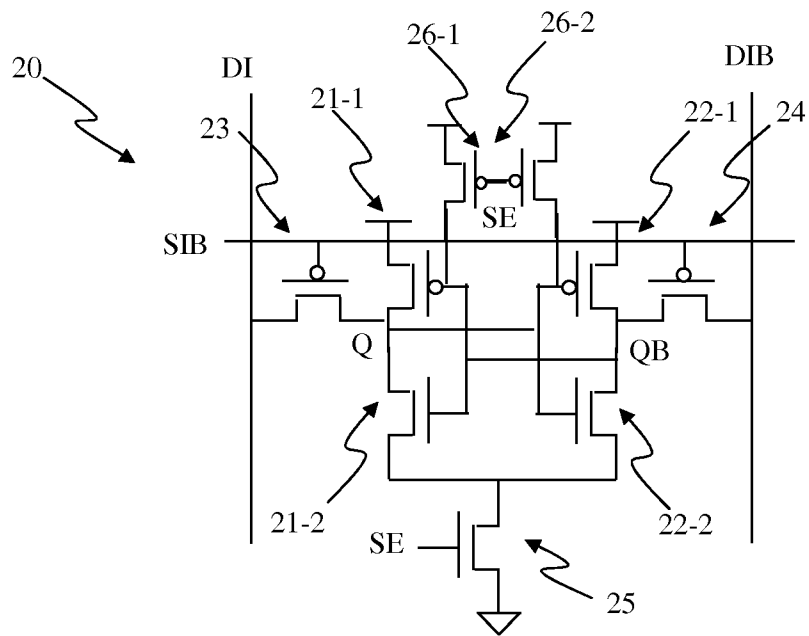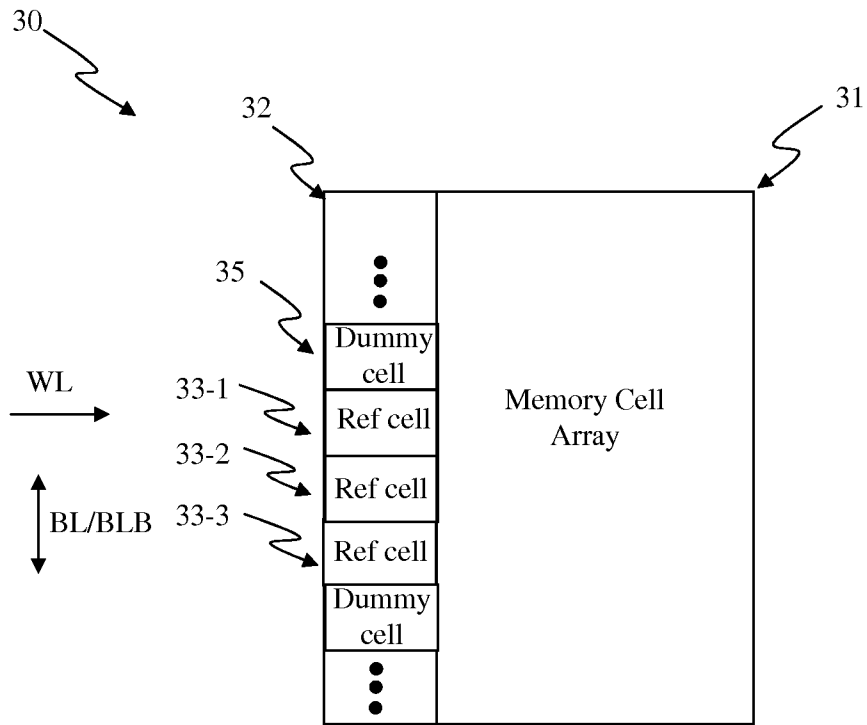13   11   14

WL

N   NB

12

BL   BLB

FIG. 1 (Prior Art)

20

DI   DIB

26-1   26-2

23   21-1   22-1   24

SIB

SE

Q   QB

21-2   SE   22-2

25

FIG. 2 (Prior Art)

30

32   31

35

WL   33-1

BL/BLB   33-2

            33-3

Dummy
cell

Ref cell

Ref cell

Ref cell

Dummy
cell

Memory Cell
Array

FIG. 3(a) (Prior Art)

40

43   41   44

N   NB

42

CLK — Delay

BLin   RBL

Delay
Cntrl

45
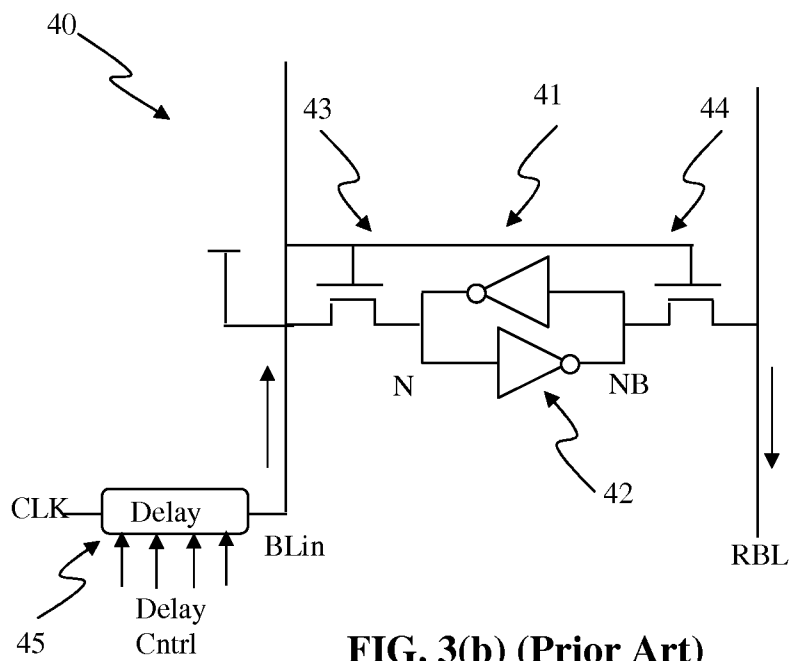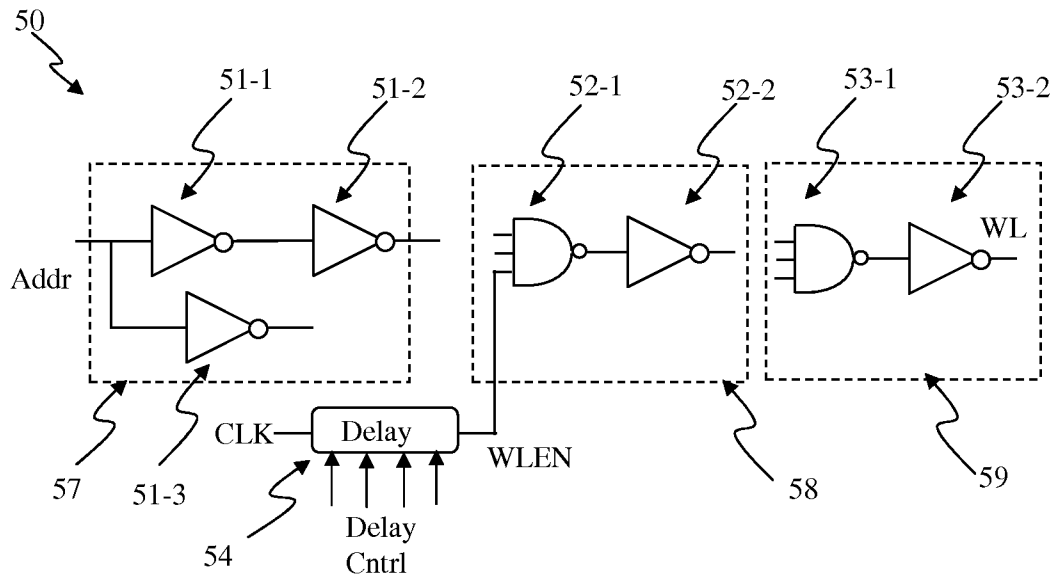
FIG. 3(b) (Prior Art)
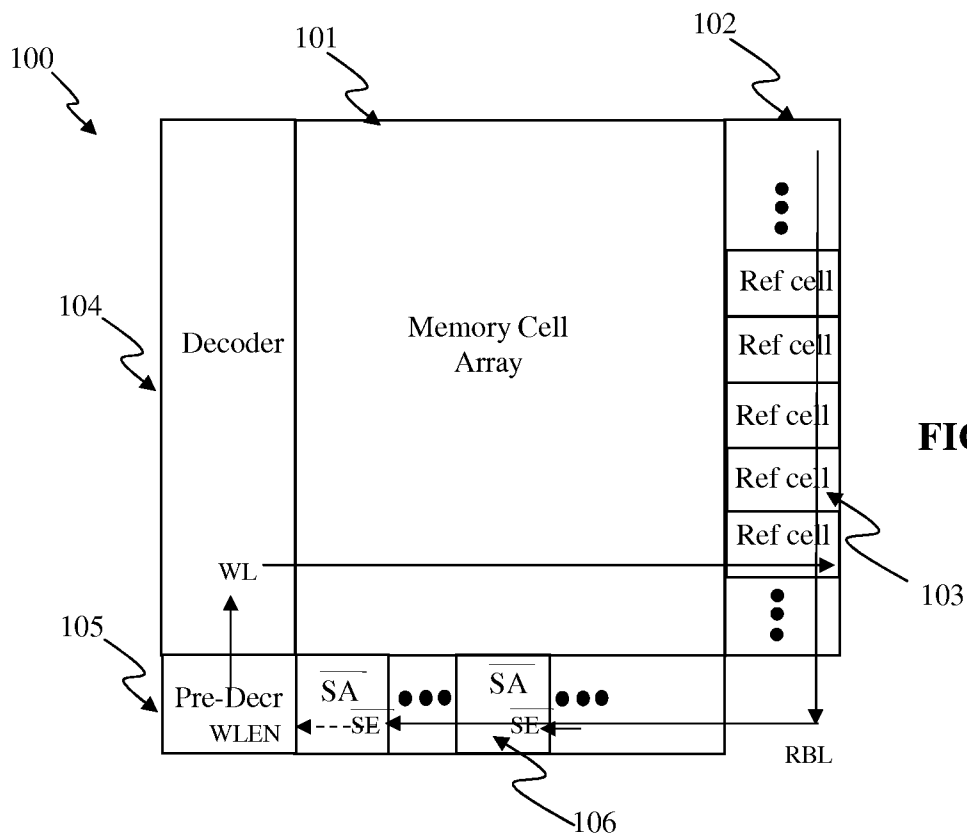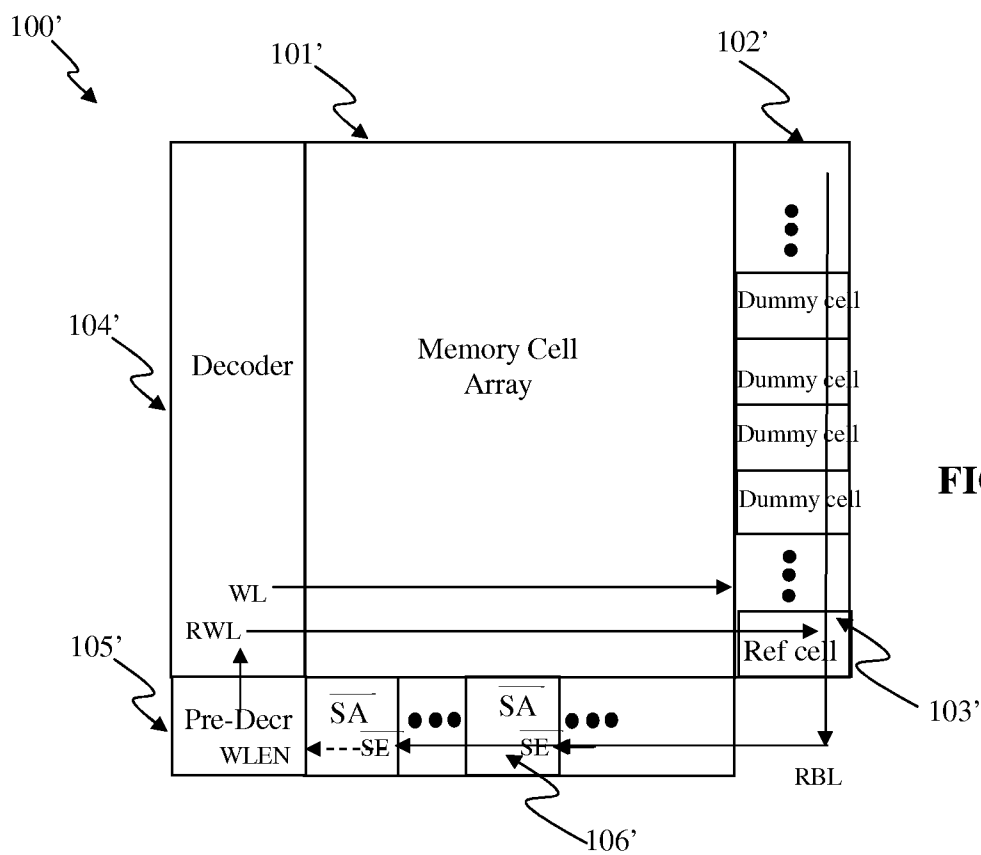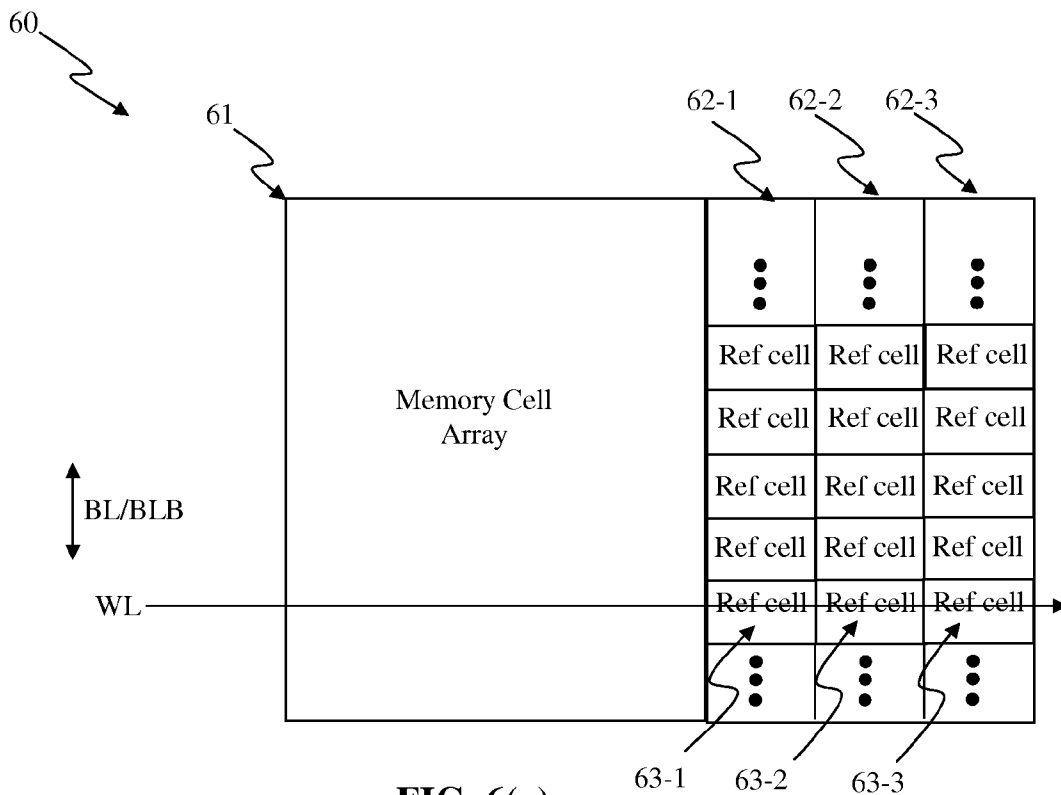
FIG. 4(a) (Prior Art)
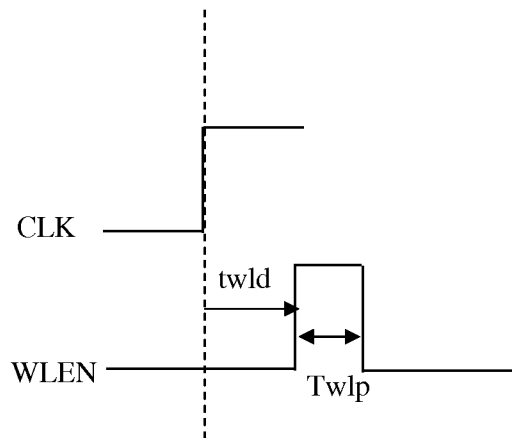
FIG. 4(b) (Prior Art)

FIG. 5(a)

FIG. 5(b)

60

61

62-1   62-2   62-3

Memory Cell Array

BL/BLB

WL

Ref cell	Ref cell	Ref cell
Ref cell	Ref cell	Ref cell
Ref cell	Ref cell	Ref cell
Ref cell	Ref cell	Ref cell
Ref cell	Ref cell	Ref cell

63-1   63-2   63-3

FIG. 6(a)

80

70-1   70-2   70-3   73   71   74

NB[1]   NB[2]

N[3]   NB[3]

72

BLin[1]   BLin[2]   BLin[3]   RBL
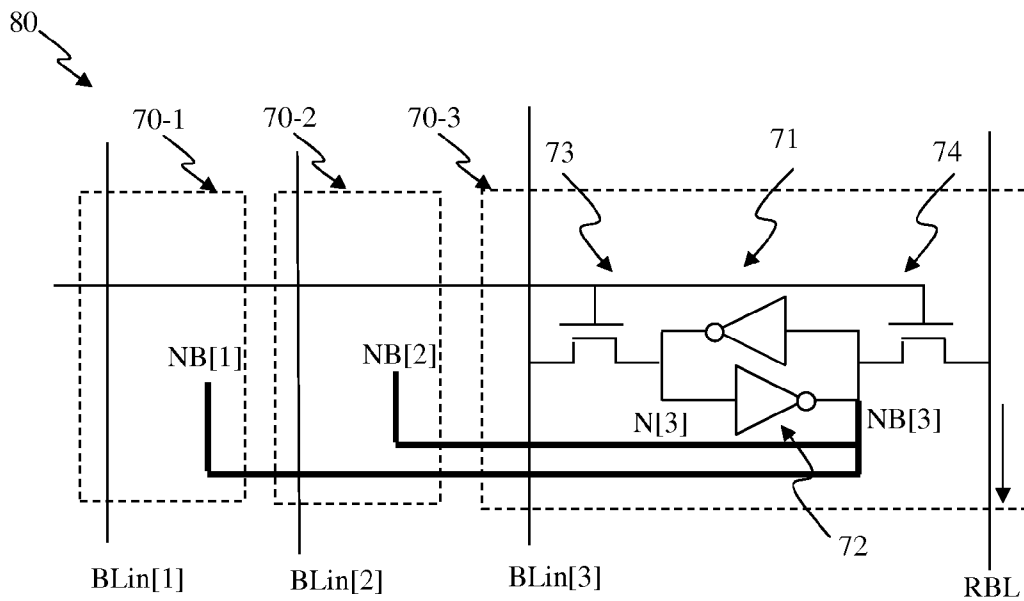
FIG. 6(b)

FIG. 6(c)

FIG. 6(d)

FIG. 7

FIG. 8

700

Select addresses for
memory access   710

Adjust delay line to
turn on WLEN   730

720

Turn on selected WL

Turn off BL pullup

740   750

Turn on ref cell and
activate RBL

760

RBL activates sense
amplfier   770

RBL turns off WLEN
and turns on BL pullup

Data from sense
amplifier output to I/O

790   799

Stop

FIG. 9

600

615

610

| CPU |

620

| I/O |

630

| Hard Disk Drive |

642

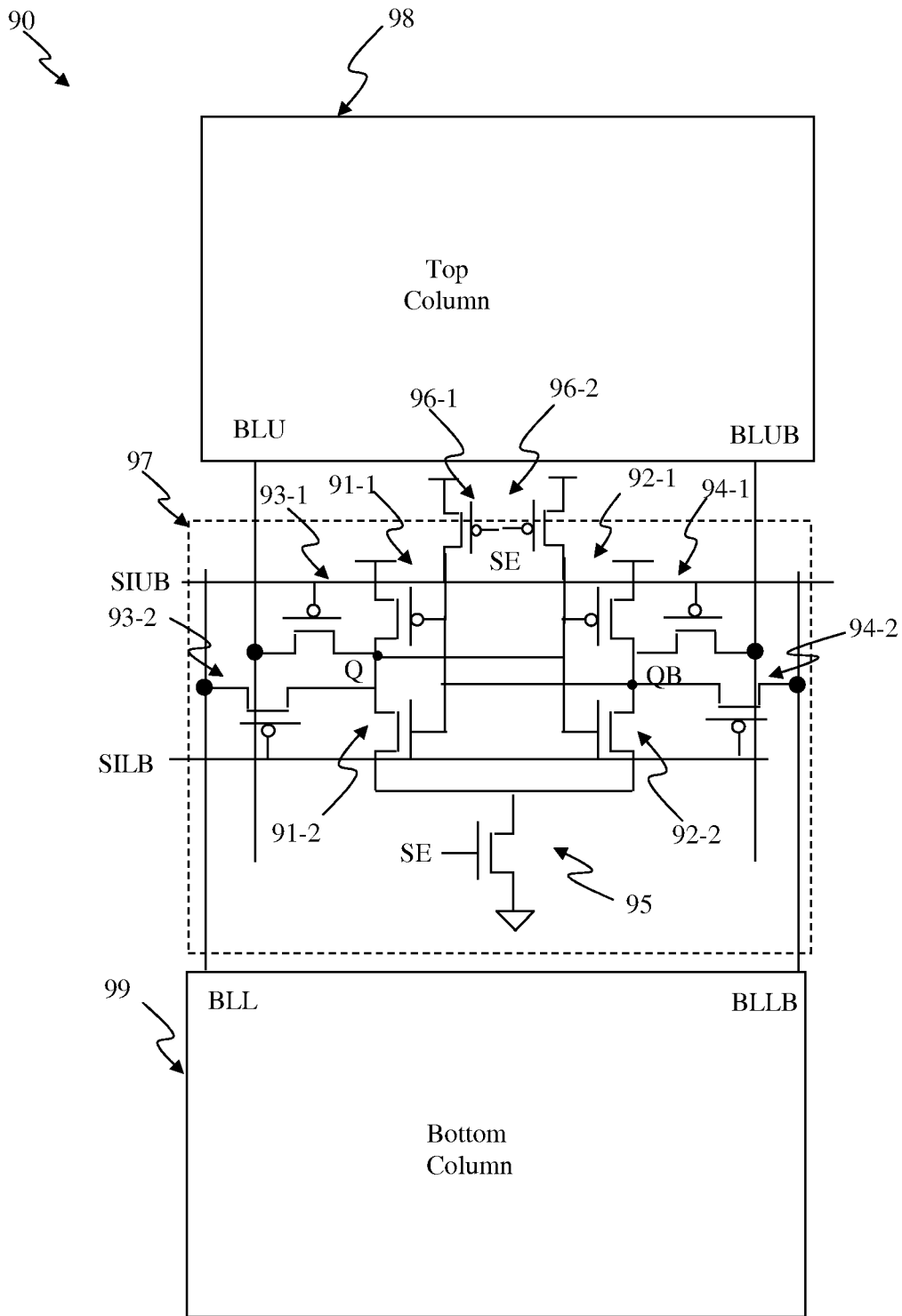644

640
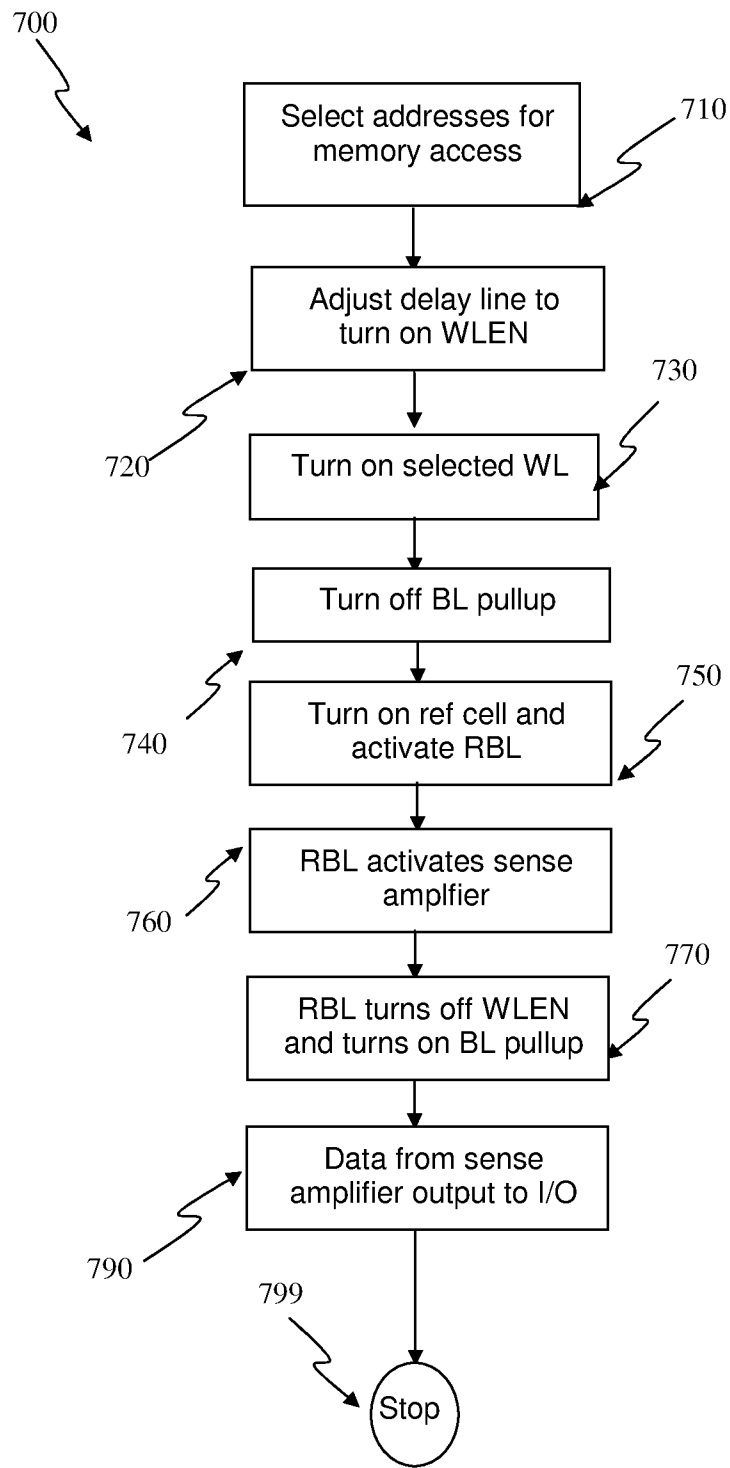
| Memory |

650

| CDROM |

| Other memory |

660

FIG. 10
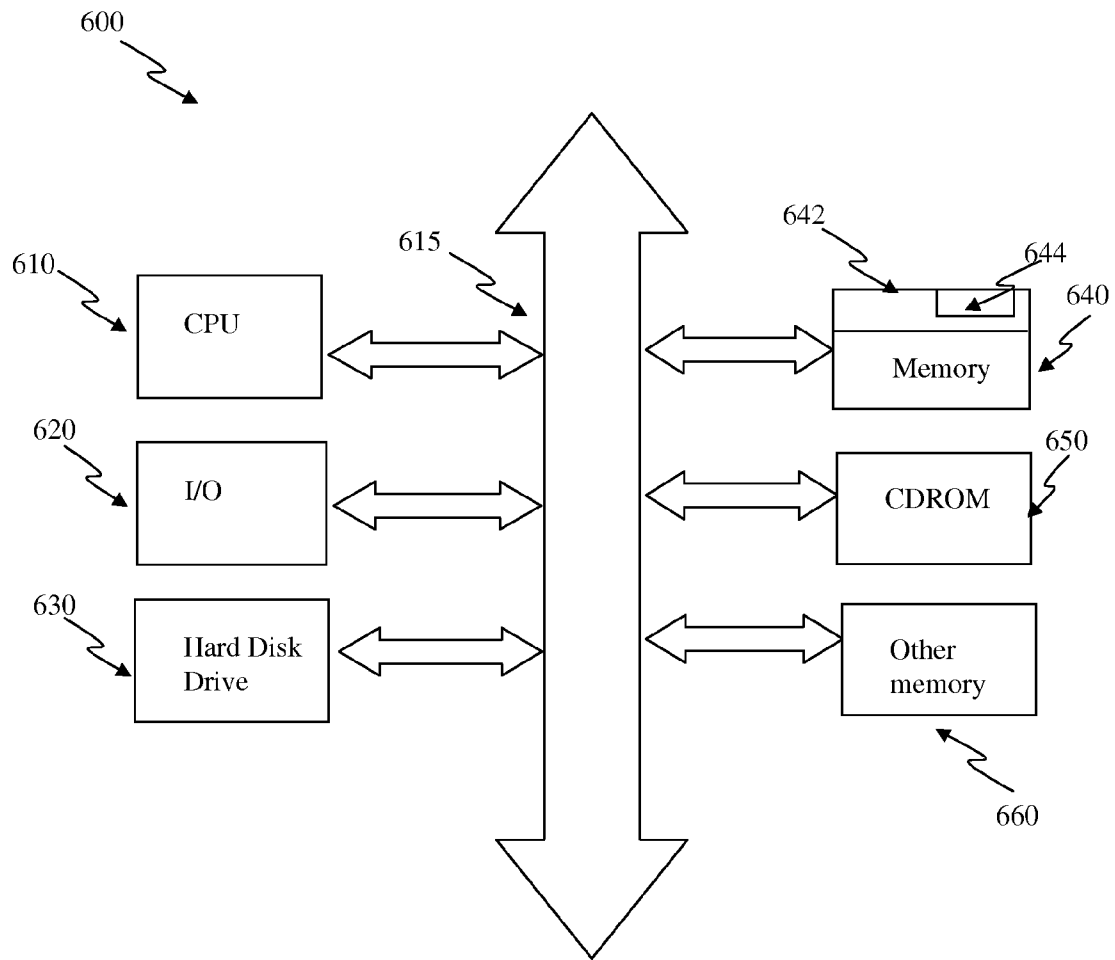
CIRCUITS AND METHODS OF A SELF-TIMED HIGH SPEED SRAM

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority of U.S. provisional Patent Application No. 61/708,040, filed on Sep. 30, 2012 and entitled "Circuits and Methods of A Self-Timed High Speed SRAM," which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to effective circuit, system designs, and methods of a self-timed SRAM for high speed and low power applications.

2. Description of the Related Art

Today's SRAM is commonly used as caches in ultra-high clock-rate CPU. A clock rate of 1 GHz CPU can be achieved easily in today's nanometer devices, such as 65 nm CMOS and beyond. For an SRAM to match such high clock rate, the access time needs to be less than 1 ns. In such short period of time, it would be very hard to generate control signals to keep propagation delay short while keeping inactive block idle to meet both high speed and low power. It is the objective of this invention to achieve high speed, low power, and small area to meet the very demanding SRAM requirements in today's applications.

A conventional SRAM memory cell is shown in FIG. 1. The cell 10 consists of a cross-coupled latch constructed from inverters 11 and 12, two pass transistors 13 and 14. The input of the inverter 11 NB is coupled to the output of the inverter 12, and the input of the invert 12 N is coupled to the output of the inverter 11. The sources of MOS 13 and 14 are coupled to the two nodes N and NB, respectively. The MOS 13 and 14 have their sources coupled to nodes N and NB, their gates coupled to a wordline (WL), their drains coupled to bitline (BL) and bitline bar (BLB), respectively. The SRAM cell can be organized as a two-dimensional array with all BLs and BLBs of the cells in the same columns coupled together in vertical direction and all wordlines of the cells in the same row coupled together in horizontal direction. The SRAM cell can be read by pre-charging the BL and BLB to a high voltage (i.e. VDD) and then let floating. The BL or BLB voltage can be pulled low by the inverter 11 or 12 in the cell, depending if the data stored is 0 or 1, when the WL is turned on. Similarly, the SRAM cell can be written with data 0 or 1, by pulling BL or BLB low, respectively, when the WL is turned on.

A conventional sense amplifier (SA) of an SRAM is shown in FIG. 2. The latch-type SA 20 has a structure very similar to the SRAM cell shown in FIG. 1. The SA is based on the positive feedback of a latch to amplifier the input signals so that the gain can be high and the power consumption can be low. The SA can be activated when the input signals reach sufficient differential voltages; otherwise incorrect data may be sensed instead. The SA 20 has PMOS 21-1 and NMOS 21-2 constructed as an inverter with their gates coupled to QB, their sources coupled to VDD and ground through a NMOS 25, respectively. The drain of PMOS 21-1 is coupled to the drain of NMOS 21-2 and to a node Q. The SA 20 also has PMOS 22-1 and NMOS 22-2 constructed as an inverter with their gates coupled to Q, their sources coupled to VDD and ground through the NMOS 25, respectively. The drain of PMOS 22-1 is coupled to the drain of NMOS 22-2 and to a node QB. The sources of NMOS 21-2 and 22-2 are coupled to the drain of the same NMOS 25, whose gate is coupled to an

SA enable (SE) and whose source is coupled to ground. The nodes Q and QB are coupled to the sources of PMOS 23 and 24, respectively. The drains of PMOS 23 and 24 are coupled to DI and DIB, respectively. The gates of PMOS 23 and 24 are coupled to an SA input enable (SIB). Two PMOS 26-1 and 26-2 are pullup devices for nodes QB and Q, respectively, with the gates coupled to SE.

The SA shown in FIG. 2 works as follows. Before sensing, SE is low and the nodes Q and QB are pulled high to VDD by a pair of PMOS pull-ups 26-2 and 26-1, respectively. When the signals at DI and DIB reach sufficient voltage difference (i.e. 100 mV split), SIB can be pulled low to allow signals coming into the nodes Q and QB, respectively. After the differential voltages are passed from DI/DIB to Q/QB, SE can be turned on to pull the drain of MOS 25 low while disabling PMOS 26-1 and 26-2. At the mean time, the SIB can be set to low to turned off the PMOS 23 and 24 to isolate the input signals from the internal nodes Q and QB in the SA. Subsequently, the cross-coupled latch consisting of PMOS 21-1 and 22-1 can be activated to make Q and QB split wider and reach rail-to-rail levels eventually. The cross-coupled latch consists of NMOS 21-2 and 22-2 can also be activated when the NMOS 25 is more heavily turned on. The timing of turning on SE is very crucial only after substantial signal splits are developed at nodes Q and QB, otherwise wrong data can be sensed and latched instead.

FIG. 3(a) shows a block diagram 30 of a portion of a self-timed circuit in a prior art. A memory cell array 31 has a reference column 32 that consists of 3 reference cells 33-1, 33-2, and 33-3, and some dummy cells 35 to fill up a column. The reference cells can be modified slightly from the normal cells to make reference BL pulled low earlier and then used as a control signal to trigger at least one SA.

FIG. 3(b) shows a schematic of a reference cell 40, corresponding to the reference cells 33-1 through 33-3 in FIG. 3(a), in a prior art. The reference cell 40 has a pair of cross-coupled inverters 41 and 42 constructed as a latch, and two pass transistors 43 and 44, similar to a normal SRAM cell. However, the gates of the pass transistor 43 and 44 are coupled to BLin (equivalent to BL in the normal cell), and the drain of the NMOS 43 is coupled to high (i.e. VDD). When BLin is set high, RBL can be pulled low. If the three reference cell 33-1, 33-2, and 33-3 in FIG. 3(a) have their BLin coupled together and have one shared RBL, RBL can be pulled down faster than any normal cells pulling down BL/BLB. As a result, RBL can be used to trigger an SA. BLin signal can be generated from a control signal, such as a clock CLK, through a multi-tap delay chain 45. Turning on BLin with respect to CLK can be adjusted by setting a plurality of delay control signals or a plurality of registers.

To achieve a reliable SRAM function with low power consumption, it is desirable to turn on the selected WL while turning off BL pullups only during the memory cells are ready for access. FIG. 4(a) shows a portion of a schematic 50 of a self-timed circuit in a prior art. The schematic 50 has a plurality of address buffers 57, pre-decoders 58, and decoders 59. The address buffer 57 consists of inverters 51-1, 51-2 and 51-3 to generate true and complement addresses, respectively. The pre-decoder 58 has a multi-input NAND 52-1 and followed by a buffer 52-2. The decoder 59 has a multi-input NAND 53-1 and followed by a wordline driver 53-2 to drive a WL. The addresses generated from the address buffers 57 are then input to a plurality of pre-decoders 58 to generate more pre-decoded signals, which are then input to a plurality of decoders 59 to fully decode the available address space. A WL can be turned on by using a wordline enable (WLEN) in one of the input in one of the pre-decoders. WLEN can be

generated from a control signal, such as a clock CLK, through a multi-tap delay line **54**. The delay line **54** can be controlled by a plurality of delay control signals or a plurality of registers.

The relative timing between CLK and WLEN is shown in FIG. **4**(*b*). There is a parameter Twld to specify the turning on of WLEN after CLK transitions to deliver a new address. If a WL is turned on too early, excess power may be wasted. If a WL is turned on too late, the speed may be penalized. Another parameter Twlp is related to the WL pulse width. If Twlp is too narrow, sufficient BL/BLB split may not be developed before the WL is turned off again. If Twlp is too wide, excess power may be wasted. These two parameters can be used to illustrate the concept of tradeoff between speed and power.

The self-timed circuit as shown in FIGS. **3**(*a*), **3**(*b*), **4**(*a*), and **4**(*b*) are not self-timed precisely. The turning on of RBL is not tracking with WL turn-on time. The turning off of a WL is not tracking with SA enabling or disabling either. As a result, RBL may turn on an SA when the input signals are not split wide enough, or even before the selected WL is turned on at the worse. The selected WL may be turned off prematurely before sufficient signal splits reaching the inputs of an SA and sensed. Consequently, wide timing margins are needed to build a robust SRAM; otherwise yield and reliable operations may suffer. Therefore, it is still very desirable to invent some precise self-timed circuits to reduce timing margins to meet today's very demanding SRAM requirements.

SUMMARY

Embodiments of highly effective and robust circuits and methods for achieving high precision self-timed designs are disclosed. Embodiment are able to achieve very high speed and yet with sufficient margins to meet both the performance and functionality requirements.

In one embodiment, the turning on of a sense amplifier (SA) can be tracked with turning on of a selected wordline (WL) and/or bitline/bitline bar (BL/BLB). In another embodiment, the turning off of a selected WL can be tracked with SA enabling or disabling. These two timings can be very critical for high performance memory designs. If the first timing is not well met, an SA may be activated before sufficient signal splits are developed at the input of the SA and sensed wrong data. If the second timing is not well met, the selected WL may be turned off prematurely even before an SA is activated. In either case, the SA may sense cell data incorrectly. To ensure proper operations, tracking can be dependent on the strength of cell devices, wordline delay, bitline delay, and the configurations of the memory array, such as number of rows and columns, so that high speed and yet reliable operation can be achieved for wide ranges of voltage supplies, process corners, and temperatures.

Circuits and methods for precisely self-timed SRAM memory are disclosed to track the wordline and/or bitline/ bitline bar (BL/BLB) propagation delays. At least one reference cell can be placed near the far end of a driver to drive a selected wordline or a reference wordline. When a wordline and/or a reference wordline is turned on, the reference cell can be selected not earlier than any selected SRAM cells and can activate a reference bitline (RBL) not later than any selected SRAM cells activating the BL or BLB. The activation of the RBL can be used to trigger at least one sense amplifier. The RBL can also be used to de-select wordline or reference wordline after the sense amplifier operation is complete to save power. The reference cell can have substantially the same device size, area, shape, and structure as a normal SRAM cell, but has a bitline in (BLin) coupled to the input of

an inverter and the reference bitline (RBL) coupled to the output of the inverter. The BLin and RBL are similar to BL and BLB of an SRAM cell, respectively. The driving capability of the reference cell can be enhanced by enlarging the size of the inverter in a single reference cell or by combining the inverter outputs in a plurality of reference cells with proper setting in BLIns. The setting can be stored in registers for loading.

The invention can be implemented in numerous ways, including as a method, system, device, or apparatus (including computer readable medium). Several embodiments of the invention are discussed below.

As an embodiment in an integrated circuit, one embodiment can, for example, include at least one reference cell associated with a normal wordline or a reference wordline. The reference cells can be very similar to the normal cells but has higher pulldown capability that can be adjusted optionally by a plurality of control signals or registers. The selected reference cells can be turned on shortly after the last normal cell in a selective wordline is turned on. The selected reference cells can pulldown a reference bitline (RBL) faster than any selected normal cells pulling down the normal BL or BLB. Then, the RBL can be used to trigger at least one sense amplifier (SA) after proper buffering. The SA triggering signal can also be used to de-assert a wordline enable (WLEN) to turn off the selected wordline and/or reference wordline to complete a memory access.

As an electronics system, one embodiment can, for example, include at least a processor, and a self-timed SRAM memory operatively connected to the processor. The SRAM memory has at least one self-timed circuit, which in one embodiment can, for example, include at least one reference cell associated with a normal wordline or a reference wordline. The reference cells can be very similar to the normal cells but has higher pulldown capability that can be adjusted optionally by a plurality of control signals or registers. The selected reference cells can be turned on shortly after the last selected normal cell is turned on. The selected reference cells can pulldown a reference bitline (RBL) faster than any selected normal cells pulling down the normal BL or BLB. Then, the RBL can be used to trigger at least one sense amplifier (SA) after proper buffering. The SA triggering signal can also be used to de-assert a wordline enable (WLEN) to turn off a wordline and/or reference wordline to complete a memory access.

As a method for providing effective self-timed embodiments for an SRAM memory, one embodiment can, for example, include at least one reference cell associated with a normal wordline or a reference wordline. The reference cells can be very similar to the normal cells but has higher pulldown capability that can be adjusted optionally by a plurality of control signals or registers. The selected reference cells can be turned on shortly after the last selected normal cell is turned on. The selected reference cells can pulldown a reference bitline (RBL) faster than any selected normal cells pulling down the normal BL or BLB. Then, the RBL can be used to trigger at least one sense amplifier (SA) after proper buffering. The SA triggering signal can also be used to de-assert a wordline enable (WLEN) to turn off a wordline and/or reference wordline to complete a memory access.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed descriptions in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

FIG. 1 shows an SRAM cell commonly used in an SRAM memory.

FIG. 2 shows a sense amplifier commonly used in an SRAM memory.

FIG. 3(a) shows a portion of a conventional block diagram of a self-timed circuit.

FIG. 3(b) shows a schematic of a conventional reference cell.

FIG. 4(a) shows a schematic of a wordline enable (WLEN) control circuit.

FIG. 4(b) shows a timing diagram of the WLEN with respect to a control signal CLK.

FIG. 5(a) shows a portion of a block diagram of a self-timed circuit according to one embodiment.

FIG. 5(b) shows a portion of a block diagram of a self-timed circuit according to another embodiment.

FIG. 6(a) shows a portion of a block diagram of a memory array using self-timed circuit according to one embodiment.

FIG. 6(b) shows a portion of a schematic of a reference cell corresponding to the reference cells in FIG. 5(a), 5(b), or 6(a) according to one embodiment.

FIG. 6(c) shows a portion of a schematic of another reference cell corresponding to the reference cells in FIG. 5(a), 5(b), or 6(a) according to another embodiment.

FIG. 6(d) shows a portion of a schematic of yet another reference cell corresponding to the reference cells in FIG. 5(a), 5(b), or 6(a) according to yet another embodiment.

FIG. 7 shows a portion of a schematic of address buffer, pre-decoder, and decoder with WLEN according to one embodiment.

FIG. 8 shows a portion of a schematic of a sense amplifier shared between upper and lower columns.

FIG. 9 depicts a method in a flow chart to read an SRAM cell in self-timed according to one embodiment.

FIG. 10 shows a processor system using at least one self-timed SRAM memory according to one embodiment.

DETAILED DESCRIPTION OF EMBODIMENTS
OF THE INVENTION

Embodiments disclosed herein can track wordline and/or bitline delays to activate at least one sense amplifier (SA) and to turn off a wordline after at least one sense amplifier (SA) is activated. A latch-type of SA is essential in today's nanometer SRAM for low power and low voltage operations. However, the latch-type of SA requires sufficient signal splits developed in the input of an SA before being activated; otherwise irrevocable incorrect data can be sensed and latched. Without sufficient timing margins, the input signals may not be split wide enough for sensing. On the other hand, if the timing margins are too wide, the speed of an SRAM can suffer. Advantageously, embodiments disclosed herein are capably of tracking critical timings to achieve reliable operations and yet high speed by using at least one reference cell, similar to the normal cell, to track wordline and/or bitline delay and to turn on at least one sense amplifier accordingly. After the SA is activated, the selected wordline can be turned off by using the same tracking signal after proper buffering. Thus robust design with high speed operations can be achieved.

Circuits and methods for precisely self-timed SRAM memory are disclosed to track the wordline and/or bitline/bitline bar (BL/BLB) propagation delays. At least one reference cell can be placed near the far end of a driver to drive a selected wordline or a reference wordline. When a wordline and/or a reference wordline is turned on, the reference cell can be selected not earlier than any selected SRAM cells and can activate a reference bitline (RBL) not later than any selected

SRAM cells activating the BL or BLB. The activation of the RBL can be used to trigger at least one sense amplifier. The RBL can also be used to de-select wordline or reference wordline after the sense amplifier operation is complete to save power. The reference cell can have substantially the same device size, area, shape, and structure as a normal SRAM cell, but has a bitline in (BLin) coupled to the input of an inverter and the reference bitline (RBL) coupled to the output of the inverter. The BLin and RBL are similar to BL and BLB of an SRAM cell, respectively. The driving capability of the reference cell can be enhanced by enlarging the size of the inverter in a single reference cell or by combining the inverter outputs in a plurality of reference cells with proper setting in BLIns. The setting can be stored in registers for loading.

Exemplary embodiments of the invention are discussed below with reference to the figures. However, those skilled in the art will readily appreciate that the detailed description given herein with respect to these figures is for explanatory purposes as the invention extends beyond these limited embodiments.

FIG. 5(a) shows a block diagram of a portion of a self-timed SRAM memory 100 according to one embodiment of the present invention. The SRAM memory 100 has an SRAM memory array 101, at least one reference column 102 that includes at least one reference cell 103, at least one sense amplifier 106, a plurality of pre-decoders 105, and decoders 104. In this embodiment, there is at least one reference cell hung on the far end of a wordline driver to drive a wordline. The SRAM 100 has incoming addresses pre-decoded in the pre-decoder 105. Then the pre-decoded addresses are further input to the decoders 104 to select one from a plurality of wordlines to access at least one memory cells in a row. The wordline can be enabled by gating a wordline enable signal (WLEN) to an input of a pre-decoder or decoder. At the far end of a wordline driver in the decoders 104, there is at least one reference cell 103 in at least one reference column 102 that can be turned on by the same selected normal wordline. The reference cell 103 has a similar circuit, device size, area, and structure as the normal cells except that the reference cell 103 has a higher pulldown capability than any normal cells, presumably the BL and RBL are pre-charged to high before accesses. After the selected wordline is turned on, the selected reference cell can pull down a reference bitline (RBL) faster than any selected normal cells pulling down BLs or BLBs, depending on the data being 0s or 1s. The RBL can be used to trigger at least one sense amplifier (SA) 106 after proper buffering. With this configuration, the activation of the SA can be ensured after all cells in the same selected row are turned on and sufficient signal splits are developed between BLs and BLBs. Once the SA is activated, the selected WL can be turned off by using the same RBL signal to de-assert WLEN in the pre-decoder 105 or decoder 104 after proper buffering. Subsequently, the wordline driver in the decoder 104 can be disabled to turn off the selected wordline. In another embodiment, the pulldown strength of the reference cells hung on each wordline can be adjusted by setting a plurality of control signals or registers.

FIG. 5(b) shows a block diagram of a portion of a self-timed SRAM memory 100' according to another embodiment of the present invention. The SRAM memory 100' has an SRAM memory array 101', at least one reference column 102' that includes at least one reference cell 103', at least one sense amplifier 106', pre-decoders 105', and decoders 104'. In this embodiment, there is at least one reference cell hung on the far end of a reference wordline driver to drive and turn on at least one reference wordline (RWL) whenever a normal

wordline is turned on. The SRAM **100'** has incoming addresses pre-decoded in the pre-decoder **105'**. Then the pre-decoded addresses are further input to decoders **104'** to select a wordline from a plurality of wordlines to access at least one cell in a row. The wordline can be enabled by gating a word-line enable signal (WLEN) to an input of a pre-decoder or decoder. At the same time, at least one reference wordline (RWL) can be turned on along with turning on a selected wordline. The reference cell **103'** has a similar circuit, size, area, and structure as any normal cells except that the refer-ence cell **103'** has a higher pulldown capability than any normal cells, presumably the BL and RBL are pre-charged to high before accesses. After the reference wordline is turned on, the selected reference cell can pulldown a reference bit-line (RBL) faster than any selected normal cells pulling down BLs or BLBs after the selected normal wordline is turned on. The RBL can be used to trigger at least one sense amplifier (SA) **106'** after proper buffering. With this configuration, the SA can be activated surely after all cells in the selected normal row are turned on and sufficient signal splits are developed between BLs and BLBs. Once the SA is activated, the WL and RWL can be turned off by using the same RBL signal to de-assert WLEN in the pre-decoders **105'** or decoders **104'** after proper buffering. Subsequently, the selected wordline and reference wordline drivers in the decoder **104'** can be de-asserted to turn off the selected wordline and reference wordline, respectively. In another embodiment, the pulldown strength of the reference cells hung on each reference word-line can be adjusted by setting a plurality of control signals or registers.

FIG. **6**(*a*) shows a block diagram **60** of a portion of an SRAM memory, corresponding to the SRAM in the FIG. **5**(*a*), according to one embodiment. The SRAM memory **60** has at least one memory cell array **61**, a plurality of reference columns **61-1**, **61-2**, and **61-3** that have at least one reference cell **63-1**, **63-2**, and **63-3**, respectively. The reference cell has a similar area, device size, circuit, and structure as the normal cells. The pulldown devices in three reference cells on the same wordline can be combined to provide three times of pulldown capability than a normal cell.

FIG. **6**(*b*) shows a schematic of a reference cell triple **80**, corresponding to the reference cell **103** in FIG. **5**(*a*), reference cell **103'** in FIG. **5**(*b*), or reference cells **63-1** through **63-3** in FIG. **6**(*a*), according to one embodiment. The reference cell triple **80** has three reference cells **70-1**, **70-2**, and **70-3**. Each reference latch has two cross-coupled inverters **71** and **72** to constitute a latch. The latch has a node N coupled to a source of an NMOS **73** and whose drain is coupled to a BLin. The latch has another node NB coupled to a source of another NMOS **74** and whose drain is coupled to a RBL. The gates of the NMOS **73** and **74** are coupled to a reference wordline (RWL) or wordline (WL). The reference cells **70-1**, **70-2**, and **70-3** can be modified from normal cells by coupling NB[1] and NB[2] of the reference cells **70-1** and **70-2** to NB[3] of the reference cell **70-3** to triple the pulldown capability, if BLin [1], BLin[2], and BLin[3] are set to high. BLin[1], BLin[2], or BLin[3] can be optionally set to high or low to adjust the pulldown strength so that the turn-on time of RBL can be adjusted accordingly. BLin[1], BLin[2], or BLin[3] can also be controlled by setting three register bits. In another embodi-ment, the invert **71** can be omitted from schematic/layout database or disabled by removing contact(s) or via(s).

FIG. **6**(*c*) shows a schematic of a reference cell triple **80'**, corresponding to the reference cell **103** in FIG. **5**(*a*), reference cell **103'** in FIG. **5**(*b*), or reference cells **63-1** through **63-3** in FIG. **6**(*a*), according to one embodiment. The reference cell triple **80'** has three reference cells **70'-1**, **70'-2**, and **70'-3**. Each

reference latch has two cross-coupled inverters **71'** and **72'** to constitute a latch. The latch has a node N coupled to a source of an NMOS **73'** and whose drain is coupled to a BLin. The latch also has a node NB coupled to a source of an NMOS **74'** and whose drain is coupled to a RBL. The source and drain of the NMOS **73'** are shorted to allow the BLin pulling RBL low easier. The gates of the NMOS **73'** and **74'** are coupled to a reference wordline (RWL) or wordline (WL). The reference cells **70'-1**, **70'-2**, and **70'-3** can be modified from normal cells by coupling the NB[1] and NB[2] of the reference cells **70'-1** and **70'-2** to NB[3] of the reference cell **70'-3** to triple the pulldown capability, if BLin[1], BLin[2], and BLin[3] are set to high. BLin[1], BLin[2], or BLin[3] can be optionally set to high or low to adjust the pulldown strength so that the turn-on time of RBL can be adjusted accordingly. BLin[1], BLin[2], or BLin[3] can also be controlled by setting three register bits. In another embodiment, the invert **71'** can be omitted from schematic/layout database or disabled by removing contact (s) or via(s).

FIG. **6**(*d*) shows a schematic of a reference cell triple **80''**, corresponding to the reference cell **103** in FIG. **5**(*a*), reference cell **103'** in FIG. **5**(*b*), or reference cells **63-1** through **63-3** in FIG. **6**(*a*), according to yet another embodiment. The refer-ence cell triple **80''** has three reference cells **70''-1**, **70''-2**, and **70''-3**. Each reference cell has two inverters **71''** and **72''** modified from a cross-coupled latch in an SRAM cell. The inverter **72''** has an input node coupled to a BLin and an output node NB coupled to a source of an NMOS **74''** and whose drain is coupled to a RBL. An NMOS **73''** can be coupled between the input of the inverter **72''** and the BLin, used as a dummy transistor with the source or drain floating, or simply omitted from the schematic or layout. The gates of the NMOS **73''** and **74''** are coupled to a reference wordline (RWL) or wordline (WL). The reference cells **70''-1**, **70''-2**, and **70''-3** also have another inverter **71''** modified from normal cell that has an input coupled to BLin and an output coupled to NB to double the pulldown capability. The reference cells **70''-1**, **70''-2**, and **70''-3** can be modified from normal cells by cou-pling the NB[1] and NB[2] of the reference cells **70''-1** and **70''-2** to NB[3] of the reference cell **70''-3** to triple the pull-down capability, if BLin[1], BLin[2], and BLin[3] are set to high. BLin[1], BLin[2], or BLin[3] can be optionally set to high or low to adjust the pulldown strength so that the turn-on time of RBL can be adjusted accordingly. BLin[1], BLin[2], or BLin[3] can also be controlled by setting a plurality of register bits.

FIGS. **6**(*a*), **6**(*b*), **6**(*c*), and **6**(*d*) only show a few of many possible embodiments of reference cells. For example, the NMOS **73'** in FIG. **6**(*c*) or NMOS **73''** in FIG. **6**(*d*) can be removed from the schematic/layout database or disabled by omitting a single or plurality of contact or via. Similarly, the inverter **71'** in FIG. **6**(*c*) can be removed from the schematic/layout database or disabled by omitting a single or plurality of contact or via. The number of reference cells in a wordline or reference wordline may vary. The number of normal/refer-ence rows or columns may vary too. It is desirable to place the reference cell near the far end of a wordline or reference wordline driver so that the selected reference cell can be turned on later than any selected normal cells. In general, it is more desirable to keep the transistors in the reference cells intact as the normal cells, but omitting some contact(s)/via(s) or using metal **1** or metal **2** for re-wiring. The more the reference cell resembles to the normal cell, the better the tracking capability. The above discussions are for illustrative purposes. There are many variations and equivalent embodi-ments of building reference cells, and that are all within the scope of this invention for those skilled in the art.

FIG. **7** shows a block diagram **50'** of a portion of address buffers, pre-decoders, and decoders according to one embodiment. The schematic **50'** has a plurality of address buffers **57'**, pre-decoders **58'**, and decoders **59'**. The address buffer **57'** consists of inverters **51'-1**, **51'-2** and **51'-3** to generate true and complement addresses, respectively. The pre-decoder **58'** has a multi-input NAND **52'-1** and followed by a buffer **52'-2**. The decoder **59'** has a multi-input NAND **53'-1** and followed by a wordline driver **53'-2** to drive a wordline. There are plural of address buffers coupled to plural of pre-decoders, and then the pre-decoders are further coupled to plural of decoders to fully decode the entire address space to generate a plurality of wordlines. A wordline enable (WLEN) can be provided to one of the inputs in the decoder **59'**, or to a pre-decoder **58'**, to shorten the wordline on/off time delay. WLEN can be generated from the RBL through a multi-tap delay line **54'**. The delay line **54'** can be controlled by a plurality of control signals or a plurality of registers. This scheme can improve the wordline turn off time much more precisely than in the prior art as shown in FIG. **4**.

FIG. **8** shows a block diagram of a portion of an SA schematic **90** with an input multiplexer according to one embodiment. The block diagram **90** has two columns, top column **98** and bottom column **99**, and an SA **97**. The SA **97** has a PMOS **91-1** and an NMOS **91-2** constructed as an inverter with input QB and output Q, but the source of NMOS **91-2** is coupled to ground through an NMOS **95**. The SA **97** also has a PMOS **92-1** and an NMOS **92-2** constructed as an inverter with input Q and output Oft but the source of NMOS **92-2** is coupled to ground through the same NMOS **95**. The gate of NMOS **95** is coupled to an SA enable (SE). Nodes Q and QB are coupled to BLU and BLUB through PMOS **93-1** and **94-1**, respectively. The gates of PMOS **93-1** and **94-1** are coupled to a sense amplifier upper input enable bar (SIUB). Nodes Q and QB are also coupled to BLL and BLLB through PMOS **93-2** and **94-2**, respectively. The gates of PMOS **93-2** and **94-2** are coupled to a sense amplifier lower input enable bar (SILB). The BLU and BLUB are the bitline and bitline bar of the upper column. Similarly, the BLL and BLLB are the bitline and bitline bar of the lower column. The upper and lower column **98** and **99** can share the same SA with two different input selects SIUB and SILB to select the upper BLs or the lower BLs, respectively.

FIG. **9** shows a flow chart **700** depicting a method to self-timed read accesses, according to one embodiment. The procedure starts at **710** to select addresses for memory access. Normally, the addresses are latched in flip-flops or latches and triggered by a clock transition for a new memory access. A wordline Enable (WLEN) can be generated from a clock CLK with a proper delay line in step **720**. Subsequently a wordline (WL) can be selected when the addresses and WLEN go through the address buffers, pre-decoders, and decoders to a wordline driver in step **730**. Then the bitline pull-ups can be turned off in step **740** to save power and to speed up BL/BLB pulldown. At least one reference cell can be turned on to activate RBL when a wordline and/or a reference wordline is turned on in step **750**. The RBL can be used to trigger at least one SA after proper buffering in step **760**. After SA is activated, the WLEN and BL pullup can be de-asserted by using RBL after proper buffering in step **770**. Finally, the data from SA outputs can be sent to I/Os after some buffering. Then, the read access is completed and the procedure stops in step **799**. Similar procedure can be applied to self-timed write.

The method **700** is described in the context a self-timed SRAM, such as the SRAM memory **100** in FIG. **5**(*a*) or **100'** in FIG. **5**(*b*). In addition, although described as a flow of steps, one of ordinary skilled in the art will recognize that at

least some of the steps may be performed in a different order, including simultaneously, or skipped.

FIG. **10** shows a processor system **600** according to one embodiment. The processor system **600** can include an SRAM cell or reference cell **644**, such as in a cell array **642**, in a self-timed SRAM memory **640**, according to one embodiment. The processor system **600** can, for example, pertain to an electronic system. The electronic system can include a Central Process Unit (CPU) **610**, which communicate through a common bus **615** to various memory and peripheral devices such as I/O **620**, hard disk drive **630**, CDROM **650**, self-timed SRAM memory **640**, and other memory **660**. Other memory **660** is a conventional memory such as conventional SRAM, DRAM, or flash, typically interfaces to CPU **610** through a memory controller. CPU **610** generally is a microcontroller, microprocessor, a digital signal processor, or other programmable digital logic devices. Self-timed SRAM Memory **640** is preferably constructed as an SRAM cell or reference cell device **644**. The memory **640** typically interfaces to CPU **610** through a bus interface unit. If desired, the memory **640** may be combined with the processor, for example CPU **610**, in a single integrated circuit.

The invention can be implemented in a part or all of an integrated circuit in a Printed Circuit Board (PCB), in a system, or as a method. The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modifications and substitutions of specific process conditions and structures can be made without departing from the spirit and scope of the present invention.

The many features and advantages of the present invention are apparent from the written description and, thus, it is intended by the appended claims to cover all such features and advantages of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation as illustrated and described. Hence, all suitable modifications and equivalents may be resorted to as falling within the scope of the invention.

What is claimed is:

1. A SRAM memory, comprising:
a plurality of SRAM cells having a bitlines (BL) and wordline (WL) that can be selected for access;
at least one reference cell having a reference bitline in (BLin) and a reference bitline (RBL) that can be selected from one of a plurality of wordlines or from at least one reference wordline, the reference cell being selectable not earlier than any selected SRAM cells and the RBL being activatable not later than any selected SRAM cells to activate the selected BL;
at least one sense amplifier to sense signals coupled to the selected BL from the at least one selected SRAM cell and convert the signals into digital data; and
wherein the sense amplifier can be activated by the RBL signal to track the wordline and BL propagating delay,
wherein the reference cell has at least one logic gate with an input coupled to BLin and an output NB coupled to RBL, and
wherein the RBL is activated by setting BLin at a voltage near a supply voltage or ground once the wordline or reference wordline is selected.

2. A SRAM memory as recited in claim **1**, wherein the at least one reference cell is placed near the far end of a driver to drive a selected wordline or a reference wordline.

3. A SRAM memory as recited in claim **1**, wherein the logic gate comprises an inverter.

4. A SRAM memory as recited in claim **3**, wherein the inverter in a reference cell have substantially the same device size, shape, and layout style of an inverter in an SRAM cell.

5. A SRAM memory as recited in claim **3**, wherein the output nodes NB of a plurality of reference cells in the same selected wordline or reference wordline are coupled together.

6. A SRAM memory as recited in claim **3**, wherein the BLin of the reference cells of the same selected wordline or reference wordline are coupled to a plurality of registers, whose contents can be loaded with data.

7. A SRAM memory as recited in claim **1**, wherein the turn-off of the selected wordline or reference wordline is controlled by the activation of the RBL.

8. A SRAM memory as recited in claim **7**, wherein the wordline or reference wordline is generated from at least one pre-decoder and decoder, which can be turned off by the activation of the RBL to at least one of the pre-decoder and/or decoder.

9. An electronics system, comprising:

a processor; and

an SRAM memory operatively connected to the processor, the SRAM memory comprising:

a plurality of SRAM cells having at least a bitline (BL) and a wordline that can be selected for access;

at least one reference cell having a reference bitline in (BLin) and a reference bitline (RBL) that can be selected from one of a plurality of wordlines or from a reference wordline, where the reference cell can be selected not earlier than any selected SRAM cells and can activate RBL not later than any selected SRAM cell to activate the selected BL; and

at least one sense amplifier to sense signals coupled from the selected BL from the at least one selected SRAM cell and convert the signals into digital data,

wherein the sense amplifier can be triggered by the RBL signal to track the wordline and BL propagating delay,

wherein the reference cell has at least one logic gate with an input coupled to BLin and an output NB coupled to RBL, and

wherein the RBL is activated by setting BLin at a voltage near a supply voltage or ground once the wordline or reference wordline is selected.

10. A SRAM memory as recited in claim **9**, wherein the at least one reference cell is placed near the far end of a driver to drive a selected wordline or a reference wordline.

11. A SRAM memory as recited in claim **9**, wherein the logic gate comprises an inverter.

12. A SRAM memory as recited in claim **11**, wherein the logic gate in a reference cell has substantially the same device size, shape, and layout style of a logic gate in an SRAM cell.

13. A SRAM memory as recited in claim **11**, wherein the output nodes NB of a plurality of reference cells in the same selected wordline or reference wordline are coupled together.

14. A SRAM memory as recited in claim **11**, wherein the BLin of the reference cells of the same selected wordline or reference wordline are coupled to a plurality of registers, whose contents can be loaded with data.

15. A SRAM memory as recited in claim **11**, wherein the turn-off of the selected wordline or reference wordline is controlled by the activation of the RBL.

16. A SRAM memory as recited in claim **11**, wherein the selected wordline or reference wordline is generated from at least one pre-decoder and decoder, which can be turned off by the activation of the RBL to at least one of the pre-decoder and/or decoder.

17. A method for providing a self-timed SRAM memory, comprising:

(i) providing a plurality of SRAM cells having at least a bitline (BL) and a wordline that can be selected for access, (ii) at least one reference cell having a bitline in (BLin) and a reference bitline (RBL) that can be selected from a wordline or a reference wordline; (iii) at least one sense amplifier to sense signals from the selected BL from the at least one selected SRAM cell and convert the signals into digital data; and (iv) the reference cell can be selected not earlier than any selected SRAM cells and can activate RBL not later than any selected SRAM cells to activate the selected BL,

wherein the sense amplifier is triggered by the activation of RBL to track the wordline and BL propagation delay,

wherein the reference cell has at least one logic gate with an input coupled to BLin and an output NB coupled to RBL, and

wherein the RBL is activated by setting BLin at a voltage near a supply voltage or ground once the wordline or reference wordline is selected.

18. A method for providing a self-timed SRAM memory as recited in claim **17**, wherein the RBL is activated by setting BLin at the voltage near the supply voltage once the wordline or reference wordline is selected.

19. A method for providing a self-timed SRAM memory as recited in claim **18**, wherein the at least one logic gate comprises an inverter and/or a reference pass transistor in a reference cell have substantially the same device size, shape, and layout style of at least one logic gate and/or a cell pass transistor in an SRAM cell.

20. A method for providing a self-timed SRAM memory as recited in claim **17**, wherein the turn-off of the selected wordline or reference wordline is controlled by the activation of the RBL.

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