(12) UK Patent Application (19) GB (11) 2 184 624 (13) A

(43) Application published 24 Jun 1987

(21) Application No 8628417

(22) Date of filing 27 Nov 1986

(30) Priority data

(31) 23363 (32) 23 Dec 1985 (33) IT

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(51) INT CL[4]
H03F 1/02

(52) Domestic classification (Edition I)
H3T 2B8 2T2X 3N 4D 4E2N UE

(56) Documents cited

GB A	2146501	GB A	2050100
GB A	2142794	EP A	0190469
GB A	2120486		

(58) Field of search
H3T
Selected US specifications from IPC sub-class H03F

(54) Current gain stage with low voltage drop

(57) A current gain stage with low voltage drop usable in place of a Darlington's current gain stage maintains the characteristics of precision of the value of the output current though presenting a lower voltage drop. The stage comprises cascade connected transistors T1, T2 and a current mirror AUXI with its input connected to the collector of transistor T1. The output from the current mirror AUXI is combined with the output from the transistor T2 to provide the stage output.

Fig. 4a

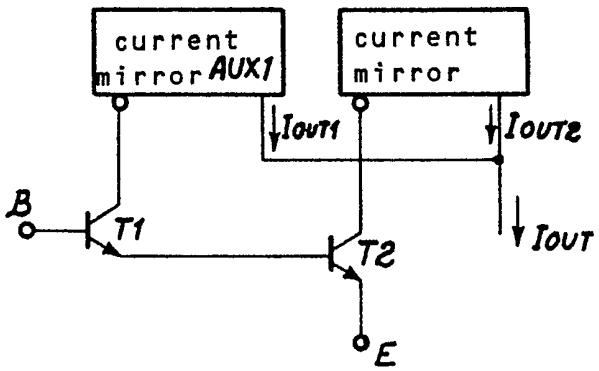

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Fig. 1a

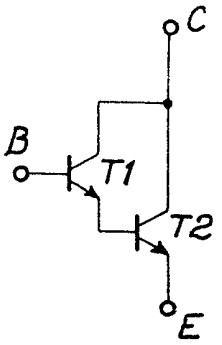

Fig. 1b

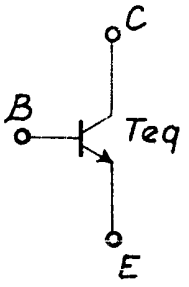

Fig. 2a

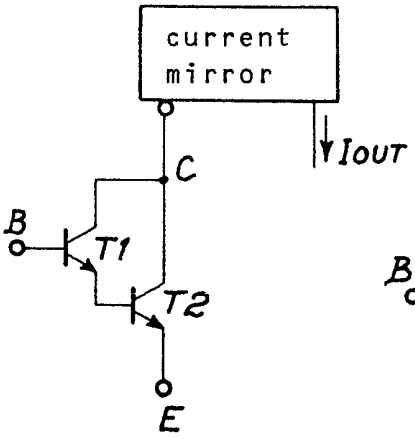

Fig. 2b

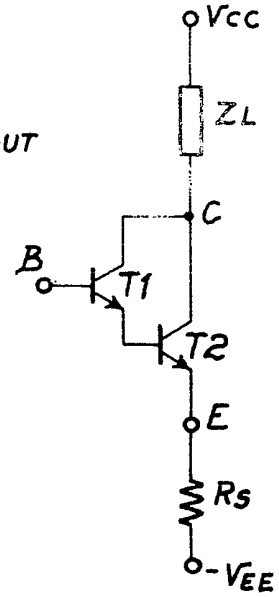

Fig. 3a

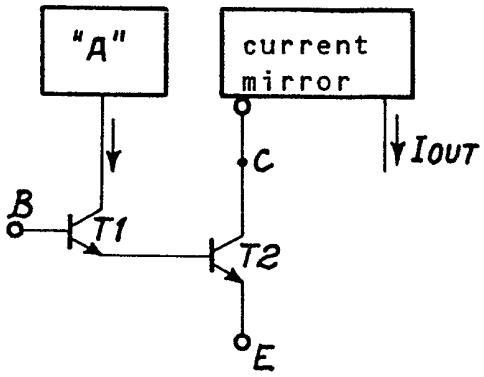

Fig. 4a

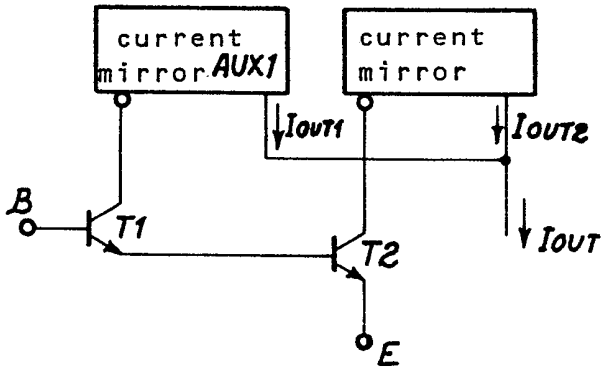

Fig. 3b

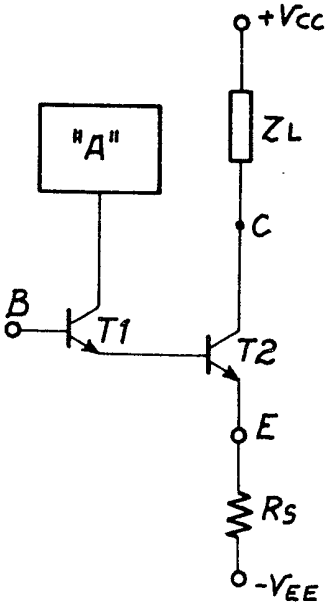

Fig. 4b

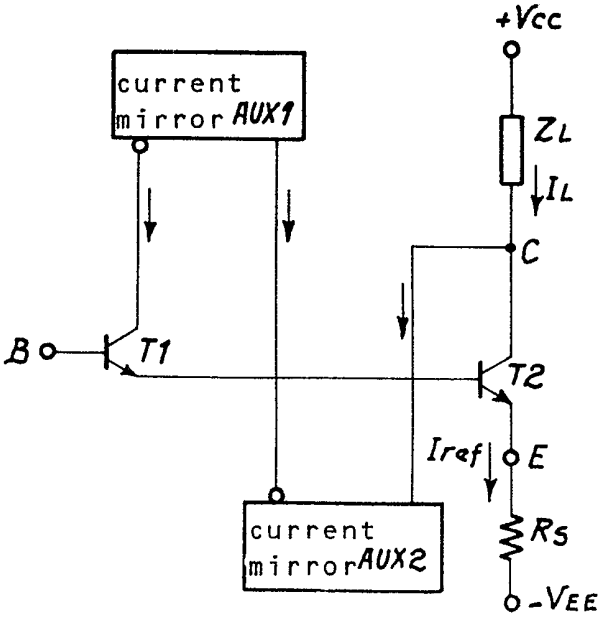

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Fig.5

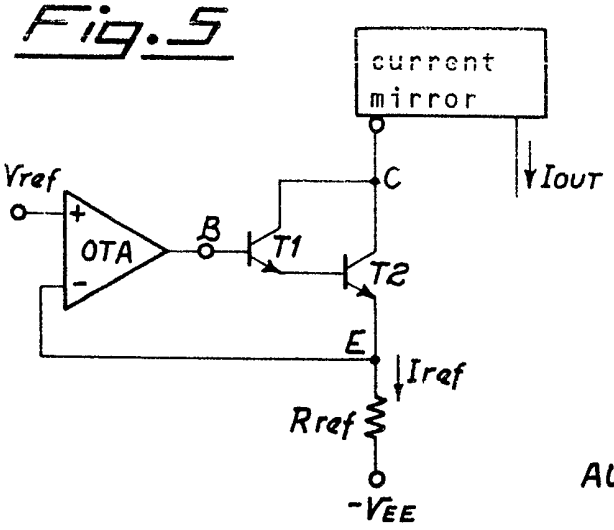


Fig.6

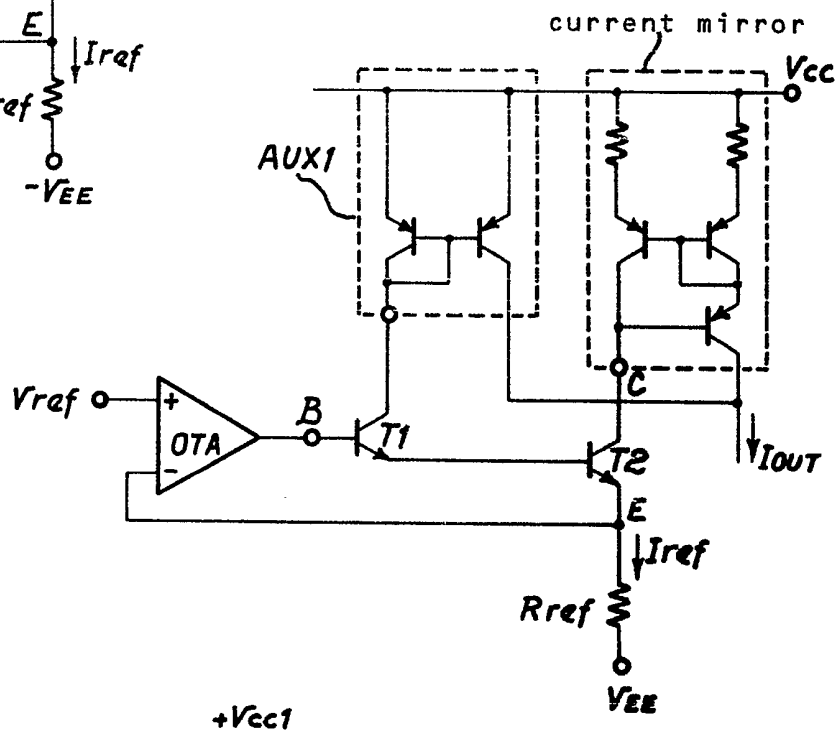


Fig.8

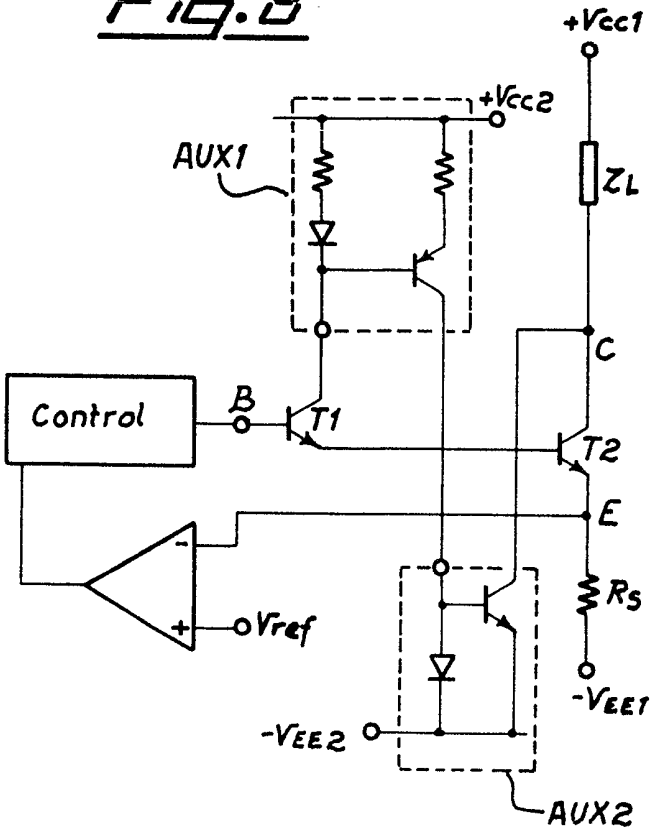
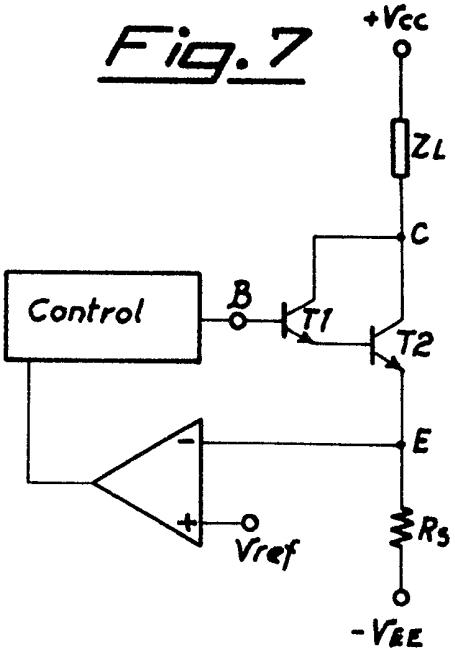


Fig.7



SPECIFICATION

Current Gain Stage with Low Voltage Drop

The present invention relates to a current gain stage with low voltage drop having a high level of precision.

The invention is particularly useful in the field of monolithic intergrated circuits, both in integrated systems of the analog type and in integrated systems of the switching or logic type.

The common collector connection of two stages (transistors) the first of which sees as load the input conductance of the second, called Darlington's connection, is widely used in applications wherein there is the necessity of obtaining a very small value for the input admittance of an amplifier utilizing semiconductor devices of the bipolar kind.

As it is well known, the current gain stages of the Darlington's type present a drawback which may exclude their utilization in many applications characterized by peculiar requirements; that is the voltage between the collector terminal and the emitter's one of the "equivalent transistor" in the Darlington's arrangement cannot fall below the value of the sum of the V_{BE} of the second transistor (T_2 in the figures) of the cascade pair and of the V_{CE} of the first transistor of the cascade pair (T_1 in the figures).

In the very frequent case where the output current of the Darlington is utilized, through a current mirror, for driving another circuit of any kind, it is often of fundamental importance that the voltage drop between the terminals C (collector) and E (emitter) of the Darlington be very small in order not to limit excessively the voltage swing, in other words the dynamic characteristic of the E node or of the C node. In fact the current mirror may have a type of circuit implementation which may be complex and this may imply a certain voltage drop which, summed to the voltage drop of the Darlington (that is between said C and E nodes), may result even incompatible with the limit imposed by the supply voltage which is often of only 5 V.

A similar inconvenience of intolerable excessive limitation of the excursion possibility of the voltage is encountered in the output stages which utilize the Darlington's connection and a sensing resistor for detection and control, by a feed back, of the current through the output transistor. Also in this type of application the voltage drop between the C and E nodes of the Darlington limits the maximum voltage developable across the load of the circuit.

With the aim of overcoming such a drawback of Darlington's stages, particularly in circuit situations of the above mentioned type, and thus to reduce the voltage drop of the current gain stage, it is known to connect the collector of the first transistor T_1 (driver) not to the collector of the second transistor T_2, in accordance with the typical Darlington's connection, but to a circuit block, distinct from the "load" or from the current mirror driven by the output transistor T_2, or even directly to the supply line.

This arrangement allows reducing the minimum voltage between said C and E nodes of the current gain stage only to the V_{CE} voltage of the output transistor T_2 to the detriment, though, of the precision of the output current, as it will be better illustrated later in the description. The degree of imprecision which is introduced through said known arrangement is not tolerable in many applications.

It is therefore a main objective of the present invention to provide a current gain stage with low voltage drop which maintains, at the same time, a high precision of the value of the output current relative to a given input signal substantially equivalent to that offered by a conventional type Darlington's stage.

This objective, as well as other advantages which will become evident through the following description, are achieved, in accordance with the present invention, by means of a current gain stage comprising two transistors T_1 and T_2 substantially connected in cascade and characterized in that the collector of the first transistor T_1 (driver) is connected to a current mirror, the output current of which is then summed to the output current of the gain stage.

The invention and the advantages it offers with respect to the known techniques in relation to the technical problems discussed above, will be more easily illustrated by reference to a series of circuit diagrams which are herein presented for purely illustrative and non-limitative purposes in the annexed drawings wherein:

Figures 1a and 1b illustrate, respectively, the typical diagram of a Darlington's type stage and of the equivalent transistor;

Figures 2a and 2b illustrate the relative diagrams of two typical circuit situations utilizing Darlington's type current gain stages;

Figures 3a and 3b illustrate current gain stages modified in accordance with the prior technique and utilized, in place of the conventional Darlington's stages, in similar circuit situations of Figures 2a and 2b;

Figures 4a and 4b illustrate current gain stages in accordance with the present invention utilized in similar circuit situations as shown in Figures 2a, 2b, 3a and 3b;

Figure 5 illustrates the diagram of a circuit using a Darlington, which is often found in many integrated systems;

Figure 6 illustrates the application of the current gain stage of the invention in the circuit of Fig. 5;

Figure 7 illustrates another diagram of another circuit using a Darlington which is often employed in many integrated systems of the digital or switching type;

Figure 8 illustrates the application of the current gain stage of the invention in the circuit of Fig. 7.

In many applications the voltage drop across the nodes C and E of a widely used current gain stage of the Darlington's type, the basic diagram of which is shown in Figures 1a and 1b, and which cannot be lower than $V_{BET2}+V_{CEsatT1}$, may result excessive.

A situation of this kind may happen for example in the case wherein the output current from the Darlington is utilized, through a current mirror, for

driving another circuit of any kind as illustrated in the diagram of Fig. 2a. The current mirror, represented in Fig. 2a by the block bearing the same name, may in fact have a circuit arrangement rather complicated and this may imply a voltage drop which, being added to the voltage drop of the Darlington's stage of current gain, may not be compatible with the available supply voltage. A similar requirement of reducing the voltage drop across the C and E nodes of the current amplifier for allowing a better dynamic characteristic may be present, for example, in the case of an output stage shown in Fig. 2b, which utilizes a Darlington, and constituted by two transistors T_1 and T_2 and by a sensing resistor R_S for the feed back control of the output current, that is the voltage drop across C and E nodes of the Darlington limits the maximum excursion of the voltage which may be developed across the load Z_L.

In both cases contemplated in Figures 2a and 2b it is often customary not to connect the collector of transistor T_1 (driver) to the collector of the output transistor T_2 so as to reduce the voltage drop across C and E nodes of the current gain stage only to the voltage $V_{CEsatT2}$ (the saturation voltage collector-emitter of transistor T_2) and to connect, instead, the collector of transistor T_1 to a circuit block distinct from the load and from the current mirror driven by the current gain stage as shown, respectively, in Figures 3a and 3b.

The distinct circuit block, indicated with A in Figures 3a and 3b, is often a direct connection of the collector of transistor T_1 to the supply line, though it may also have, in general, any suitable circuit arrangement.

This arrangement of the prior art involves, though, an imprecision of the output current of magnitude equal to the collector current of transistor T_1 which, in many instances, cannot be tolerated. An example may be the application wherein the output current has to be set with high precision by controlling the emitter current of the Darlington. In fact, with reference to Fig. 3a, it may be observed that:

$$\begin{aligned} I_{E2} &= I_{C2} + I_{B2} \\ I_{C2} &= I_{E2} - I_{B2} \\ &= I_{E2} - I_{E1} \\ &= I_{E2} - (I_{C1} + I_{B1}) \\ &= I_{E2} - (\beta_1 + 1)\, I_{B1} \end{aligned}$$

wherein the notations are conventional and the suffixes 1 or 2 serve to indicate reference, respectively, to transistors T_1 and T_2 of the gain stage.

Also in the second of the contemplated instances, with reference to Fig. 3b, it may be observed that the current measured on the sensing resistor R_S will be:

$$\begin{aligned} {}_{E2} &= I_{C2} + I_{B2} = I_{C2} + I_{E1} \\ &= I_L + I_{E1} \end{aligned}$$

it is therefore admitted an error of magnitude equal to the base current of transistor T_2 which, under saturation conditions of the same transistor T_2, may not be negligible.

Such problems of loss of precision consequential to the necessity of reducing the voltage drop across the C and E nodes of the current gain stage by connecting the collector of transistor T_1 (driver) to a distinct circuit block, are overcome in an effective way by utilizing the current gain stage object of the present invention.

As schematically illustrated in Fig. 4a which represents the same type of application already examined in the preceding Figures 2a and 3a, the current gain stage of the invention contemplates the connection of the collector of transistor T_1 (driver) to an auxiliary current mirror AUX 1. The output current of said auxiliary current mirror, I_{OUT1}, is then added to the output current, I_{OUT2}, of the current mirror driven by the gain stage as a correction current.

In this way, assuming that the current mirrors be precise, it may easily be observed that:

$$\begin{aligned} I_{OUT} &= I_{OUT1} + I_{OUT2} \\ I_{OUT1} &= I_{C1} = I_{E1} - I_{B1} \\ I_{OUT2} &= I_{C2} = I_{E2} - I_{B2} \end{aligned}$$

and given that:

$$I_{B2} = I_{E1}$$

one has:

$$\begin{aligned} I_{OUT1} + I_{OUT2} &= I_{E1} - I_{B1} + I_{E2} - I_{B2} \\ &= I_{B2} - I_{B1} + I_{E2} - I_{B2} \\ &= I_{E2} - I_{B1} \end{aligned}$$

Thus, the imprecision of the output current results reduced to a magnitude equal only to the base current of transistor T_1 which, as may be evidenced through easy considerations, is inferior by a factor equal to β^2 with respect to the emitter current of the same transistor T_2 and thence such an imprecision results of magnitude certainly negligible.

The diagram of Fig. 4b illustrates the current gain stage of the invention applied to the same circuit situation already examined with reference to Figures 2b and 3b.

In this instance, the addition of the collector current of transistor T_1 to the output current of the current gain stage is made by drawing from node C, that is directly from the load, using to this aim a second auxiliary current mirror AUX 2, a current equal to the collector current of transistor T_1. Also in this instance, assuming the current mirrors to be precise, it may easily be observed that:

$$\begin{aligned} I_L &= I_{C2} + I_{E1} \\ I_{sens} &= I_{E2} = I_{C2} + I_{C1} + I_{B1} = \\ &= I_L + I_{B1} \end{aligned}$$

That is the imprecision of the output currents results of magnitude equal to the base current I_{B1} of transistor T_1 (driver) and so practically negligible.

The description proceeds now to illustrate few typical examples of circuit situations wherein the gain stage object of the present invention finds a

particularly effective utilization.

In some integrated ciruits may be necessary setting from outside by means of a reference voltage and/or resistor R_{ref}, a current for internal uses. In these instances, the typical structure is the one shown in Fig. 5, wherein it may be observed that to a differential stage (input transconductance stage) OTA follows a current gain stage of the Darlington's type for driving the output current mirror.

The reference voltage V_{ref}, applied across the reference resistor R_{ref}, sets the emitter current of transistor T_2.

Therefore the value of the output current I_{OUT} should be the most precisely close to the value of the current I_{ref} as possible.

The maximum value admitted for the voltage V_{ref} is:

$$V_{ref,\ max}=V_s-(V_{BET2}+V_{CEsatT1})-V_{ds}$$

where:

V_s =supply voltage and

V_{ds}=minimum drop necessary for the operation of the output current mirror.

Generally the selection of a certain current mirror is dictated by precision requirements because normally a current mirror with high characteristics of precision has a more complex circuit and therefore presents a higher voltage drop necessarily. It is common practice, therefore, to reduce the voltage drop due to the current gain stage making it, to the limit, equal only to the value $V_{CEsatT2}$, in accordance with the technique described in relation to Fig. 3a, but that, as has been observed, implies the introduction of a non-negligible imprecision in the transfer of the data (that is imprecision of I_{OUT} as a function of V_{ref}).

The application of the current gain stage of the invention in this particular instance may be implemented as shown in the diagram of Fig. 6 wherein the symbols and the designations of the various components or blocks are the same of those used in the preceding figures and wherein the output current mirror and the auxiliary current mirror AUX 1 are shown according to one of the possible circuital implementations of the same.

As it may be easily observed, the utilization of the current gain stage of the invention in this specific instance, allows increasing the superior limit for the voltage V_{ref}, or employing a more complex current mirror (more precise) at the output for example, as shown in Fig. 6, a Wilson's mirror which is an extremely precise mirror but requires a larger dynamics.

In integrated systems of the switching kind, the output current, that is the current supplied by the current gain stage to a load Z_L, is controlled under feed back by means of measuring across the sensing resistor R_S and by comparing with a reference voltage V_{ref} as shown in the diagram of Fig. 7.

Utilizing in place of the Darlington of Fig. 7 the current gain stage of the invention, as shown in Fig. 8, it is possible to increase the voltage applied to the load Z_L, thus reducing the minimum drop of the gain stage only to $V_{CEsatT2}$, though maintaining a high level of precision in the output current. In fact the collector current of transistor T_1 (driver) is added directly across the load Z_L to the output current of transistor T_2 by mirroring the collector current of T_1 through the two auxiliary current mirrors AUX 1 and AUX 2 identified, respectively, by the two dash line rectangles of Fig. 8.

CLAIMS

1. A current gain stage comprising two transistors T_1 and T_2 substantially connected in cascade characterized in that the collector of the first transistor T_1 is connected to a current mirror the output current of which is substantially added to the output current of the stage.

2. The stage of claim 1 wherein the output current of said current mirror is added to the output current of an output current mirror driven by the collector current of transistor T_2.

3. The stage of claim 1 wherein the output current of said current mirror is added directly on a load driven by transistor T_2 by means of a second current mirror.

4. A current gain stage substantially as described herein with reference to figs. 4a to 8 of the accompanying drawings.

Printed for Her Majesty's Stationery Office by Courier Press, Leamington Spa, 6/1987. Demand No. 8991685.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.