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(54) METHOD AND APPARATUS FOR DISPLAYING TEST RESULTS AND RECORDING MEDIUM

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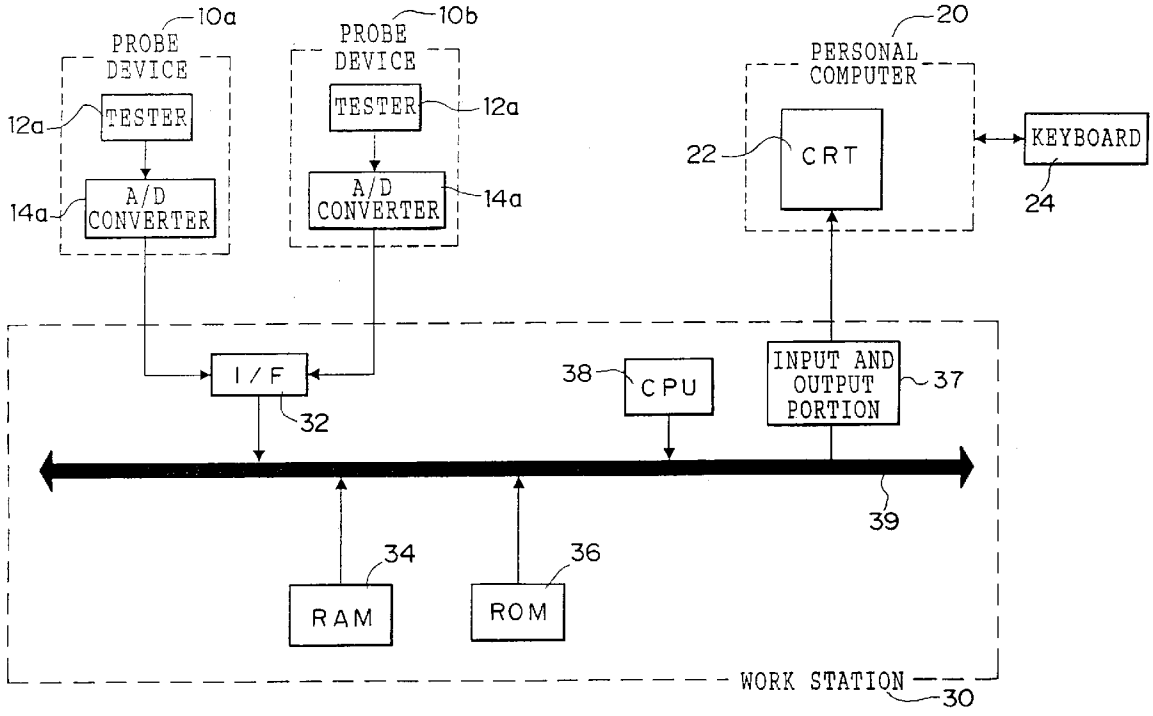
(57) **ABSTRACT**

There are provided a method and an apparatus for displaying test results and a recording medium, which allow easy detection of DUT's in which probes are destroyed. The apparatus has two wafer probers, a work station, and a PC. On the basis of a display program and a display mode switching program stored in a ROM of the work station, respective test results of testing semiconductor chips by the two wafer probers are displayed on a CRT of the PC in correspondence to positions of the semiconductor chips on a wafer substrate, and, at the same time, a pass/fail ratio for each of the DUT's is displayed in parallel with the test results of the semiconductor chips.



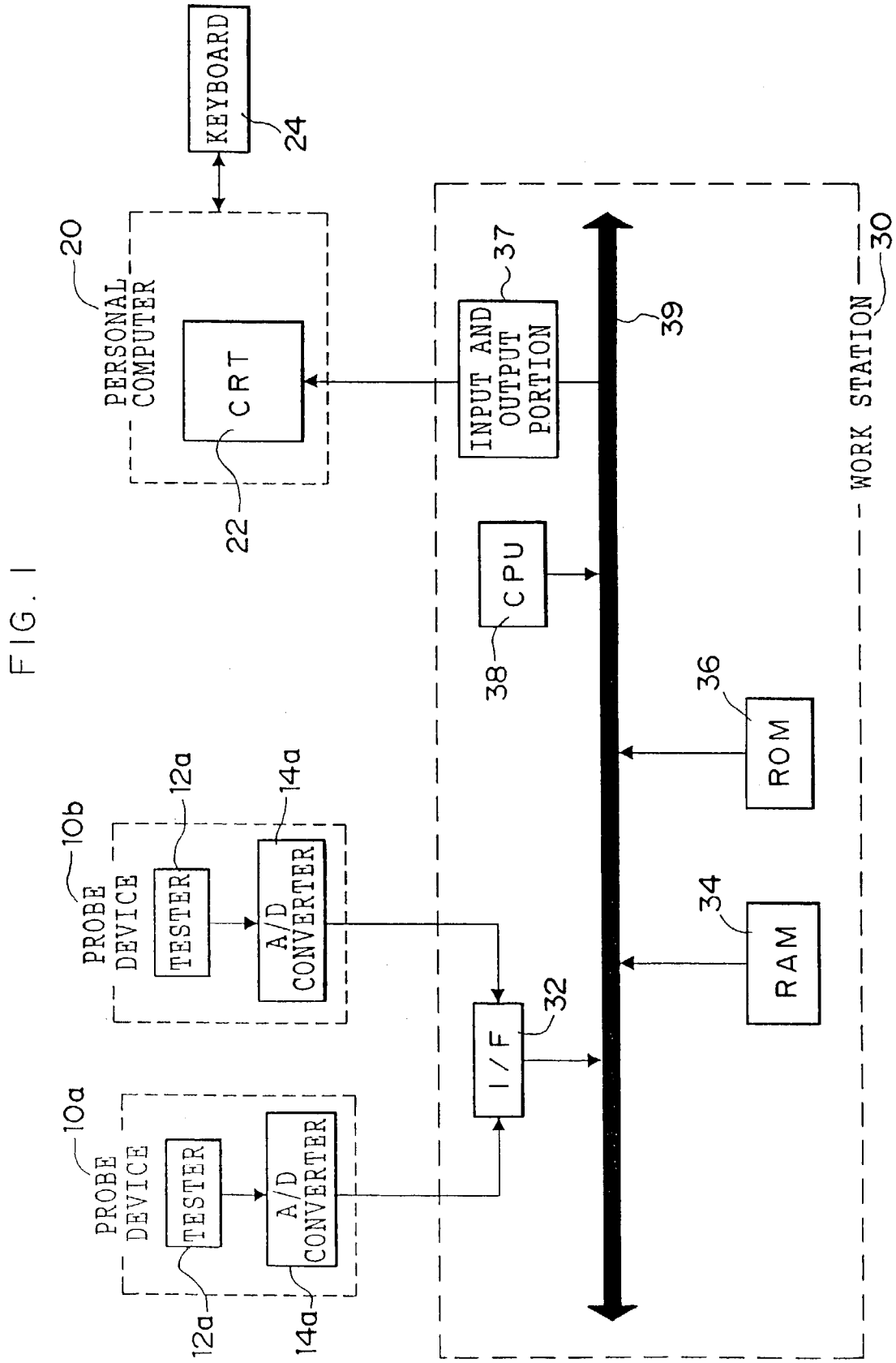

KEYBOARD
24
20
PERSONAL COMPUTER
CRT
22
INPUT AND OUTPUT PORTION
37
39
WORK STATION
30
CPU
38
36
ROM
34
RAM
32
I/F
10b
PROBE DEVICE
TESTER
12a
A/D CONVERTER
14a
10a
PROBE DEVICE
TESTER
12a
A/D CONVERTER
14a

FIG. 1

FIG. 2

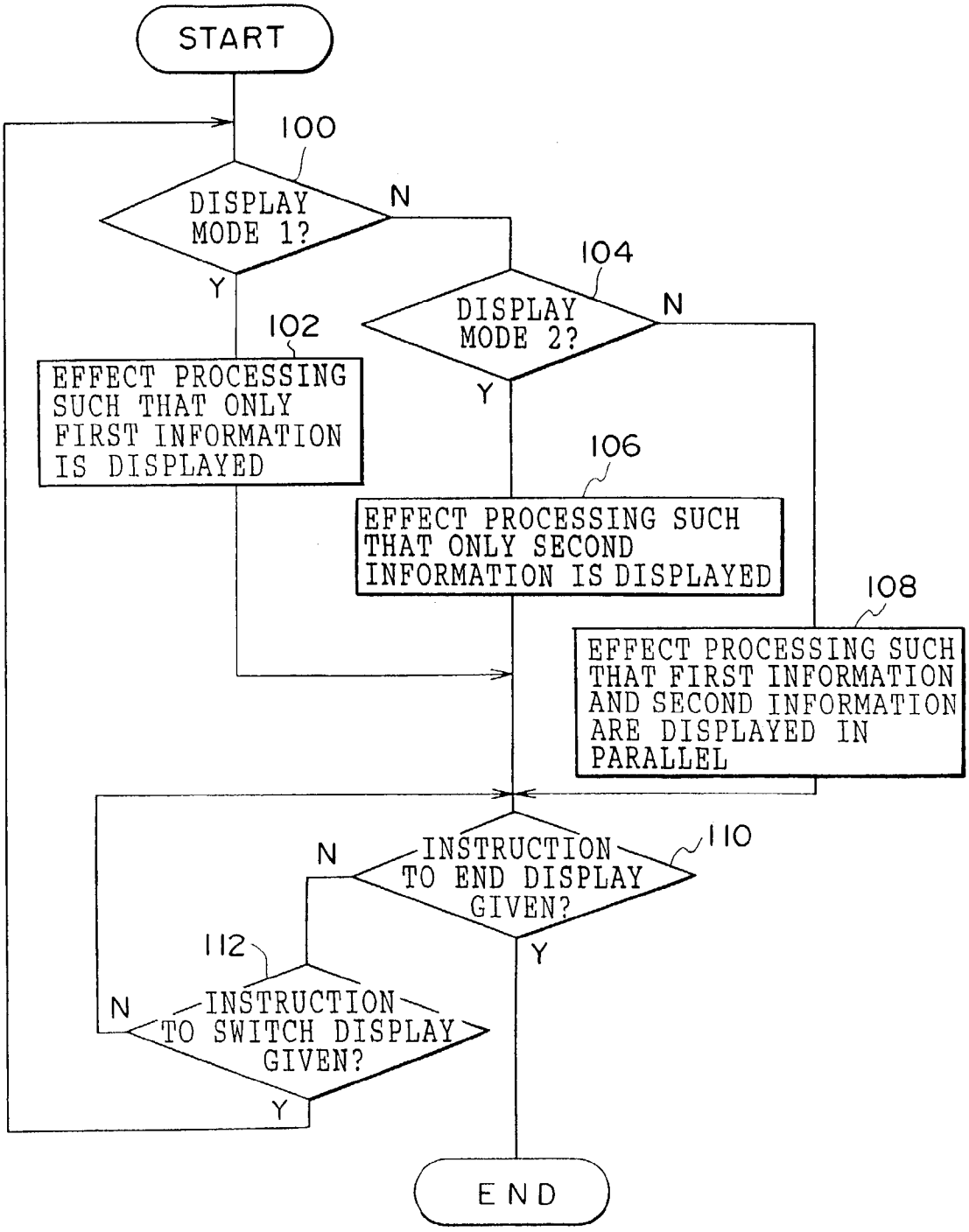
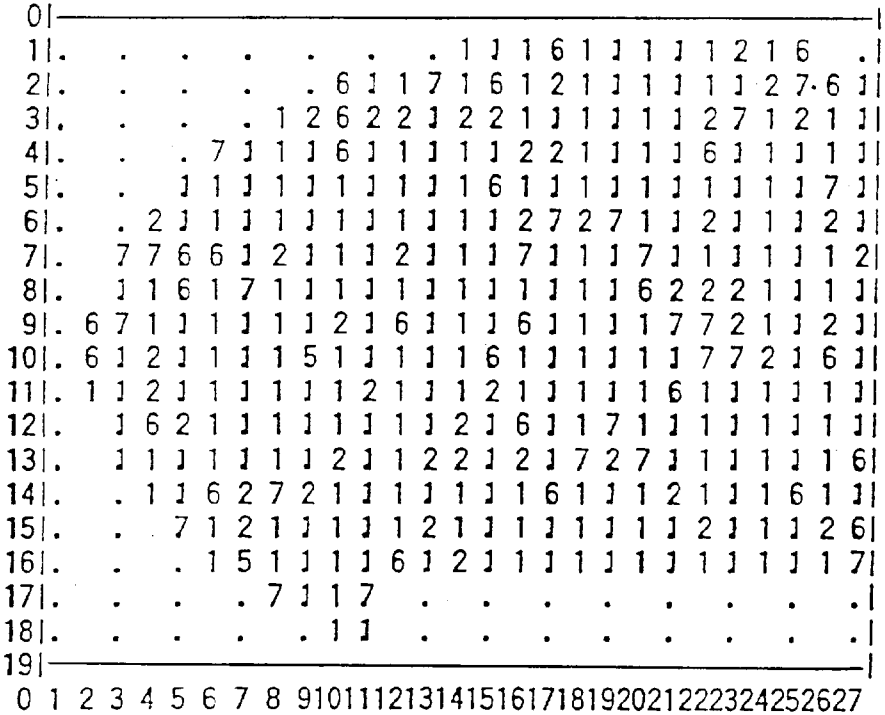

START
100
DISPLAY MODE 1?
N
Y
104
DISPLAY MODE 2?
N
Y
102
EFFECT PROCESSING SUCH THAT ONLY FIRST INFORMATION IS DISPLAYED
106
EFFECT PROCESSING SUCH THAT ONLY SECOND INFORMATION IS DISPLAYED
108
EFFECT PROCESSING SUCH THAT FIRST INFORMATION AND SECOND INFORMATION ARE DISPLAYED IN PARALLEL
110
INSTRUCTION TO END DISPLAY GIVEN?
N
Y
112
INSTRUCTION TO SWITCH DISPLAY GIVEN?
N
Y
END

FIG. 3A

FIRST PROBE DEVICE

TESTED: 488 PASSED: 416 FAILED: 72 YIELD: 85.2%



DUT No.	TOTAL NUMBER	DETECTION RATIO OF GOOD PRODUCTS	DETECTION RATIO OF VOLTAGE FAILURE	DETECTION RATIO OF OPERATION FAILURE
1	26	92.3%	0.0%	7.7%
2	29	82.8%	10.3%	6.9%
3	31	93.5%	6.5%	0.0%
4	33	81.8%	15.2%	3.0%
5	34	79.4%	2.9%	17.6%
6	33	90.9%	0.0%	9.1%
7	32	75.0%	12.5%	12.5%
8	26	84.6%	3.8%	11.5%
9	26	92.3%	3.8%	3.8%
10	29	96.6%	0.0%	3.4%
11	31	74.2%	9.7%	16.1%
12	33	84.8%	6.1%	9.1%
13	34	94.1%	2.9%	2.9%
14	33	84.8%	9.1%	6.1%
15	32	81.3%	12.5%	6.3%
16	26	76.9%	11.5%	11.5%

FIG. 3B

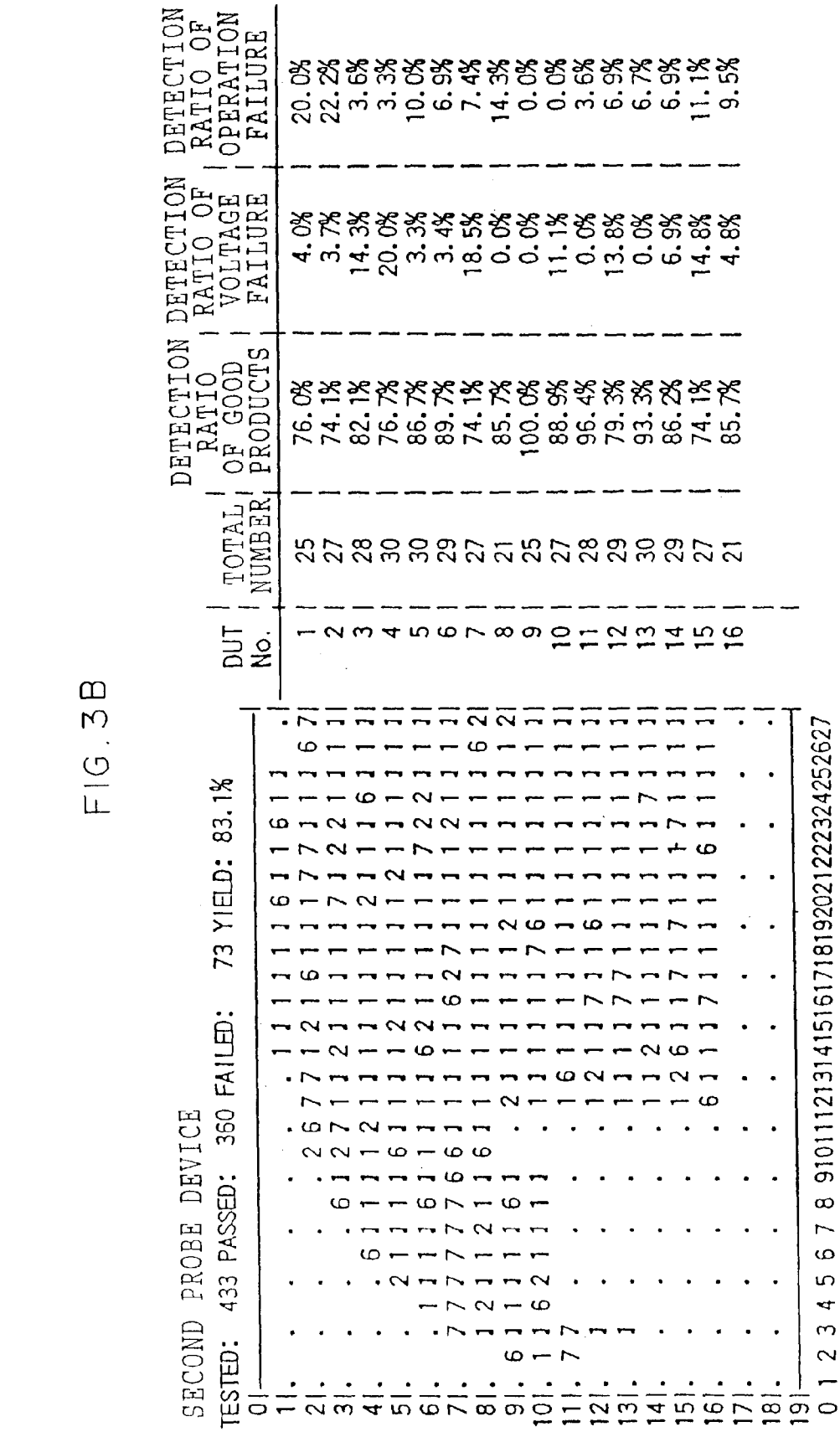

SECOND PROBE DEVICE
TESTED: 433 PASSED: 360 FAILED: 73 YIELD: 83.1%
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
DUT No. | TOTAL NUMBER | DETECTION RATIO OF GOOD PRODUCTS | DETECTION RATIO OF VOLTAGE FAILURE | DETECTION RATIO OF OPERATION FAILURE
1 | 25 | 76.0% | 4.0% | 20.0%
2 | 27 | 74.1% | 3.7% | 22.2%
3 | 28 | 82.1% | 14.3% | 3.6%
4 | 30 | 76.7% | 20.0% | 3.3%
5 | 30 | 86.7% | 3.3% | 10.0%
6 | 29 | 89.7% | 3.4% | 6.9%
7 | 27 | 74.1% | 18.5% | 7.4%
8 | 21 | 85.7% | 0.0% | 14.3%
9 | 25 | 100.0% | 0.0% | 0.0%
10 | 27 | 88.9% | 11.1% | 0.0%
11 | 28 | 96.4% | 0.0% | 3.6%
12 | 29 | 79.3% | 13.8% | 6.9%
13 | 30 | 93.3% | 0.0% | 6.7%
14 | 29 | 86.2% | 6.9% | 6.9%
15 | 27 | 74.1% | 14.8% | 11.1%
16 | 21 | 85.7% | 4.8% | 9.5%

FIG. 4

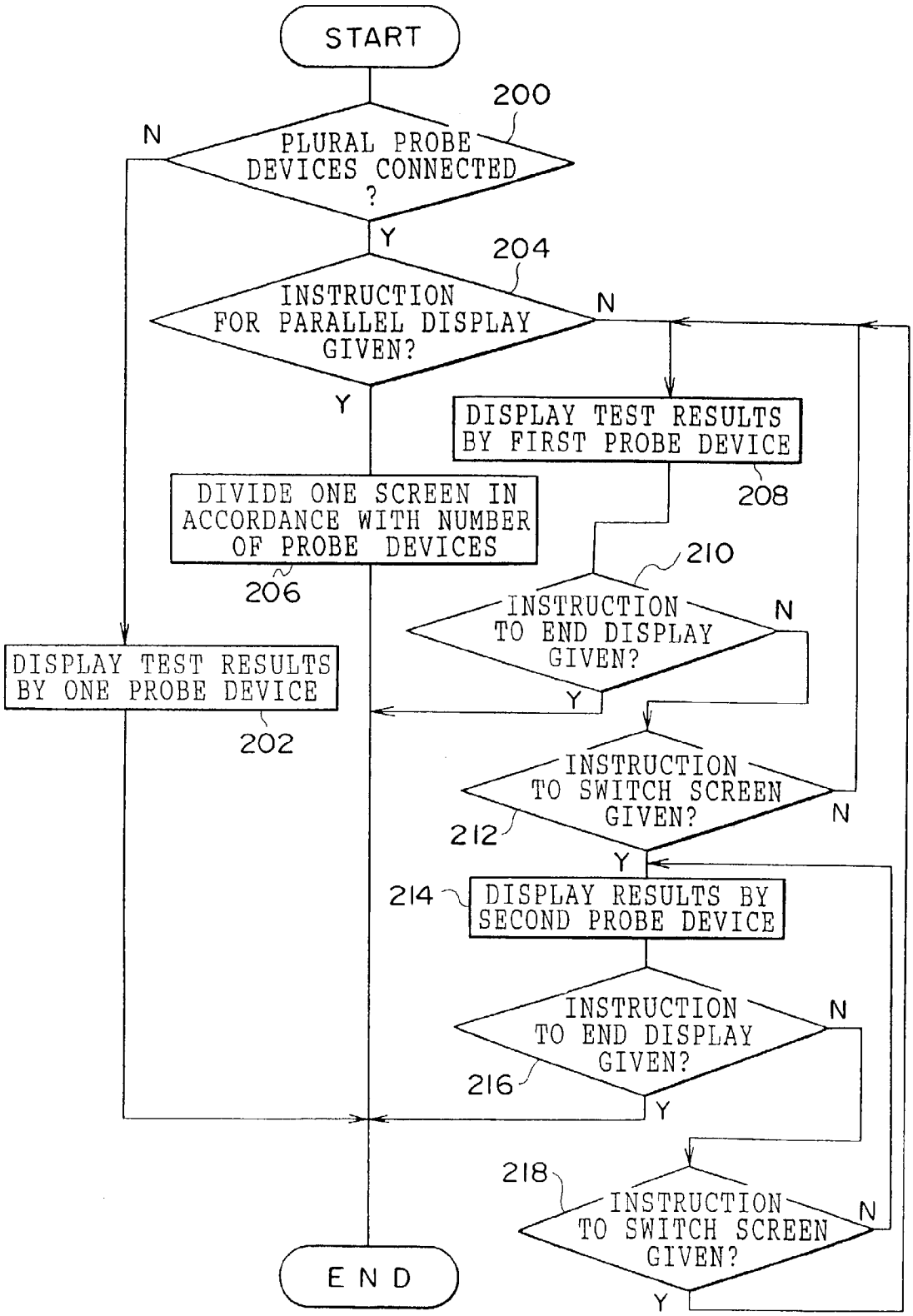

START
200
PLURAL PROBE DEVICES CONNECTED ?
N
Y
204
INSTRUCTION FOR PARALLEL DISPLAY GIVEN?
N
Y
DISPLAY TEST RESULTS BY FIRST PROBE DEVICE
208
DIVIDE ONE SCREEN IN ACCORDANCE WITH NUMBER OF PROBE DEVICES
206
210
INSTRUCTION TO END DISPLAY GIVEN?
N
Y
DISPLAY TEST RESULTS BY ONE PROBE DEVICE
202
INSTRUCTION TO SWITCH SCREEN GIVEN?
212
N
Y
214
DISPLAY RESULTS BY SECOND PROBE DEVICE
INSTRUCTION TO END DISPLAY GIVEN?
216
N
Y
218
INSTRUCTION TO SWITCH SCREEN GIVEN?
N
Y
END

FIG. 5A

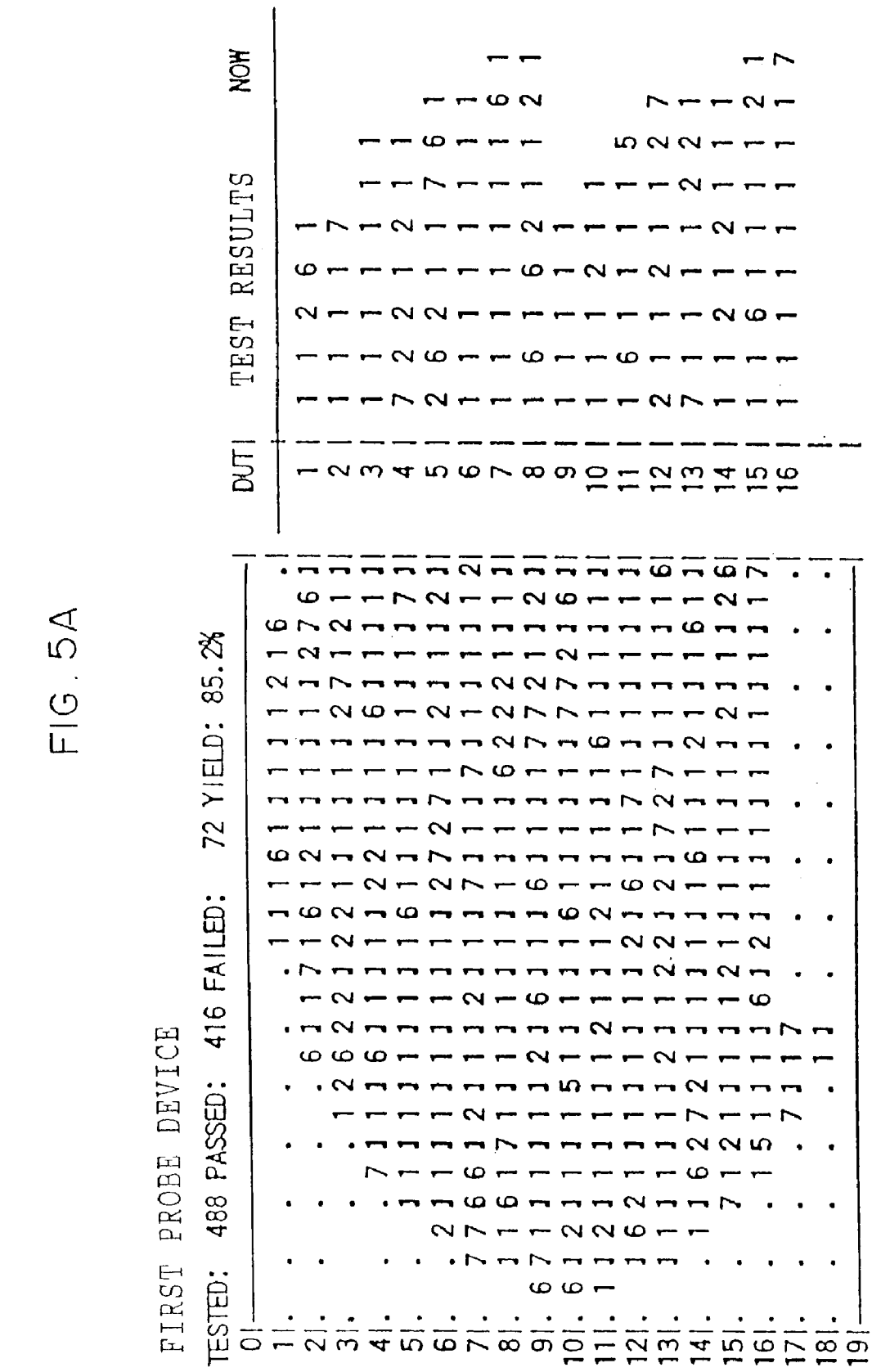
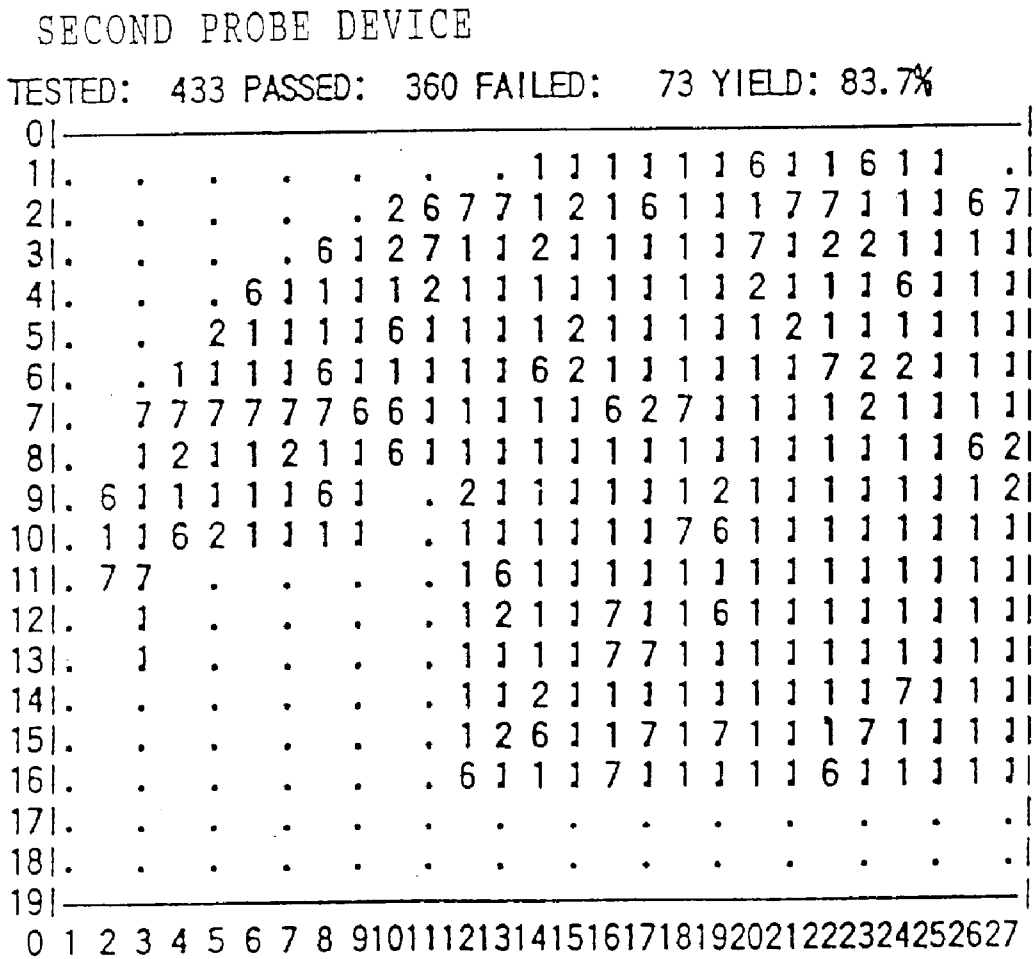

FIRST PROBE DEVICE
TESTED: 488 PASSED: 416 FAILED: 72 YIELD: 85.2%
DUT| TEST RESULTS NOW
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27

FIG. 5B



DUT	TEST RESULTS								NOW
1	1	1	1	6	1	1	7	1	6
2	1	1	1	1	1	1	1	6	1
3	1	1	7	1	1	1	1	2	1
4	1	1	1	1	1	1	7	1	1
5	1	1	1	1	1	1	7	1	1
6	1	1	1	1	1	1	1	1	1
7	1	1	1	1	1	7	1	1	1
8	1	1	1	1	1	1	1	1	2
9	1	1	1	1	1	1	1	1	1
10	1	1	1	7	1	7	7	1	2
11	1	1	1	1	1	1	1	1	1
12	1	1	1	1	1	1	7	1	1
13	1	1	1	1	1	6	1	1	2
14	1	1	1	1	1	1	1	1	6
15	1	1	1	1	1	6	1	1	1
16	1	2	1	1	1	2	1	1	1

LEVEL OF CHIP	DETECTED NUMBER OF CHIPS
1	
2	
3	
4	
5	
6	
7	

FIG. 6

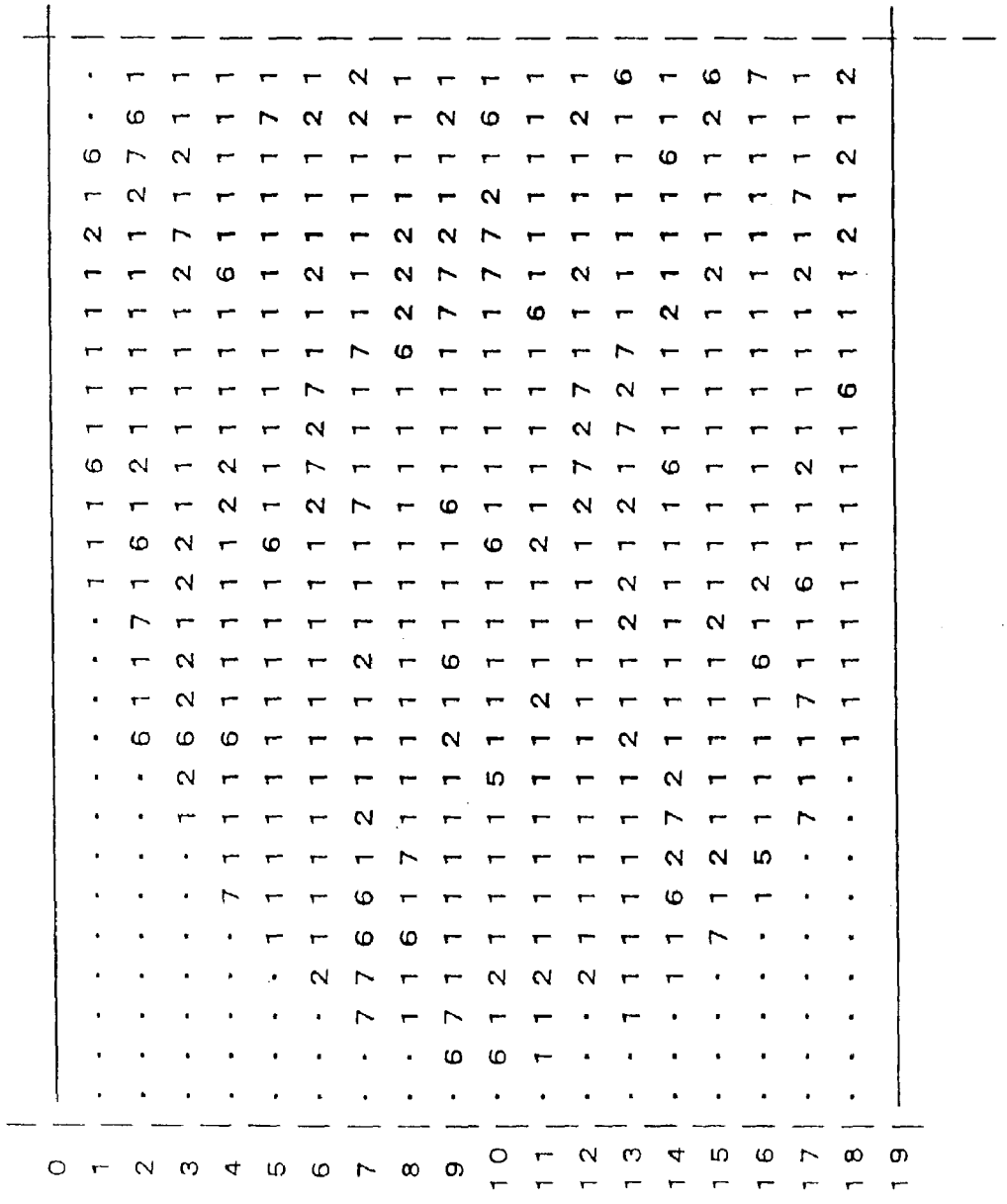


FIG. 7

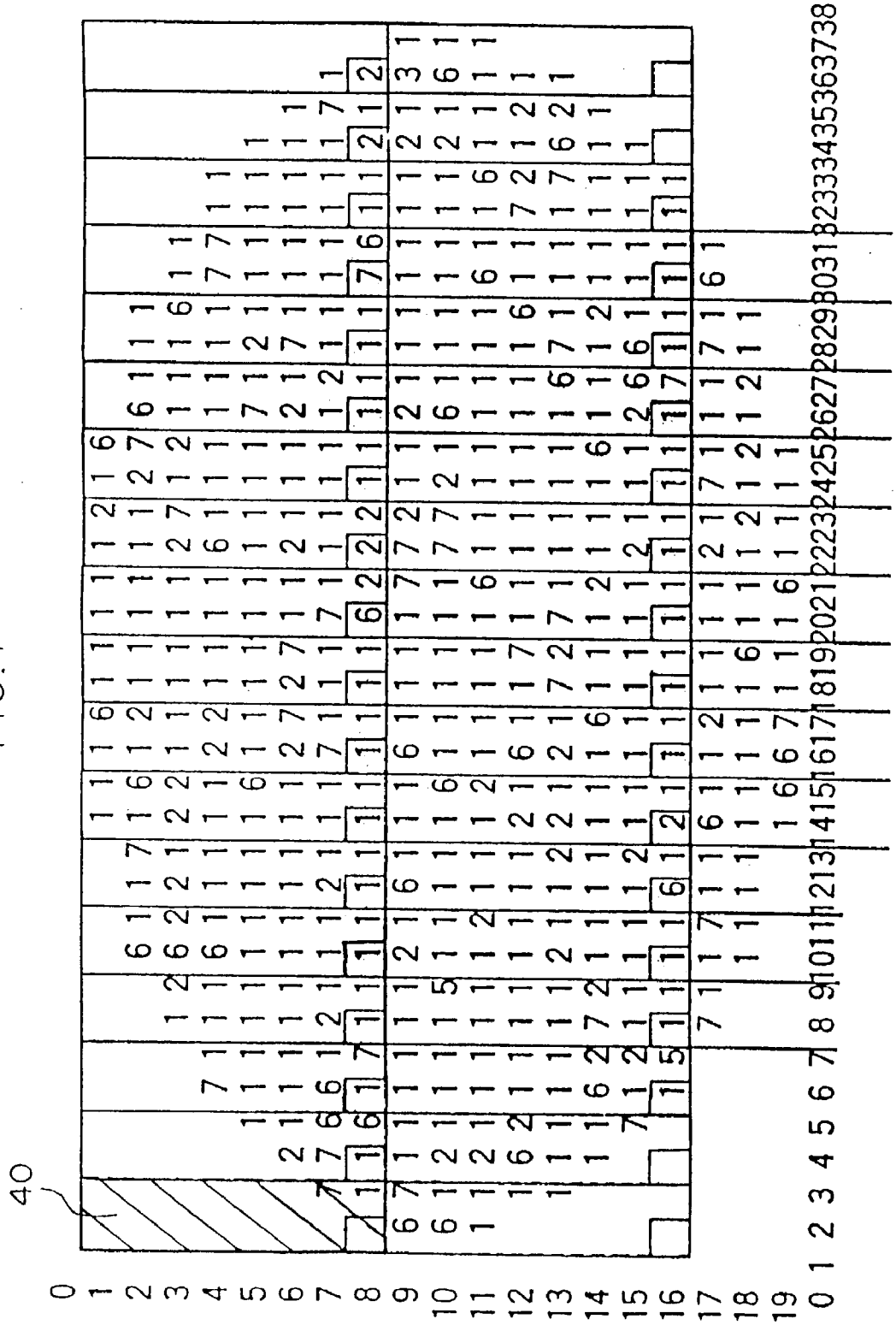
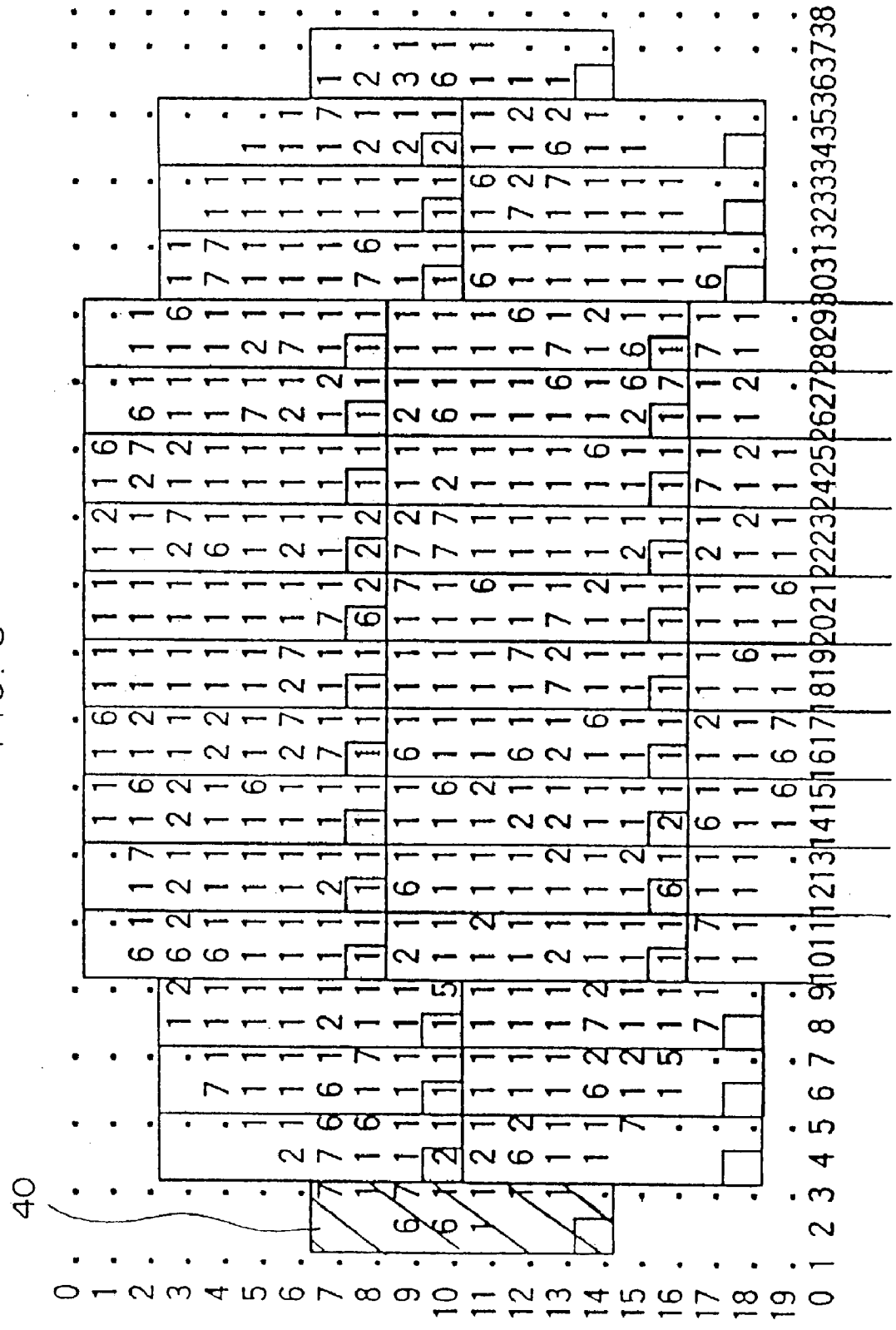

40
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38

FIG. 8



METHOD AND APPARATUS FOR DISPLAYING TEST RESULTS AND RECORDING MEDIUM

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an apparatus and method for displaying test results, and to a recording medium, and in particular, to an apparatus and method for displaying results of a test in which each of a plurality of semiconductor chips formed on a wafer substrate is tested, and to a recording medium on which a display program is recorded.

[0003] 2. Description of the Prior Art

[0004] Conventionally, for example, a predetermined voltage is applied to each of semiconductor chips formed on a wafer substrate to carry out a test (a probe test or the like) to check whether memories and devices formed on the semiconductor chips are operating in a normal state by checking whether predetermined voltage value which the chip was designed to exhibit is in fact detected when the predetermined voltage is applied to the semiconductor chips. In this way, the quality of the chips (memories and devices) is checked.

[0005] At this time, as shown in **FIG. 6**, numbers (1-7) indicative of the results of the test of the chips are displayed on a screen in correspondence with the each of positions of the semiconductor chips on the wafer substrate. At the same time, the number of semiconductor chips detected as having a given value (one of 1-7) is displayed on the screen for each of the detected values. These numbers (1-7) indicate the quality level of the semiconductor chips. For example, the number 1 denotes a good quality, 2 denotes a quality that can be made good through a very simple correction processing, 3 denotes a quality that can be made good through a relatively simple correction processing, 4 denotes a quality that can be made good through a complicated correction processing, 5 denotes a device failure (defective device), 6 denotes a memory failure, and 7 denotes a function failure. The quality level is determined every time in accordance with the test contents and the test results.

[0006] By summing up such quality level, the quality level (failure level) in which the detected number of the semiconductor chips is large is clarified. The causes of the failure are investigated and the results of the investigation are fed back to the manufacturing step for the prevention failures for the same reason the next time the product is manufactured.

[0007] Generally, in testing semiconductor chips, a wafer prober or the like is used which has a tester having a plurality of groups of probes which are each a test portion for testing one semiconductor chip. The wafer prober is used to carry out parallel measurement for testing a plurality of semiconductor chips at the same time, thereby shorting the test time.

[0008] For example, there will be considered a case of a wafer prober in which a tester having sixteen groups of probes arranged in eight rows and two columns is provided. The semiconductor chips formed on the wafer substrate are positioned in rows and columns as shown in **FIG. 7**. As shown in **FIG. 7**, the tester is disposed at a test start reference position (the slanted line region of **FIG. 7**). In the case where a semiconductor chip corresponding to at least one of the sixteen groups of probes of the tester is present, the semiconductor chip is tested by the group of probes corresponding thereto. When the test by the groups of probes is completed, the tester is shifted two rows, and a test region **40** is shifted by two rows. When a semiconductor chip is present which corresponds to at least one of the probes, the semiconductor chip is tested with the group of probes corresponding thereto. When testing of all the semiconductor chips formed at the positions of rows one to eight on the wafer substrate is completed by repeating the aforementioned process, the tester is returned to the test start reference position and is shifted eight columns. Thereafter, testing of the semiconductor chips formed at the positions of rows nine to sixteen on the wafer substrate is carried out as described above.

[0009] By repeating such operations, all of the 536 semiconductor chips formed on one wafer substrate are tested by the movement of the tester 48 times (carrying out testing 48 times).

[0010] Shortening of the test time is important in terms of improving manufacturing efficiency. Conventionally, there has been proposed a wafer prober that is capable of moving the tester freely in order to carry out testing in a short time. As shown in **FIG. 8**, there is proposed a system in which the test region **40** can be set in correspondence with the configuration of a disc-shaped wafer substrate by moving the tester along the configuration of the disc-like wafer substrate so that the number of times testing is carried out by the tester is decreased.

[0011] In the example shown in **FIG. 7**, all of the 536 semiconductor chips are tested by carrying out testing 48 times. However, by moving the tester in accordance with the configuration of the disc-shaped wafer substrate, it becomes possible to test all of the 536 semiconductor chips in 44 tests. The time required for testing can thus be shortened by the amount of time required for four tests.

[0012] Since the semiconductor chips are very small and the electrodes formed on the semiconductor chips are also considerably minute, the probe for applying voltage to the semiconductor chips by contacting the electrode of the chip is also extremely small. As a result, the probe is liable to be broken because a load is applied to the probe during the movement of the tester, or the probe gets caught on the edge of the wafer substrate.

[0013] Accurate test results cannot be obtained from damaged probes. Thus, even a good quality semiconductor chip which is subjected to testing may be detected as being a poor product. Such incorrect test results are unfavorable. Therefore, it is necessary to detect at an early stage the fact that the probe has been damaged, so that adjustments to the semiconductor test device can be made and the test instruments can be checked with a view to restoring normal operation in a short time.

[0014] Conventionally, when results of testing the semiconductor chip (the quality levels of the semiconductor chips) are displayed on the screen in correspondence to the positions of the semiconductor chips on the substrate, the relative position of the probe with respect to the tester (test subject lane, hereinafter referred to as DUT (Device under Test)) is displayed on the screen in an overlaid manner on the test results of the semiconductor chips on the monitor, so that the operator can detect the damage caused to the probe as soon as possible.

[0015] With a wafer prober in which the movement of the tester is restricted, for example, as shown in **FIG. 7**, since each of the DUT's is shifted (arranged) along the same column on the wafer substrate, the damage on the probe can be detected relatively easily. However, in a case where testing is carried out by using a wafer prober in which the tester is moved freely, for example, as shown in **FIG. 8**, the respective DUT's are not necessarily shifted along the same column on the wafer substrate. Thus, it is difficult to detect at an early stage which of the DUT's of the probe is damaged.

[0016] Furthermore, in recent years, owing to the smaller sizing resulting from the shrinkage or the like of the semiconductor chips and an increase in the diameter of the wafer substrate, the number of chips which can be formed on a single wafer substrate has become very large. As a result, it becomes difficult to display on one screen of the monitor the test results for one wafer substrate. Therefore, only a portion of the test results for one wafer substrate is displayed on one screen of the monitor. For this reason as well, it is difficult to correspond each of the semiconductor chips being tested by the one of the DUT's with each of the DUT's, and thus, it becomes difficult to detect at an early stage which of the probes of the DUT are damaged.

SUMMARY OF THE INVENTION

[0017] In view of the aforementioned, the present invention aims to provide a method and an apparatus for displaying test results, and a recording medium, which provide easy detection of which of the probe of the DUT is damaged.

[0018] In order to attain the above object, the first aspect of the present invention is a method for displaying test results comprising the step of: on the basis of test results obtained by a tester provided with plural testing portions, each of the testing portions testing a plurality of semiconductor chips formed on a wafer substrate, displaying on a same screen of displaying means two types of information which are a first information which expresses test results of the semiconductor chips in accordance with positions of the semiconductor chips on the wafer substrate, and a second information which expresses test results of the semiconductor chips for the respective testing portions of the tester.

[0019] The second aspect of the present invention is a method for displaying test results according to the first aspect, wherein at least two of the two types of information obtained from at least two testers are displayed on the same screen of the displaying means.

[0020] The third aspect of the present invention is a method for displaying test results according to the first or the second aspect, wherein a display mode is switchable between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first information and the second information on the screen of the displaying means.

[0021] The forth aspect of the present invention is a method for displaying test results according to any one of the first to third aspect, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

[0022] The fifth aspect of the present invention is an apparatus for displaying test results comprising: control means for controlling a displaying means such that, on the basis of test results obtained by a tester provided with plural testing portions, each of the testing portions testing a plurality of semiconductor chips formed on a wafer substrate, the displaying means displays on a same screen two types of information which are a first information which expresses test results of the semiconductor chips in accordance with positions of the semiconductor chips on the wafer substrate, and a second information which expresses test results of the semiconductor chips for the respective testing portions of the tester.

[0023] The sixth aspect of the present invention is an apparatus for displaying test results according to fifth aspect, wherein the control means is connected to at least two testers, and controls the displaying means so that at least two of the two types of information which are obtained from each of the testers are displayed on the same screen of the displaying means.

[0024] The seventh aspect of the present invention is an apparatus for displaying test results according to fifth or sixth aspect, further comprising switching means for switching a display mode between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first and the second information on the screen of the displaying means.

[0025] The eighth aspect of the present invention is an apparatus for displaying test results according to any one of fifth to seventh aspect, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

[0026] The ninth aspect of the present invention is a recording medium which can be read by a computer, the medium having a display program recorded therein for, on the basis of test results obtained by a tester provided with plural testing portions, each of the testing portions testing a plurality of semiconductor chips formed on a wafer substrate, displaying on a same screen of displaying means two types of information which are a first information which expresses test results of the semiconductor chips in accordance with positions of the semiconductor chips on the wafer substrate, and a second information which expresses test results of the semiconductor chips for the respective testing portions of the tester.

[0027] The tenth aspect of the present invention is a recording medium according to ninth aspect, wherein a parallel display program, for displaying in a parallel manner and on the same screen, at least two sets of the two types of information inputted independently from at least two testers, is also recorded on the recording medium.

[0028] The eleventh aspect of the present invention is a recording medium according to ninth or tenth aspect, wherein a display switch program, for switching a display mode between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for

displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first information and the second information on the screen of the displaying means, is also recorded on the recording medium.

[0029] The twelfth aspect of the present invention is a recording medium according to any one of ninth to eleventh aspect, wherein the test results of the second information is at least one of a detection ratio of detective semiconductor and a value reflecting the detection ratio.

[0030] In other words, in the first aspect, two types of information are displayed on the same screen: first information which expresses test results of the semiconductor chips in accordance with positions on the wafer substrate of the semiconductor chips which have been tested, and second information which expresses the test results of the semiconductor chips, each of the chips being tested by one of the plurality of test portions, for each of the testing portions of the tester. Therefore, the operator can confirm by the first information the test results of the semiconductor chips which are formed on the wafer substrate, and can confirm by the second information the test results of each of the test portions. Consequently, it is easy to confirm the presence of abnormalities in each of the plurality of the test portions, so that breakage of and trouble with the test portions can be immediately detected.

[0031] Even in the case where the semiconductor chips which should be tested by the tester are randomly selected, by using the display of the second information, it can immediately be detected whether the test results of any of the plural testing portions are abnormal. Thus, it is possible to detect at an early stage breakage of or trouble with the test portions.

[0032] In order to realize the method of the first aspect, for example, as described in the fifth aspect, an apparatus for displaying test results may be provided with a control means for controlling the displaying means so that the two types of information (the first information and the second information) are displayed on the same screen.

[0033] Furthermore, as described in the second aspect, the results of simultaneously testing semiconductor chips formed individually on each of at least two wafer substrates can be confirmed at one time by displaying on the same screen at least two of the two kinds of information obtained at least from two testers, thereby increasing efficiency.

[0034] In order to realize the method according to the second aspect, as in the sixth aspect, the apparatus for displaying test results may be structured such that a control means controls the display means so that at least two of the aforementioned two kinds of information obtained from at least two testers can be displayed on the same screen.

[0035] Furthermore, as in the third aspect, it is possible to selectively display only information required by the operator by switching between at least three display modes which are a first display mode for displaying only the first information, a second display mode for displaying only the second information, and a third display mode for displaying both the first and second information.

[0036] In order to realize the method according to the third aspect, for example, as in the seventh aspect, the apparatus for displaying test results may be structured so as to further comprise switching means for switching the display mode of the displaying means between at least the three display modes which are the first display mode, the second display mode, and the third display mode.

[0037] In this case, as in the second and the sixth aspects, the invention is advantageous in cases where there is a large amount of display information, as in the case where testing of the semiconductor chips formed on each of at least two wafer substrates is carried out simultaneously in a parallel manner.

[0038] On the basis of test results obtained by a tester provided with plural testing portions, each of the testing portions testing a plurality of semiconductor chips formed on a wafer substrate, the method for displaying test results of the first aspect and the apparatus for displaying test results of the fifth aspect effect processing on the basis of a display program for displaying on a same screen of displaying means two types of information which are a first information which expresses test results of the semiconductor chips in accordance with positions of the semiconductor chips on the wafer substrate, and second information which expresses test results of the semiconductor chips for the respective testing portions of the tester.

[0039] This display program is recorded on a recording medium that can be read by a computer, as in the ninth aspect. Thus, the display program can be applied such that after the display program is installed from the recording medium onto a predetermined region of the apparatus for displaying test results, the apparatus for displaying test results is controlled by the program, or such that the display program is directly read from the recording medium and the apparatus for displaying test results is controlled by the program.

[0040] Furthermore, in addition to the display program as in the ninth aspect, the recording medium according to the tenth aspect further includes a parallel display program for displaying in a parallel manner and on the same screen at least two sets of the two types of information inputted independently from at least two of the testers, is also recorded on the recording medium. The apparatus for displaying test results as in sixth aspect carries out processing on the basis of this parallel display program.

[0041] This parallel display program can be applied such that after the display program is installed from the recording medium onto a predetermined region of the apparatus for displaying test results, the apparatus for displaying test results is controlled, or such that the display program is directly read from the recording medium and the apparatus for displaying test results is controlled.

[0042] Furthermore, in addition to the display program as in the ninth or tenth aspect, the recording medium in eleventh aspect further includes a display switching program for switching the display mode of the displaying means between at least three display modes which are a first display mode for displaying only the first information, a second display mode for displaying only the second information, and a third display mode for displaying the first information and the second information. The apparatus for displaying test results of as in seventh aspect carries out processing on the basis of the display switching program.

[0043] The display switching program can be applied such that after the display program is installed from the recording medium onto a predetermined region of the apparatus for displaying test results, the apparatus for displaying test results is controlled, or such that the display program is directly read from the recording medium and the apparatus for displaying test results is controlled.

[0044] The test results of the first information may be a quality level of the semiconductor chip that is determined each time in accordance with the test contents and the required test results. Furthermore, the test results of the second information may be actual test results such as the quality level of the semiconductor chips, in the same manner as the first information. However, the second information may be at least one of a detection rate of poor products (defective semiconductor chips) or a value reflecting a detection rate as can be seen in the forth, eighth and twelfth aspects. The setting of the second information in this manner is preferable because abnormalities in the test results of the test portions can be clearly displayed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0045] **FIG. 1** is a block diagram showing a schematic structure of a semiconductor chip test apparatus according to an embodiment of the present invention.

[0046] **FIG. 2** is a flowchart showing an operation of a CPU based on a display mode switching program in the semiconductor chip test apparatus according to the embodiment of the present invention.

[0047] **FIG. 3**A and **FIG. 3B** are views showing an example of a display of the semiconductor chip test apparatus according to the embodiment of the present invention.

[0048] **FIG. 4** is a flowchart showing an operation of the CPU based on a screen switching program in the semiconductor chip test apparatus of **FIG. 1**.

[0049] **FIG. 5**A and **FIG. 5B** are views showing a different example of a display of the semiconductor chip test apparatus according to the embodiment of the present invention.

[0050] **FIG. 6** is an explanatory view showing a display example of test results by a conventional wafer prober (probe device).

[0051] **FIG. 7** is a view for explaining movement of a test region in a conventional wafer prober in which movement of a tester is limited.

[0052] **FIG. 8** is a view for explaining movement of a test region in a conventional wafer prober in which movement of a tester is not limited.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0053] Embodiments of the present invention will be explained in detail hereinafter by referring to **FIGS. 1 through 4**. In the embodiments, the apparatus and the method for displaying test results according to the present invention are applied to a semiconductor chip test apparatus.

[0054] As shown in **FIG. 1**, the semiconductor chip test apparatus according to the embodiment of the present invention basically comprises a first and a second wafer prober **10***a* and **10***b* which test semiconductor chips of different wafers substrates and which are independent from each other, a work station **30** connected to the first and the second wafer probers **10***a* and **10***b* for processing the output from the two wafer probers **10***a* and **10***b* on the basis of a display program which will be described later, and a personal computer **20** (hereinafter referred to as a PC) **20** for displaying respective test results of the two wafer probers **10***a* and **10***b* on a CRT **22** on the basis of display information from the work station **30**.

[0055] The first wafer prober **10***a* is provided with a tester **12***a* at which are provided sixteen groups of probes arranged in eight rows and two columns. The first wafer prober **10***a* outputs the test results for each of the relative positions of the groups of probes with respect to the tester (a test subject lane, hereinafter referred to as DUT).

[0056] A number indicative of the quality of the semiconductor chip is displayed as test results of the semiconductor chip. For example, the number 1 denotes a good product, 2 a product which can be made good through a very simple correction processing, 3 a product which can be made good through a relatively simple correction processing, 4 a product which can be made good through a complicated correction processing, 5 a device failure, 6 a memory failure, and 7 a function failure. The semiconductor chips which are judged to be levels 1 through 4 are regarded as chips which have "passed" while the semiconductor chips which are judged to be levels 5 through 7 are regarded as chips which have "failed". The total numbers of semiconductor chips which have "passed" and "failed" are counted for each. It goes without saying that the method for displaying the test results is not limited to such a method. The operator can determine the display method depending on the test contents and the required test results each time.

[0057] In addition, a DC power source (not shown) is connected to the tester **12***a*, and a certain level of voltage is applied to each of the sixteen DUT's. The output from each of the sixteen DUT's is converted into a digital value by an A/D converter **14***a*. This output includes position information of the DUT that outputs this output and position information of the tested semiconductor chip on the wafer substrate. The second wafer prober **10***b* has the same structure as the first wafer prober **10***a*, and explanation thereof is omitted.

[0058] The PC **20** displays the test results on the CRT **22** on the basis of the data from an input and output portion **37** (which will be described later). In addition, the PC **20** outputs to the input and output portion **37** an instruction inputted by the operator from a keyboard **24**.

[0059] The work station **30** basically comprises an interface (I/F) **32**, a RAM **34**, a ROM **36**, the input and output portion **37**, and a CPU (a control portion) **38** which are connected via a bus **39**.

[0060] The outputs from the two wafer probers **10***a* and **10***b* are inputted to the interface (I/F) **32**, and are stored in the RAM **34** as two independent test result data from the interface (I/F) **32** through the bus **39**.

[0061] A display program, a display mode switching program and a screen switching program are stored in the ROM **36**. The display program corresponds the test results of the measured semiconductor chips (first information) with the

positions of the semiconductor chips on the wafer substrate. Further, the display program is a program for calculating the pass/fail ratio which is a value reflecting the detection ratio of the defective products for each of the DUT's on the basis of the position information of the respective DUT's and the test results by the respective DUT's.

[0062] The display mode switching program is a program for switching (changing over) the display mode between a display mode **1** for displaying the test results of the semiconductor chips on the CRT **22** of the PC **20** in correspondence with the positions on the wafer substrate, a display mode **2** for displaying on the CRT **22** of the PC **20** the pass/fail ratio for each of the DUT's, and a display mode **3** for displaying on the CRT **22** of the PC **20** the pass/fail ratio for each of the DUT's in parallel with the test results of the semiconductor chips in correspondence with the positions on the wafer substrate. Namely, in the display mode **3**, the pass/fail ratio and the test results are displayed in one screen of the CRT **22**.

[0063] Furthermore, the screen switching program is a program for switching the display mode between a parallel display mode for displaying the test results of each of the wafer probers simultaneously by dividing a screen of the CRT **22** of the PC **20** in accordance with the number of the wafer probers which are connected, and a selected display mode in which one of the wafer probers is selected, the test results of the selected wafer prober are displayed on the entire screen, and instructions may be given to select another wafer prober to display the test results of that wafer prober.

[0064] In the present embodiment, since the two wafer probers **10***a* and **10***b* are connected, processing is performed such that the screen is divided into two portions in the parallel display mode. In addition, in the selected display mode, processing is performed so that the test results of one of the two wafer probers **10***a* and **10***b* are displayed on one screen.

[0065] The CPU **38** reads the data of the test results stored in the RAM **34**, and carries out data processing on the basis of the display program which is called up from the ROM **36**. The data displayed on the CRT **22** of the PC **20** on the basis of the display mode switching program and the screen switching program are output to the input and output portion **37** via the bus **29**. The input and output portion **37** is connected to the PC **20** so that the results of processing by the CPU **38** are output to the PC **20**.

[0066] Here, operation of the CPU **38** on the basis of the display mode switching program will be explained by referring to the flowchart of **FIG. 2**.

[0067] First, at step **100**, a judgment is made as to whether or not the display mode instructed by the PC **20** is the display mode **1**. When it is judged at step **100** that the display mode is the display mode **1**, the process proceeds to step **102** where, on the basis of test results data read from the RAM **34**, processing is performed in such a manner that the test results of the semiconductor chips (the first information) are displayed on the CRT **22** of the PC **20** in correspondence to the positions on the wafer substrate, and the routine proceeds to step **110**.

[0068] At step **100**, when it is judged that the mode is not the display mode **1**, the process proceeds to step **104** where a judgment is made as to whether or not the display mode instructed by the PC **20** is the display mode **2**.

[0069] At step **104**, if it is judged that the mode is the display mode **2**, the process proceeds to step **106**. Processing is carried out in such a manner that the pass/fail ratio for each of the DUT's (second information) which is calculated on the basis of the test results data read from the RAM **34** is displayed on the CRT **22** of the PC **20**, and the process proceeds to step **110**.

[0070] At step **106**, if it is judged that the mode is not the display mode **2**, it is judged that the mode is the display mode **3**, and the routine proceeds to step **108**. In step **108**, processing is performed such that the test results of the semiconductor chips are displayed on the CRT **22** of the PC **20** in correspondence to the positions on the wafer substrate, and such that the pass/fail ratio for each of the DUT's is displayed in parallel with the test results of the semiconductor chip, and the process proceeds to step **110**.

[0071] At step **110**, a judgment is made as to whether or not an instruction has been given to end display by the CRT **22** of the PC **20**. When it is judged that no instruction to end display has been given, the process proceeds to step **112** where a judgment is made as to whether or not an instruction has been given to switch the display.

[0072] At step **112**, when it is judged that an instruction has been given to switch the display, the process returns to step **100** and the processings described above are repeated. When it is judged at step **112** that no instruction has been given to switch the display, the process returns to step **110**, and a judgment is made as to whether or not an instruction has been given to end display by the CRT **22** of the PC **20**.

[0073] On the other hand, when it is judged in step **110** that an instruction has been given to end display, the routine ends.

[0074] As described above, the test results of the semiconductor chips are displayed on the CRT **22** of the PC **20** in correspondence to the positions on the wafer substrate. Further, by providing the display mode **3** for displaying in parallel the test results and the pass/fail ratios for the respective DUT's, the test results of the semiconductor chips and the pass/fail ratios for the respective DUT's are displayed in parallel as illustrated in **FIG. 3**A and **FIG. 3B**. Thus, the existence of breakage of the probes can be confirmed quite easily at the same time as testing the semiconductor chips, at all of the positions that the tester can be positioned at on the semiconductor substrate. Furthermore, since the probes can easily detect the damaged DUT's, the damage of the probes for each of the DUT's can be detected at an early stage.

[0075] Furthermore, there is also the advantage that a display mode suitable for the operator can be selected because the display state can be selected by switching the display mode of the test results between three kinds of display modes: a display mode for only the testing of the semiconductor chips, a display mode for only checking destruction of the probes, and a display mode for checking destruction of the probes and for the testing of the semiconductor chips.

[0076] Operation of the CPU **38** on the basis of the screen switching program will be explained by referring to the

flowchart of **FIG. 4**. First, at step **200**, judgment is made as to whether or not a plurality of wafer probers are connected.

[**0077**] At step **200**, if it is judged that a plurality of wafer probers are not connected, the process proceeds to step **202** where processing is performed in such a manner that the test results by the wafer prober is displayed on the entire CRT **22** of the PC **20**. Then, the routine ends.

[**0078**] Furthermore, at step **200**, if it is judged that a plurality of wafer probers are connected, the routine proceeds to step **204** where a judgment is made as to whether or not an instruction for parallel display has been given. When it is judged at step **204** that an instruction for parallel display has been given, the process proceeds to step **206** where one screen on the CRT **22** of the PC **20** is divided into regions of a number corresponding to the number of the wafer probers such that the test results by one wafer prober is displayed in one divisional region. Then, this routine ends. In the present embodiment, since the two wafer probers **10***a* and **10***b* are connected, one screen is divided into two portions as shown in **FIG. 5**A and **FIG. 5B** so that the test results of the two wafer probers **10***a* and **10***b* can be displayed in the respective regions. Then, this routine ends.

[**0079**] Furthermore, when it is judged at step **204** that no instruction for parallel display has been given, the process proceeds to step **208** to set the display such that the test results by the first wafer prober **10***a* is displayed on the entire one screen.

[**0080**] At the subsequent step **210**, it is judged whether or not an instruction has been given to end display. If it is judged that an instruction has been given to terminate display, the routine ends. Furthermore, if it is judged at step **210** that no instruction has been given to end display, a judgment is made at step **212** as to whether or not an instruction has been given to switch the screen.

[**0081**] If it is judged at step **212** that no instruction has been given to switch the screen, the process returns to step **208**, and the aforementioned processings are repeated. Furthermore, if it is judged at step **212** that an instruction has been given to switch the screen, the process proceeds to step **214** to set the display so that the test results by the second wafer prober **10***b* is displayed on the one entire screen.

[**0082**] At the subsequent step **216**, it is judged whether or not an instruction has been given to end display. If it is judged that an instruction has been given to terminate the display, the routine ends. Furthermore, if it is judged at step **216** that no instruction has been given to end display, a judgment is made at step **218** whether or not an instruction has been given to switch the screen.

[**0083**] If it is judged at step **218** that no instruction has been given to switch the screen, the process returns to step **214**, and the aforementioned processings are repeated. Furthermore, the program is set such that if it is judged at step **218** that an instruction has been given to switch the screen, the test results of a different wafer prober is displayed on the entire one screen. In the present embodiment, since the number of connected wafer probers is two, the process returns to step **208**, and the aforementioned processings are repeated.

[**0084**] As described above, since parallel display can be carried out to set the screen such that the test results by all of the connected wafer probers are displayed on one screen, the testing of the wafer substrate by all of the connected wafer probers can be confirmed at the same time, and thus, the efficiency of the testing processing improves. Furthermore, also in the case where the display is set in such a manner that the test results of the respective wafer probers are displayed on respective screens, switching between the respective screens can be carried out freely. Thus, such display is preferable because a screen suited to the operator can be switched to, for example, in such a manner that the screen is switched each time a predetermined time passes in order for the operator to check the test results or the like of the respective wafer probers.

[**0085**] In the present embodiment, the pass/fail ratio is calculated from the test results obtained for each of the DUT's, and is displayed. Since it is preferable that the operator be informed when the detection ratio of poor products by a DUT is unusually large, the display is not limited to the display of the pass/fail ratio for each of the DUT's. For example, as shown in **FIG. 5**, the test results may be displayed for each of the DUT's, and the detection ratio of the poor products may be displayed. Any value may be displayed as long as it reflects the detection ratio of the poor products.

[**0086**] In the embodiment described above, the ROM **36** stores the display program, the display mode switching program, and the screen switching program. However, the present invention is not limited to the same. These programs may be stored on a floppy disk, and, at the same time, the main body of the computer may be provided with a hard disk so that the program may be read from the floppy disk to be installed in the hard disk. Or, the programs may be installed by transmission through a transmission means via a wired or wireless network (for example, telephone line). The programs do not have to be stored on a floppy disk. The programs may be stored in a CD-ROM or a magnetic tape and then installed from the CD-ROM or the magnetic tape into the hard disk. Furthermore, a hard disk storing the programs may be provided. Still further, the programs may be written directly on the hard disk or the RAM of the PC. In this manner, the programs may be transmitted via at least one of a concrete recording medium or transmission means.

What is claimed is:

1. A method for displaying test results comprising the step of:

on the basis of test results obtained by a tester provided with plural testing portions, each of the testing portions testing a plurality of semiconductor chips formed on a wafer substrate, displaying on a same screen of a displaying means two types of information which are a first information which expresses test results of the semiconductor chips in accordance with positions of the semiconductor chips on the wafer substrate, and a second information which expresses for each testing portions of the tester test results of the semiconductor chips obtained by the testing portion.

2. A method for displaying test results according to claim 1, wherein the two types of information obtained from at least two testers are displayed on the same screen of the displaying means.

3. A method for displaying test results according to claim 1, wherein a display mode is switchable between at least

three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first information and the second information on the screen of the displaying means.

4. A method for displaying test results according to claim 2, wherein a display mode is switchable between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first information and the second information on the screen of the displaying means.

5. A method for displaying test results according to claim 1, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

6. A method for displaying test results according to claim 2, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

7. A method for displaying test results according to claim 3, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

8. An apparatus for displaying test results comprising:

control means for controlling a displaying means such that, on the basis of test results obtained by a tester provided with plural testing portions, each of the testing portions testing a plurality of semiconductor chips formed on a wafer substrate, the displaying means displays on a same screen two types of information which are a first information which expresses test results of the semiconductor chips in accordance with positions of the semiconductor chips on the wafer substrate, and a second information which expresses for each testing portions of the tester test results of the semiconductor chips obtained by the testing portion.

9. An apparatus for displaying test results according to claim 8, wherein said control means is connected to at least two testers, and controls the displaying means so that the two types of information which are obtained from each of the testers are displayed on the same screen of the displaying means.

10. An apparatus for displaying test results according to claim 8, further comprising switching means for switching a display mode between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first and the second information on the screen of the displaying means.

11. An apparatus for displaying test results according to claim 9, further comprising switching means for switching a display mode between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first and the second information on the screen of the displaying means.

12. An apparatus for displaying test results according to **8**, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

13. An apparatus for displaying test results according to **9**, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

14. An apparatus for displaying test results according to **10**, wherein the test results of the second information is at least one of a detection ratio of defective semiconductor chip and a value reflecting the detection ratio.

15. A recording medium which can be read by a computer, the medium having a display program recorded therein for on the basis of test results obtained by a tester provided with plural testing portions, each of the testing portions testing a plurality of semiconductor chips formed on a wafer substrate, displaying on a same screen of displaying means two types of information which are a first information which expresses test results of the semiconductor chips in accordance with positions of the semiconductor chips on the wafer substrate, and a second information which expresses for each testing portions of the tester test results of the semiconductor chips obtained by the testing portion.

16. A recording medium according to claim 15, wherein a parallel display program, for displaying in a parallel manner and on the same screen, the two types of information inputted independently from at least two testers, is also recorded on said recording medium.

17. A recording medium according to claim 15, wherein a display switch program, for switching a display mode between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first information and the second information on the screen of the displaying means, is also recorded on said recording medium.

18. A recording medium according to claim 16, wherein a display switch program, for switching a display mode between at least three display modes which are a first display mode for displaying only the first information on the screen of the displaying means, a second display mode for displaying only the second information on the screen of the displaying means, and a third display mode for displaying both the first information and the second information on the screen of the displaying means, is also recorded on said recording medium.

19. A recording medium according to claim 15, wherein the test results of the second information is at least one of a detection ratio of detective semiconductor and a value reflecting the detection ratio.

20. A recording medium according to claim 16, wherein the test results of the second information is at least one of a detection ratio of detective semiconductor and a value reflecting the detection ratio.

21. A recording medium according to claim 17, wherein the test results of the second information is at least one of a detection ratio of detective semiconductor and a value reflecting the detection ratio.

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