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(54) **Title:** FREQUENCY CONTROL SYSTEM WITH DUAL-INPUT BIAS GENERATOR TO SEPARATELY RECEIVE MANAGEMENT AND OPERATIONAL CONTROLS

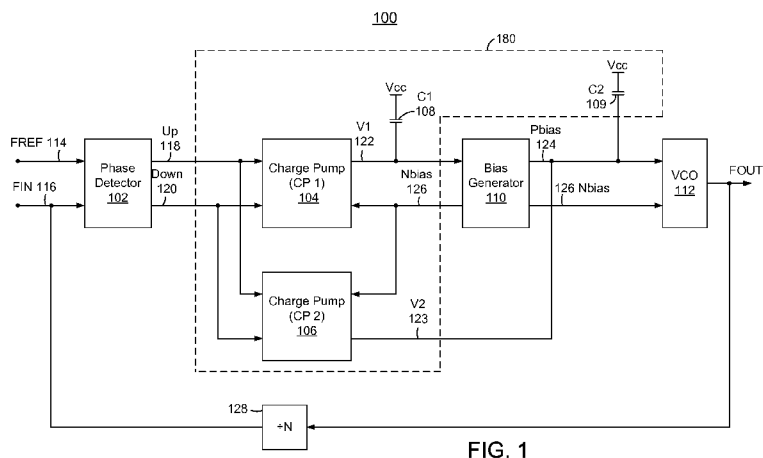


FIG. 1

(57) **Abstract:** Methods and systems to control an output frequency relative to a reference frequency. A frequency control system includes a dual-input bias generator to separately receive management and operational controls. The bias generator includes a first bias generator circuit to generate a bias control based on a difference between the management control and a bias feedback reference during a first mode of operation, a second bias generator circuit to generate the bias control based on a difference between the operational control and the bias feedback reference during a second mode of operation, and a bias feedback reference circuit to generate the bias feedback reference based on the bias control. The first mode may include a characterization and/or a start-up mode. The second mode may include an operational mode, such as a feedback-controlled mode.

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FREQUENCY CONTROL SYSTEM WITH DUAL-INPUT BIAS GENERATOR TO SEPARATELY RECEIVE MANAGEMENT AND OPERATIONAL CONTROLS

BACKGROUND

5 A phase locked loop (PLL) may include a phase detector, loop filter, VCO, reference input, and frequency divider. After an initial power-on, the PLL may perform a lock acquisition process in to attempt to phase and/or frequency lock a VCO output to the reference input. Lock acquisition may take time due to an indeterminate state of the PLL at power-on.

10 A PLL may be calibrated or characterized to determine or generate a frequency versus tuning voltage curve for the VCO, which may be used to optimize PLL operation. Characterization may include comparing a range of voltages applied to the bias generator, to corresponding output frequencies of the VCO.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

15 FIG. 1 is a block diagram of a frequency control system including a bias generator to generate one or more bias controls to control an output frequency relative to a reference frequency.

FIG. 2 is a block diagram of the frequency control system of FIG. 1, where the bias generator includes a single input to receive a management control and an operational control.

20 FIG. 3 is a block diagram of another frequency control system including a bias generator having a first input to receive a management control during a first mode of operation and a second input to receive an operational control during a second mode of operation.

25 FIG. 4 is a circuit diagram of an example implementation of the frequency control system of FIG. 3, where the bias generator includes an Nbias generator and a Pbias generator, and where the Nbias generator includes first and second bias generator circuits and a bias feedback reference circuit.

FIG. 5 is a diagram of a circuit in which the first and second bias generator circuits of FIG. 4 are integrated in a differential transistor pair configuration.

30 FIG. 6 is a block diagram of a processor-based system that includes a frequency control system.

In the drawings, the leftmost digit(s) of a reference number identifies the drawing in which the reference number first appears.

DETAILED DESCRIPTION

FIG. 1 is a block diagram of a frequency control system 100, including a bias generator 110 to generate one or more bias controls to control an output frequency, FOUT, relative to a reference frequency FREF 114.

5 In the example of FIG. 1, system 100 includes a phase detector 102, charge pumps 104 and 106, loop filters 108 and 109, a voltage-controlled oscillator (VCO) 112, and a frequency divider 228. Frequency control system 100 may represent a phase locked loop (PLL). For illustrative purposes, frequency control system 100 is illustrated as a self-biased phase locked loop (SBPLL). Methods and systems disclosed herein are not, however, limited
10 to SBPLLs or PLLs.

Bias generator 110 is implemented to generate bias controls Nbias 126 and Pbias 124. Nbias 126 is provided to VCO 112 and charge pumps 104 and 106. Pbias 124 is provided to VCO 112.

15 Charge pumps 104 and 106 may be implemented to vary corresponding output current drives based on Nbias 126.

Phase detector 102 may be implemented to compare a reference clock, input FREF 114, and a feedback clock, input FIN 116, and to control or assert an Up control 118 and/or a Down control 120 based on a phase difference. Phase detector 102 may generate a pulse width having a width substantially equal to the phase difference. The pulse may be provided
20 as Up control 118 when FREF leads FIN, and as Down control 120 when FREF lags FIN. In the example of FIG. 1, Up control 118 and Down control 120 are provided to charge pumps 104 and 106.

Control pump 104 generates and/or regulates an operating control V1 122 110 based on Up control 118 and Down control 120.

25 Control pump 106 generates and/or regulates a control V2 123, which may be further regulated as Pbias 124 by bias generator 110, such as illustrated in FIG. 4 with a Pbias generator 309.

In FIG. 1, loop filters 108 and 109 include capacitors C1 and C2, each to filter a corresponding one of V1 122 and V2 123/Pbias 124. Loop filter 108 and 109 may include
30 low-pass filters. Loop filter 108 may be implemented to integrate current generated by charge pump 104, such as to smooth operational control V1 122. Loop filter 109 may be implemented to integrate current generated by charge pump 106, such as to smooth V2 123.

Charge pumps 104 and 106 and loop filters 108 and 109 may define a loop filter circuit 180 to translate an output of phase detector 102 into an operational control or control

voltage. Loop filter circuit 180 is not, however, limited to the example of FIG. 1, as one or more features of loop filter circuit 180 may be omitted and/or replaced with other components. In an embodiment, one or both of charge pumps 104 and 106, and/or loop filters 108 and 109 may be replaced with one or more other loop filter components. For example, one or more of loop filters 108 and 109 may be replaced with sample-reset type filters. As another example, charge pump 104 may be replaced with a sample and hold circuit, a counter, a passive component, and/or combinations thereof. In such embodiments, a control module may assert appropriate control over the loop filter circuit components to implement features disclosed herein.

System 100 may be implemented to operate in a closed-loop feedback-controlled mode to control and/or minimize phase and/or frequency differences between FREF 114 and FIN 116, such as to lock the frequency and/or phase of FIN 116 with that of FREF 114. A feedback loop may include phase detector 102, charge pumps 104 and 106, loop filters 108 and 109, bias generator 110, VCO 112, and divider 128. The closed-loop feedback-controlled mode may also be referred to as a feedback-controlled mode and an operating mode of system 100.

Upon power-up of system 100, one or more loop signals may have an indeterminate and/or known state that differs from a desired state. In time, and without assistance, bias generator 110 may converge on bias levels to lock the frequency and/or phase of FREF 116 with that of FIN 116.

Described below are methods and systems to selectively implement a startup mode prior to the feedback controlled mode, such as to reduce the lock or acquisition time after power-on. Also described below are methods and systems to selectively implement a characterization mode, such as to perform a frequency versus tuning voltage (FV) characterization or calibration of VCO 112.

A frequency control system as disclosed herein may be configurable to operate in multiple modes. A first mode may include the start-up mode and/or the characterization mode during which bias generator 110 receives a management control. A second mode may include the feedback-controlled mode during which bias generator 110 receives a feedback control, illustrated here as operational control V1 122.

FIG. 2 is a block diagram of a frequency control system 200, including frequency control system 100 of FIG. 1 and a management control module 204 having a controller 206 to generate management control CV.

In FIG. 2, bias generator 110 includes a single input 211 to receive management control CV during the first mode of operation and operational control V1 122 during the second mode of operation.

Control module 204 may further include a switch device, illustrated here as a pass gate PG1, to provide management control CV to input 211. Controller 206 may be implemented to control PG1 to selectively provide management control CV to input 211 during the first mode of operation. Charge pump 104 may be disabled during the first mode of operation.

When PG1 is open, system 100 may operate in the second mode of operation, or feedback-controlled mode, to provide operational control V1 122 to input 211 of bias generator 110.

Where the first mode includes the FV characterization mode, controller 206 may increment management control CV through a tuning range of voltages, which may include voltages between zero volts and an operating voltage, V_{cc} , of system 100. Corresponding frequencies and/or phases of FOUT may be monitored and/or recorded to generate FV characteristics, which may be used to calibrate system 100 and/or another frequency control system.

Where the first mode includes the start-up mode, controller 206 may set management control CV to a nominal tuning voltage, which may be approximately midway between V_{ss} and V_{cc} . Thereafter, power may be applied to charge pump 104 and PG1 may be opened to operate system 100 in the feedback-controlled mode.

In the feedback-controlled mode, where PG1 is open, a leakage current may flow through PG1, which may offset operational control V1 122. Charge pump 104 may compensate for the offset, but the compensation may result in a static phase error. Excessive leakage may preclude frequency and/or phase locking.

FIG. 3 is a block diagram of a frequency control system 300, including a bias generator 310 having a first input 311 to receive a management control V1x from a control module 304 during the first mode of operation, and a second input 312 to receive operational control V1 122 during the second mode of operation. In other words, bias generator 310 is implemented to receive management control V1x and operational control V1 122 via separate paths, which may reduce and/or eliminate the current leakage flow described above with reference to FIG. 2.

Bias generator 310 may be implemented to receive management control V1x during the first mode of operation and to receive operational control V1 122 during the second mode

of operation, and to control bias control Nbias 126 during each of the first and second modes to control output frequency FOUT. Management control V1x may include a start-up control and/or a FV characterization control, such as described above.

5 System 300 further includes charge pumps 104 and 106, and VCO 112, as described above with reference to system 100. For ease of illustration, phase detector 102 and divider 108 are omitted in FIG. 3.

In FIG. 3, bias generator 310 includes an Nbias generator 308 to generate Nbias 126 based on one of inputs 311 and 312, and a Pbias generator 309 to control Pbias 124 based on Nbias 126. Bias generator 310 further includes a capacitor Cnbias connected to an electrical
10 path of Nbias 126 and to a voltage reference Vss, which may correspond to ground.

FIG. 4 is a circuit diagram 400 of an example implementation of system 300.

In FIG. 4, Nbias generator 308 includes a first bias Nbias generator circuit 420, a second bias generator circuit 422, and a bias feedback reference circuit 424.

15 First Nbias generator circuit 420 may be implemented to generate Nbias 126 based on a difference between management control V1x and a bias feedback reference Vfbk from bias feedback reference circuit 424.

Second Nbias generator 420 may be implemented to generate Nbias 126 based on a difference between operational control V1 122 and bias feedback reference Vfbk.

20 Bias feedback reference circuit 424 may be implemented to generate bias feedback reference Vfbk based on Nbias 126.

Control module 304 may be implemented to selectively enable one of first and second Nbias generator circuits 420 and 422 with corresponding controls Strt1 and Strt2, to generate Nbias 124 based on a corresponding one of management control V1x and operational control V1 122.

25 First bias generator circuit 420 may include an operational amplifier (OpAmp) 421 to receive and compare management control V1x and bias feedback reference Vfbk.

Second bias generator 422 may include an operational amplifier (OpAmp) 423 to receive and compare operational control V1 and bias feedback reference Vfbk.

30 OpAmp 421 may be implemented or fabricated with a smaller scale process technology (*i.e.*, smaller channel length, smaller channel width, and/or smaller feature size), than OpAmp 423. A larger scale process for OpAmp 423 may help to reduce device noise and offsets during the feedback-controlled mode. Device noise and offsets may be of little or no concern in FV characterization mode and/or start-up mode, and a smaller scale process technology for OpAmp 421 may help to conserve power and/or area. Example

implementations of OpAmps 421 and 423 are described further below with reference to FIG. 5.

One or more elements of system 300 may be controllable to be placed in a reduced power-consumption state. In the example of FIG. 4, circuit diagram 400 includes gates N1 and P1, which may be referred to as power gates, to place bias generator 310 in a reduced power-consumption state. Gate N1 may represent an N-type device to pull-down Nbias 126 to Vss responsive to a PGn control, to effectively turn-off charge pumps 104 and 106. Gate P1 may represent a P-type device to pull-up V1 122 to Vcc responsive to a PGp control, which may help to prevent oscillations within bias generator 310. Controls PGn and PGp may be generated by control module 304.

To enter the FV characterization mode from the reduced power-consumption mode, gate N1 may be opened, gate P1 may remain closed, first bias generator circuit 420 may be enabled with Strt1, and second bias generator circuit 422 may be disabled with Strt2. Management control V1x may then be incremented by control module 304 to cause first bias generator circuit 420 to generate Nbias 126 based on management control V1x and Vfbk. Calibration data may be collected as described above.

To transition from the FV characterization mode to the start-up mode, PG1 may be opened, first bias generator circuit 420 may be enabled with Strt1, and second bias generator circuit 422 may be disabled with Strt2.

To enter the start-up mode directly from the reduced power-consumption mode, gates N1 and P1 may be opened, first bias generator circuit 420 may be enabled with Strt1, and second bias generator circuit 422 may be disabled with Strt2.

When gate P1 is closed, Vcc may be applied to input 312 through capacitor C1 108. When gate P1 is initially opened, charge within capacitor C1 108 may hold input 312 at Vcc. In start-up mode, control module 304 may be implemented to control charge pump 104 to cause charge pump 104 to draw charge from capacitor C1 108, which may reduce the voltage at input 312.

For example, control module 304 may be implemented to assert Down control 120 until operational control V1 122 on input 312 reaches a nominal value, referred to herein as a reference startup voltage, Vstrtup. Vstrtup may correspond to a midpoint between Vss and Vcc. Assertion of Down control 120 may include pulling Down control 120 to Vss. Assertion of Down control 120 may cause charge pump 104 to draw charge from C1 108. The nominal value of operational control V1 122 may drive Nbias 126 to a relatively low voltage, which

may cause charge pump 104 to draw a relatively high current from C1 108, which may discharge capacitor C1 relatively quickly.

To transition from the start-up mode to the feedback-controlled mode, first bias generator circuit 420 may be disabled with Strt1, and second bias generator circuit 422 may be enabled with Strt2.

Control module 304 may be implemented to monitor operational control V1 122 as capacitor C1 is discharged through charge pump 104, and to transition to the feedback-controlled mode when operational control V1 122 falls to or below a threshold value. Control module 304 may include, for example, a comparator to receive and compare operational control V1 122 with reference startup voltage Vstrtup. Control module 304 may be implemented to transition to the feedback-controlled mode when operational control V1 122 is equal to or less than Vstrtup.

System 300 may be implemented and/or controllable to transition between any pair of the reduced power-consumption mode, the FV characterization mode, the start-up mode, and the feedback-controlled mode, and may be implemented to traverse through one or more combinations of the modes. For example, and without limitation, system 300 may be implemented to sequentially transition from the reduced power-consumption mode, to the FV characterization mode, to the power-up mode, and to feedback-controlled mode. Alternatively, or additionally, system 300 may be implemented to sequentially transition from the reduced power-consumption mode, to the power-up mode, and to feedback-controlled mode.

FIG. 5 is a diagram of a circuit 500 in which first and second bias generator circuits 420 and 422 are integrated in a differential transistor pair configuration.

Circuit 500 includes a first set of differentially configured p-channel devices P5 and P6, which may represent an example implementation of OpAmp 421 of FIG. 4.

Circuit 500 further includes second set differentially configured p-channel devices P3 and P4, which may represent an example implementation of OpAmp 423 of FIG. 4.

The first and second sets of differentially configured devices may share a load circuit and/or a bias circuit. In FIG. 5, a shared bias circuit is illustrated as a p-channel device P11. A shared load circuit is illustrated as n-channel device N2 and N3. Circuit sharing may help to conserve power and area.

In FIG. 5, complementary OpAmp enable and disable controls, stup and stupb, respectively, may represent controls Strt1 and Strt2 in FIG. 4, and may be controlled to selectively enable and disable corresponding first and second bias generator circuits 420 and

422. For example, when *stup* is low, or logic 0, P3 and P4 turn on to generate *Nbias* 126 based on a difference between *V1* and *Vfbk*. When *stup* is high, or logic 1, the P5 and P6 turn on to generate *Nbias* 126 based on a difference between *V1x* and *Vfbk*.

5 Methods and systems disclosed herein may be implemented with respect to one or more of a variety of systems such as described below with reference to FIG. 6. Methods and systems disclosed herein are not, however, limited to the example of FIG. 6.

10 FIG. 6 is a block diagram of a system 600, including a frequency control system 602 to provide an output frequency as a reference clock to one or more other modules of system 600. Frequency control system 602 may include a bias generator, such as described in one or more examples herein.

System 600 may further include one or more of a processor 604, a communication system 606, a user interface system 610, and communication infrastructure to communicate amongst processor 604, communication system 606, and user interface system 610.

Communication system 606 may include a wired and/or wireless communication system.

15 System 600 or portions thereof may be implemented within one or more integrated circuit dies, and may be implemented as a system-on-a-chip (SoC).

User interface system 610 may include a monitor or display 632 to display information from processor 604 and/or communication system 606.

20 User interface system 610 may include a human interface device (HID) 634 to provide user input to processor 604 and/or communication system 606. HID 634 may include, for example and without limitation, one or more of a key board, a cursor device, a touch-sensitive device, and or a motion and/or image sensor. HID 634 may include a physical device and/or a virtual device, such as a monitor-displayed or virtual keyboard.

25 User interface system 610 may include an audio system 636 to receive and/or output audible sound.

System 600 may represent, for example, a computer system, a personal communication device, and/or a television set-top box.

30 System 600 may include a housing, and one or more of system 602, processor 604, communication system 606, and user interface system 610, or portions thereof may be positioned within the housing. The housing may include, without limitation, a rack-mountable housing, a desk-top housing, a lap-top housing, a notebook housing, a net-book housing, a set-top box housing, a portable housing, and/or other conventional electronic housing and/or future-developed housing. System 600 may further include a battery, and system 600 may be portable.

As disclosed herein, a frequency control apparatus may include a bias generator to control an output frequency during each of first and second modes of operation. The bias generator may include a first input to receive a management control during the first mode of operation and a second input to receive an operational control during the second mode of operation.

The bias generator may include a first bias generator circuit, including the first input to receive the management control, to generate a bias control based on a difference between the management control and a bias feedback reference during the first mode of operation. The bias generator may further include a second bias generator circuit, including the second input to receive the operational control, to generate the bias control based on a difference between the operational control and the bias feedback reference during the second mode of operation. The bias generator may further include a bias feedback reference circuit to generate the bias feedback reference based on the bias control.

The first and second bias generator circuits may each include a respective one of first and second operational amplifiers.

The first and second operational amplifiers may be integrated as a differential transistor pair.

The first and second operational amplifiers may be implemented to share a common load circuit and a common bias circuit.

The first and second operational amplifiers may be implemented on an integrated circuit die, and wherein the first operational amplifier is implemented with one or more of smaller channel lengths, smaller channel widths, and smaller feature sizes, than that of the second operational amplifier.

The frequency control apparatus may include a control module to provide the management control.

The control may be implemented to disable the first bias generator circuit, enable the second bias generator circuit, and provide the management control during the first mode, and to enable the first bias generator and disable the second bias generator during the second mode.

The first mode may include a characterization mode, and the control module may be implemented to provide the management control at each of multiple voltage levels to generate calibration data in the characterization mode.

The first mode may include a start-up mode and the second mode may include a feedback-controlled mode. The frequency control apparatus may include a loop filter circuit,

which include a charge pump to provide the operational control during the feedback-controlled mode, and to vary a current drive of the charge pump output based on the bias control. The control module may be implemented to provide the management control during the start-up mode to initialize the charge pump output current drive, and to switch the bias generator from the start-up mode to the feedback-controlled mode after the charge pump output current drive is initialized. The control module may be implemented to compare a voltage of the charge pump output to a reference during the start-up mode, and to switch from the start-up mode to the feedback-controlled mode when the voltage of charge pump output is equal to the reference.

5 The control module may be implemented to configure the frequency control system in a reduced power-consumption mode, transition the frequency control system from the reduced power-consumption mode to the start-up mode, and transition the frequency control system from the start-up mode to the feedback-controlled mode.

The bias generator may correspond to an Nbias generator to generate the bias control as an Nbias control, and the frequency control apparatus may further include a Pbias generator to generate a Pbias control. The frequency control apparatus may further include a voltage controlled oscillator (VCO) to generate the output frequency, and a loop filter circuit to provide the operational control to the bias generator. The Nbias control may be applied to a component of the loop filter circuit and to the Pbias generator. The Pbias control may be provided to the VCO.

15 As further disclosed herein, a system may include a processor, a communication system to communicate with a network, communication infrastructure to permit communications amongst the processor, the communication system, and a user interface system, and a frequency control apparatus as described in one or more examples above, to provide an output frequency as a reference clock to one or more of the processor, the communication system, and the user interface system.

20 The processor, the communication system, and the frequency control system may be positioned within a housing.

The communication system may include a wireless communication system.

30 The processor, the communication system, a battery, and at least a portion of the user interface system may be positioned within the housing.

Methods and systems disclosed herein may be implemented in hardware, software, firmware, and combinations thereof, including discrete and integrated circuit logic, application specific integrated circuit (ASIC) logic, and microcontrollers, and may be

implemented as part of a domain-specific integrated circuit package, and/or a combination of integrated circuit packages.

5 Methods and systems are disclosed herein with the aid of functional building blocks illustrating functions, features, and relationships thereof. At least some of the boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries may be defined so long as the specified functions and relationships thereof are appropriately performed.

10 While various embodiments are disclosed herein, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail may be made therein without departing from the spirit and scope of the methods and systems disclosed herein. Thus, the breadth and scope of the claims should not be limited by any of the examples provided herein.

CLAIMS

What is claimed is:

1. A frequency control apparatus, comprising:
a bias generator to control an output frequency of the frequency control system during
5 each of first and second modes of operation, wherein the bias generator
includes a first input to receive a management control during the first mode of
operation and a second input to receive an operational control during the
second mode of operation.
2. The apparatus of claim 1, wherein the bias generator includes:
10 a first bias generator circuit, including the first input to receive the management
control, to generate a bias control based on a difference between the
management control and a bias feedback reference during the first mode of
operation;
a second bias generator circuit, including the second input to receive the operational
15 control, to generate the bias control based on a difference between the
operational control and the bias feedback reference during the second mode of
operation; and
a bias feedback reference circuit to generate the bias feedback reference based on the
bias control.
- 20 3. The apparatus of claim 2, wherein the first and second bias generator circuits each
include a respective one of first and second operational amplifiers.
4. The apparatus of claim 3, wherein the first and second operational amplifiers are
integrated as a differential transistor pair.
5. The apparatus of claim 3, wherein the first and second operational amplifiers are
25 implemented to share a common load circuit and a common bias circuit.
6. The apparatus of claim 3, wherein the first and second operational amplifiers are
implemented on an integrated circuit die, and wherein the first operational amplifier is
implemented with one or more of smaller channel lengths, smaller channel widths,
and smaller feature sizes, than that of the second operational amplifier.
- 30 7. The apparatus of any one of claims 2 through 6, further including:
a control module to disable the first bias generator circuit, enable the second bias
generator circuit, and provide the management control during the first mode,
and to enable the first bias generator and disable the second bias generator
during the second mode.

8. The apparatus of any one of claims 1 through 6, wherein the first mode includes a characterization mode, and wherein the apparatus further includes a control module to provide the management control at each of multiple voltage levels to generate calibration data in the characterization mode.
- 5 9. The apparatus of any one of claims 1 through 6, wherein the first mode includes a start-up mode and the second mode includes a feedback-controlled mode.
10. The apparatus of claim 9, further including:
a loop filter circuit, including a charge pump to provide the operational control during the feedback-controlled mode, and to vary a current drive of the charge pump output based on the bias control; and
10 a control module to provide the management control during the start-up mode to initialize the charge pump output current drive, and to switch the bias generator from the start-up mode to the feedback-controlled mode after the charge pump output current drive is initialized.
- 15 11. The apparatus of claim 10, wherein the control module is implemented to compare a voltage of the charge pump output to a reference during the start-up mode, and to switch from the start-up mode to the feedback-controlled mode when the voltage of charge pump output is equal to the reference.
- 20 12. The apparatus of any one of claims 1 through 6, further including a control module to configure the frequency control system in a reduced power-consumption mode, transition the frequency control system from the reduced power-consumption mode to the start-up mode, and transition the frequency control system from the start-up mode to the feedback-controlled mode.
- 25 13. The apparatus of any one of claims 1 through 6, further including:
a voltage controlled oscillator (VCO) to generate the output frequency; and
a loop filter circuit to provide the operational control to the bias generator;
wherein the bias control is applied to a component of the loop filter circuit and to another bias generator to bias the VCO.
- 30 14. A system, comprising:
a processor;
a communication system to communicate with a network;
communication infrastructure to permit communications amongst the processor, the communication system, and a user interface system; and

a frequency control system are recited in any one of claims 1 through 6 to provide the output frequency to one or more of the processor, the communication system, and the user interface system.

5 15. The system of claim 14, further including a housing, wherein the processor, the communication system, and the frequency control system are positioned within the housing.

10 16. The system of claim 15, wherein:
the communication system includes a wireless communication system; and
the processor, the communication system, a battery, and at least a portion of the user interface system are positioned within the housing.

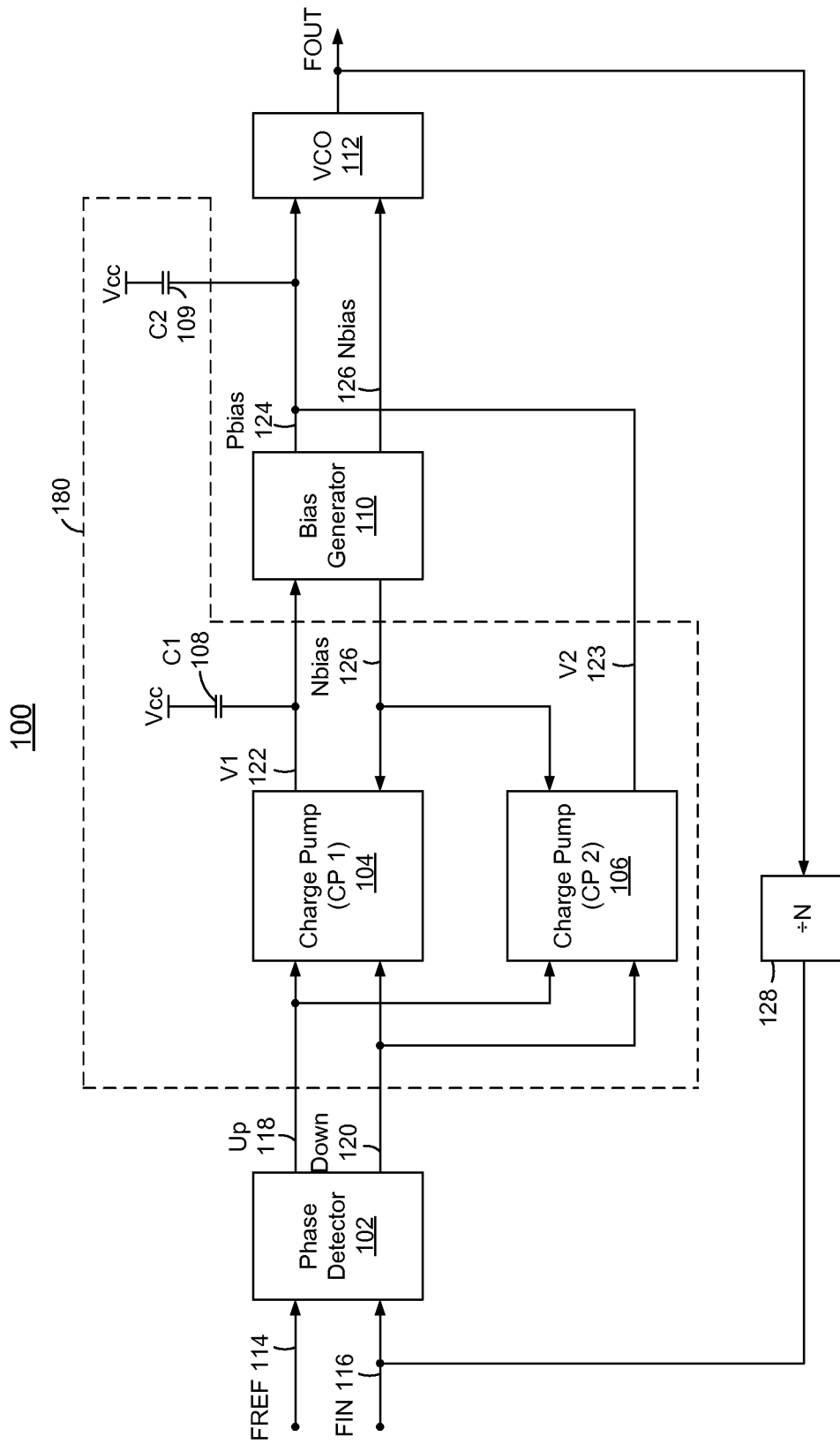


FIG. 1

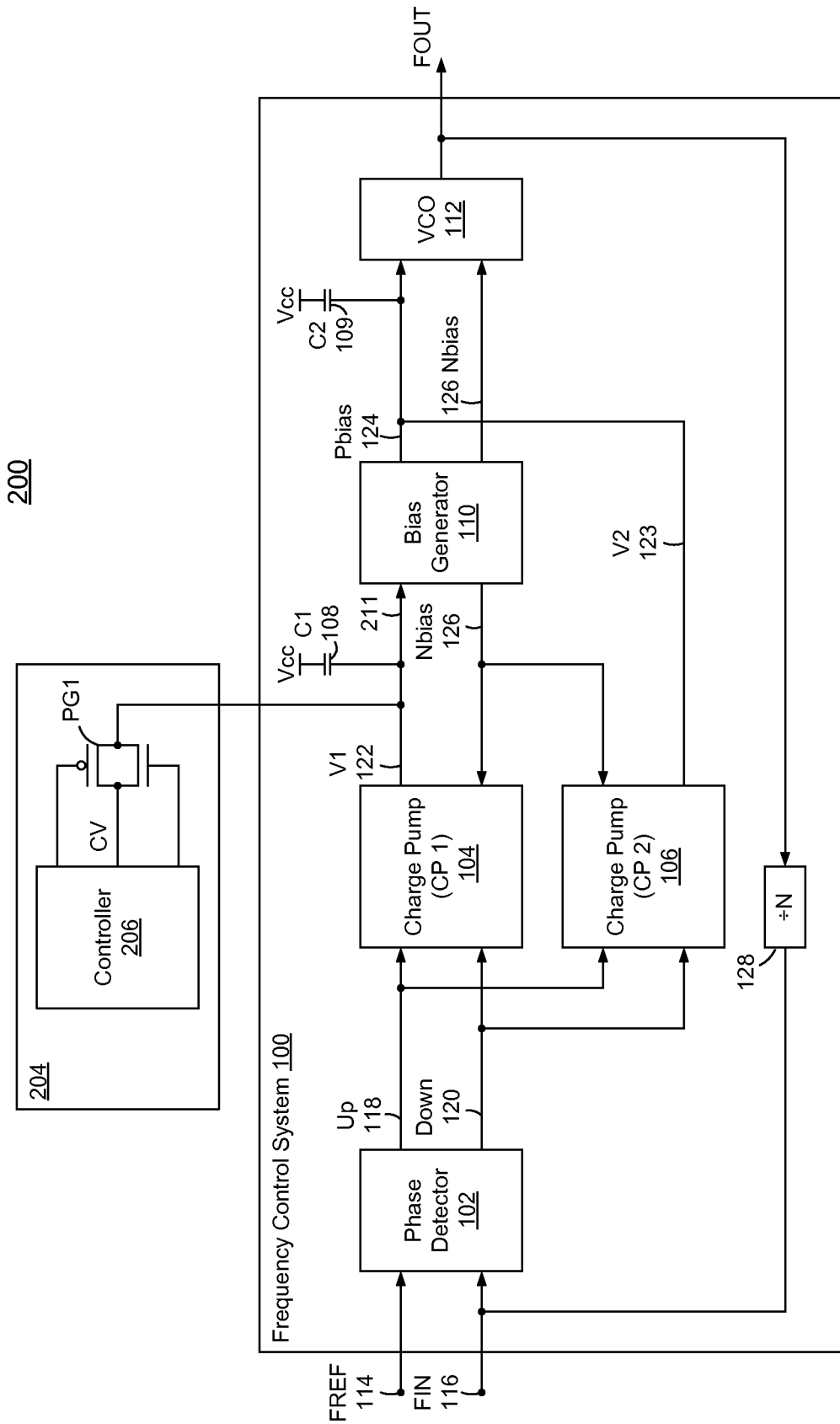


FIG. 2

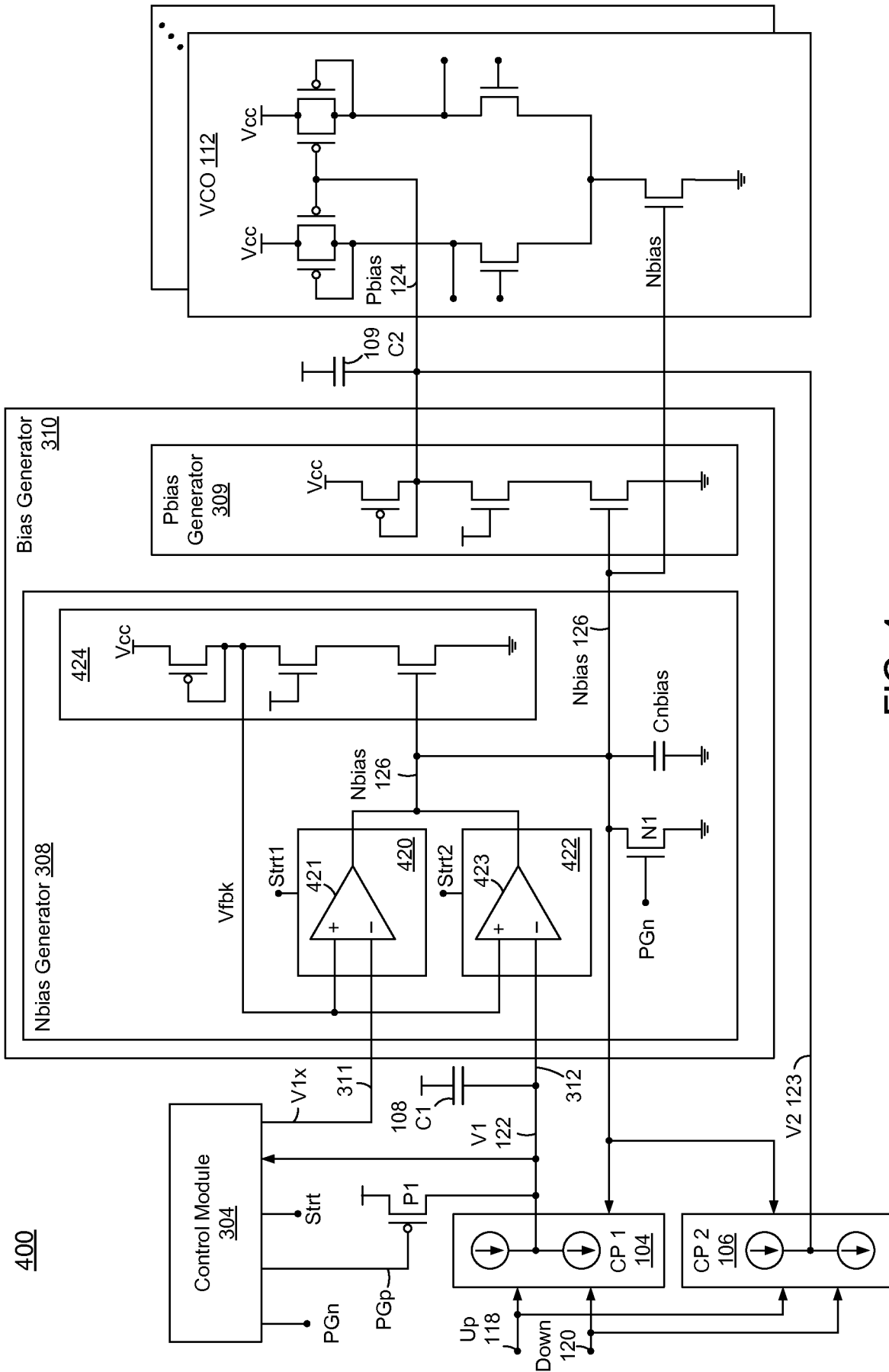


FIG. 4

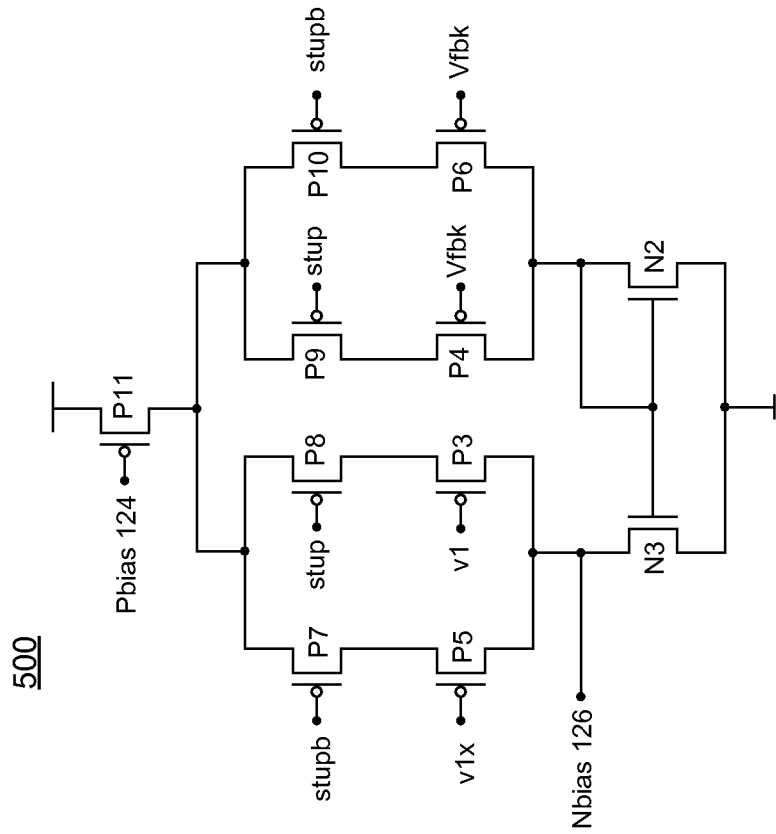


FIG. 5

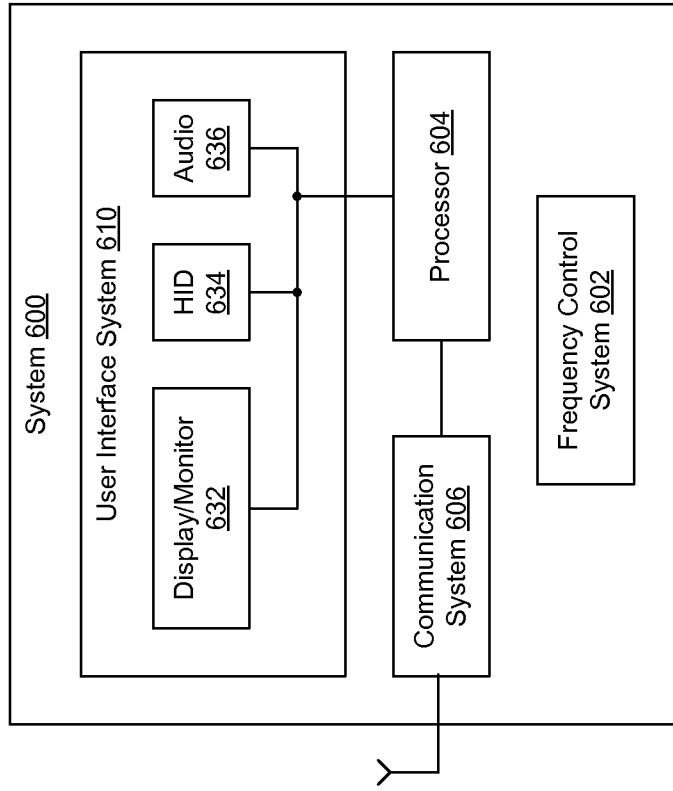


FIG. 6

A. CLASSIFICATION OF SUBJECT MATTER***H03L 7/099(2006.01)i, G05F 1/10(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03L 7/099; G01R 23/12; H03L 7/00; H03L 7/18; H03L 7/06; H03L 7/089

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: PLL, bias generator, static, dynamic, dual control

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6407600 B1 (LU; YI et al.) 18 June 2002 See abstract, claim 1 and figures 1, 2	1-16
A	US 6922047 B2 (ERNEST KNOLL et al.) 26 July 2005 See abstract, claims 1, 6, 8-10 and figure 2	1-16
A	US 2004-0135640 A1 (JOHN G. MANEATIS) 15 July 2004 See abstract, claim 1 and figure 1	1-16
A	US 05870003 A (BOERSTLER; DAVID WILLIAM) 09 February 1999 See abstract, claims 1, 2, 6, 8 and figure 1	1-16

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 DECEMBER 2012 (12.12.2012)

Date of mailing of the international search report

14 DECEMBER 2012 (14.12.2012)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/033612

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6407600 B1	18.06.2002	None	
US 6922047 B2	26.07.2005	US 2004-0239354 A1 US 2005-0206459 A1 US 2006-0244542 A1 US 7095289 B2 US 7265637 B2	02.12.2004 22.09.2005 02.11.2006 22.08.2006 04.09.2007
US 2004-0135640 A1	15.07.2004	US 2002-0101289 A1 US 2006-0012441 A1 US 6710665 B2 US 7292106 B2	01.08.2002 19.01.2006 23.03.2004 06.11.2007
US 05870003 A	09.02.1999	None	