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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title**: SINGLE SUPPLY CLASS-D AMPLIFIER

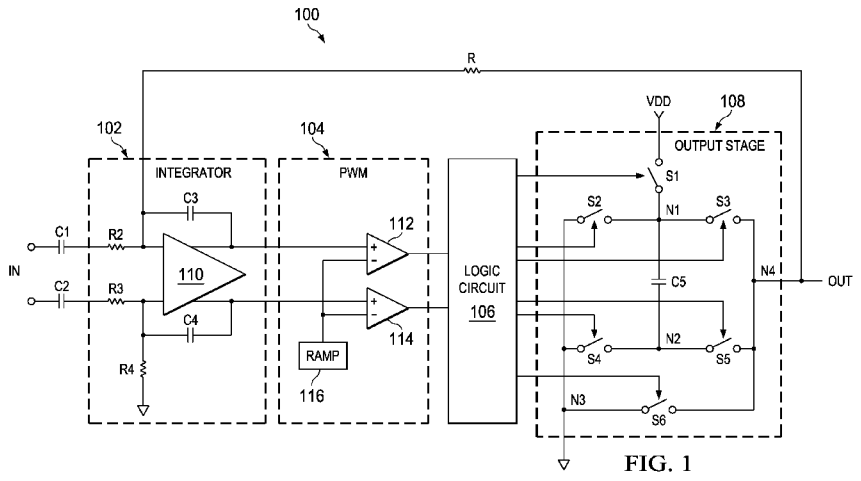

FIG. 1

(57) **Abstract**: A class-D amplifier is provided with an output stage that provides negative supply voltages, positive supply voltages, and ground. In a described amplifier 100, an analog input signal (IN) is provided to capacitors (C1, C2) and resistors (R2, R3) to substantially remove DC components and then integrated by an integrator (102). Comparators (112, 114) receive portions of the (differential) integrated signal for comparison with a ramp signal from a ramp generator 116. The comparison results are used by logic circuit (106) to generate control signals for switches (S1 through S6) of an output stage (108).

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SINGLE SUPPLY CLASS-D AMPLIFIER

[0001] The invention relates generally to a class-D amplifier and, more particularly, to a class-D amplifier that uses a signal supply.

BACKGROUND

[0002] Currently, Texas Instruments Incorporated (TI) offers a number of audio amplifiers that a include DIRECTPATH™ architecture. Some features of this architecture are that an output direct current or DC blocking capacitor is not needed and that there is a negative supply rail. An example is TI's TPA6140A2, which is a class-G amplifier that uses a charge pump to invert the voltage (from a positive supply) to create a negative supply voltage so that the headphone amplifier output can be centered at 0V without the need for DC blocking capacitors. However, there are some tradeoffs associated with this architecture; namely, supplying a negative supply voltage requires several external components as well as it reduces efficiency. Additionally, these types of devices may have also need to have separate power management circuits (i.e., buck converters). Therefore, there is a need for a method or an apparatus that offers similar advantages without the drawbacks.

[0003] Some other conventional circuits are described in: U.S. Patent Nos. 6,320,460; 6,753,729; 7,330,069; and 7,400,191.

SUMMARY

[0004] An example embodiment of the invention provides an apparatus including an integrator that receives an input signal; a pulse width modulator (PWM) that is coupled to the integrator; a logic circuit coupled to the PWM; and an output stage having: a first node; a second node; a third node; a fourth node that is coupled to ground; a capacitor that is coupled between the first and second nodes; and a switch network that is coupled to the first node, the second node, the third node, the fourth node, and a supply rail, wherein the switch network is controlled by logic circuit so as to operate in first mode, a second mode, and a third mode, and wherein, in the first mode, the voltage supply charges the capacitor and the third node is grounded, and

wherein, in the second mode, the capacitor provides a positive supply voltage to the third node, and wherein, in the third mode, the capacitor provides a negative supply voltage in the third mode.

[0005] In accordance with an example embodiment of the invention, the switch network further comprises: a first switch that is coupled between the supply rail and the first node, wherein the first switch is closed in the first mode; a second switch that is coupled between the first node and the fourth node, wherein the second switch is closed in the third mode; a third switch that is coupled between the first node and the third node, wherein the third switch is closed in the second mode; a fourth switch that is coupled between the second node and the fourth node, wherein the fourth switch is closed in the first mode and the second mode; a fifth switch that is coupled between the second node and the fourth node, wherein the fifth switch is closed in the third mode; and a sixth switch that is coupled between the third node and the fourth node, wherein the sixth switch is closed in the first mode.

[0006] In accordance with an example embodiment of the invention, the input signal is differential.

[0007] In accordance with an example embodiment of the invention, the integrator further comprises: an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second output terminal; and a first feedback capacitor that is coupled between the first input terminal and the first output terminal; and a second feedback capacitor that is coupled between the second input terminal and the second output terminal.

[0008] In accordance with an example embodiment of the invention, the PWM further comprises: a first comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the integrator, and wherein the output terminal of the first comparator is coupled to the logic circuit; a second comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the integrator, and wherein the output terminal of the second comparator is coupled to the logic circuit; and a ramp generator that is coupled to the second input terminal of the first comparator and the second input terminal of the second comparator.

[0009] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises an audio source that generates an audio signal; a class-D amplifier having: a first capacitor that is coupled to the audio source so as to receive the audio signal; an integrator is coupled to the first capacitor; a pulse width modulator (PWM) that is coupled to the integrator; a logic circuit coupled to the PWM; and an output stage having: a first node; a second node; a third node; a fourth node that is coupled to ground; a capacitor that is coupled between the first and second nodes; and a switch network that is coupled to the first node, the second node, the third node, the fourth node, and a supply rail, wherein the switch network is controlled by logic circuit so as to operate in first mode, a second mode, and a third mode, and wherein, in the first mode, the voltage supply charges the capacitor and the third node is grounded, and wherein, in the second mode, the capacitor provides a positive supply voltage to the third node, and wherein, in the third mode, the capacitor provides a negative supply voltage in the third mode; and a speaker that is coupled to the third node.

[0010] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a supply rail; a first node; a second node; a third node; a fourth node that is coupled to ground; a first direct current (DC) blocking capacitor that receives a first portion of an input signal; a second DC blocking capacitor that receives a second portion of the input signal; an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second output terminal, wherein the first input terminal of the amplifier is coupled to the first DC blocking capacitor, and wherein the second input terminal of the amplifier is coupled to the second DC blocking capacitor; a first feedback capacitor that is coupled between the first input terminal and the first output terminal; a second feedback capacitor that is coupled between the second input terminal and the second output terminal; a first comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the first output terminal of the amplifier; a second comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the second output terminal of the amplifier; a ramp generator that is coupled to the second input terminal of the first comparator and the second input terminal of the second comparator; a logic circuit coupled to the output terminals of the first and second comparators; an output capacitor that is coupled between the first and second nodes; a first switch that is coupled between the

supply rail and the first node, wherein the first switch is closed by the logic circuit in a first mode; a second switch that is coupled between the first node and the fourth node, wherein the second switch is closed by the logic circuit in a second mode; a third switch that is coupled between the first node and the third node, wherein the third switch is closed by the logic circuit in a third mode; a fourth switch that is coupled between the second node and the fourth node, wherein the fourth switch is closed by the logic circuit in the first mode and the third mode; a fifth switch that is coupled between the second node and the fourth node, wherein the fifth switch is closed by the logic circuit in the second mode; and a sixth switch that is coupled between the third node and the fourth node, wherein the sixth switch is closed by the logic circuit in the first mode.

[0011] In accordance with an example embodiment of the invention, the apparatus further comprises an audio source that is coupled to the first and second DC blocking capacitors so as to provide the input signal.

[0012] In accordance with an example embodiment of the invention, the apparatus further comprises a speaker that is coupled to the third node.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Example embodiments are described with reference to accompanying drawings, wherein:

[0014] FIG. 1 is a circuit diagram of an example of a class-D amplifier in accordance with an example embodiment of the invention; and

[0015] FIG. 2 is a system that employs the class-D amplifier of FIG. 1.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0016] In FIG. 1, the reference numeral 100 generally designates an example of a class-D amplifier in accordance with an example embodiment of the invention. Amplifier 100 generally comprises direct current (DC) blocking capacitors C1 and C2, input resistors R2 and R3, an integrator 102, a pulse width modulator (PWM) 104, logic circuit 106, and output stage 108. The integrator 102 generally comprises amplifier 110, feedback capacitors C3 and C4, and resistors R1 and R4 PWM 104 generally comprises comparators 112 and 114 and ramp generator 116, and output stage 108 generally comprises output capacitor C5 (which may be a signal capacitor or multiple capacitors) and switches S1 through S6. Additionally, supply rail VDD is typically coupled to a battery, a cell, or another power source.

[0017] In operation, amplifier 100 receives an analog input signal IN and generates an output signal OUT (which generally has values of "0" or ground, "-1" or negative supply voltage, and "+1" or positive supply voltage). To accomplish this, the input signal IN (which is generally differential, but may also be single ended) is provided to capacitors C1 and C2 and resistors R2 and R3, where capacitors C1 and C2 operate to substantially remove DC components from input signal IN. Additionally, capacitors C1 and C2 are optional components, which are not necessary for amplifier 100 to operate. The integrator 102 then integrates the signal from capacitors C1 and C2 and resistors R1 and R2. Each of comparators 112 and 114 receives a portion of the (differential) integrated signal from integrator 102 and compares its portion to a ramp signal from ramp generator 116. The comparison results from comparators 112 and 114 can then be used by logic circuit 106 to generate control signals for switches S1 through S6.

[0018] In particular, there are three modes of operation. In a first mode, logic circuit 106 closes switches S1, S4, and S6, which couples the output node N4 and node N2 to node N3 (which is coupled to ground) and couples node N1 to the supply rail VDD. Thus, output capacitor C5 can be charged to the voltage on supply rail VDD, while a "0" is output from node N4. In a second mode, logic circuit 106 closes switches S3 and S4 to provide a positive supply voltage or "+1" at node N4 because the positive plate of capacitor C5 (plate charged to the voltage on supply rail VDD) is coupled to node N4, while the opposite, negative plate of C5 is coupled to ground. Alternatively, for a second mode, switches S1 and S3 can be closed to provide a positive supply voltage or "+1" at node N4 directly from supply rail VDD. In a third mode, logic circuit 106 closes switches S2 and S5 to provide a negative supply voltage or "-1" to output node N4 because the positive plate of capacitor C5 is coupled to ground while the negative plate of capacitor C5 is coupled to node N4. Alternatively, five switches may be used to accomplish substantially the same result.

[0019] As a result of this configuration, large external capacitors (on the order of about 1 μF to about 47μF) used for conventional circuits to generate a negative rail voltage can be eliminated. Additionally, there is a reduction in the DC power loss, and there is the efficiency in increased over conventional amplifiers. In particular, simulation results show a 40-50% increase over the TI's TPA6140 when delivering 1mW at 16Ω. Additionally, simulation results

have also shown a total harmonic distortion of THD of about 0.2% for about 1mW delivered at 1kHz for a supply voltage of 3.6V on rail VDD, and a load resistance of about 32Ω.

[0020] There are some limitations, however, with this amplifier 100. Capacitor C5 is not a true voltage source (like a battery or power supply) because it has a relatively short discharge time. This short discharge time limits the output pulse width through node N4, but if the control loop within logic circuit 106 is sufficiently fast and capacitor C5 is sufficiently large, the rapid discharge time of capacitor C5 should not significantly affect performance. For example, using an internal clock frequency of about 1MHz with a capacitance of about 1μF is generally sufficient. Additionally, the output duty cycle is generally limited to about 50% because the logic circuit 106 generally converts the simple differential PWM modulation into an SE ternary PWM modulation.

[0021] Turning now to FIG. 2, an example of a system 200 that employs amplifier 100 can be seen. Generally, system 200 is a portable media device (i.e., mp3 player) that generates an audio signal from an audio source 202. Amplifier 100 receives this audio signal from source 202 and provides an amplified signal through output N4 to a speaker 204 (i.e., headphones). Each of the audio device 202 and amplifier 100 are powered by an onboard power cell 206 (i.e., battery).

[0022] Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are intended to be covered hereby. Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

an integrator that receives an input signal;

a pulse width modulator (PWM) that is coupled to the integrator;

a logic circuit coupled to the pulse width modulator; and

an output stage having:

a first node;

a second node;

a third node;

a fourth node that is coupled to ground;

a capacitor that is coupled between the first and second nodes; and

a switch network that is coupled to the first node, the second node, the third node, the fourth node, and a supply rail;

wherein the switch network is controlled by the logic circuit so as to operate in first mode, a second mode, and a third mode;

wherein, in the first mode, the voltage supply charges the capacitor and the third node is grounded;

wherein, in the second mode, the capacitor provides a positive supply voltage to the third node; and

wherein, in the third mode, the capacitor provides a negative supply voltage in the third mode.

2. The apparatus of Claim 1, wherein the switch network further comprises:

a first switch that is coupled between the supply rail and the first node, wherein the first switch is closed in the first mode;

a second switch that is coupled between the first node and the fourth node, wherein the second switch is closed in the third mode;

a third switch that is coupled between the first node and the third node, wherein the third switch is closed in the second mode;

a fourth switch that is coupled between the second node and the fourth node, wherein the fourth switch is closed in the first mode and the second mode;

a fifth switch that is coupled between the second node and the fourth node, wherein the fifth switch is closed in the third mode; and

a sixth switch that is coupled between the third node and the fourth node, wherein the sixth switch is closed in the first mode.

3. The apparatus of Claim 1, wherein the input signal is differential.

4. The apparatus of Claim 3, wherein the integrator further comprises:

an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second output terminal;

a first feedback capacitor that is coupled between the first input terminal and the first output terminal; and

a second feedback capacitor that is coupled between the second input terminal and the second output terminal.

5. The apparatus of Claim 1, wherein the pulse width modulator further comprises:

a first comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the integrator, and wherein the output terminal of the first comparator is coupled to the logic circuit;

a second comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the integrator, and wherein the output terminal of the second comparator is coupled to the logic circuit; and

a ramp generator that is coupled to the second input terminal of the first comparator and the second input terminal of the second comparator.

6. The apparatus of Claim 1, further comprising an audio source that generates an audio signal; a second capacitor that is coupled to the audio source so as to receive the audio signal; and a speaker that is coupled to the third node; and wherein the integrator is coupled to the

second capacitor; and the second capacitor, integrator, pulse width modulator, logic circuit, and output stage provide a class-D amplifier.

7. The apparatus of Claim 6, wherein the switch network further comprises:

a first switch that is coupled between the supply rail and the first node, wherein the first switch is closed in the first mode;

a second switch that is coupled between the first node and the fourth node, wherein the second switch is closed in the third mode;

a third switch that is coupled between the first node and the third node, wherein the third switch is closed in the second mode;

a fourth switch that is coupled between the second node and the fourth node, wherein the fourth switch is closed in the first mode and the second mode;

a fifth switch that is coupled between the second node and the fourth node, wherein the fifth switch is closed in the third mode; and

a sixth switch that is coupled between the third node and the fourth node, wherein the sixth switch is closed in the first mode.

8. The apparatus of Claim 7, wherein the integrator further comprises:

an amplifier having a first input terminal, a second input terminal, a first output terminal, and a second output terminal; and

a first feedback capacitor that is coupled between the first input terminal and the first output terminal; and

a second feedback capacitor that is coupled between the second input terminal and the second output terminal.

9. The apparatus of Claim 8, wherein the pulse width modulator further comprises:

a first comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the integrator, and wherein the output terminal of the first comparator is coupled to the logic circuit;

a second comparator having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the integrator, and wherein the output terminal of the second comparator is coupled to the logic circuit; and

a ramp generator that is coupled to the second input terminal of the first comparator and the second input terminal of the second comparator.

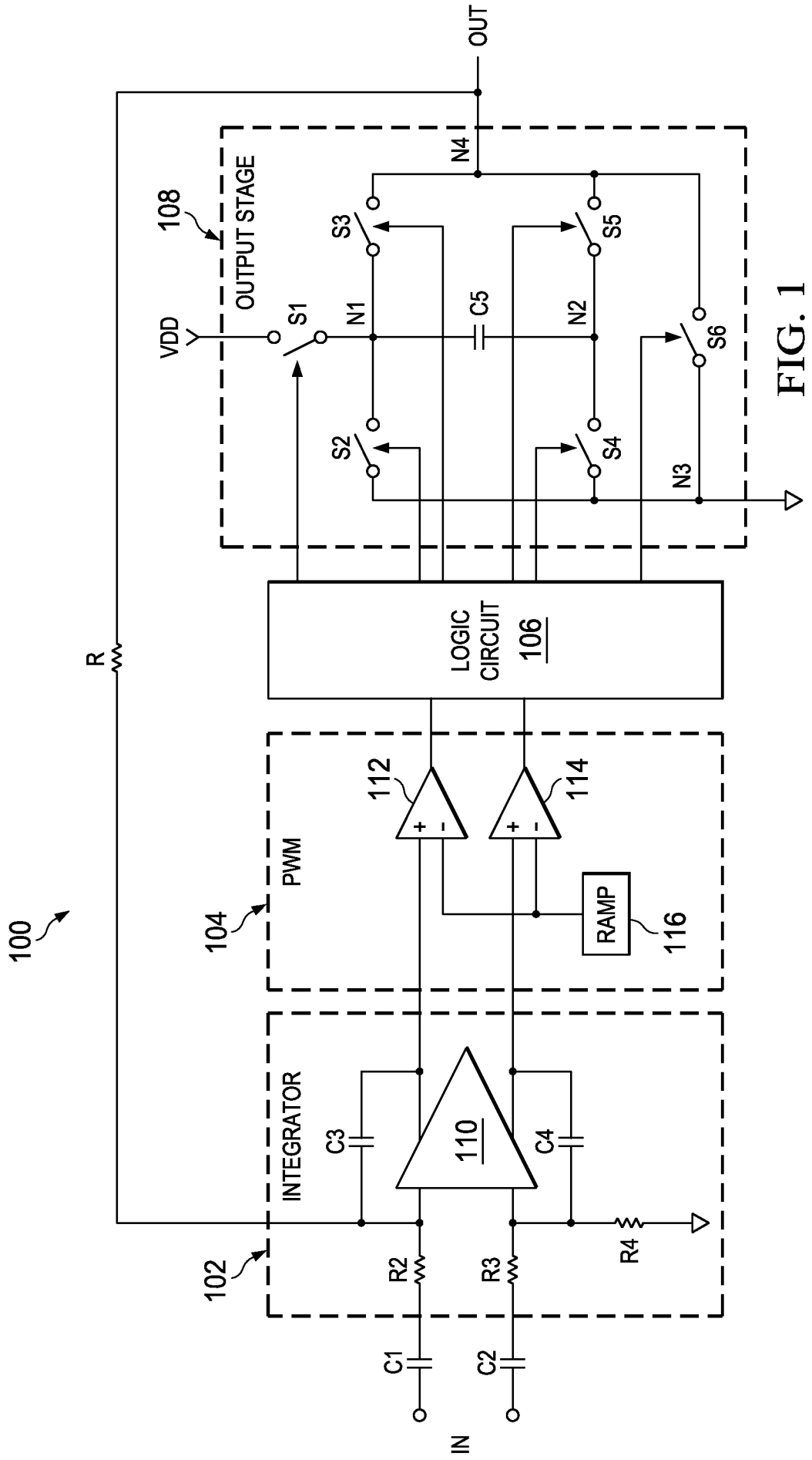
OUT
N4
108
OUTPUT STAGE
S3
S5
VDD
S1
N1
C5
N2
S6
S2
S4
N3
R
LOGIC CIRCUIT 106
112
114
PWM
104
RAMP
116
100
C3
110
C4
INTEGRATOR
102
R2
R3
R4
C1
C2
IN

FIG. 1

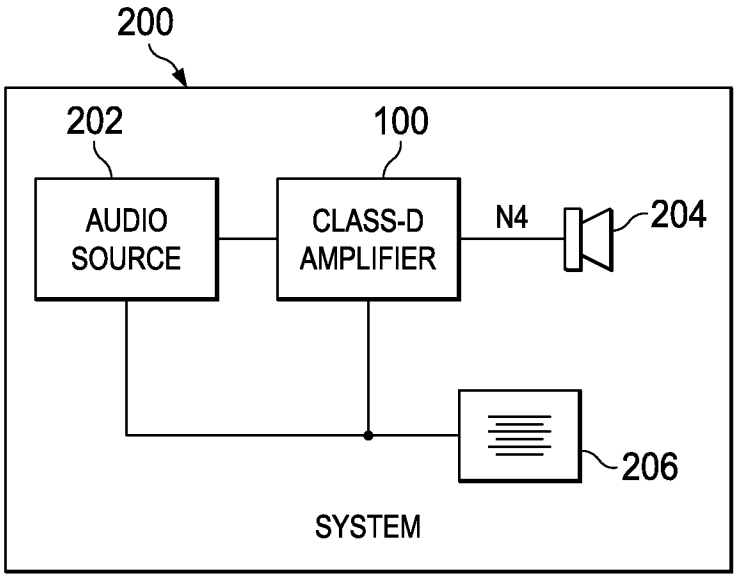

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/061522

A. CLASSIFICATION OF SUBJECT MATTER

H03F 3/217(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 3/217; H03F 3/38; H04B 1/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:single supply,PWM,switch network,supply,logic circuit,integrator,capacitor,negative supply voltage,positive supply voltage,feedback capacitor,ramp generator,comparator

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0054023 A1 (BEAN RONNIE A. et al.) 26 February 2009 See Fig.4, claims 1-26	1-9
A	US 7518442 B1 (DIJKSTRA GERRIT et al.) 14 April 2009 See Fig.2-6, claims 1-21	1-9
A	US 2008-0030268 A1 (PATRICK QUILTER) 07 February 2008 See Fig.1A, claims 1-38	1-9
A	US 2008-0030267 A1 (Cheng-Chung Yang) 07 February 2008 See Fig.3-6,claims 1-27	1-9
A	Patrick P.Siniscalchi et al, 2009 IEEE Interntional solid-state circuits conference "a 20W/channel class D amplifier with significantly reduced common-mode radiated emmissions", 28 February 2009 See Fig.26.4.2	1-9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 AUGUST 2011 (24.08.2011)	**25 AUGUST 2011 (25.08.2011)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer JUNG, BYEONG HONG Telephone No. 82-42-481-5752

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2010/061522

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