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Vellianitis et al.

(54) **FINFET WITH TWO FINS ON STI**

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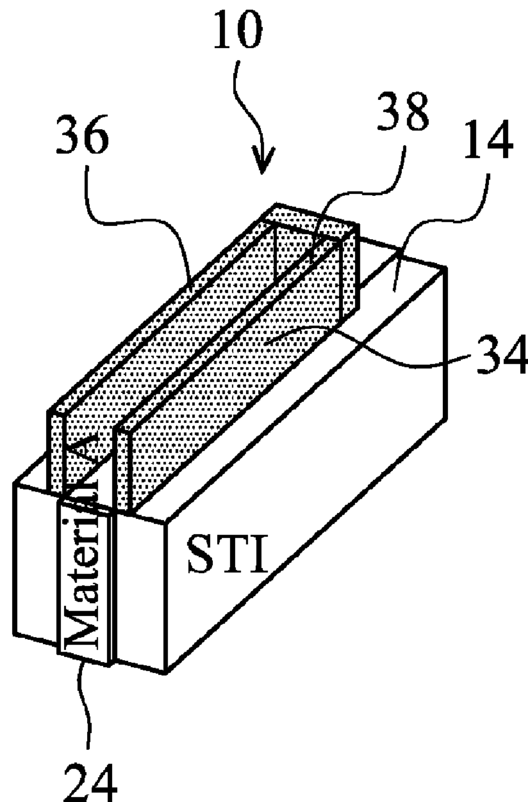
(57) **ABSTRACT**

A fin structure for a fin field effect transistor (FinFET) device is provided. The device includes a substrate, a first semiconductor material disposed on the substrate, a shallow trench isolation (STI) region disposed over the substrate and formed on opposing sides of the first semiconductor material, and a second semiconductor material forming a first fin and a second fin disposed on the STI region, the first fin spaced apart from the second fin by a width of the first semiconductor material. The fin structure may be used to generate the FinFET device by forming a gate layer formed over the first fin, a top surface of the first semiconductor material disposed between the first and second fins, and the second fin.



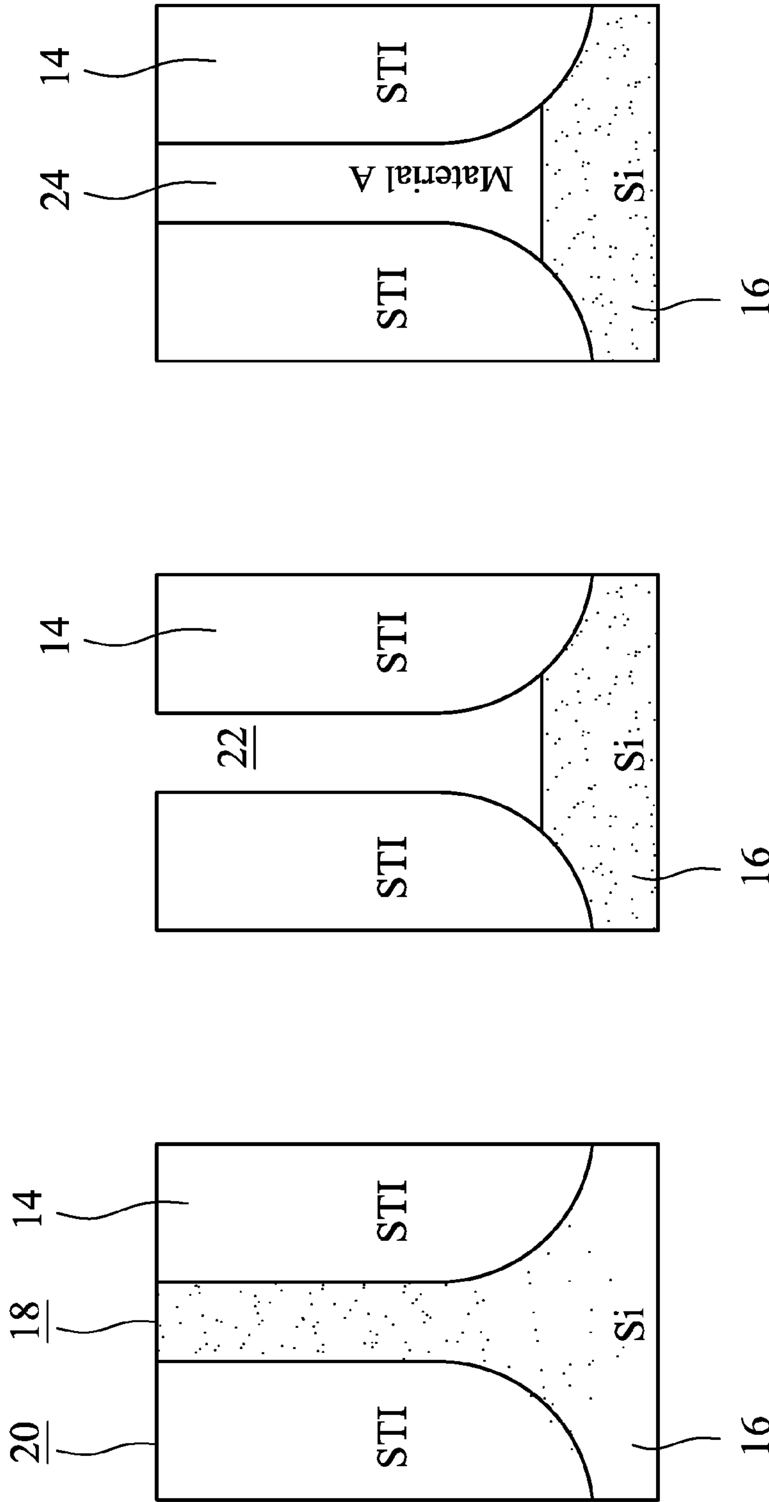


Fig. 1c

Fig. 1b

Fig. 1a

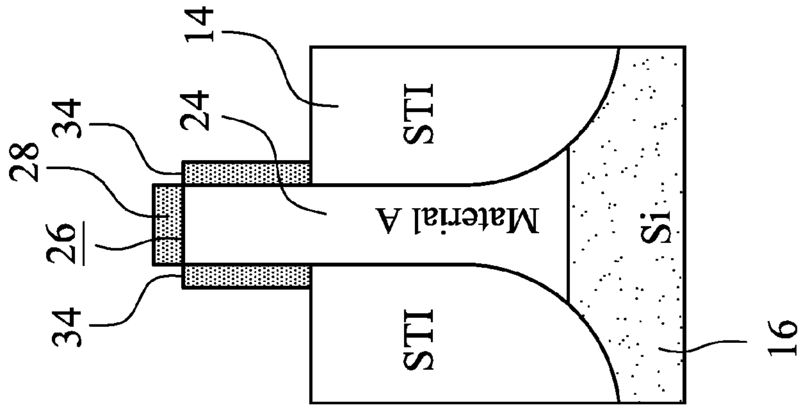


Fig. 1f

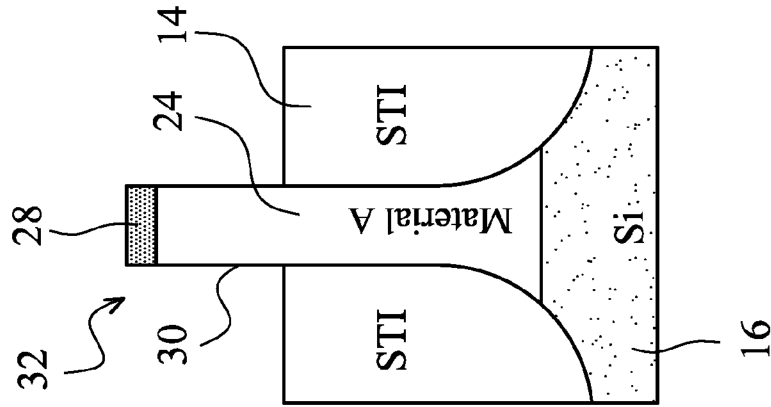


Fig. 1e

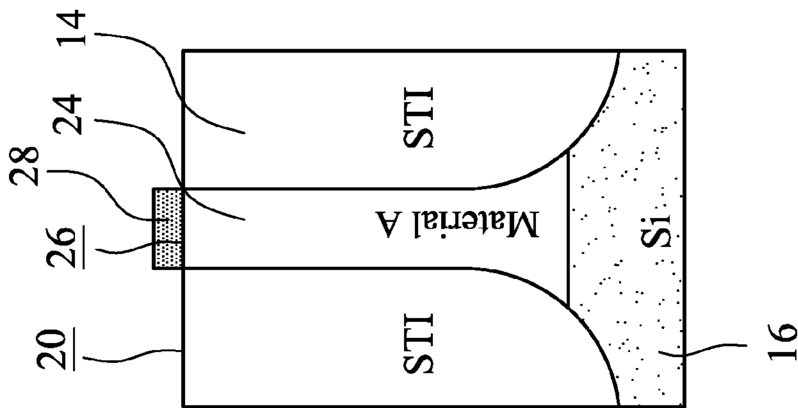


Fig. 1d

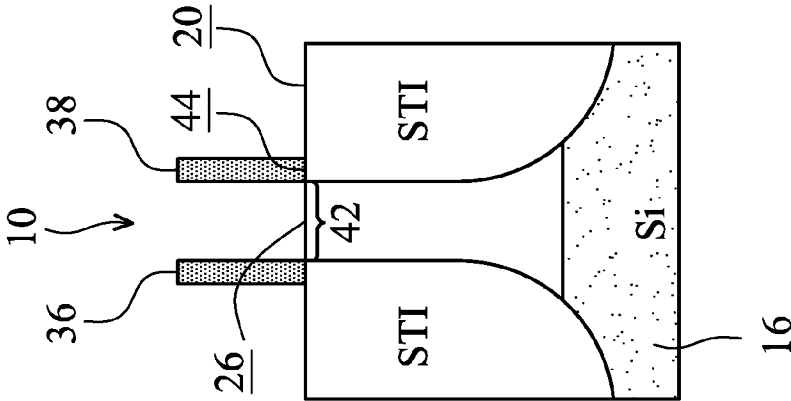


Fig. 1h

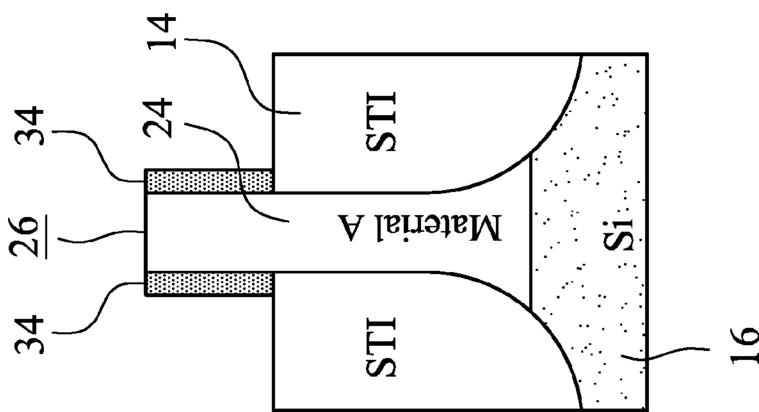


Fig. 1g

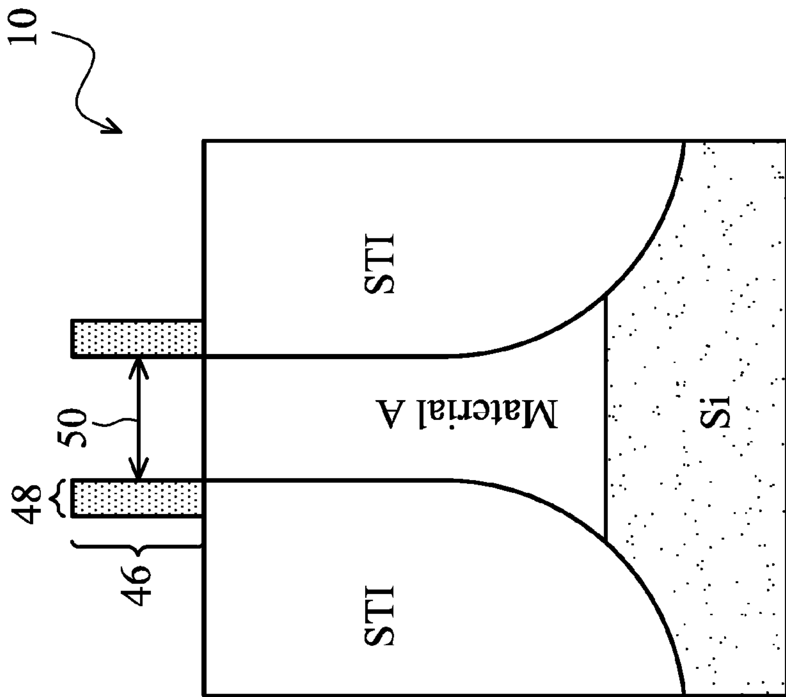


Fig. 2

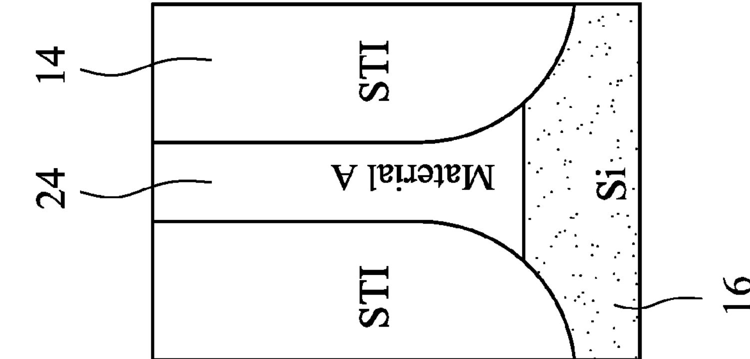
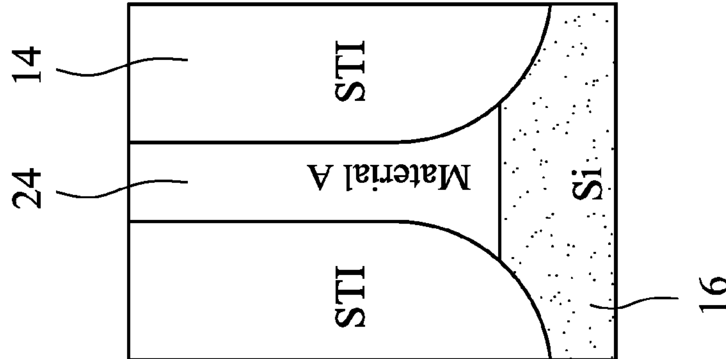



Fig. 3c

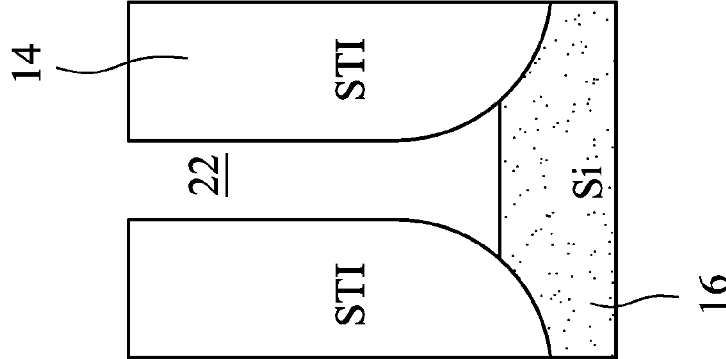


Fig. 3b

Fig. 3a

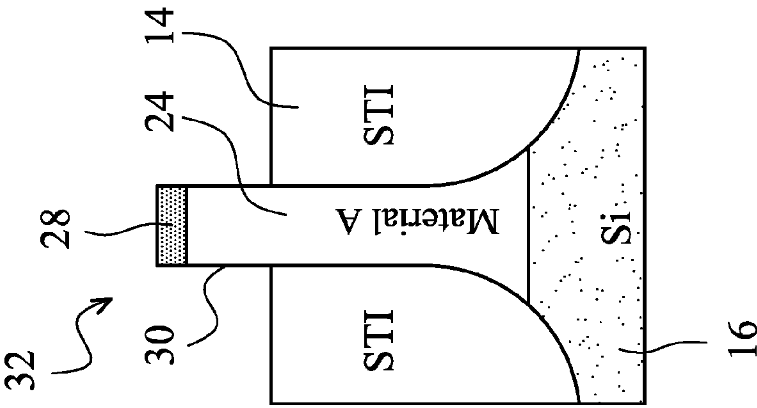


Fig. 3f

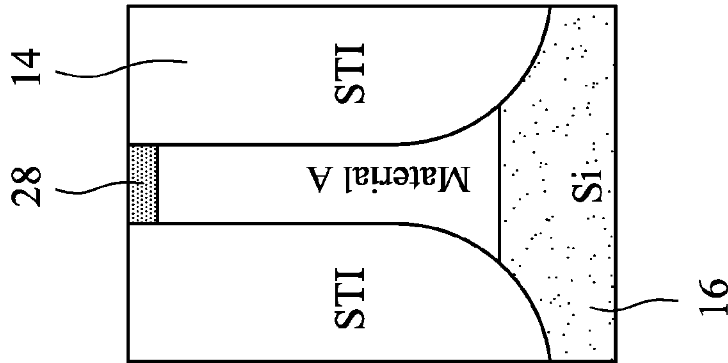


Fig. 3e

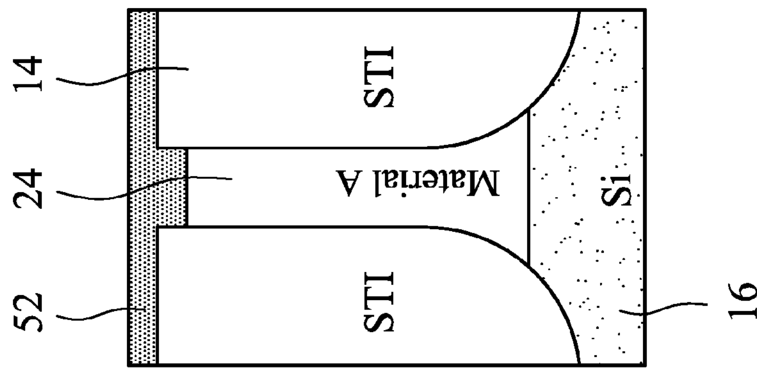


Fig. 3d

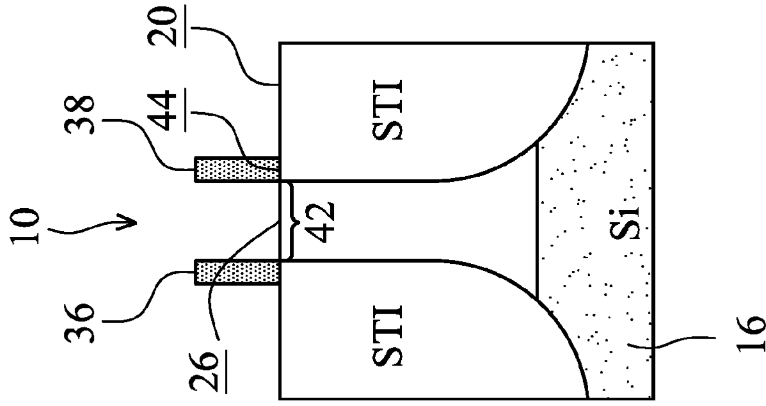


Fig. 3i

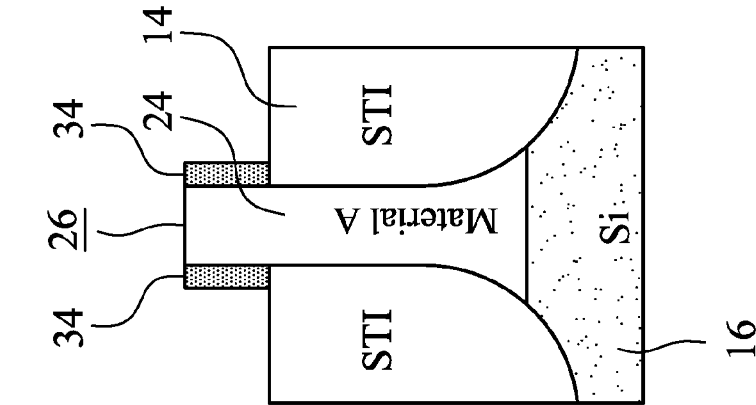


Fig. 3h

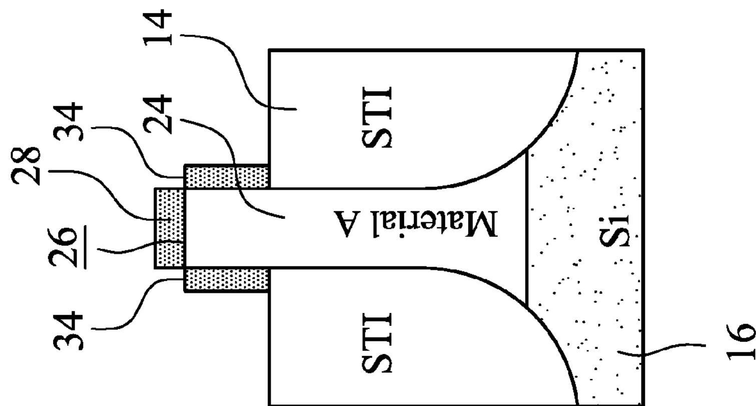


Fig. 3g

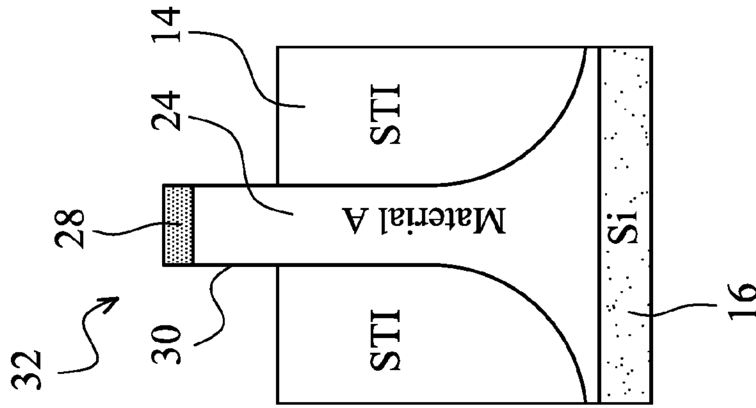


Fig. 4c

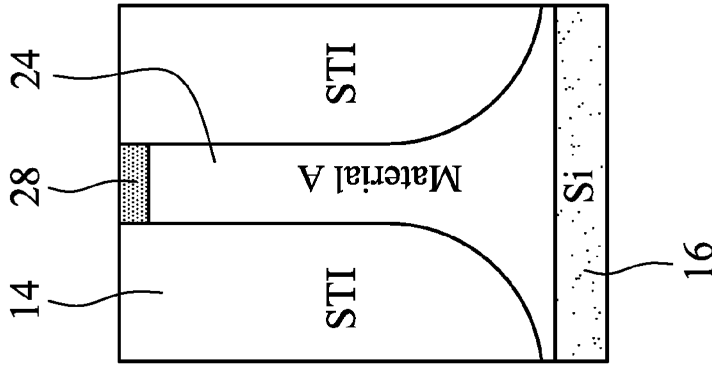


Fig. 4b

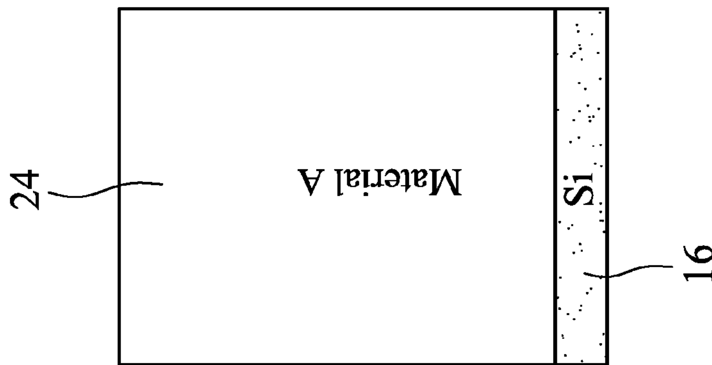


Fig. 4a

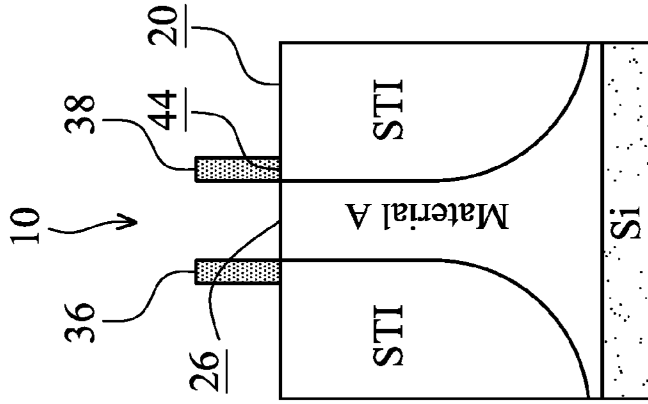


Fig. 4f

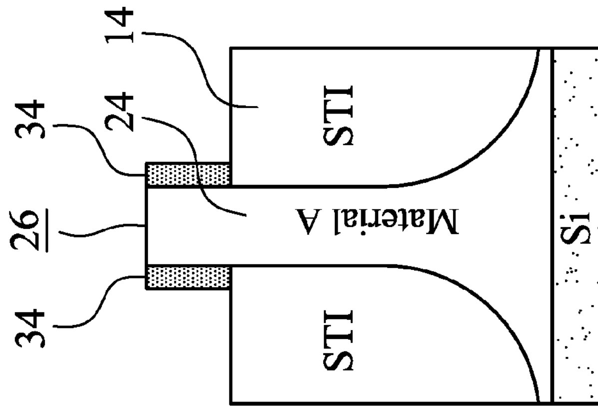


Fig. 4e

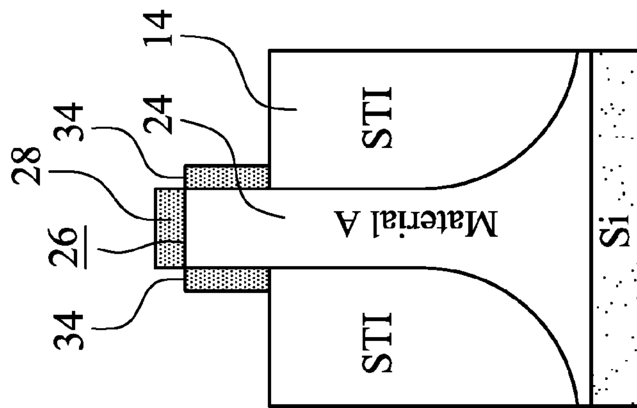


Fig. 4d

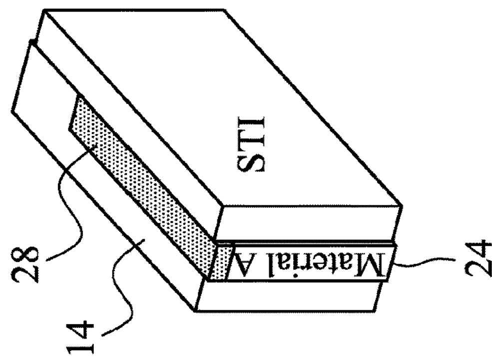


Fig. 5a

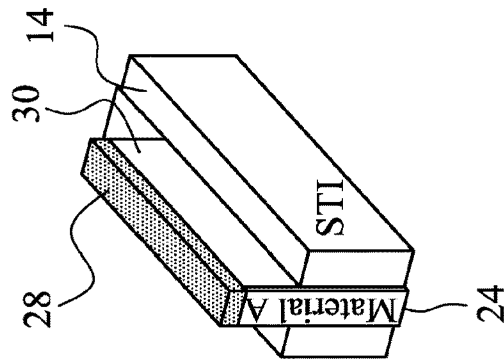


Fig. 5b

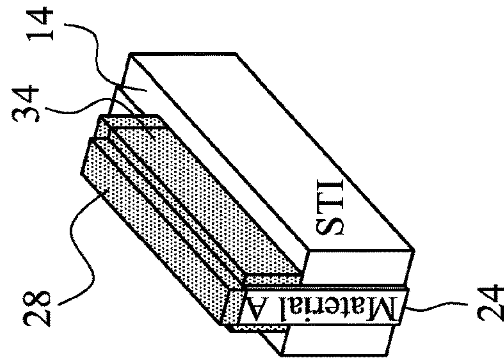


Fig. 5c

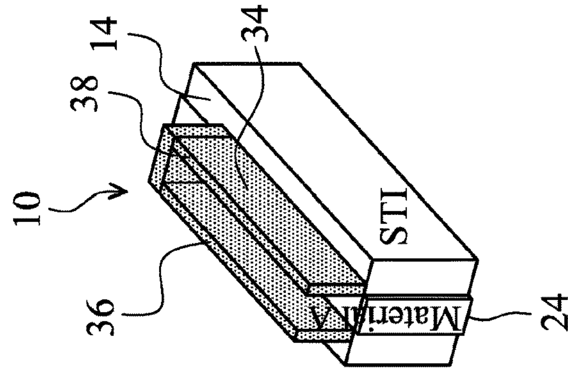


Fig. 5d

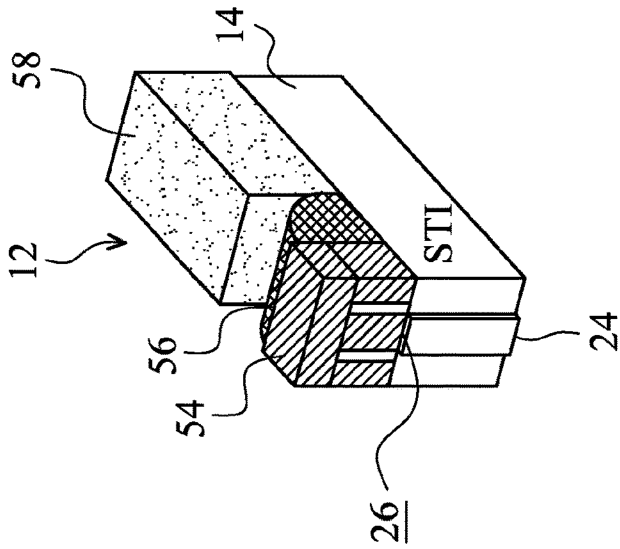


Fig. 5g

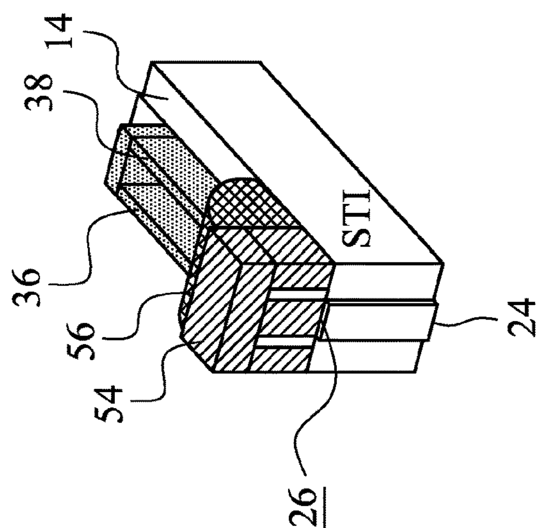


Fig. 5f

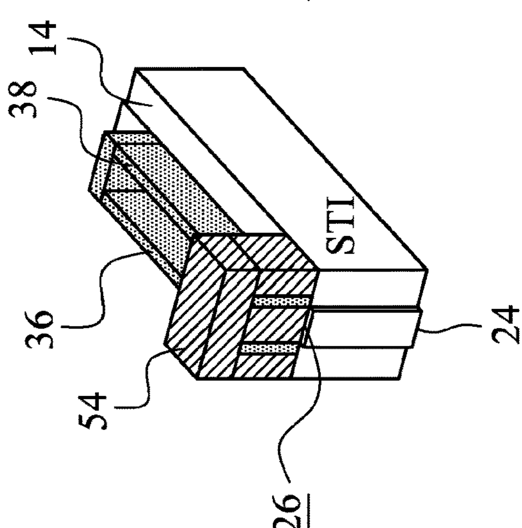


Fig. 5e

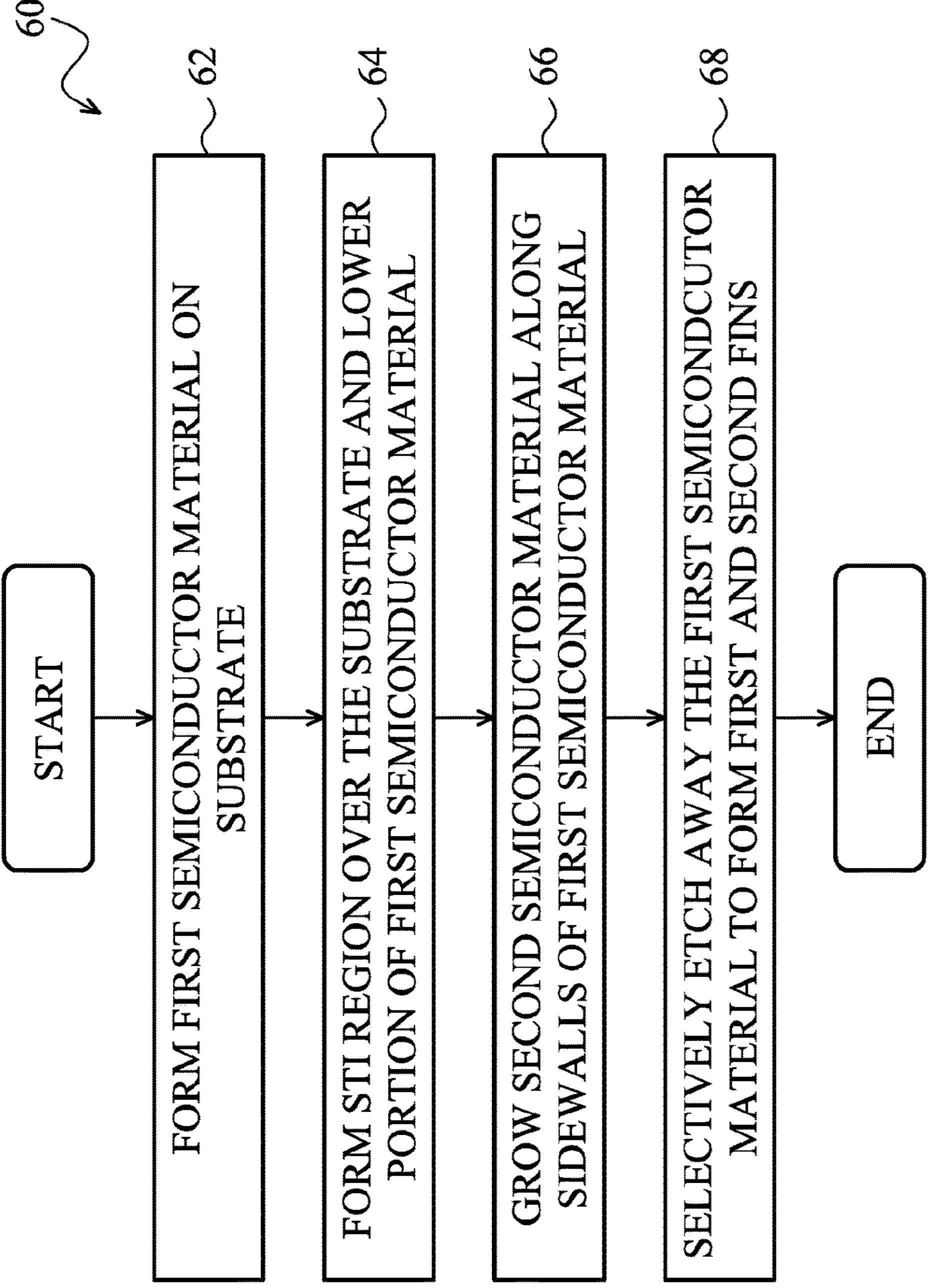


Fig. 6

FINFET WITH TWO FINS ON STI

[0001] This application is a continuation application of and claims the benefit of U.S. application Ser. No. 15/357,839, filed Nov. 21, 2016, entitled "FinFET with Two Fins on STI," which is a continuation application of and claims the benefit of U.S. application Ser. No. 14/604,401, filed Jan. 23, 2015, entitled "Forming Fins on the Sidewalls of a Sacrificial Fin to Form a FinFET," now U.S. Pat. No. 9,502,541, which is a divisional application of and claims the benefit of U.S. application Ser. No. 13/431,727, filed Mar. 27, 2012, entitled, "Fin Structure for a FinFET Device," now U.S. Pat. No. 8,987,835, each application is hereby incorporated herein by reference.

BACKGROUND

[0002] Semiconductor devices are used in a large number of electronic devices, such as computers, cell phones, and others. Semiconductor devices comprise integrated circuits that are formed on semiconductor wafers by depositing many types of thin films of material over the semiconductor wafers, and patterning the thin films of material to form the integrated circuits. Integrated circuits include field-effect transistors (FETs) such as metal oxide semiconductor (MOS) transistors.

[0003] One of the goals of the semiconductor industry is to continue shrinking the size and increasing the speed of individual FETs. To achieve these goals, fin FETs (FinFETs) or multiple gate transistors will be used in advanced transistor nodes. For example, FinFETs not only improve areal density but also improve gate control of the channel.

[0004] In an effort to increase the performance and reduce the power consumption of complementary metal-oxide-semiconductor (CMOS) and MOSFET devices, the semiconductor industry has employed high mobility semiconductors to replace silicon as the transistor channel. The semiconductor industry has also encouraged substrate isolation techniques through, for example, silicon on insulator (SOI) and heterostructure devices, which can improve off-state characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0006] FIGS. **1***a*-**1***h* collectively illustrate an embodiment of a process of forming a fin structure for a FinFET device;

[0007] FIG. **2** is a cross section of an embodiment of the fin structure produced using the process of FIG. **1**;

[0008] FIGS. **3***a*-**3***i* collectively illustrate an embodiment of a process of forming the fin structure of FIG. **2**;

[0009] FIGS. **4***a*-**4***f* collectively illustrate an embodiment of a process of forming the fin structure of FIG. **2**;

[0010] FIGS. **5***a*-**5***g* is a collectively illustrate an embodiment of a process of forming a FinFET device using one of the processes collectively illustrated in FIGS. **1***a*-**1***h*, **3***a*-**3***i*, or **4***a*-**4***f*; and

[0011] FIG. **6** is an embodiment of a method of forming the fin structure of FIG. **2**.

[0012] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0013] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

[0014] The present disclosure will be described with respect to preferred embodiments in a specific context, namely a FinFET metal oxide semiconductor (MOS). The invention may also be applied, however, to other integrated circuits, electronic structures, and the like.

[0015] FIGS. **1***a*-**1***h* collectively illustrate an embodiment of a process of forming a fin structure **10**, which is depicted in FIG. **2**, for a FinFET device **12**, which is depicted in FIG. **5***g*. As will be more fully explained below, the fin structure **10** produces a FinFET device **12** with enhanced transistor performance and improved power consumption by doubling fin density and improving substrate isolation. Indeed, the FinFET device **12** implementing the fin structure **10** provides superior performance, a short channel effect, and desirable off-state leakage control. In addition, the FinFET device **12** formed using the fin structure **10** disclosed herein increases the gate controlled area and decreases the width of the gate in the FinFET device **12** without having to increase the device footprint.

[0016] Referring now to FIG. **1***a*, a shallow trench isolation (STI) region **14** is formed around a substrate **16**. In an embodiment, the STI region **14** is formed from silicon dioxide or other suitable dielectric material. In an embodiment, the substrate **16** is silicon or other suitable semiconductor material. As shown, the substrate **16** generally projects upwardly between portions of the STI region **14**. In addition, a top surface **18** of the substrate **16** and a top surface **20** of the STI regions **14** are generally co-planar.

[0017] Referring now to FIG. **1***b*, a recess **22** is formed by etching away an upper portion of the substrate **16**. Thereafter, in FIG. **1***c*, a first semiconductor material **24** (a.k.a., Material A) is formed in the recess **22**. In an embodiment, the first semiconductor material **24** is epitaxially grown in the recess **22**. In an embodiment, after the recess **22** is filled with the first semiconductor material **24** a chemical mechanical planarization (CMP) process is performed to smooth a top surface **26** of the first semiconductor material **24** and the top surface **20** of the adjacent STI regions **14**.

[0018] In an embodiment, the first semiconductor material **24** is germanium (Ge), indium phosphide (InP), indium gallium arsenide (InGaAs), indium arsenide (InAs), gallium antimonide (GaSb), or silicon germanium (SiGe). In an embodiment, the first semiconductor material **24** is a group IV, a group III-V, or a group II-VI semiconductor material. In an embodiment, the first semiconductor material **24** is an alloy of SiGe having the formula $Si_{1-x}Ge_x$ (with $1>x>0$).

[0019] Referring to FIG. **1***d*, a hard mask **28** is formed upon the first semiconductor material **24**. In an embodiment, the hard mask **28** is formed from silicon nitride or other suitable mask material. Once the hard mask **28** has been deposited, a photolithography process is performed to pat-

tern the hard mask as shown in FIG. **1***d*. Next, the upper portion of the STI region **14** is etched selectively to the hard mask as shown in FIG. **1***e*. As depicted in FIG. **1***e*, opposing sidewalls **30** from an upper portion **32** of the first semiconductor material **24** are now exposed.

[0020] Referring now to FIG. **1***f*, a second semiconductor material **34** (a.k.a., Material B) is formed on and over the sidewalls **30** of the first semiconductor material **24**. In an embodiment, the second semiconductor material **34** is epitaxially grown along the sidewalls **30** of the first semiconductor material **24**. As shown, the second semiconductor material **34** is seated upon and projects above the STI region **14**. Because the hard mask **28** has not been removed, the second semiconductor material **34** is not grown or otherwise formed upon the top surface **26** of the first semiconductor material **24**.

[0021] With the second semiconductor material **34** disposed on the sidewalls **30** of the first semiconductor material **24**, the hard mask **28** may be removed as illustrated in FIG. **1***g*. In an embodiment, the hard mask **28** is removed without attacking the adjacent second semiconductor material **34** and STI regions **14**. Thereafter, a selective etch process is performed to remove the upper portion **32** (FIG. **1***e*) of the first semiconductor material **24** as shown in FIG. **1***h*. As shown in FIG. **1***h*, after the first semiconductor material **24** has been etched away, the second semiconductor material **24** forms a first fin **36** and a second fin **38** of the overall fin structure **10**.

[0022] The first and second fins **36**, **38** are generally disposed upon and directly contact the STI region **14** and have a recess **40** interposed between them. In addition, in an embodiment the first fin **36** is spaced apart from the second fin **38** by a width **42** of the first semiconductor material **24**. Still referring to FIG. **1***h*, the top surface **26** of the first semiconductor material **24** and/or the top surface **20** of the STI region **14** is generally co-planar with a bottom surface **44** of the first and second fins **36**, **38**. In an embodiment, the top surface **26** of the first semiconductor material **24** may be disposed vertically below the top surface **20** of the STI region **14**. As shown, the first and second fins **36**, **38** project vertically above the top surface of the first semiconductor material **24**. In an embodiment, the first semiconductor material **24** is doped to inhibit or prevent conduction through the first semiconductor material **24**.

[0023] In an embodiment, the second semiconductor material **34** is silicon (Si) when the first semiconductor material **24** is germanium (Ge). In such an embodiment, the germanium may be etched away with very high selectivity using a solution of hydrochloric acid (HCl). In an embodiment, the second semiconductor material **34** is indium gallium arsenide (InGaAs) when the first semiconductor material **24** is indium phosphide (InP). In such an embodiment, the indium phosphide may be etched away with very high selectivity using a solution of hydrochloric acid (HCl).

[0024] In an embodiment, the second semiconductor material **34** is indium phosphide (InP) when the first semiconductor material **24** is indium gallium arsenide (InGaAs). In such an embodiment, the indium gallium arsenide may be etched away with very high selectivity using a solution of phosphoric acid and hydrogen peroxide ($H_3PO_4+H_2O_2$). In an embodiment, the second semiconductor material **34** is gallium antimonide (GaSb) when the first semiconductor material **24** indium arsenide (InAs). In such an embodiment, the indium arsenide may be etched away with very high selectivity using a solution of citric acid and hydrogen peroxide ($C_6H_8O_7+H_2O_2$).

[0025] In an embodiment, the second semiconductor material **34** is indium arsenide (InAs) when the first semiconductor material **24** gallium antimonide (GaSb). In such an embodiment, the gallium antimonide may be etched away with very high selectivity using a solution of ammonium hydroxide (NH_4OH). Other combinations and other etch compounds are possible in other embodiments. In some embodiments, selectivity may approach or achieve one hundred percent.

[0026] In an embodiment, the second semiconductor material **34** is a group IV, a group III-V, or a group II-VI semiconductor material. In an embodiment, the second semiconductor material **34** is an alloy of SiGe having the formula $Si_{1-y}Ge_y$ (with $1>y>0$) when the first semiconductor material **24** is an alloy of SiGe having the formula $Si_{1-x}Ge_x$ (with $1>x>0$), in which case $x>y$. In such an embodiment, the alloy of SiGe having the formula $Si_{1-x}Ge_x$ may be etched away with very high selectivity using a solution of hydrochloric acid (HCl).

[0027] Referring now to FIG. **2**, in an embodiment a height **46** of the first and second fins **36**, **38** on the fin structure **10** may be between about five nanometers (5 nm) and about forty nanometers (40 nm). In an embodiment, a width **48** of the first and second fins **36**, **38** may be between about two nanometers (2 nm) and about ten nanometers (10 nm). In an embodiment, a distance **50** between the first and second fins **36**, **38** (which generally equates to the width of the upper portion **42** of first semiconductor material **24**, as shown in FIG. **1***h*) may be between about five nanometers (5 nm) and about twenty nanometers (20 nm). Other dimensions may be possible in other embodiments.

[0028] FIGS. **3***a*-**1***i* collectively illustrate another embodiment of a process of forming a fin structure for a FinFET device. After performing the steps of FIGS. **3***a*-**3***c* as previously described above, the first semiconductor material **24** is recessed and a hard mask layer **52** is formed as depicted in FIG. **3***d*. Thereafter, as shown in FIG. **3***e* a CMP process is performed to generate the hard mask **28**, which is embedded within the STI region **14**. Thereafter, the steps of FIGS. **3***f*-**3***i* are performed as previously described above.

[0029] FIGS. **4***a*-**4***f* collectively illustrate another embodiment of a process of forming a fin structure for a FinFET device. As shown in FIG. **4***a*, a blanket layer of the first semiconductor material **24** is grown or deposited upon the substrate **16**. Thereafter, a portion of the first semiconductor material **24** is etched away and replaced by STI region **14** as shown in FIG. **4***b*. In FIG. **4***b* the first semiconductor material **24** is also etched to provide room for formation of the hard mask **28** thereon. Thereafter, the steps of FIGS. **4***c*-**4***f* are performed as previously described above.

[0030] FIGS. **5***a*-**5***g* collectively illustrate an embodiment of a process of forming the FinFET device **12** using, for example, one of the processes collectively illustrated in FIGS. **1***a*-**1***h*, **3***a*-**3***i*, or **4***a*-**4***f* to generate the fin structure **10**. As shown in FIG. **5***a*, the hard mask **28** has been formed upon the first semiconductor material **24**, which is surrounded by the STI region **14**. Thereafter, in FIG. **5***b* an upper portion of the STI region **14** is removed to expose the sidewalls **30** of the first semiconductor material **24**. Notably, the hard mask **28** is still present. Next, as shown in FIG. **5***c*

the second semiconductor material **34** is epitaxially grown on and over the sidewalls **30** and above the STI region **14**.

[0031] Once the second semiconductor material **34** has been formed, the hard mask **28** and then the upper portion of the first semiconductor material **24** (i.e., the portion of the first semiconductor material **24** disposed above the STI region **14**) are removed, which leaves the fin structure **10**. As noted above, the first semiconductor material **24** is selectively removed relative to the second semiconductor material **34**. As shown in FIG. **5***d*, the removal of the upper portion of the first semiconductor material **24** leaves first and second fins **36**, **38**, which are spaced apart from each other a distance equal to the width of the first semiconductor material **24**. The fins **36**, **38** are formed from the second semiconductor material **34**.

[0032] As shown in FIG. **5***e*, a gate layer **54** is formed over a portion of the STI region **14**, the first fin **36**, the top surface **26** of the first semiconductor material **24**, the second fin **38**, and then an additional portion of the STI region **14**. As shown in FIGS. **5***f*-**5***g*, a spacer **56** and a source/drain contact **58** is formed. For ease of illustration, only one of the spacers **56** and one of the source/drain contacts **58** has been shown in FIG. **5***g*. However, those skilled in the art will appreciate that additional spacers **56** and additional source/drain contacts **58** may be formed and employed by the FinFET device **12**. In an embodiment, the source/drain contact **58** is formed through an epitaxial growth process.

[0033] Referring now to FIG. **6**, a method **60** of forming a FinFET device is provided. In block **62**, the first semiconductor material **24** is formed on the substrate. In block **64**, the STI region **14** is formed over the substrate **16** and a lower portion of the first semiconductor material **24**. In block **66**, a second semiconductor material is epitaxially grown along sidewalls **30** of the upper portion **32** of the first semiconductor material **24**. In block **68**, the upper portion of the first semiconductor material is selectively etched away to form the first fin **36** and the second fin **38**, which are spaced apart from each other by a width of the first semiconductor material **24**.

[0034] A fin structure for a fin field effect transistor (FinFET) device. The device comprises a substrate, a first semiconductor material disposed on the substrate, a shallow trench isolation (STI) region disposed over the substrate and formed on opposing sides of the first semiconductor material, and a second semiconductor material forming a first fin and a second fin disposed on the STI region, the first fin spaced apart from the second fin by a width of the first semiconductor material.

[0035] A field effect transistor (FinFET) device. The device comprises a substrate, a first semiconductor material disposed on the substrate, a shallow trench isolation (STI) region disposed over the substrate and formed on opposing sides of the first semiconductor material, a second semiconductor material forming a first fin and a second fin disposed on the STI region, the first fin spaced apart from the second fin by a width of the first semiconductor material, and a gate layer formed over the first fin, a top surface of the first semiconductor material disposed between the first and second fins, and the second fin.

[0036] A method of forming a fin field effect transistor (FinFET) device. The method comprises forming a first semiconductor material on a substrate, forming a shallow trench isolation (STI) region over the substrate and a lower portion of the first semiconductor material, epitaxially growing a second semiconductor material along sidewalls of an upper portion of the first semiconductor material, and selectively etching away the upper portion of the first semiconductor material to form a first fin and a second fin, the first fin spaced apart from the second fin by a width of the first semiconductor material.

[0037] While the disclosure provides illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A method of forming a fin field effect transistor (FinFET) device, the method comprising:
- forming a first fin, the first fin having a top surface, a first sidewall, and a second sidewall, the first sidewall facing a first isolation region and the second sidewall facing a second isolation region;
- forming a mask on the top surface of the first fin;
- recessing the first isolation region and the second isolation region to expose the first sidewall and the second sidewall;
- epitaxially growing a second fin on the first sidewall and a third fin on the second sidewall, wherein
  - a first sidewall of the second fin contacts the first sidewall of the first fin,
  - a second sidewall of the second fin faces away from the first fin, the first sidewall of the second fin and the second sidewall of the second fin being on opposing sides of the second fin,
  - a first sidewall of the third fin contacts the second sidewall of the first fin, and
  - a second sidewall of the third fin faces away from the first fin, the first sidewall of the third fin and the second sidewall of the third fin being on opposing sides of the second fin;
- recessing the first fin to expose the first sidewall of the second fin and the first sidewall of the third fin; and
- forming a gate structure along the first sidewall of the second fin and the first sidewall of the third fin.

2. The method of claim **1**, wherein forming the mask comprises:
- forming the mask over the first fin while an upper surface of the first fin is level with an upper surface of the first isolation region.

3. The method of claim **1**, wherein forming the mask comprises:
- etching the first fin to form a recess between an upper surface of the first fin and an upper surface of the first isolation region and the second isolation region; and
- forming the mask in the recess.

4. The method of claim **3**, wherein forming the mask in the recess comprises:
- depositing a mask layer in the recess and over a top surface of the first isolation region and the second isolation region; and
- planarizing the mask layer to remove the mask layer from over the first isolation region and the second isolation region, thereby forming the mask in the recess.

5. The method of claim **1**, wherein the second fin is completely over the first isolation region and the third fin is completely over the second isolation region.

6. The method of claim **1**, wherein the first fin are formed of a different material than the second fin and the third fin.

7. The method of claim **1**, wherein the gate structure extends continuously between the second fin and the third fin.

8. A method of forming a fin field effect transistor (FinFET) device, the method comprising:
- forming a sacrificial fin on a substrate, the sacrificial fin comprising a first semiconductor material;
- after forming the sacrificial fin, epitaxially growing a first fin and a second fin along opposing sides of the sacrificial fin, the first fin having a first sidewall facing the first fin and a second sidewall facing away from the first fin, the second fin having a first sidewall facing the first fin and a second sidewall facing away from the first fin;
- after epitaxially growing the first fin and the second fin, recessing the sacrificial fin to expose the first sidewall and the second sidewall of the first fin and to expose the first sidewall and the second sidewall of the second fin; and
- after recessing the sacrificial fin, forming a gate structure extending along the first sidewall and the second sidewall of the first fin and along the first sidewall and the second sidewall of the second fin.

9. The method of claim **8**, wherein the sacrificial fin extends between isolation regions along opposing sidewalls of the sacrificial fin, wherein the first fin and the second fin directly contact the isolation regions.

10. The method of claim **9**, wherein after recessing the sacrificial fin, an upper surface of the sacrificial fin is recessed to an upper surface of the isolation regions.

11. The method of claim **8**, wherein after recessing the sacrificial fin, lowermost surfaces of the first fin and the second fin are above an uppermost surface of the sacrificial fin.

12. The method of claim **8**, wherein the sacrificial fin is formed of a different semiconductor material than the substrate.

13. The method of claim **8**, wherein the first fin and the second fin are formed of a different semiconductor material than the substrate.

14. The method of claim **8** further comprising, prior to epitaxially growing the first fin and the second fin, forming a dielectric mask on a top surface of the sacrificial fin.

15. A method of forming a fin field effect transistor (FinFET) device, the method comprising:
- forming a shallow trench isolation (STI) region over a substrate, the STI region having a first fin extending from the substrate, the first fin being a first semiconductor material, sidewalls of an upper portion of the first fin being exposed;
- after forming the STI region, epitaxially growing a second fin along a first sidewall of the first fin and a third fin along a second sidewall of the first fin, the second fin and the third fin comprising a second semiconductor material different than the first semiconductor material, bottom surfaces of the second fin and the third fin contacting the STI region; and
- after epitaxially growing the second fin and the third fin, selectively etching the first fin, wherein after selectively etching the first fin, opposing sidewalls of the second fin and opposing sidewalls of the third fin are exposed.

16. The method of claim **15**, further comprising forming a mask on an upper surface of the first fin, wherein the mask prevents epitaxial growth on the upper surface of the first fin while epitaxially growing the second fin and the third fin.

17. The method of claim **15**, wherein an entirety of a bottom surface of the second fin and the third fin contacts the STI region.

18. The method of claim **15**, wherein a distance from the second fin to the third fin about 5 nm and about 20 nm.

19. The method of claim **18**, wherein a width of the second fin and the third fin is between about 2 nm and about 10 nm.

20. The method of claim **15**, further comprising forming a gate structure over the second fin and the third fin, the gate structure extending continuously between the second fin and the third fin.

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