(19) **United States**
(12) **Patent Application Publication**
XIAO et al.
(10) **Pub. No.: US 2023/0292485 A1**
(43) **Pub. Date: Sep. 14, 2023**

(54) **MEMORY AND MEMORY FORMING METHOD**

(71) Applicant: **CHANGXIN MEMORY TECHNOLOGIES, INC.**, Hefei City (CN)

(72) Inventors: **Deyuan XIAO**, Hefei City (CN); **Guangsu Shao**, Hefei City (CN)

(21) Appl. No.: **17/805,966**

(22) Filed: **Jun. 8, 2022**

Related U.S. Application Data

(63) Continuation of application No. PCT/CN2022/086255, filed on Apr. 12, 2022.

(30) **Foreign Application Priority Data**

Mar. 10, 2022 (CN) 202210237320.3

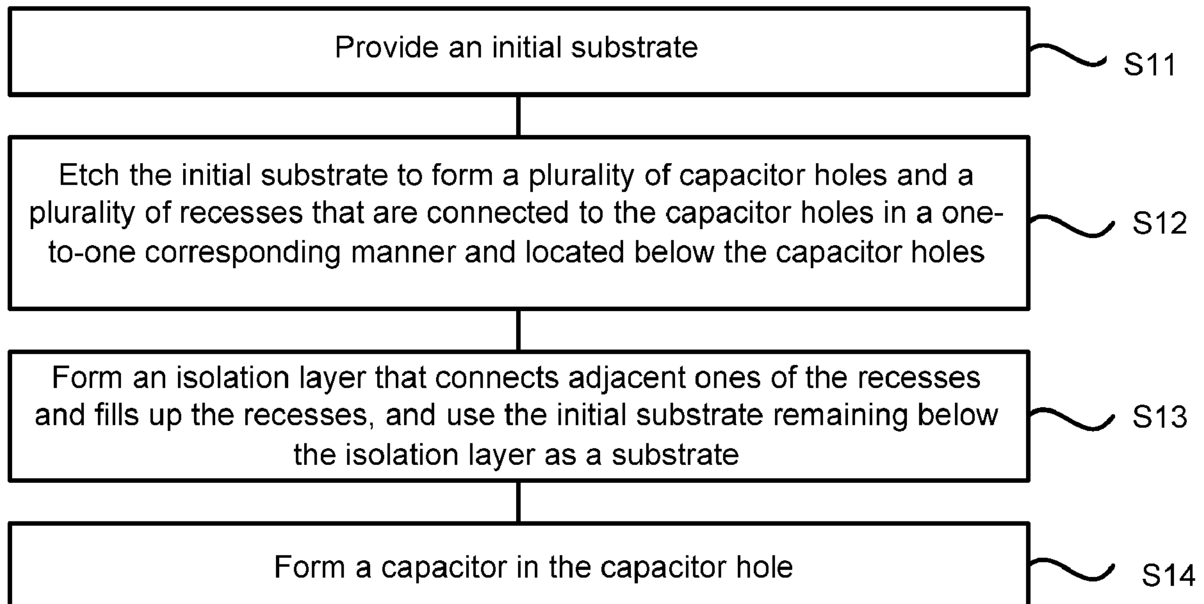
Publication Classification

(51) **Int. Cl.**
H01L 27/108 (2006.01)

(52) **U.S. Cl.**
CPC *H01L 27/1087* (2013.01); *H01L 27/10829* (2013.01)

(57) **ABSTRACT**

The present disclosure relates to a memory and a memory forming method. The memory forming method includes: providing an initial substrate; etching the initial substrate to form a plurality of capacitor holes and a plurality of recesses that are connected to the capacitor holes in a one-to-one corresponding manner and located below the capacitor holes; forming an isolation layer that connects adjacent ones of the recesses and fills up the recesses, and using the initial substrate remaining below the isolation layer as a substrate; and forming a capacitor in the capacitor hole.



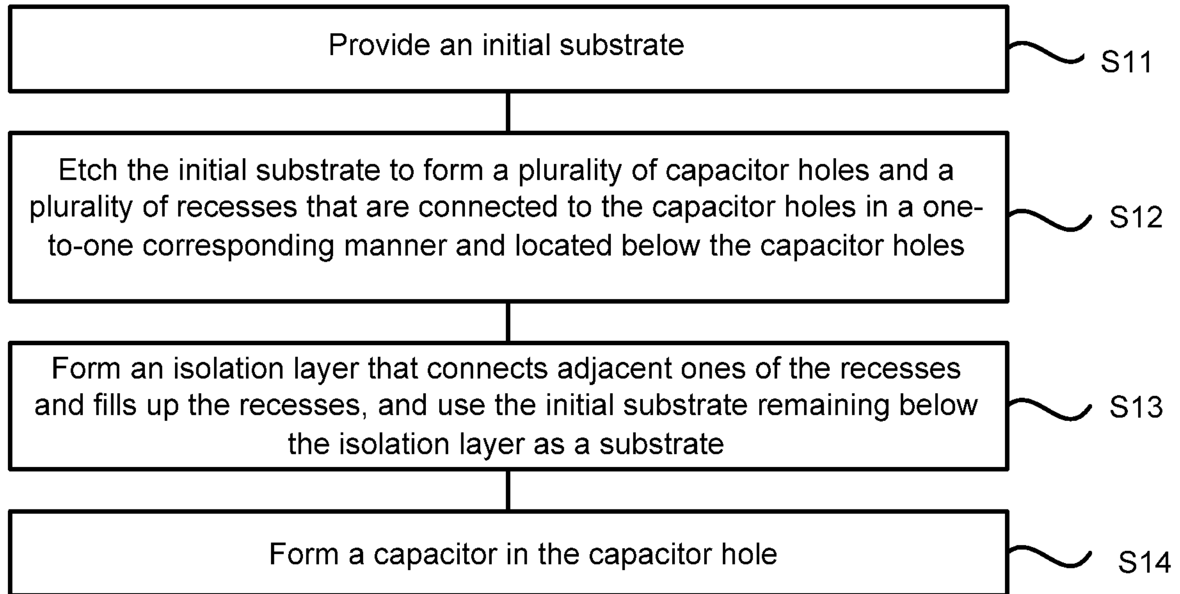


FIG. 1

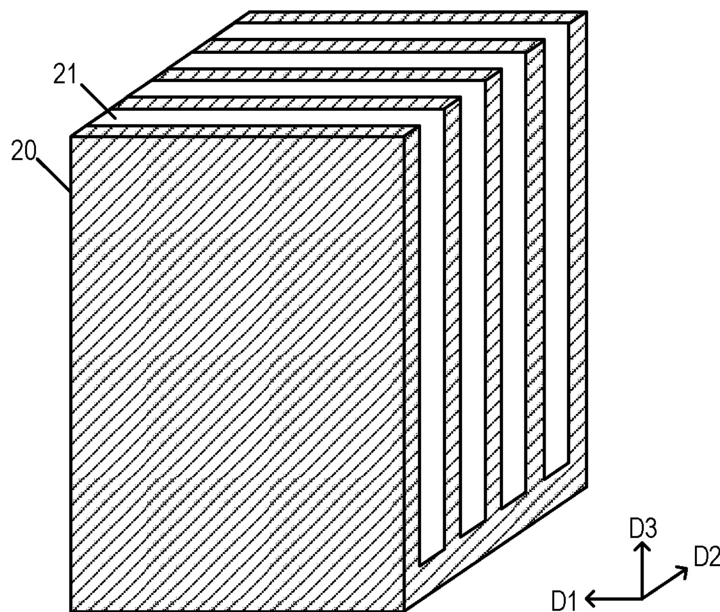


FIG. 2A

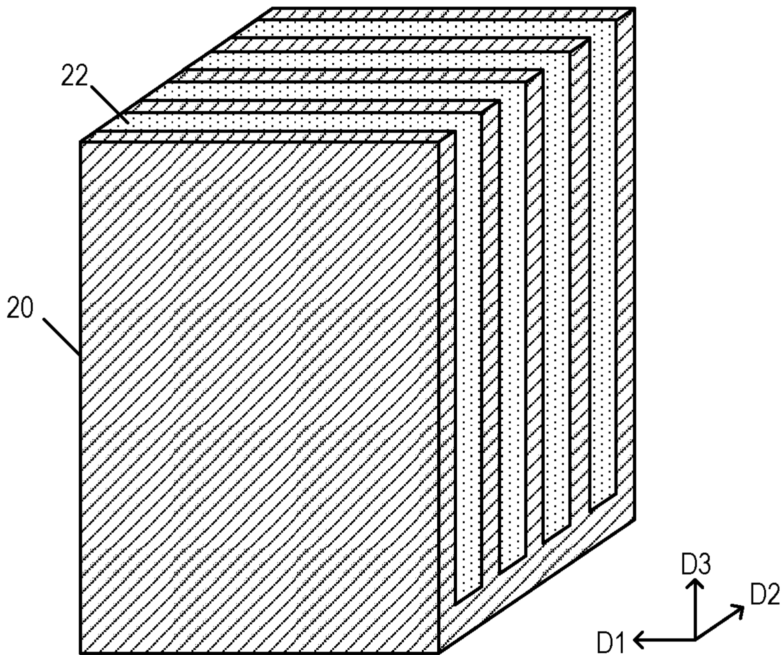


FIG. 2B

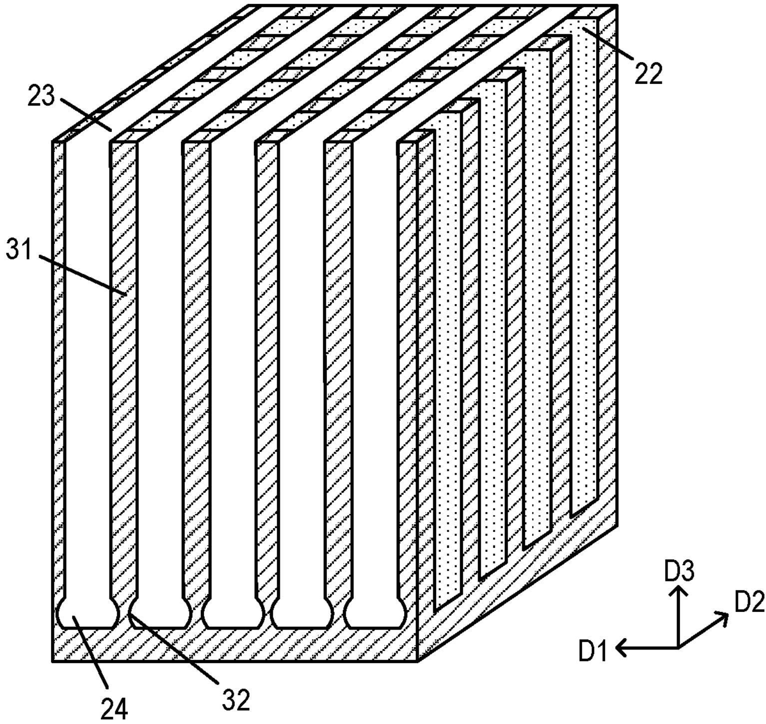


FIG. 2C

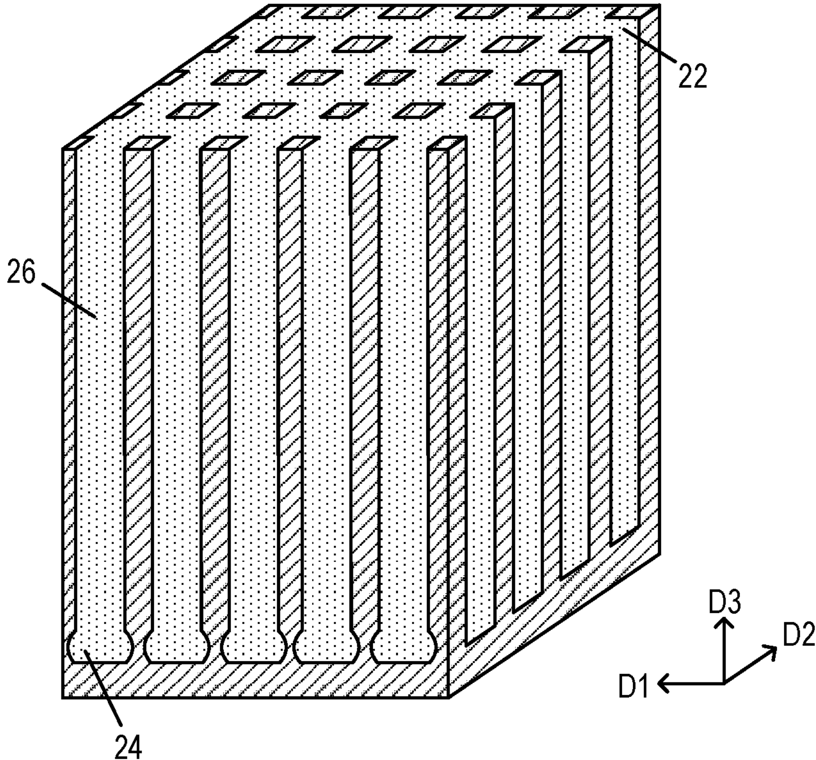


FIG. 2D

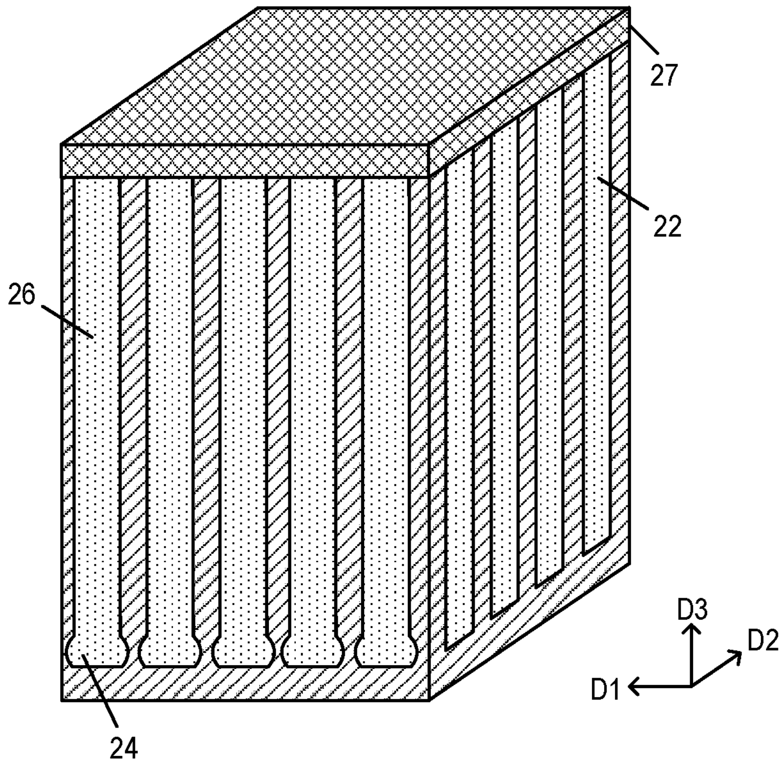


FIG. 2E

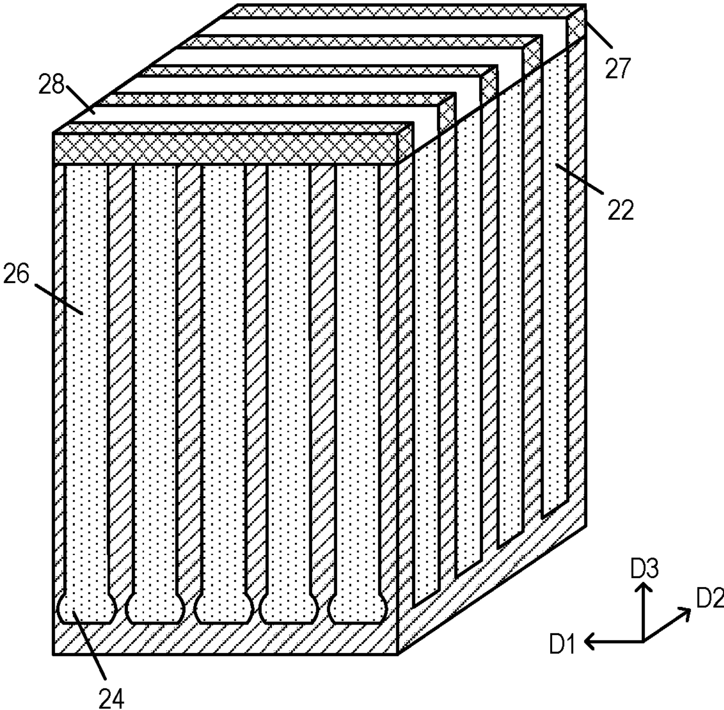


FIG. 2F

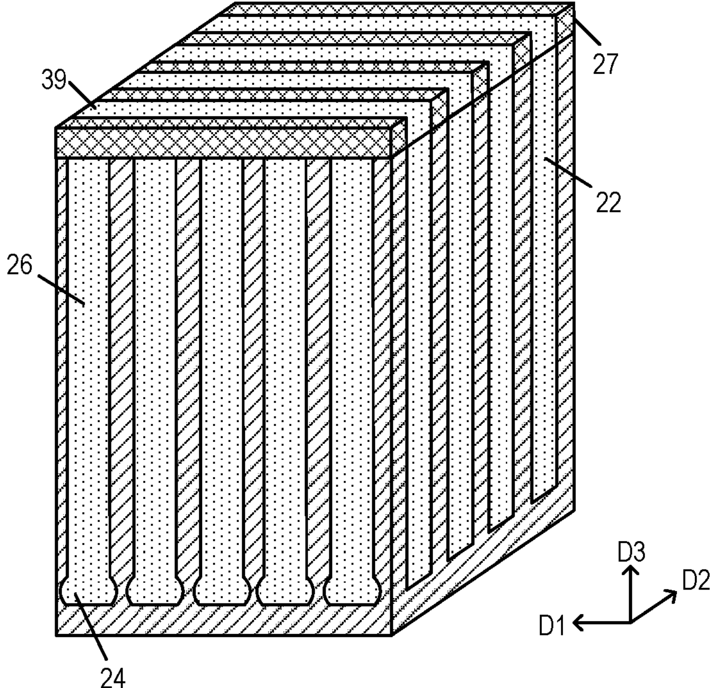


FIG. 2G

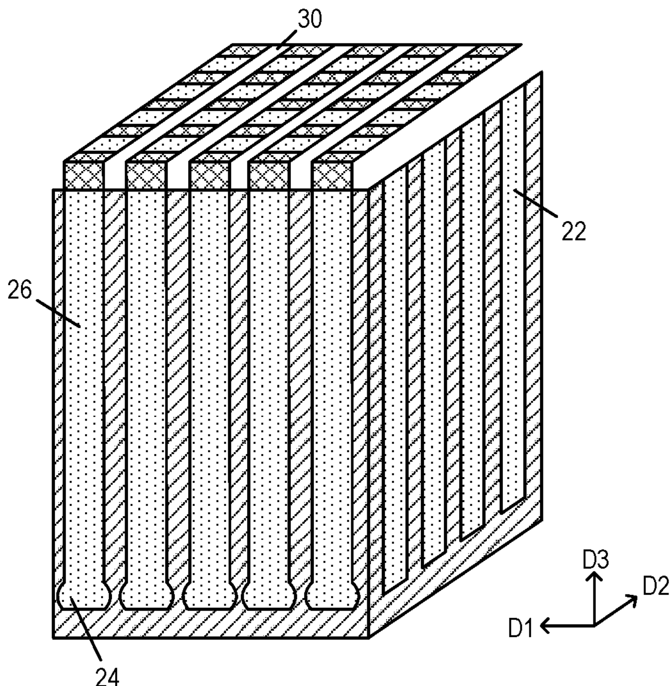


FIG. 2H

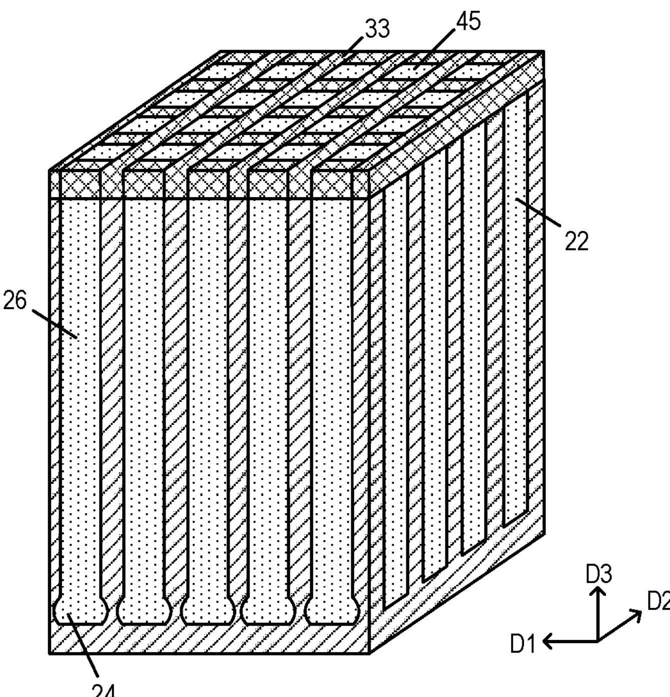


FIG. 2I

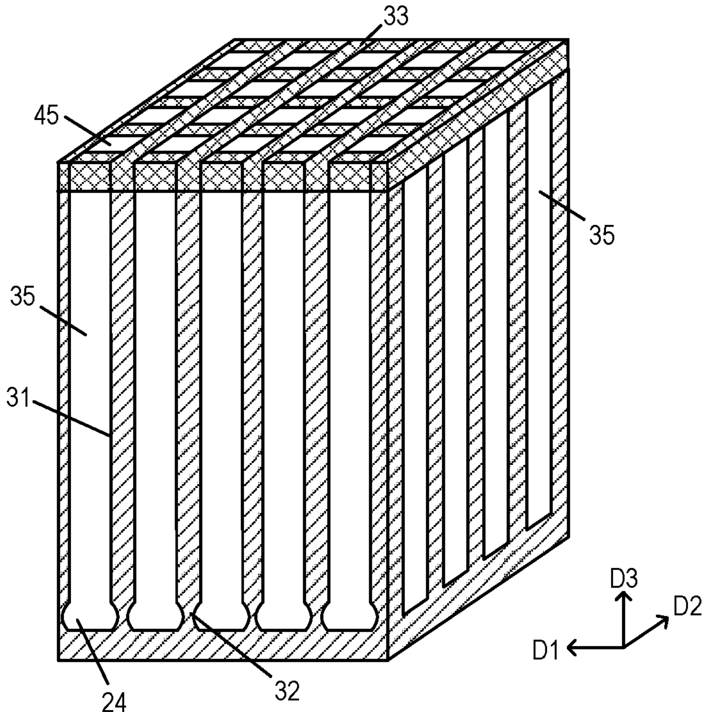


FIG. 2J

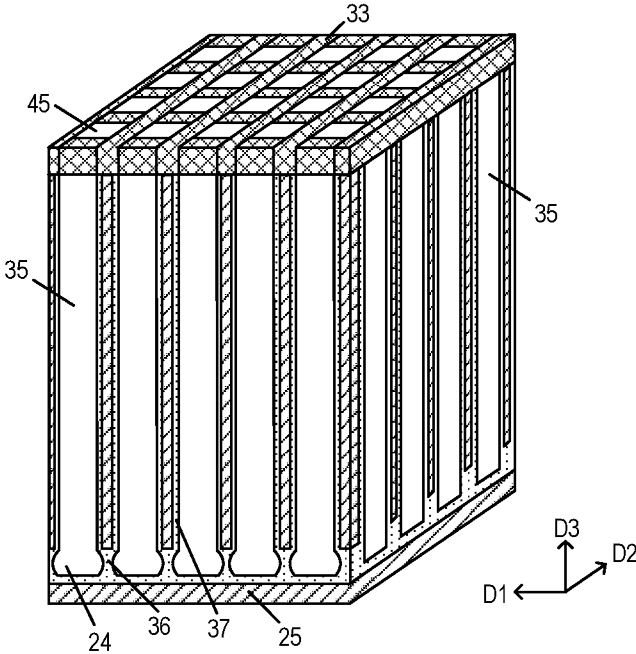


FIG. 2K

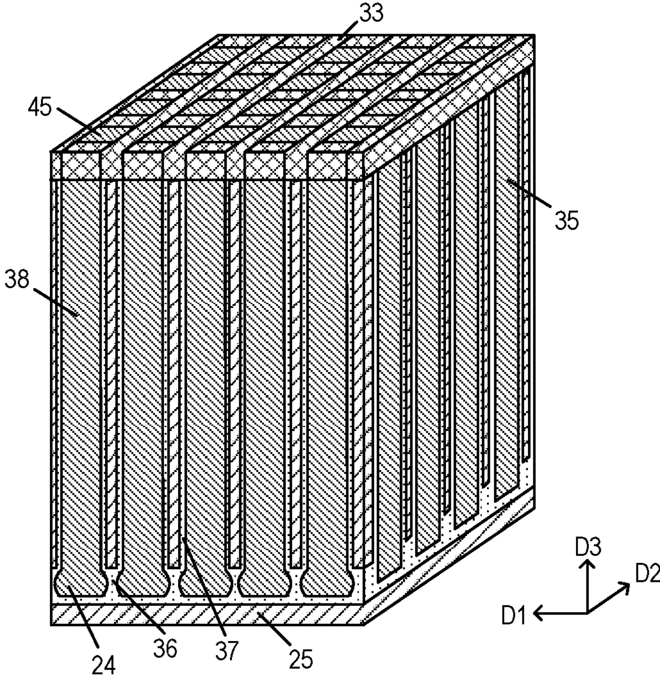


FIG. 2L

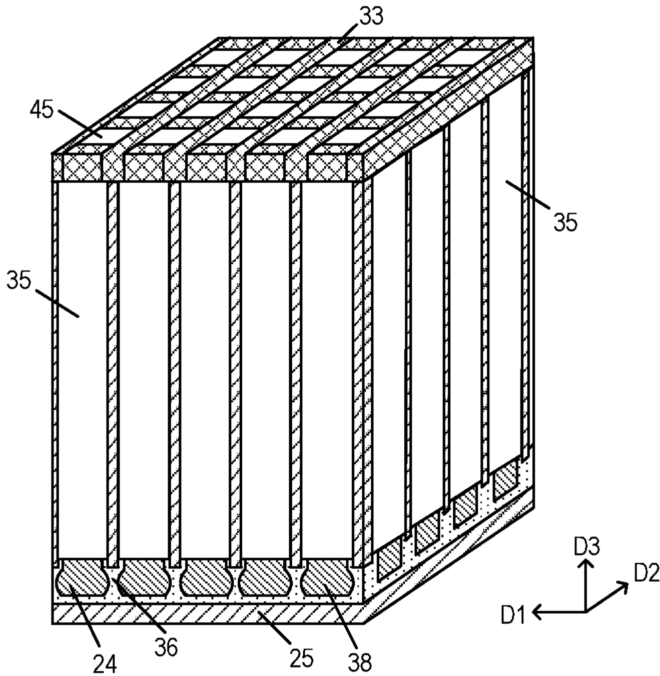


FIG. 2M

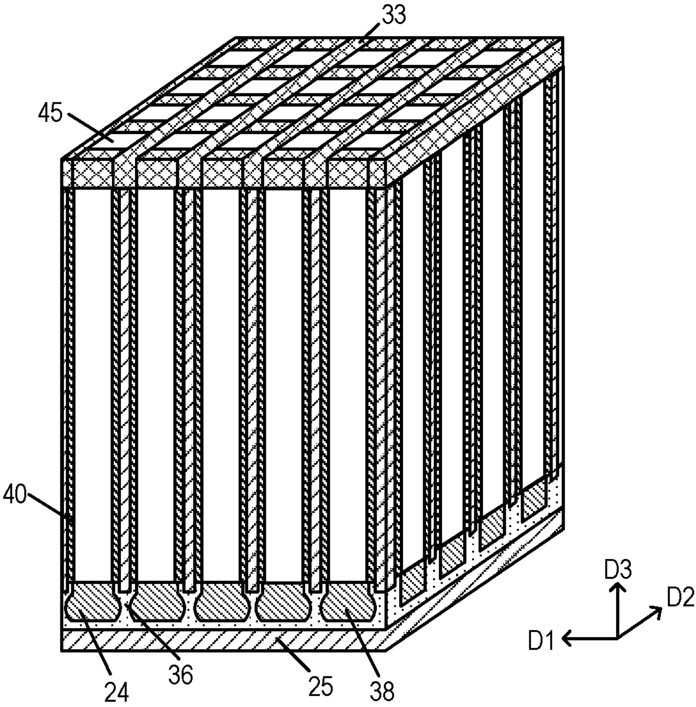


FIG. 2N

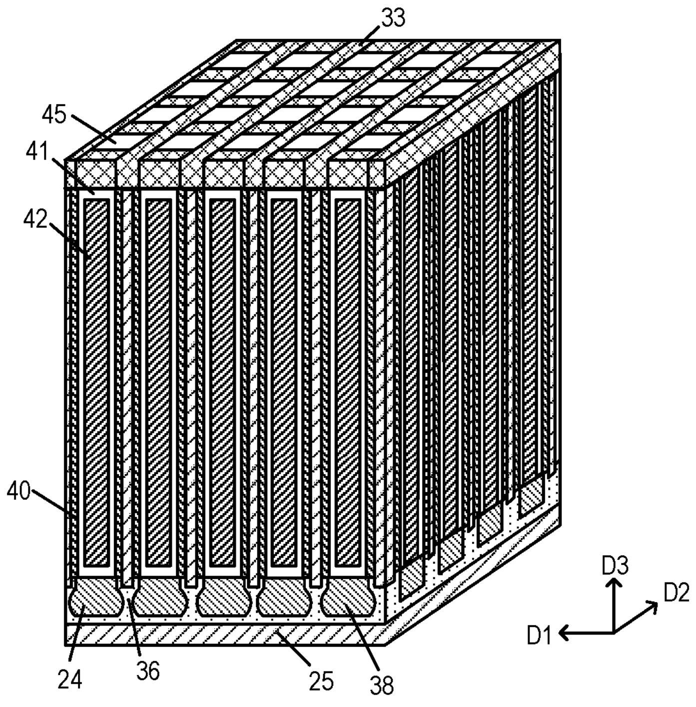


FIG. 2O

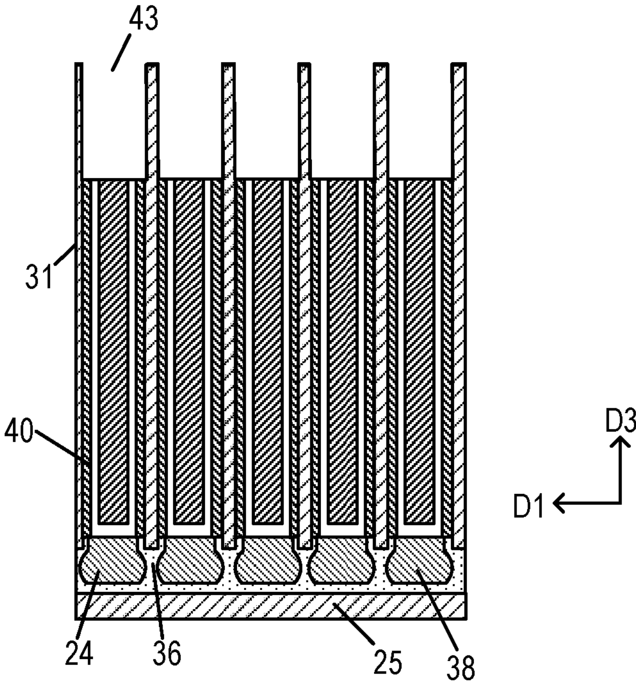


FIG. 2P

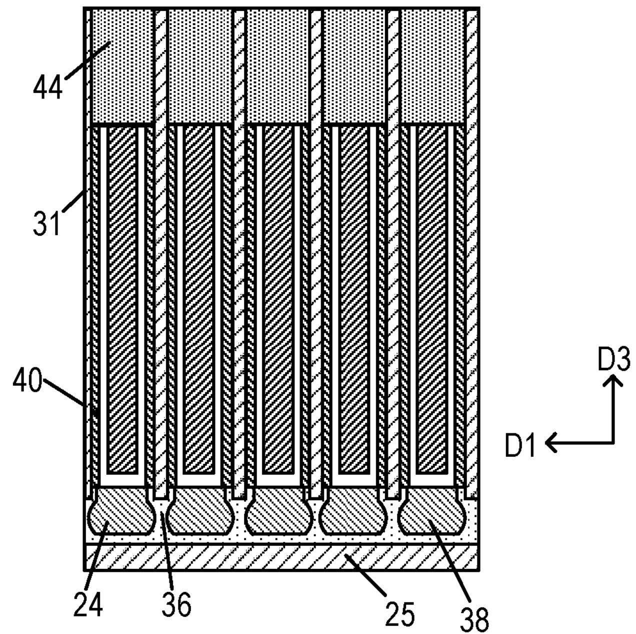


FIG. 2Q

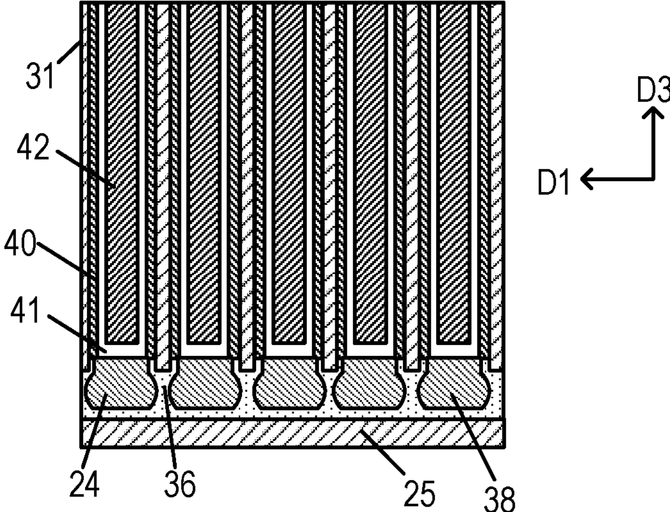


FIG. 3

MEMORY AND MEMORY FORMING METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation application of International Patent Application No. PCT/CN2022/086255, filed on Apr. 12, 2022, which claims the priority to Chinese Patent Application No. 202210237320.3, titled "MEMORY AND MEMORY FORMING METHOD" and filed on Mar. 10, 2022. The entire contents of International Patent Application No. PCT/CN2022/086255 and Chinese Patent Application No. 202210237320.3 are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to the technical field of semiconductor manufacturing, and in particular, to a memory device and a memory forming method.

BACKGROUND

[0003] As a semiconductor device commonly used in an electronic device such as a computer, a dynamic random access memory (DRAM) includes a plurality of memory cells, and each of the memory cells usually includes a transistor and a capacitor. The transistor has a gate being electrically connected to a word line, a source being electrically connected to a bit line, and a drain being electrically connected to the capacitor. A word line voltage on the word line can control on and off of the transistor, such that data information stored in the capacitor can be read through the bit line or data information can be written into the capacitor through the bit line.

[0004] However, in an existing memory such as the DRAM, especially in a memory with a transistor on capacitor (TOC) structure, electric leakage is easy to occur at the bottom of the capacitor, which reduces performance of the memory.

[0005] Therefore, how to reduce the electric leakage at the bottom of the capacitor to improve an electrical property of the memory is an urgent technical problem to be resolved.

SUMMARY

[0006] According to some embodiments, the present disclosure provides a memory forming method, including:

[0007] providing an initial substrate;

[0008] etching the initial substrate to form a plurality of capacitor holes and a plurality of recesses that are connected to the capacitor holes in a one-to-one corresponding manner and located below the capacitor holes;

[0009] forming an isolation layer that connects adjacent ones of the recesses and fills up the recesses, and using the initial substrate remaining below the isolation layer as a substrate; and

[0010] forming a capacitor in the capacitor hole.

[0011] According to some other embodiments, the present disclosure further provides a memory, including:

[0012] a substrate;

[0013] an isolation layer, located above the substrate; and

[0014] a capacitor array, located above the isolation layer and including a plurality of capacitors, where the capacitors each include a first electrode extending along a direction perpendicular to a top surface of the substrate, a dielectric layer covering a surface of the first electrode, and a second electrode covering a surface of the dielectric layer.

BRIEF DESCRIPTIONS OF THE DRAWINGS

[0015] FIG. **1** is a flowchart of a memory forming method according to a specific implementation of the present disclosure;

[0016] FIG. **2**A to FIG. **2**Q are schematic structural diagrams of main processes for forming a memory according to a specific implementation of the present disclosure; and

[0017] FIG. **3** is a schematic structural diagram of a memory according to a specific implementation of the present disclosure.

DETAILED DESCRIPTION

[0018] Specific implementations of a memory and a memory forming method provided in the present disclosure will be described below in detail with reference to the accompanying drawings.

[0019] The specific implementations provide a memory forming method. FIG. **1** is a flowchart of a memory forming method according to a specific implementation of the present disclosure. FIG. **2**A to FIG. **2**Q are schematic structural diagrams of main processes for forming a memory according to a specific implementation of the present disclosure. The memory in the specific implementations may be, but not limited to, a DRAM. As shown in FIG. **1** and FIG. **2**A to FIG. **2**Q, the memory forming method provided in this specific implementation includes the following steps:

[0020] Step S**11**: Provide an initial substrate **20**.

[0021] Specifically, the initial substrate **20** may be, but not limited to, a silicon substrate. This specific implementation is described by using an example in which the initial substrate **20** is the silicon substrate. In other examples, the initial substrate **20** may be a semiconductor substrate such as a gallium nitride substrate, a gallium arsenide substrate, a gallium carbide substrate, a silicon carbide substrate or a silicon-on-insulator (SOI) substrate.

[0022] Step S**12**: Etch the initial substrate **20** to form a plurality of capacitor holes **35** and a plurality of recesses **24** that are connected to the capacitor holes **35** in a one-to-one corresponding manner and located below the capacitor holes **35**, and use a remaining part, below the recess **24**, of the initial substrate as a substrate **25**.

[0023] In some embodiments, the forming a plurality of capacitor holes **35** and a plurality of recesses **24** that are connected to the capacitor holes **35** in a one-to-one corresponding manner and located below the capacitor holes **35** specifically includes:

[0024] etching the initial substrate **20** to form a plurality of first etching tanks **21**, where the first etching tanks **21** each extend along a first direction D**1**, the first etching tanks **21** are parallel to each other and spaced apart in a second direction D**2**, the first direction D**1** and the second direction D**2** are parallel to a top surface of the initial substrate **20**, and the first direction D**1** is orthogonal to the second direction D**2**, as shown in FIG. **2**A;

[0025] etching the initial substrate **20** to form a plurality of second etching tanks **23**, where the second etching tanks **23** each extend along the second direction D**2**, and the second etching tanks **23** are parallel to each other and spaced apart in the first direction D**1**;

[0026] etching the initial substrate **20** at the bottom of the second etching tank **23** to form the recess **24** whose inner diameter is greater than an inner diameter of the second etching tank **23**, as shown in FIG. **2**C; and

[0027] connecting the first etching tank **21** and the second etching tank **23** to form the capacitor hole **35**, as shown in FIG. **2**J.

[0028] Specifically, the initial substrate **20** can be etched along a direction perpendicular to the top surface of the initial substrate **20** (for example, a third direction D**3** in FIG. **2**A) by using a dry etching process, to form the first etching tanks **21**. The first etching tanks **21** each extend along the first direction D**1**, and the first etching tanks **21** are parallel to each other and spaced apart along the second direction D**2**. In a process of etching the initial substrate **20** to form the first etching tank **21**, etching parameters such as a dosage of etching gas and/or etching time can be controlled to make the first etching tank **21** not penetrate through the initial substrate **20** in the direction perpendicular to the top surface of the initial substrate **20**.

[0029] In some embodiments, before the forming a plurality of second etching tanks **23**, the memory forming method further includes the following step:

[0030] forming a first filling layer **22** that fills up the first etching tank **21**, as shown in FIG. **2**B.

[0031] In some embodiments, the forming the recess **24** whose inner diameter is greater than an inner diameter of the second etching tank **23** specifically includes:

[0032] etching the initial substrate **20** at the bottom of the second etching tank **23** by using a Bosch etching process, to form the recess **24**, as shown in FIG. **2**C.

[0033] Specifically, in order to avoid collapse or tip-over when etching the initial substrate **20** to form the second etching tank **23**, before the second etching tank **23** is formed, an insulating material such as silicon dioxide can also be deposited in the first etching tank **21** by using a chemical vapor deposition process, a physical vapor deposition process, or an atomic layer deposition process, to form the first filling layer **22** that fills up the first etching tank **21**, as shown in FIG. **2**B. Then, the initial substrate **20** can be etched along the direction perpendicular to the top surface of the initial substrate **20** (for example, the third direction D**3** in FIG. **2**A) by using the dry etching process, to form the second etching tanks **23**. The second etching tanks **23** each extend along the second direction D**2**, and the second etching tanks **23** are parallel to each other and spaced apart along the first direction D**1**. That is, a projection of the second etching tank **23** along the direction perpendicular to the top surface of the initial substrate **20** is orthogonal to a projection of the first etching tank **21** along the direction perpendicular to the top surface of the initial substrate **20**. After that, the initial substrate **20** at the bottom of the second etching tank **23** is continuously etched along the first etching tank **21** by using the Bosch etching process, to form the recess **24** that is connected to the bottom of the second etching tank **23** and whose inner diameter is greater than the inner diameter of the second etching tank **23**. The inner diameter of the recess **24** is greater than the inner diameter of the second etching tank **23**. Therefore, in the first direction D**1**, a width of the initial substrate **20** remaining between adjacent ones of the second etching tanks **23** (namely, a first isolation column **31**) is greater than a width of the initial substrate **20** remaining between adjacent ones of the recesses **24** (namely, a second isolation column **32**).

[0034] In this specific implementation, the recess **24** is formed by using the Bosch etching process after the second etching tank **23** is formed, so as to simplify a forming process of a memory. In other specific implementations, those skilled in the art can also select another etching process as needed to form the second etching tank **23** and the recess **24** connected to the second etching tank **23**.

[0035] In some embodiments, the connecting the first etching tank **21** and the second etching tank **23** to form the capacitor hole **35** specifically includes:

[0036] forming a second filling layer **26** that fills up the second etching tank **23** and the recess **24**, as shown in FIG. **2**D;

[0037] forming, above the initial substrate **20**, a patterned mask layer that includes a plurality of openings **45** exposing an overlapping region of the first etching tank **21** and the second etching tank **23**, as shown in FIG. **2**I; and

[0038] removing the first filling layer **22** and the second filling layer **26** along the opening **45** to form the capacitor hole **35**, as shown in FIG. **2**J.

[0039] Specifically, an appropriate material can be selected for the first filling layer **22** and the second filling layer **26**, so as to remove the first filling layer **22** and the second filling layer **26** through selective etching, and connect the first etching tank **21** and the second etching tank **23** inside the initial substrate **20**.

[0040] In some embodiments, the forming, above the initial substrate **20**, a patterned mask layer that includes a plurality of openings **45** exposing an overlapping region of the first etching tank **21** and the second etching tank **23** specifically includes:

[0041] forming a first mask sublayer **27** above the initial substrate **20**, as shown in FIG. **2**E;

[0042] etching the first mask sublayer **27** to form a plurality of first sub-openings **28** exposing the first filling layer **22**, where the first sub-openings **28** each extend along the first direction D**1**, and the first sub-openings **28** are arranged in parallel along the second direction D**2**, as shown in FIG. **2**F;

[0043] forming a third filling layer **39** that fills up the first sub-opening **28**, as shown in FIG. **2**G;

[0044] etching the first mask sublayer **27** and the third filling layer **39** to form a plurality of second sub-openings **30** exposing the initial substrate **20**, where the second sub-openings **30** each extend along a direction parallel to the second direction D**2**, and the second sub-openings **30** are arranged in parallel along the first direction D**1**, as shown in FIG. **2**H;

[0045] filling a second mask sublayer **33** in the second sub-opening **30** to form the mask layer including the second mask sublayer **33** and a remaining part of the first mask sublayer **27**, where the mask layer includes a plurality of openings **45** exposing the third filling layer **39**, as shown in FIGS. **2**I; and

[0046] removing the third filling layer **39** along the opening **45** to expose the overlapping region of the first etching tank **21** and the second etching tank **23**.

[0047] Specifically, after the second filling layer **26** that fills up the second etching tank **23** and the recess **24** is formed, a hard mask material such as silicon nitride or an organic mask material such as carbon is deposited on the top surface of the initial substrate **20** to form the first mask sublayer **27**, as shown in FIG. **2**E. The first mask sublayer **27** is used as a mask for removing the first filling layer **22** and

the second filling layer **26** subsequently, and is further configured to support the first isolation column **31** between the adjacent ones of the second etching tanks **23** to avoid tip-over or collapse in a subsequent process for removing the first filling layer **22** and the second filling layer **26**. Then, the first mask sublayer **27** can be etched by etching a same mask that forms the first etching tank **21**, to form the first sub-openings **28** exposing the first filling layer **22**, where the first sub-openings **28** each extend along the first direction D**1**, and the first sub-openings **28** are arranged in parallel along the second direction D**2**, as shown in FIG. **2**F. After that, the first sub-opening **28** is filled to form the third filling layer **39**, as shown in FIG. **2**G. Then, the first mask sublayer **27** and the third filling layer **39** are etched to form the second sub-openings **30** exposing the initial substrate **20**, where the second sub-openings **30** each extend along the direction parallel to the second direction D**2**, and the second sub-openings **30** are parallel to each other and spaced apart along the first direction D**1**, as shown in FIG. **2**H. The second mask sublayer **33** made of a nitride material (for example, a silicon nitride material) is filled in the second sub-opening **30** to form the mask layer including the second mask sublayer **33** and the remaining part of the first mask sublayer **27**. In the direction parallel to the top surface of the initial substrate **20**, the remaining part of the first mask sublayer **27** intersects the second mask sublayer **33** to form the openings **45** exposing the third filling layer **39**, as shown in FIG. **2**I. The third filling layer **39**, the first filling layer **22**, and the second filling layer **26** are removed along the opening **45** by using the etching process, to connect the first etching tank **21** and the second etching tank **23** inside the initial substrate **20** to form the capacitor hole **35**, as shown in FIG. **2**J.

[0048] In an embodiment, the first filling layer **22**, the second filling layer **26**, and the third filling layer **39** are made of a same material. For example, the first filling layer **22**, the second filling layer **26**, and the third filling layer **39** are made of the silicon dioxide, so as to remove the first filling layer **22**, the second filling layer **26**, and the third filling layer **39** at the same time by using a one-step etching process. In this way, a manufacturing process of the memory is further simplified.

[0049] Step S**13**: Form an isolation layer that connects the adjacent ones of the recesses **24** and fills up the recesses **24**, and use the initial substrate **20** remaining below the isolation layer as the substrate **25**, as shown in FIG. **2**M.

[0050] In some embodiments, the initial substrate **20** remaining between adjacent ones of the capacitor holes **35** is used as the first isolation column **31**, and the initial substrate **20** remaining between the adjacent ones of the recesses **24** is used as the second isolation column **32**, as shown in FIG. **2**J; and

[0051] in the first direction D**1**, a width of the second isolation column **32** is ½ to ⅓ of a width of the first isolation column **31**, and in the second direction D**2**, a width of the second isolation column **32** is equal to a width of the first isolation column **31**.

[0052] Specifically, the inner diameter of the recess **24** is set to be greater than an inner diameter of the capacitor hole **35** above the recess **24**, such that the width of the second isolation column **32** between the adjacent ones of the recesses **24** in the first direction D**1** is less than the width of the first isolation column **31** between the adjacent ones of the capacitor holes **35** in the first direction. In this way, the second isolation column **32** can be fully modified later, so as to fully isolate the substrate **25** and a capacitor later. In addition, the width of the second isolation column **32** should not be too small. If the width of the second isolation column **32** is too small, the first isolation column **31** above the second isolation column **32** cannot be supported stably.

[0053] In some embodiments, the forming an isolation layer that connects adjacent ones of the recesses **24** and fills up the recesses **24** specifically includes:

[0054] oxidizing a part of the first isolation column **31** and the whole second isolation column **32** along the opening **45** to form an isolation sidewall **37** on a sidewall of the capacitor hole **35** and form a first isolation sublayer **36** between the adjacent ones of the recesses **24**, as shown in FIG. **2**K; and

[0055] depositing a second isolation sublayer **38** in the recess **24** along the opening **45** to form the isolation layer including the first isolation sublayer **36** and the second isolation sublayer **38**, as shown in FIG. **2**M.

[0056] In some embodiments, the initial substrate **20** is made of silicon, and the first isolation sublayer **36** and the second isolation sublayer **38** are made of the silicon dioxide.

[0057] The following provides description by using an example in which the initial substrate **20** is made of the silicon, and the first isolation sublayer **36** and the second isolation sublayer **38** are made of the silicon dioxide. For example, in-situ oxidation (for example, in-situ steam generation) is performed on the first isolation column **31**, the second isolation column **32**, and a part of the initial substrate **20** at the bottom of the recess **24**. The width of the first isolation column **31** in the first direction D**1** is greater than that of the second isolation column **32** in the first direction D**1**. Therefore, oxidation parameters (for example, oxidation time and an oxidant dosage) can be controlled to completely oxidize the second isolation column **32** and oxidize only a surface of the first isolation column **31**, so as to form the isolation sidewall **37** covering the sidewall of the capacitor hole **35**, and the first isolation sublayer **36** located between the adjacent ones of the recesses **24** and covering a bottom surface of the recess **24**, as shown in FIG. **2**K. Then, a silicon dioxide material is deposited in the capacitor hole **35** and the recess **24** along the opening **45** to form the second isolation sublayer **38** that fills up the opening **45**, the capacitor hole **35**, and the recess **24**, as shown in FIG. **2**L. After that, the second isolation sublayer **38** is partially etched back, the isolation sidewall **37** is partially removed to expose the first isolation column **31**, and the recess **24** is filled up with a remaining part of the second isolation sublayer **38**, as shown in FIG. **2**M.

[0058] In some embodiments, the depositing a second isolation sublayer **38** in the recess **24** along the opening **45** specifically includes:

[0059] depositing the second isolation sublayer **38** in the recess **24** and at the bottom of the capacitor hole **35** along the opening **45**, such that a top surface of the second isolation sublayer **38** is located above a bottom surface of the first isolation column **31**.

[0060] Specifically, when the second isolation sublayer **38** is partially etched back, a parameter condition of the back etching is controlled such that a top surface of the remaining part of the second isolation sublayer **38** is located above the bottom surface of the first isolation column **31**, so as to fully isolate adjacent capacitors and avoid electric leakage between the adjacent capacitors.

[0061] This specific implementation is described by using an example in which the second isolation column **32** is oxidized to form the first isolation sublayer **36**. In other specific implementations, another modification manner can alternatively be used to process the second isolation column **32** to form the first isolation sublayer **36**. The another modification manner may be, but not limited to, doping.

[0062] Step S**14**: Form the capacitor in the capacitor hole **35**, as shown in FIG. **2**O.

[0063] In some embodiments, the forming the capacitor in the capacitor hole **35** specifically includes:

[0064] removing the isolation sidewall **37**;

[0065] forming a first electrode **40** covering the sidewall of the capacitor hole **35**, as shown in FIG. **2**N;

[0066] forming a dielectric layer **41** covering a surface of the first electrode **40**, a top surface of the isolation layer, and a bottom surface of the mask layer; and

[0067] forming a second electrode **42** covering the dielectric layer **41** to form the capacitor including the first electrode **40**, the dielectric layer **41**, and the second electrode **42**, as shown in FIG. **2**O.

[0068] Specifically, the atomic layer deposition process can be used to selectively deposit a first conductive material on the sidewall of the capacitor hole **35** rather than on a bottom surface of the capacitor hole **35**. In this way, there is no need to remove the first conductive material at the bottom of the capacitor hole, which helps to further simplify the forming process of the memory. Then, the dielectric layer **41** is deposited on the surface of the first electrode **40**, the top surface of the isolation layer, and the bottom surface of the mask layer by using the atomic layer deposition process. After that, the second electrode **42** covering the dielectric layer **41** is formed. The first electrode **40** and the second electrode **42** may be made of Ru, RuO_2, or TiN to enhance conductivity of the capacitor. The dielectric layer **41** may be made of one of STO ($SrTiO_3$), Al_2O_3, ZrO, and HfO_2, or a combination of more than two of them.

[0069] In some embodiments, after the forming a second electrode **42** covering the dielectric layer **41**, the memory forming method further includes the following steps:

[0070] removing the mask layer, and partially etching back the first electrode **40**, the dielectric layer **41**, and the second electrode **42** to expose an upper part of the first isolation column **31**, as shown in FIG. **2**P, where FIG. **2**P is a schematic cross-sectional view of a plane on which the first direction D**1** and the second direction D**3** in FIG. **2**O are located; and

[0071] forming a coating layer **44** wrapping the exposed part of the first isolation column **31**, as shown in FIG. **2**Q.

[0072] In some embodiments, after the forming a coating layer **44** wrapping the exposed part of the first isolation column **31**, the memory forming method further includes the following step:

[0073] doping the first isolation column **31** in the coating layer **44** to form an active region of a transistor.

[0074] Specifically, after the capacitor is formed, the mask layer is removed, the capacitor is partially etched back to expose the upper part of the first isolation column **31** by a preset height, and a spacing slot **43** is formed between adjacent first isolation columns **31**, as shown in FIG. **2**P. Then, the insulating material such as the silicon dioxide is deposited in the spacing slot **43** to form the coating layer **44** that fills up the spacing slot **43**, as shown in FIG. **2**Q. After that, the first isolation column **31** wrapped by the coating layer **44** is doped to form the active region to form a TOC structure. The active region includes a trench region, and a source region and a drain region that are distributed on two opposite sides of the trench region along a direction perpendicular to a top surface of the substrate **25** (for example, the third direction D**3** in FIG. **2**Q). The drain region is electrically connected to the capacitor, and the source region is used to connect a bit line, such that the bit line can be disposed above the capacitor. This reduces resistance of the bit line, and can make the manufacturing process of the memory easier, reduce area occupied by a single memory, and improve integration of the memory.

[0075] The specific implementations further provide a memory. FIG. **3** is a schematic structural diagram of a memory according to a specific implementation of the present disclosure. The memory provided in this specific implementation may be formed by using the memory forming method shown in FIG. **1** and FIG. **2**A to FIG. **2**Q. As shown in FIG. **3**, the memory includes:

[0076] a substrate **25**;

[0077] an isolation layer located above the substrate **25**; and

[0078] a capacitor array located above the isolation layer and including a plurality of capacitors, where the capacitors each include a first electrode **40** extending along a direction perpendicular to a top surface of the substrate **25**, a dielectric layer **41** covering a surface of the first electrode **40**, and a second electrode **42** covering a surface of the dielectric layer **41**.

[0079] In some embodiments, the memory further includes:

[0080] a first isolation column **31** located between two adjacent ones of the capacitors; where

[0081] the isolation layer includes a first isolation sublayer **36** between the first isolation column **31** and the substrate **25**, and a second isolation sublayer **38** below the capacitor.

[0082] In some embodiments, the first isolation sublayer **36** and the second isolation sublayer **38** are made of a same material.

[0083] In some embodiments, the substrate **25** and the first isolation column **31** are made of silicon, and the first isolation sublayer **36** and the second isolation sublayer **38** are made of silicon dioxide.

[0084] In some embodiments, the first electrode **40** covers a sidewall of the first isolation column **31**, and the dielectric layer **41** covers the surface of the first electrode **40** and a surface of the second isolation sublayer **38**.

[0085] In some embodiments, a bottom surface of the first isolation column **31** is located below a bottom surface of the first electrode **40**.

[0086] In some embodiments, the memory further includes:

[0087] a trench region located above the first isolation column **31**; and

[0088] a gate disposed around the trench region.

[0089] According to the memory and the memory forming method provided in some embodiments of the specific implementations, before the capacitor is formed, the recess is formed below the capacitor hole for forming the capacitor, and after the isolation layer that connects the adjacent ones of the recesses and fills up the recesses is formed, the capacitor is formed in the capacitor hole above the isolation layer, to electrically isolate the bottom of the capacitor from the substrate through the isolation layer. This reduces and

even avoids electric leakage at the bottom of the capacitor, so as to improve an electrical property of the memory. In addition, compared with a method for forming the isolation layer directly on the substrate by using a deposition or oxidation process, the memory forming method provided in the present disclosure integrates a forming process of the capacitor hole and a forming process of the isolation layer, such that the forming process of the isolation layer can be carried out while the capacitor hole is formed. The isolation layer is directly formed below the capacitor to ensure that the isolation layer can be fully aligned with the bottom of the capacitor. This simplifies a manufacturing process of the memory and reduces process difficulty of the memory, and can further improve an effect of electrical isolation between the capacitor and the substrate.

[0090] The above described are merely preferred implementations of the present disclosure. It should be noted that several improvements and modifications may further be made by a person of ordinary skill in the art without departing from the principle of the present disclosure, and such improvements and modifications should also be deemed as falling within the protection scope of the present disclosure.

1. A memory forming method, comprising:
- providing an initial substrate;
- etching the initial substrate to form a plurality of capacitor holes and a plurality of recesses that are connected to the capacitor holes in a one-to-one corresponding manner and located below the capacitor holes;
- forming an isolation layer that connects adjacent ones of the recesses and fills up the recesses, and using the initial substrate remaining below the isolation layer as a substrate; and
- forming a capacitor in the capacitor hole.

2. The memory forming method according to claim **1**, wherein forming a plurality of capacitor holes and a plurality of recesses that are connected to the capacitor holes in a one-to-one corresponding manner and located below the capacitor holes specifically comprises:
- etching the initial substrate to form a plurality of first etching tanks, wherein the first etching tanks each extend along a first direction, the first etching tanks are parallel to each other and spaced apart in a second direction, the first direction and the second direction are parallel to a top surface of the initial substrate, and the first direction is orthogonal to the second direction;
- etching the initial substrate to form a plurality of second etching tanks, wherein the second etching tanks each extend along the second direction, and the second etching tanks are parallel to each other and spaced apart in the first direction;
- etching the initial substrate at a bottom of the second etching tank to form, in the first direction, the recess whose width is greater than a width of the second etching tank; and
- connecting the first etching tank and the second etching tank to form the capacitor hole.

3. The memory forming method according to claim **2**, wherein before forming a plurality of second etching tanks, the memory forming method further comprises:
- forming a first filling layer that fills up the first etching tank.

4. The memory forming method according to claim **3**, wherein forming the recess whose width is greater than a width of the second etching tank specifically comprises:
- etching the initial substrate at the bottom of the second etching tank by a Bosch etching process, to form the recess.

5. The memory forming method according to claim **3**, wherein the connecting the first etching tank and the second etching tank to form the capacitor hole specifically comprises:
- forming a second filling layer that fills up the second etching tank and the recess;
- forming, above the initial substrate, a patterned mask layer that comprises a plurality of openings exposing an overlapping region of the first etching tank and the second etching tank; and
- removing the first filling layer and the second filling layer along the opening to form the capacitor hole.

6. The memory forming method according to claim **5**, wherein the forming, above the initial substrate, a patterned mask layer that comprises a plurality of openings exposing an overlapping region of the first etching tank and the second etching tank specifically comprises:
- forming a first mask sublayer above the initial substrate;
- etching the first mask sublayer to form a plurality of first sub-openings exposing the first filling layer, wherein the first sub-openings each extend along the first direction, and the first sub-openings are spaced apart along the second direction;
- forming a third filling layer that fills up the first sub-opening;
- etching the first mask sublayer and the third filling layer to form a plurality of second sub-openings exposing the initial substrate, wherein the second sub-openings each extend along a direction parallel to the second direction, and the second sub-openings are spaced apart along the first direction;
- filling a second mask sublayer in the second sub-opening to form the mask layer comprising the second mask sublayer and a remaining part of the first mask sublayer, wherein the mask layer comprises a plurality of openings exposing the third filling layer; and
- removing the third filling layer along the opening to expose the overlapping region of the first etching tank and the second etching tank.

7. The memory forming method according to claim **6**, wherein the initial substrate remaining between adjacent ones of the capacitor holes is used as a first isolation column, and the initial substrate remaining between the adjacent ones of the recesses is used as a second isolation column; and
- in the first direction, a width of the second isolation column is ½ to ⅓ of a width of the first isolation column, and in the second direction, a width of the second isolation column is equal to a width of the first isolation column.

8. The memory forming method according to claim **7**, wherein the forming an isolation layer that connects adjacent ones of the recesses and fills up the recesses specifically comprises:
- oxidizing a part of the first isolation column and the whole second isolation column along the opening to form an isolation sidewall on a sidewall of the capacitor hole and form a first isolation sublayer between the adjacent ones of the recesses; and

depositing a second isolation sublayer in the recess along the opening to form the isolation layer comprising the first isolation sublayer and the second isolation sublayer.

9. The memory forming method according to claim **8**, wherein the depositing a second isolation sublayer in the recess along the opening specifically comprises:

depositing the second isolation sublayer in the recess and at a bottom of the capacitor hole along the opening, such that a top surface of the second isolation sublayer is located above a bottom surface of the first isolation column.

10. The memory forming method according to claim **8**, wherein the initial substrate is made of silicon, and the first isolation sublayer and the second isolation sublayer are made of silicon dioxide.

11. The memory forming method according to claim **8**, wherein the forming a capacitor in the capacitor hole specifically comprises:

removing the isolation sidewall;

forming a first electrode covering the sidewall of the capacitor hole;

forming a dielectric layer covering a surface of the first electrode, a top surface of the isolation layer, and a bottom surface of the mask layer; and

forming a second electrode covering the dielectric layer to form the capacitor comprising the first electrode, the dielectric layer, and the second electrode.

12. The memory forming method according to claim **11**, wherein after the forming a second electrode covering the dielectric layer, the memory forming method further comprises:

removing the mask layer, and partially etching back the first electrode, the dielectric layer, and the second electrode to expose an upper part of the first isolation column; and

forming a coating layer wrapping the exposed part of the first isolation column.

13. The memory forming method according to claim **12**, wherein after the forming a coating layer wrapping the exposed part of the first isolation column, the memory forming method further comprises:

doping the first isolation column in the coating layer to form an active region of a transistor.

14. A memory, comprising:

a substrate;

an isolation layer, located above the substrate; and

a capacitor array, located above the isolation layer and comprising a plurality of capacitors, wherein the capacitors each comprise a first electrode extending along a direction perpendicular to a top surface of the substrate, a dielectric layer covering a surface of the first electrode, and a second electrode covering a surface of the dielectric layer.

15. The memory according to claim **14**, the memory further comprises:

a first isolation column, located between two adjacent ones of the capacitors; wherein

the isolation layer comprises a first isolation sublayer between the first isolation column and the substrate, and a second isolation sublayer below the capacitor.

16. The memory according to claim **15**, wherein the first isolation sublayer and the second isolation sublayer are made of a same material.

17. The memory according to claim **16**, wherein the substrate and the first isolation column are made of silicon, and the first isolation sublayer and the second isolation sublayer are made of silicon dioxide.

18. The memory according to claim **17**, wherein the first electrode covers a sidewall of the first isolation column, and the dielectric layer covers the surface of the first electrode and a surface of the second isolation sublayer.

19. The memory according to claim **16**, wherein a bottom surface of the first isolation column is located below a bottom surface of the first electrode.

20. The memory according to claim **15**, the memory further comprises:

a trench region, located above the first isolation column; and

a gate, disposed around the trench region.

* * * * *