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(54) **MATCHED FEEDBACK INTEGRATE-AND-FIRE NEURON CIRCUIT**

(57) The present invention relates to an integrate-and-fire neuron circuit for signed processing which is characterized by a feedback subcircuit connected to the positive and negative outputs of the circuit. This feedback subcircuit is configured to generate and output positive charge packets to a common line of the neuron circuit on each negative spike output signal and stored weights and to generate and output negative charge packets to the common line based on each positive spike output signal and stored weights. Due to this feedback circuit that is build in the same way as the input weighting circuit, structural matching and therefore higher accuracy and less variation of the behavior over PVT variations is achieved.

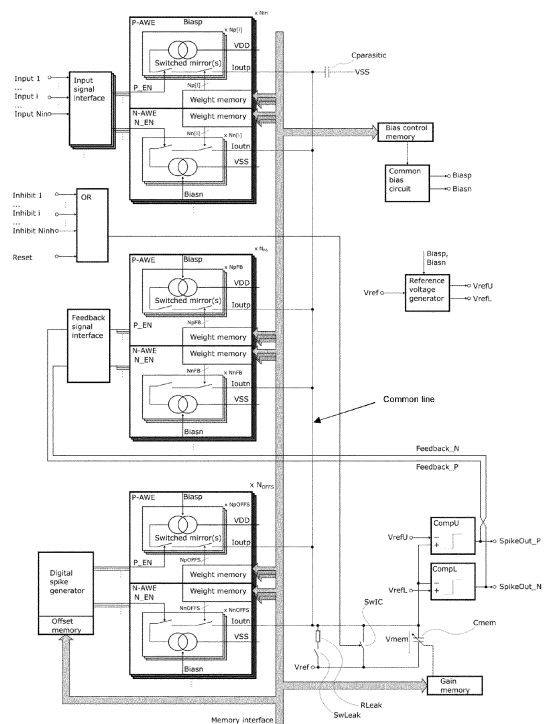


Fig. 1

Description**Technical field**

5 [0001] The present invention relates to an integrate-and-fire neuron circuit comprising at least one input to receive input signals and at least a positive and a negative output to deliver positive and negative spike output signals, a weighting subcircuit configured to generate and output positive and/or negative charge packets to a common line based on the input signals and an arrangement of a capacitor or integrator and two comparators generating the positive spike output signals at the positive output and the negative spike output signals at the negative output.

10 [0002] Such circuits for roughly imitating the function of a neuron are used in artificial neuronal networks (ANN), especially artificial spiking neuronal networks (SNN). Neuronal dynamics can be seen as a summation process combined with a mechanism that triggers action potentials above some critical voltage. One known representation of a neuron circuit is the integrate-and-fire neuron circuit. Information is contained in the presence or absence of a spike which is generated with such a neuron circuit.

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Prior art

[0003] R. Serrano-Gotarredona et al., "A Neuromorphic Cortical-Layer Microchip for Spike-Based Event Processing Vision Systems," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 53, no. 12, pp. 2548-2566, Dec. 2006, propose integrate-and-fire neuron circuits for signed and unsigned processing. These circuits comprise subcircuits for generating positive and/or negative charge packets and output these charge packets to a common line based on input signals. The charges of the positive and negative charge packets are stored in a capacitor converting the sum of charges into a voltage. The voltage is compared with a reference voltage by a comparator which generates a positive and/or negative spike output signal if the voltage is larger or lower than the corresponding reference voltage. The circuit performs a reset that clears all charge on the capacitor when an output spike is created. While this reset is performed, continuing inputs can be lost (blind period). Since the reset removes all information on previous operation there is also no quantization error stored. Averaging over multiple operations of the same kind would not reveal more resolution and accuracy in averaged results. Here the amount, how much the voltage exceeds the reference voltage can be considered as the quantization error. The overall gain of such a neuron circuit depends on the absolute values of the capacitor, the input current and the reference voltage. Therefore, the result will vary heavily with temperature, process and supply variations, also known as PVT-variations (PVT: process-voltage-temperature).

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[0004] EP 2877958 B1 describes a spike domain asynchronous neuron circuit with feedback. The feedback is realized as proportional feedback, continuously in value and time, and influences the adjustable gain subcircuits of this neuron circuit.

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[0005] It is an object of the present invention to provide an integrate-and-fire neuron circuit which provides higher accuracy and less variation in case of temperature, process and supply variations (PVT-variations).

Summary of the invention

40 [0006] The object is achieved with the integrate-and-fire neuron circuit according to claim 1. Advantageous embodiments of the circuit are subject of the dependent claims or may be deduced from the subsequent description and exemplary embodiment.

[0007] The proposed circuit comprises at least one input to receive input signals and at least a positive and a negative output to deliver positive and negative spike output signals. The input signals maybe spiking signals but may also be pulse width-modulated (pwm) or static signals. The circuit further comprises a weighting subcircuit configured to generate and output positive and/or negative charge packets to a common line of the neuron circuit based on the input signals and stored weights. A capacitance between the common line and a reference potential stores the charges from the positive and negative charge packets and converts the sum of the charges into a voltage. This capacitance can be formed of a capacitor connected between the common line and a reference potential but can also be an intrinsic (or parasitic) capacitance between the common line and at least one supply voltage or ground potential (as a reference potential) caused by the elements and wiring of the circuit. Instead of the capacitance an integrator can also be used to sum up the charges of the positive and negative charge packets and to convert the sum of the charges into a voltage. A first comparator compares this voltage against an upper reference voltage for quantization and is configured to generate the positive spike output signals at the positive output, while said voltage is larger than the upper reference voltage. A second comparator compares said voltage against a lower reference voltage for quantization and is configured to generate the negative spike output signals at the negative output, while said voltage is smaller than the lower reference voltage. The above components enable the circuit to realize signed processing, i.e., processing with positive and with negative weights as known in the art, for example from the above publication of R. Serrano-Gotarredona et al. The

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proposed neuron circuit is characterized by a feedback subcircuit connected to the positive and negative outputs. This feedback subcircuit is configured to generate and output positive charge packets to the common line based on each negative spike output signal (and stored weights) and to generate and output negative charge packets to the common line based on each positive spike output signal (and stored weights). In the proposed neuron circuit thus, the feedback based on the generated spike output signals is not used to reset the capacitance, but to feedback charge packets of opposite sign. The feedback subcircuit is build in the same way as the input weighting subcircuit. Due to this feedback subcircuit the input is taking information all the time and does not have any blind period. Furthermore, since there is no complete reset of the capacitance after each spike output, an accumulation of the quantization error (difference between upper/lower reference voltage and summed up voltage) and also a more exact compensation of the output is achieved. This and the integration on the next stage, the following integrate-and-fire neuron circuit, will reduce noise an improve accuracy, because averaging then becomes more meaningful. It is possible to wait longer for more accuracy in the calculated results because then the quantization errors of the previous operations will add up or compensate during the longer period. As will be shown later in connection with the exemplary embodiment, the voltage gain between two of these neuron circuits does only depend on the weight ratio and the capacitor ratio and not from the absolute current value and absolute pulse width. Therefore, using structural matching in preferred embodiments the proposed neuron circuit provides higher accuracy and less variation of the behavior over PVT variations. Structural matching means that functional blocks or functional units which are intended to do the same are all implemented in the same structural and physical way from the same subblocks, parts and/or elements. Functional blocks or functional units that need to do the opposite (e.g. compensate a positive current by a negative current) are implemented in a complementary structure from complementary elements (e.g. NMOS instead of PMOS transistors in a mirrored arrangement). Namely - in the preferred configurations of the circuit described later - all P-AWE are built as multiple instantiations of one block, as well as all N-AWE are built from multiple instantiations of a second block and also their subparts, which are mainly the current sources and switches inside, where N-AWE contains complementary elements that are arranged in a complementary structure to P_AWE. This implies that all the functional blocks or units will vary in the same manner with PVT and therefore the influence of this variation cancels out in overall behaviour. With the present invention a digitally configurable (leaky) integrate-and-fire neuron is proposed which can be used for mixed-signal spiking neuronal networks.

[0008] The proposed feedback enables the usage of local clocking created by small circuits. The highly variable pulse width and period from such a small circuit does not influence multistage accuracy because there is only one clock source for the consideration of the same charge packet in the sending and receiving circuit. The information in pulse width compensates for the non-ideal circuitry. The proposed feedback also gives the opportunity to calculate the result in a short period of time roughly or to count output spikes over multiple periods of time with the same input spike density and yield a higher accuracy for the same operation, because the rest of previous calculations is not removed and therefore adds up over time. The special implementation relies on structural matching of the parts and makes the circuit accuracy less dependent of variations of bias current and capacitance caused by production or environmental influences.

[0009] In the following, preferred embodiments of the proposed neuron circuit are described. These embodiments may also be combined. In a first embodiment, the weighting subcircuit comprises at least one, preferably a multiplicity of first positive analog weight emulators (P-AWE) each configured to generate and output a positive charge packet to the common line when enabled by a first enabling signal in combination with an additional enabling signal. The additional enabling signal is provided based on the desired weight. The subcircuit also comprises at least one, preferably a multiplicity of first negative analog weight emulators (N-AWE) each configured to generate and output a negative charge packet to the common line when enabled by a first enabling signal in combination with an additional enabling signal (depending on the desired weight). An input signal interface of the weighting subcircuit receives the input signals and generates the first enabling signals, based on the input signals, for the first positive and negative analog weight emulators.

[0010] In a further embodiment, also the feedback subcircuit comprises at least one, preferably a multiplicity of (second) positive analog weight emulators each configured to generate and output a positive charge packet to the common line when enabled by a second enabling signal in combination with an additional enabling signal, at least one, preferably a multiplicity of (second) negative analog weight emulators each configured to generate and output a negative charge packet to the common line when enabled by a second enabling signal in combination with an additional enabling signal. A feedback signal interface of the feedback subcircuit is connected to the positive and negative outputs of the neuron circuit and configured to generate the second enabling signals for the second positive analog weight emulators based on each negative spike output signal, and to generate the second enabling signals for the second negative analog weight emulators based on each positive spike output signal. Preferably, the first and/or second positive and negative analog weight emulators of one or both above embodiments each have a memory or are connected to a memory storing the weights based on which the additional enabling signals are provided.

[0011] Preferably the first and/or second positive and negative analog weight emulators of the above embodiments each comprise a switched current source for generating the charge packets. The neuron circuit may also comprise a common bias circuit to bias these switched current sources of at least one of the first and second positive and negative analog weight emulators.

[0012] In a further embodiment, the neuron circuit comprises a reference voltage generator to generate the reference potential, the upper reference voltage and the lower reference voltage, preferably using positive and negative analog weight emulators and capacitors.

[0013] In a further embodiment, the proposed neuron circuit comprises an offset subcircuit for generating an offset to the created charge packages. This offset subcircuit includes at least one, preferably a multiplicity of third positive analog weight emulators each configured to generate and output a positive charge packet to the common line when enabled by a third enabling signal in combination with an additional enabling signal, and at least one, preferably a multiplicity of third negative analog weight emulators each configured to generate and output a negative charge packet to the common line when enabled by a third enabling signal in combination with an additional enabling signal. The third enabling signals are generated by a digital spike generator which is connected to the third positive and negative analog weight emulators. This spike generator generates digital spike signals based on a received digital offset value, wherein the digital spike signals represent the third enabling signals for the third positive and negative analog weight emulators.

[0014] The proposed neuron circuit can be advantageously used in spiking neuronal networks or in interfaces between non-spiking and spiking neuron networks.

Short description of the drawings

[0015] The proposed neuron circuit is described in the following by way of example in connection with the corresponding figures. The figures show:

Fig. 1 an exemplary embodiment of the proposed neuron circuit;

Fig. 2 an example of cascading two neuron circuits of the prior art; and

Fig. 3 an example of cascading two neuron circuits according to the present invention.

Detailed description of embodiments

[0016] An exemplary embodiment of the proposed neuron circuit including several optional components is schematically depicted in figure 1. This figure shows on the left side the weighting subcircuit, the feedback subcircuit and the offset subcircuit. On the right hand side, the optional common bias circuit and the optional reference voltage generator are indicated as well as the comparators and the capacitor (C_{mem}). The different memories indicated in figure 1 are connected to a memory interface as indicated by the broad line with arrows.

[0017] The input signals are received at the corresponding inputs Input i ($i = 1 \dots N$) of an input signal interface. Each of it is enabling at least one of a multiplicity of positive analog weight emulators (P-AWE) and of a multiplicity of negative analog weight emulators (N-AWE) via the interface which receives the input signals and generates the enabling signals (P_{EN} , N_{EN}). The positive analog weight emulators (P-AWE) generate positive charge packets (add charge) from input spikes (input signals) and have a weight memory to hold additional enabling data influencing the number of activating currents depending on the stored weights. The negative analog weight emulators (N-AWE) to generate negative charge packets (remove charge) from input spikes and comprise also a weight memory to hold additional enabling data influencing the number of activating currents depending on the stored weights. The currents or charge packages are generated by switched current sources in the emulators of this weighting subcircuit and fed to a common line of the neuron circuit as depicted in figure 1.

[0018] A capacitor C_{mem} in parallel to a parasitic capacitance $C_{parasitic}$ and connected to the common line stores the charges created by the P-AWE and N-AWE and converts the sum of charges into a voltage V_{mem} . The capacitor C_{mem} might be modified in size by a digital value, stored in a memory (gain memory). Instead of the capacitor, the capacitance $C_{parasitic}$ can also be used to store and convert the charges into the voltage V_{mem} . Alternatively, the capacitor C_{mem} of figure 1 can be replaced by an integrator made from an OpAmp and another capacitor to integrate the charges and generate the voltage V_{mem} . The circuit further comprises a first comparator ($CompU$) to compare V_{mem} against an upper reference voltage V_{RefU} and to generate spikes $SpikeOUT_P$ on the positive output, while V_{mem} is larger than V_{RefU} , and a second comparator ($CompL$) to compare V_{mem} against a lower reference voltage V_{RefL} and to generate spikes $SpikeOUT_N$ on the negative output, while V_{mem} is smaller than V_{RefL} .

[0019] A positive feedback signal ($Feedback_P$) is derived from $SpikeOUT_N$ in a feedback signal interface of the feedback subcircuit, which enables another multiplicity of positive analog weight emulators (P-AWE). A negative feedback signal ($Feedback_N$) is derived from $SpikeOUT_P$ in the feedback signal interface, which enables another multiplicity of negative analog weight emulators (N-AWE). As in the case of the above weighting subcircuit the emulators comprise means to store the weights in or near the analog weight emulators (Weight memory) that might be SRAM cells or NVM cells.

[0020] The neuron circuit of figure 1 also comprises an offset subcircuit having a digital spike generator to generate

spikes from a digital offset input (offset memory). The digital spike generator is wired to at least one positive analog weight emulator (P-AWE) having the same or different multiplicity as for the input spikes and at least one negative analog weight emulator (N-AWE) having same or different multiplicity as for the input spikes. These analog weight emulators generate positive and negative charge packets fed to the common line to be treated as additional input spiking signals.

[0021] Further (optional) components of the neuron circuit of figure 1 are a common bias circuit, a reference voltage generator, an additional switch SwIC and a combination of a resistor RLeak and a switch SwLeak. The common bias circuit generates and feeds a bias (Biasp, Biasn) to the switched current sources of the N-AWEs and P-AWEs. The reference voltage generator generates the upper and lower reference voltages VRefU and VRefL versus Vref. These reference voltages may be created from currents using N-AWE and P-AWE circuits and capacitors, for making the comparator limits dependent on the absolute value of the bias current and therefore making the overall gain independent of the absolute value of the bias current. The switch SwIC is used to set an initial condition on the capacitor Cmem when a Reset input is active or one of at least one optional Inhibit inputs is activated. The resistor RLeak and the switch SwLeak are implemented to create a defined leaky integrator behavior, where the resistor can also be implemented as a switched capacitor.

[0022] The most important advantage of the proposed neuron circuit arises when cascading the neurons (neuron circuits). Figures 2 and 3 show a comparison between the prior art (figure 2) and the proposed invention (figure 3) where inactive parts are omitted and parts that precede or follow the focused parts are shown using dashed lines. Both examples show a series of two neuron circuits, with the capacitors Cmem1 and Cmem2 and the corresponding current sources and comparators. In both figures the fire feedback of the first stage and the pulse reception in the second stage can be recognized. In the system of figure 2 according to the prior art, when the first neuron fires a pulse, the charge removed from the first capacitor Cmem1 in the first stage is at least

$$Q_{\text{remove1}} = (V_{\text{refU}} - V_{\text{ref}}) * C_{\text{mem1}}$$

while in the second stage the charge added to the second stage's capacitor Cmem2 is

$$Q_{\text{add2}} = W_2 * I_{\text{unit}} * t_{\text{pulse}} * C_{\text{mem2}}$$

[0023] The ratio of $Q_{\text{add2}}/Q_{\text{remove1}}$, which is the voltage gain from Vmem1 to Vmem2 of the circuit, is depending on the ratio of absolute weight value W2, absolute current value Iunit and absolute pulse width tpulse over absolute voltage times a capacitance ratio.

[0024] On the other hand, in the system according to the present invention according to figure 3, when the first neuron fires a pulse, the charge removed from the first capacitor Cmem1 in the first stage is exactly and not more than

$$Q_{\text{remove1}} = W_1 * I_{\text{unit}} * t_{\text{pulse}} * C_{\text{mem1}}$$

while in the second stage the charge added to the second stage's capacitor Cmem2 is still

$$Q_{\text{add2}} = W_2 * I_{\text{unit}} * t_{\text{pulse}} * C_{\text{mem2}}$$

[0025] Therefore, the gain $Q_{\text{add2}}/Q_{\text{remove1}}$ depends on a weight ratio W_2/W_1 and a capacitor ratio $C_{\text{mem2}}/C_{\text{mem1}}$ which are quite exact (e.g. 0.1%), when realized with the same unit circuits, although the absolute value of each capacitor varies in a larger range (e.g. 20%). Iunit and tpulse cancel out. This results in a very high accuracy and less dependency on variations of the bias current and capacitance.

Claims

1. Integrate-and-fire neuron circuit, at least comprising:

- at least one input to receive input signals and at least a positive and a negative output to deliver positive and negative spike output signals,
- a weighting subcircuit configured to generate and output positive and/or negative charge packets to a common line based on the input signals and stored weights,

- a capacitance (Cmem) between the common line and a reference potential (Vref) or an integrator, said capacitance (Cmem) or integrator storing the charges of the positive and negative charge packets and converting the sum of charges into a voltage (Vmem),
 - a first comparator (CompU) comparing said voltage (Vmem) against an upper reference voltage (VRefU) and configured to generate the positive spike output signals at the positive output, while said voltage (Vmem) is larger than the upper reference voltage (VRefU),
 - a second comparator (CompL) comparing said voltage (Vmem) against a lower reference voltage (VRefL) and configured to generate the negative spike output signals at the negative output, while said voltage (Vmem) is smaller than the lower reference voltage (VRefL), and
 - a feedback subcircuit connected to the positive and negative outputs and configured to generate and output positive charge packets to the common line based on each negative spike output signal and stored weights and to generate and output negative charge packets to the common line based on each positive spike output signal and stored weights.
- 15 **2.** Integrate-and-fire neuron circuit according to claim 1, **characterized in that** the weighting subcircuit comprises
- at least one or a multiplicity of first positive analog weight emulators (P-AWE) each configured to generate and output a positive charge packet to the common line when enabled by a first enabling signal in combination with an additional enabling signal,
 - at least one or a multiplicity of first negative analog weight emulators (N-AWE) each configured to generate and output a negative charge packet to the common line when enabled by a first enabling signal in combination with an additional enabling signal, and
 - an input signal interface which receives the input signals and generates the first enabling signals, based on the input signals, for the first positive and negative analog weight emulators (P-AWE, N-AWE).
- 25 **3.** Integrate-and-fire neuron circuit according to claim 2, **characterized in that** the feedback subcircuit comprises
- at least one or a multiplicity of second positive analog weight emulators (P-AWE) each configured to generate and output a positive charge packet to the common line when enabled by a second enabling signal in combination with an additional enabling signal,
 - at least one or a multiplicity of second negative analog weight emulators (N-AWE) each configured to generate and output a negative charge packet to the common line when enabled by a second enabling signal in combination with an additional enabling signal, and
 - a feedback signal interface connected to the positive and negative outputs and configured to generate the second enabling signals for the second positive analog weight emulators (P-AWE) based on each negative spike output signal, and to generate the second enabling signals for the second negative analog weight emulators (N-AWE) based on each positive spike output signal.
- 40 **4.** Integrate-and-fire neuron circuit according to claim 2 or claim 3, **characterized in that** the first and/or second positive and negative analog weight emulators (P-AWE, N-AWE) each having a memory or being connected to a memory storing weights and/or holding additional enabling data.
- 45 **5.** Integrate-and-fire neuron circuit according to one or more of claims 2 to 4, **characterized in that** the first and/or second positive and negative analog weight emulators (P-AWE, N-AWE) each comprise a switched current source for generating the charge packets.
- 50 **6.** Integrate-and-fire neuron circuit according to claim 5, **characterized in that** the circuit comprises a common bias circuit to bias the switched current sources of at least one of the first and second positive and negative analog weight emulators (P-AWE, N-AWE).
- 55 **7.** Integrate-and-fire neuron circuit according to one or several of claims 1 to 6, **characterized in that** the circuit comprises a reference voltage generator to generate the reference potential (Vref), the upper reference voltage (VRefU) and the lower reference voltage (VRefL) using positive and negative analog weight emulators and capacitors.

8. Integrate-and-fire neuron circuit according to one or several of claims 1 to 7,
characterized in that
the circuit includes an offset subcircuit comprising

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- at least one or a multiplicity of third positive analog weight emulators (P-AWE) each configured to generate and output a positive charge packet to the common line when enabled by a third enabling signal in combination with an additional enabling signal,
 - at least one or a multiplicity of third negative analog weight emulators (N-AWE) each configured to generate and output a negative charge packet to the common line when enabled by a third enabling signal in combination with an additional enabling signal, and
 - a digital spike generator connected to the third positive and negative analog weight emulators (P-AWE, N-AWE) and generating digital spike signals based on a received digital offset value, said digital spike signals representing the third enabling signals for the third positive and negative analog weight emulators (P-AWE, N-AWE).
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9. Integrate-and-fire neuron circuit according to one or several of claims 2 to 8,
characterized in that
the first and second positive analog weight emulators are formed identically, the first and second negative analog weight emulators are formed identically and the positive and negative analog weight emulators are formed in complementary manner to achieve structural matching.

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10. Integrate-and-fire neuron circuit according to one or several of claims 1 to 9,
characterized in that
the capacitance (Cmem) is formed of a capacitor connected between the common line and the reference potential (Vref) or at least one supply line.

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11. Integrate-and-fire neuron circuit according to claim 10,
characterized in that
said capacitor is configured to be modified in size by a digital value stored in an additional memory.

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12. Integrate-and-fire neuron circuit according to one or several of claims 1 to 11,
characterized in that a resistor can be switched in parallel to the capacitance (Cmem) to implement a controlled leaky behavior.

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13. Integrate-and-fire neuron circuit according to claim 12,
characterized in that
said resistor is implemented using switched capacitors.

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14. Integrate-and-fire neuron circuit according to one or several of claims 1 to 13,
characterized in that a switch is arranged between the common line and the reference potential (Vref) allowing to set the common line to the reference potential (Vref) when activated by at least one inhibitory input or a reset input.

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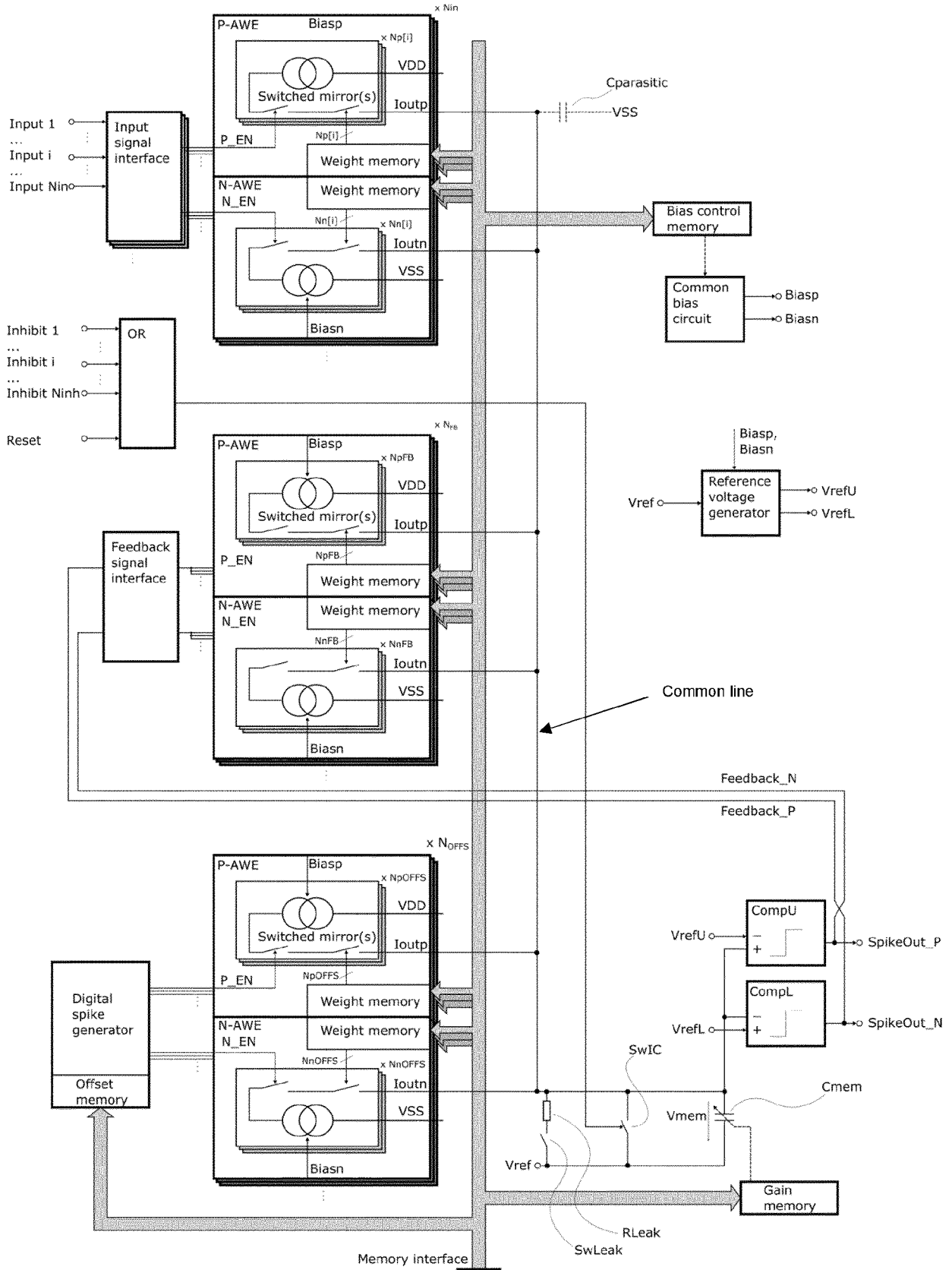


Fig. 1

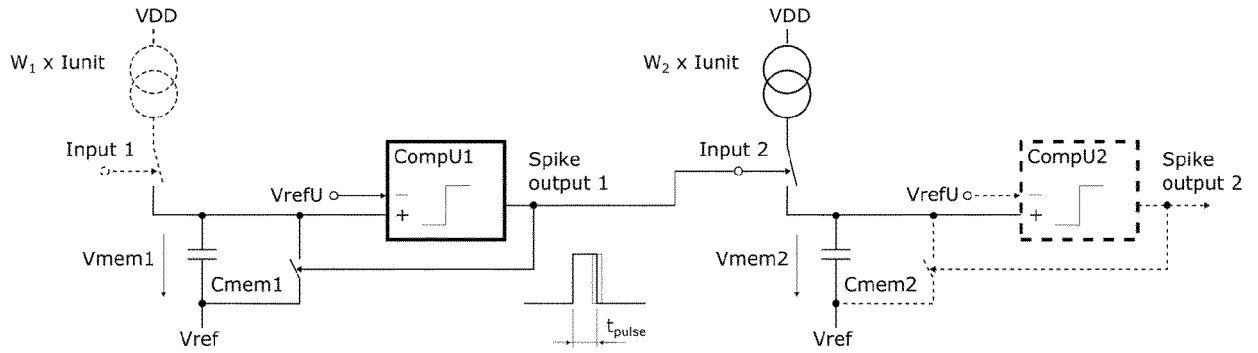


Fig. 2

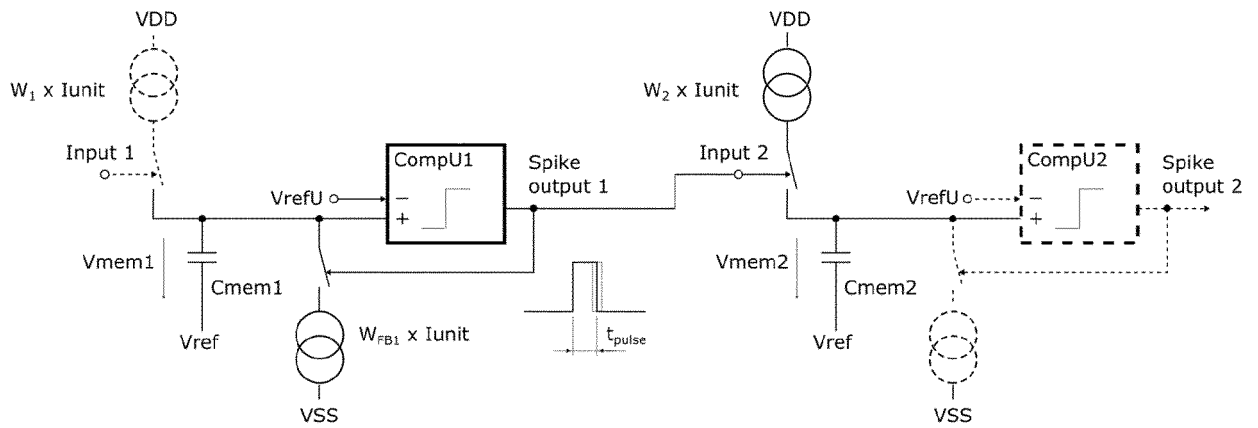


Fig. 3



EUROPEAN SEARCH REPORT

Application Number

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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A	<p>BODO RUECKAUER ET AL: "Conversion of Continuous-Valued Deep Networks to Efficient Event-Driven Networks for Image Classification", FRONTIERS IN NEUROSCIENCE, vol. 11, 7 December 2017 (2017-12-07), XP055570440, CH ISSN: 1662-4548, DOI: 10.3389/fnins.2017.00682 * Sections 2.1.1 *</p>	1-14	<p>TECHNICAL FIELDS SEARCHED (IPC) G06N</p>
A, D	<p>EP 2 877 958 B1 (HRL LAB LLC [US]) 4 September 2019 (2019-09-04) * 24; figure 4A *</p>	1-14	

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The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
The Hague		26 January 2023	Tebbal Barracosa, B
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

1 EPO FORM 1503 03.82 (P04C01)



EUROPEAN SEARCH REPORT

Application Number
EP 22 18 6414

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	<p>QIANG YU ET AL: "Constructing Accurate and Efficient Deep Spiking Neural Networks with Double-threshold and Augmented Schemes", ARXIV.ORG, CORNELL UNIVERSITY LIBRARY, 201 OLIN LIBRARY CORNELL UNIVERSITY ITHACA, NY 14853, 5 May 2020 (2020-05-05), XP081670022, * section II.A; figure 1 *</p>	1-14	
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The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (IPC)
Place of search The Hague		Date of completion of the search 26 January 2023	Examiner Tebbal Barracosa, B
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

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26-01-2023

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