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(58) Field of Search:
INT CL **H02M**
Other: **EPO-Internal, WPI Data**

(54) Title of the Invention: **DC voltage converters**
Abstract Title: **DC voltage converters**

(57) This application relates to methods and apparatus for DC voltage conversion. A DC converter (100) is described, with a charge pump circuit comprising a plurality of charge pump stages (1401, 1402-2,1402-2) each charge pump stage comprising connections for respective first and second capacitors for that stage (C1A, C1B; C2A,C2B; C3A, C3B). The charge pump also has a switch network, wherein the switch network comprises, between each successive stage, four switching paths (S7AA, S7AB, S7Ba, S7BB; S6AA, S6AB, S6Ba, S6BB) for separately connecting a respective first electrode of each of the first and second capacitors of one stage to a first electrode either of the first and second capacitors of the preceding stage, so that the relevant capacitor of the one stage can be charged by the relevant capacitor of the preceding stage.

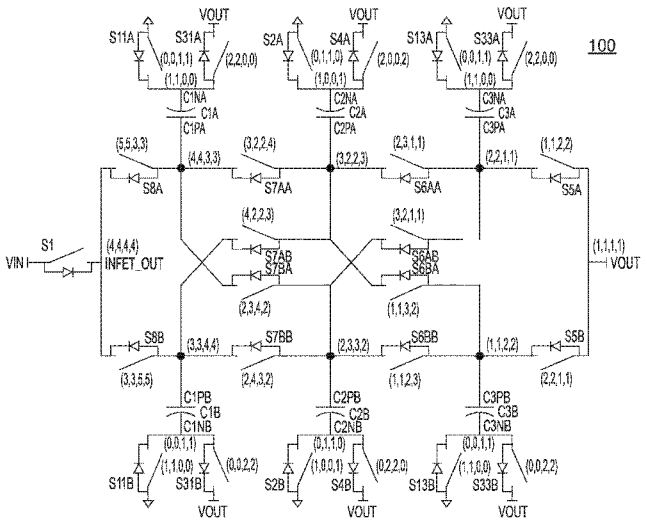

FIG. 2

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