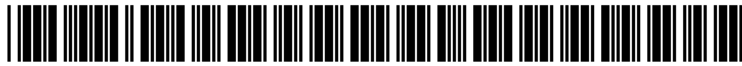

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(54) **IMAGING PANEL AND X-RAY IMAGING DEVICE**

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(57) **ABSTRACT**

The present invention aims at inhibiting the occurrence of thinning or disconnecting of the bias wiring line in an imaging panel and X-ray imaging device, thereby inhibiting signal delays, signal transmission defects, and the like. A second contact hole electrically connecting an electrode of a photodiode to a bias wiring line penetrates a second interlayer insulating film and photosensitive resin layer. In the second contact hole, an area of a region where the photosensitive resin layer opens is smaller than an area of a region where the second interlayer insulating film opens.

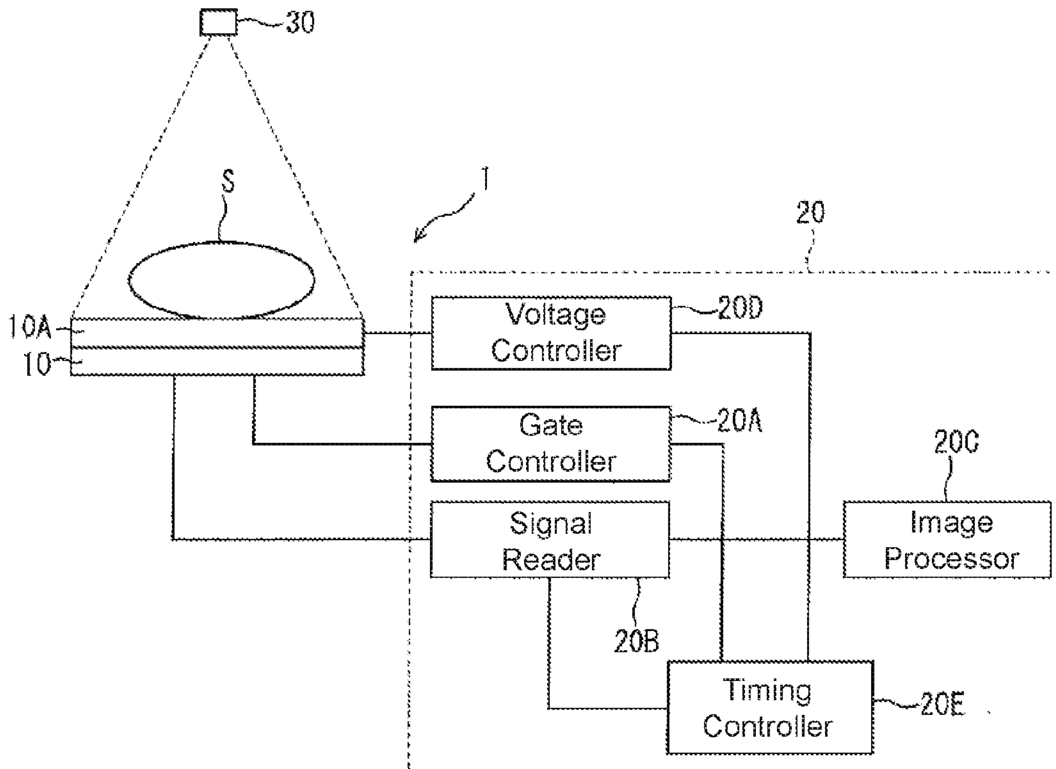


FIG. 1

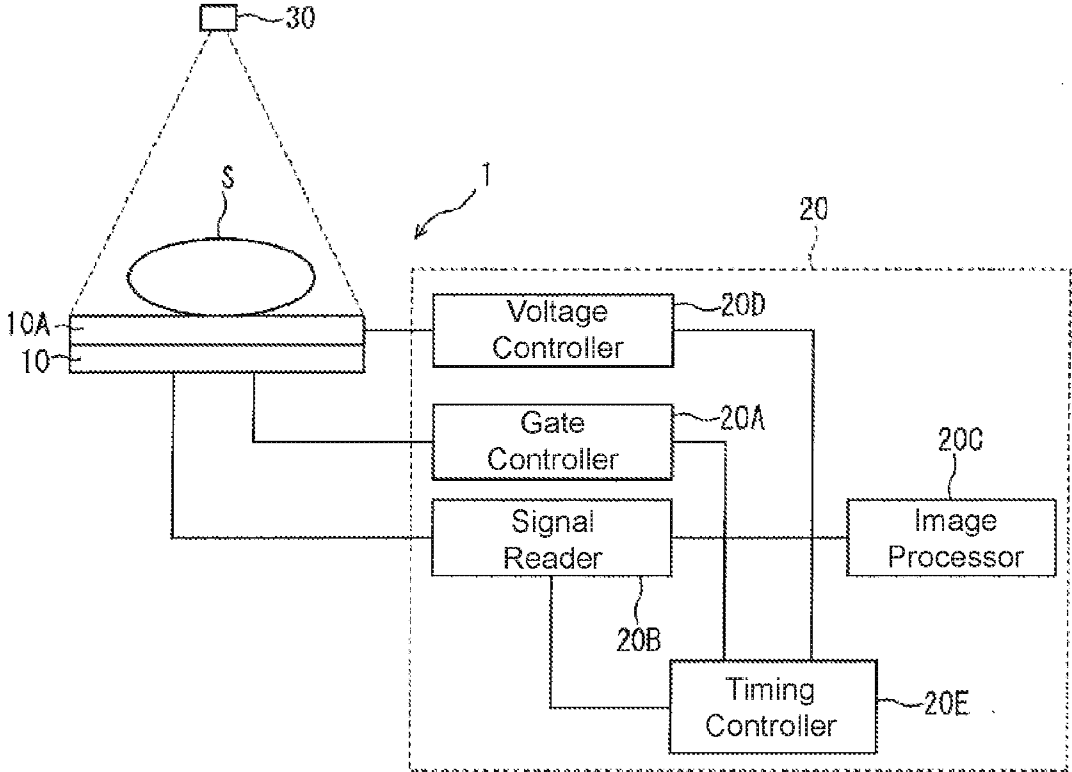


FIG. 2

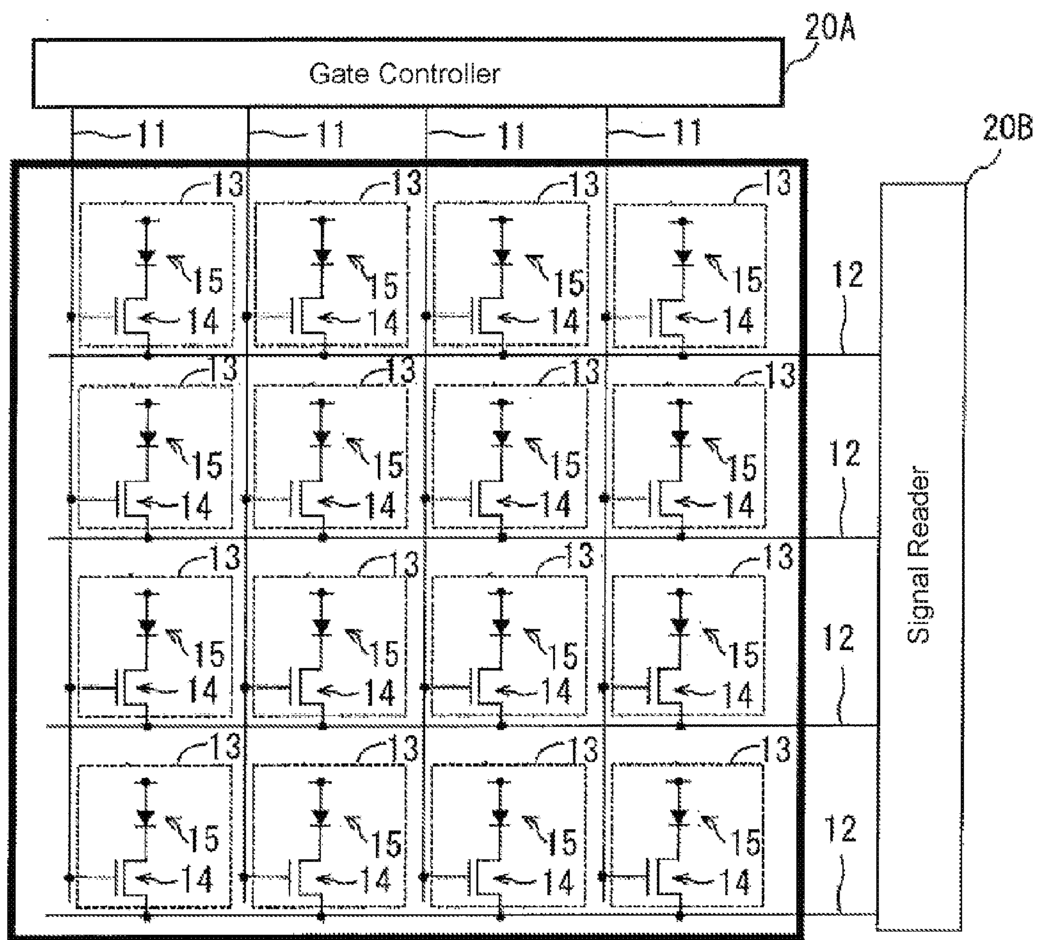


FIG. 3

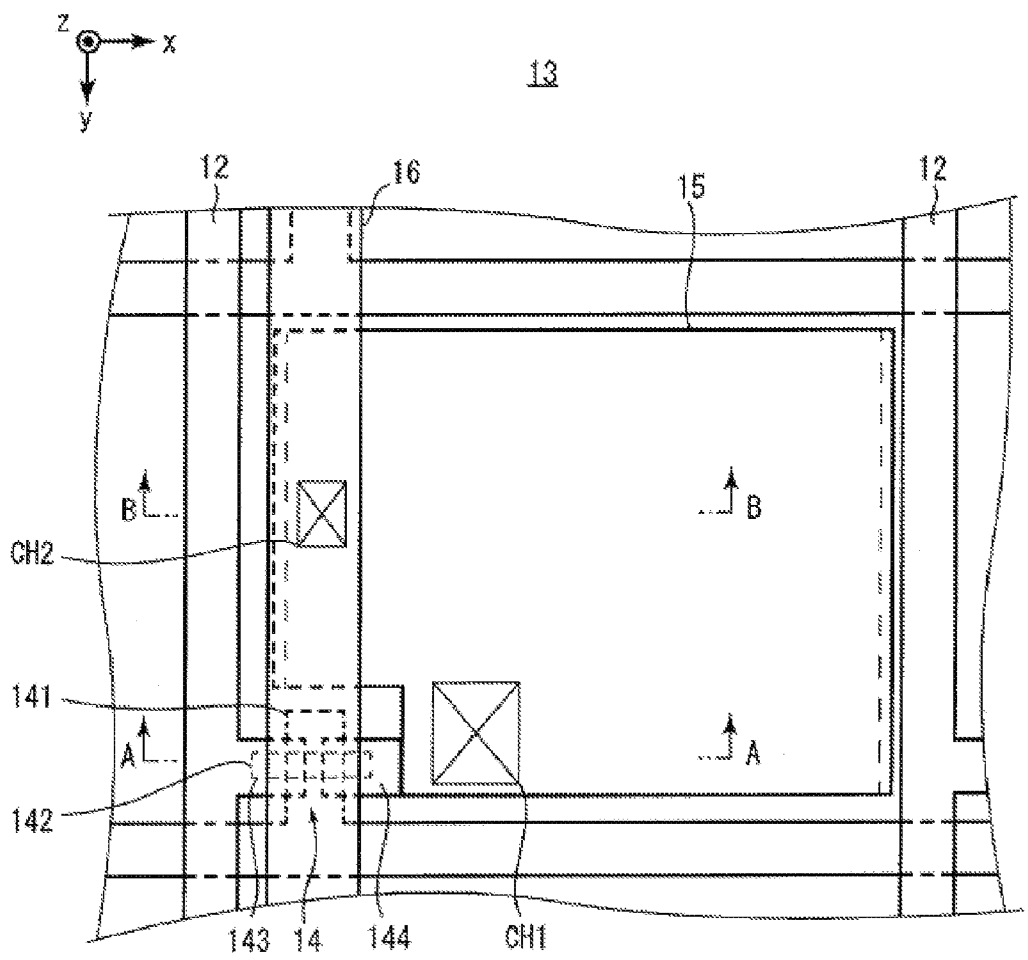
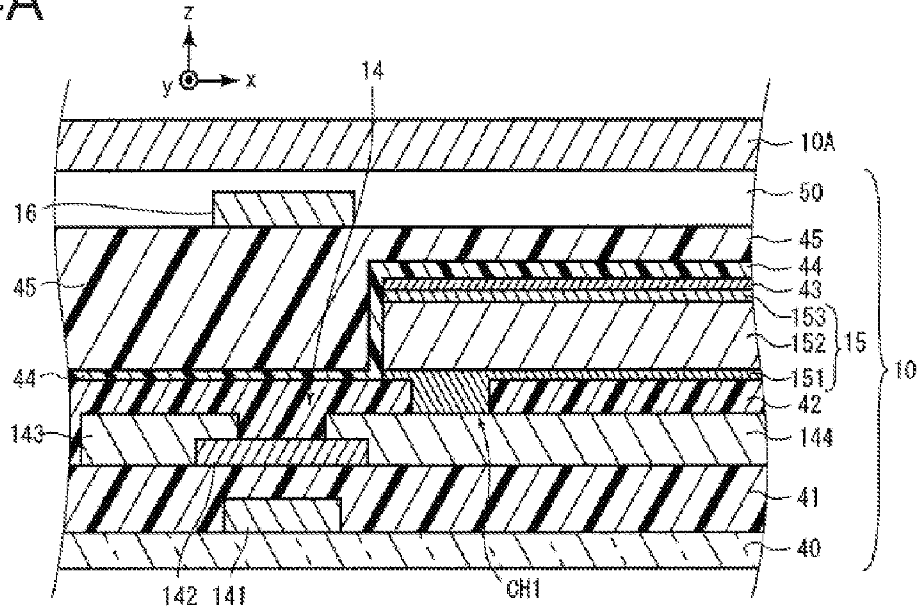
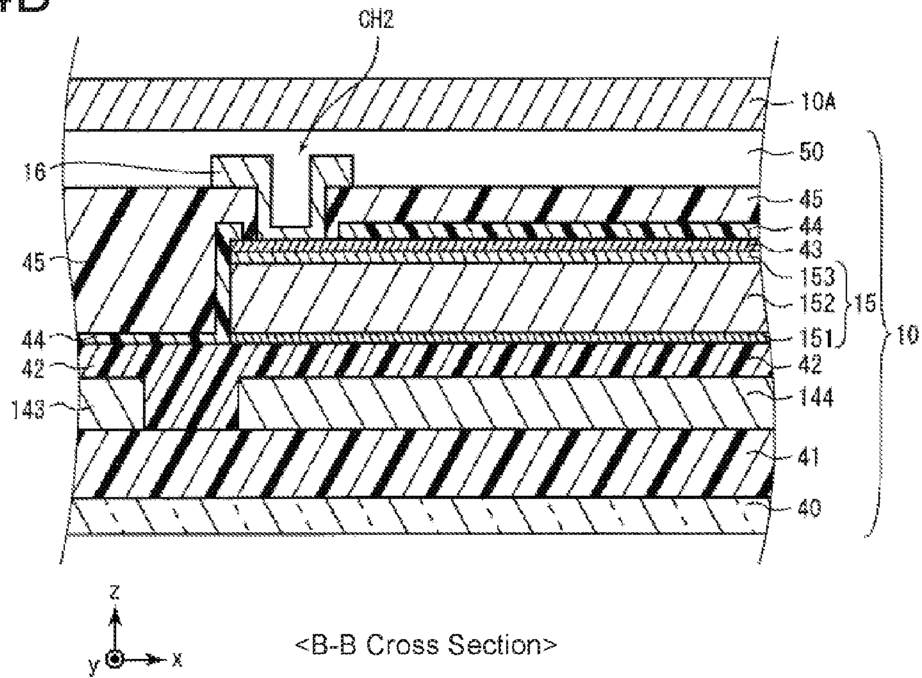


FIG. 4A



<A-A Cross Section>

FIG. 4B



<B-B Cross Section>

FIG. 5

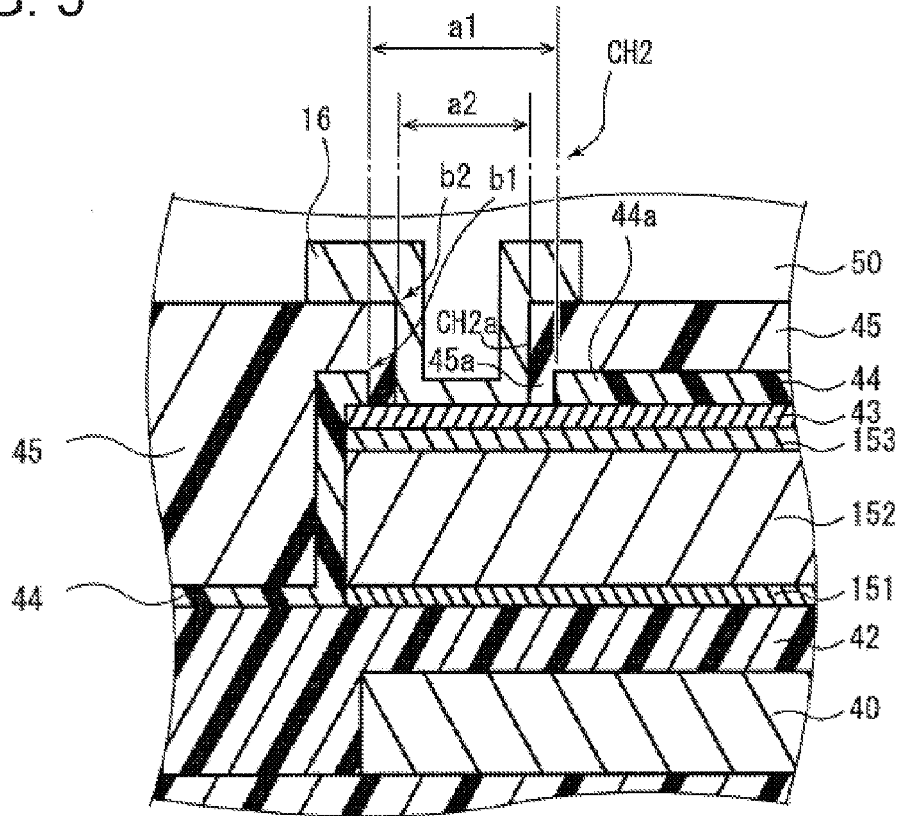


FIG. 6

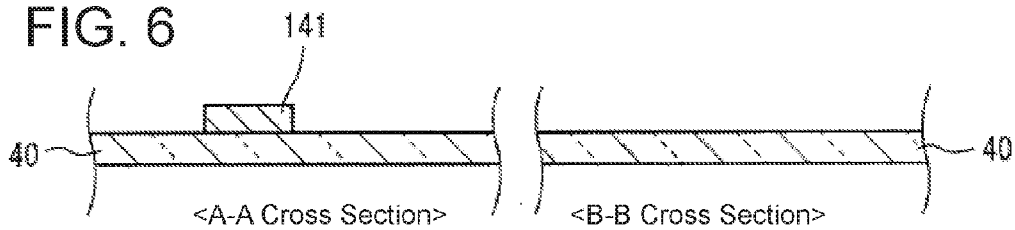


FIG. 7

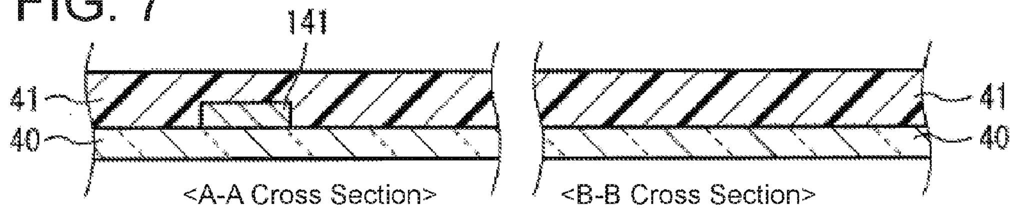


FIG. 8

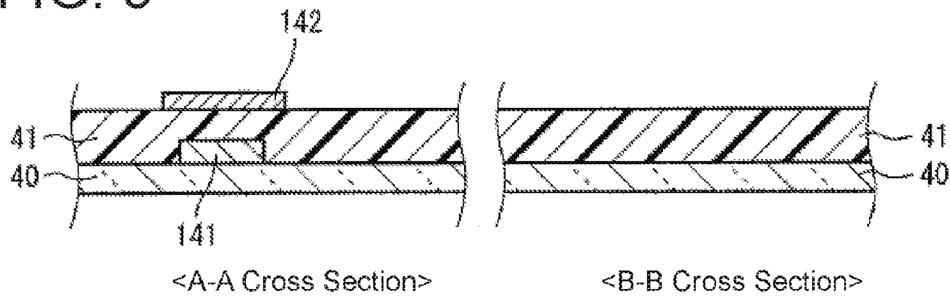


FIG. 9

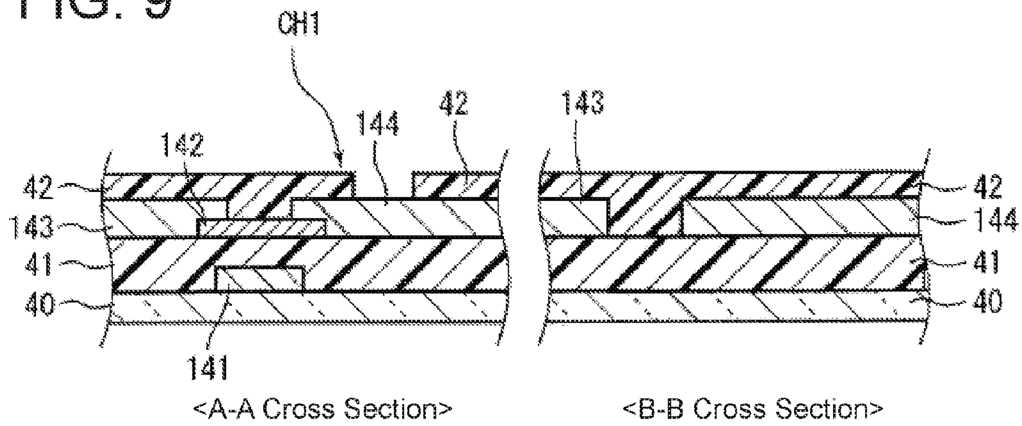


FIG. 10

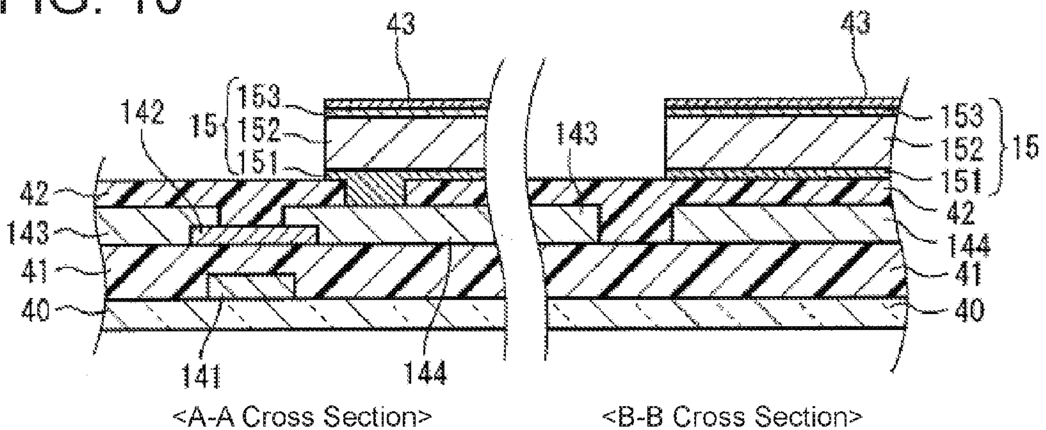
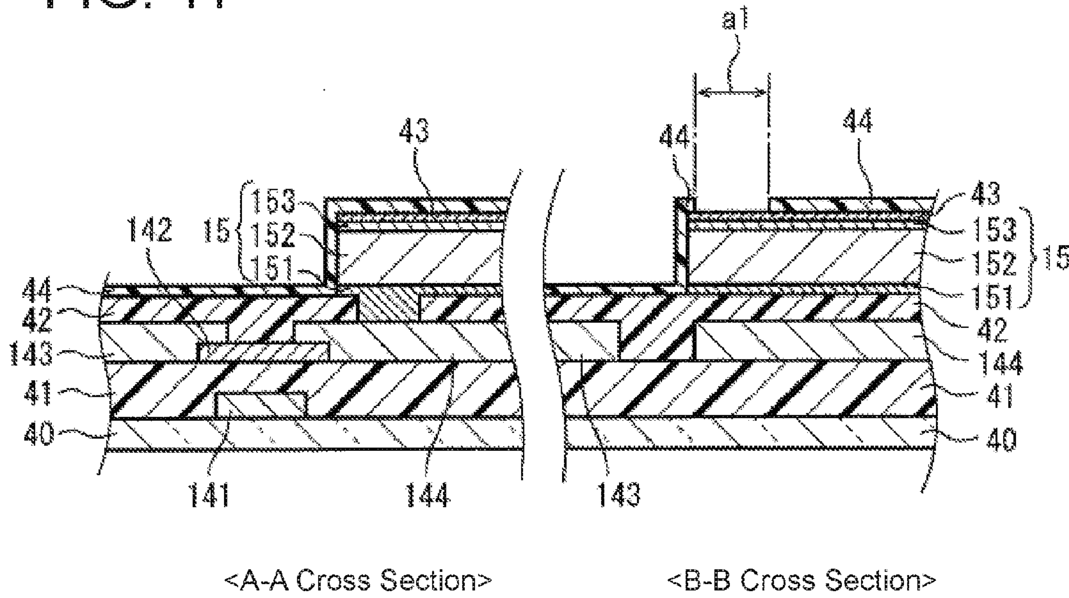
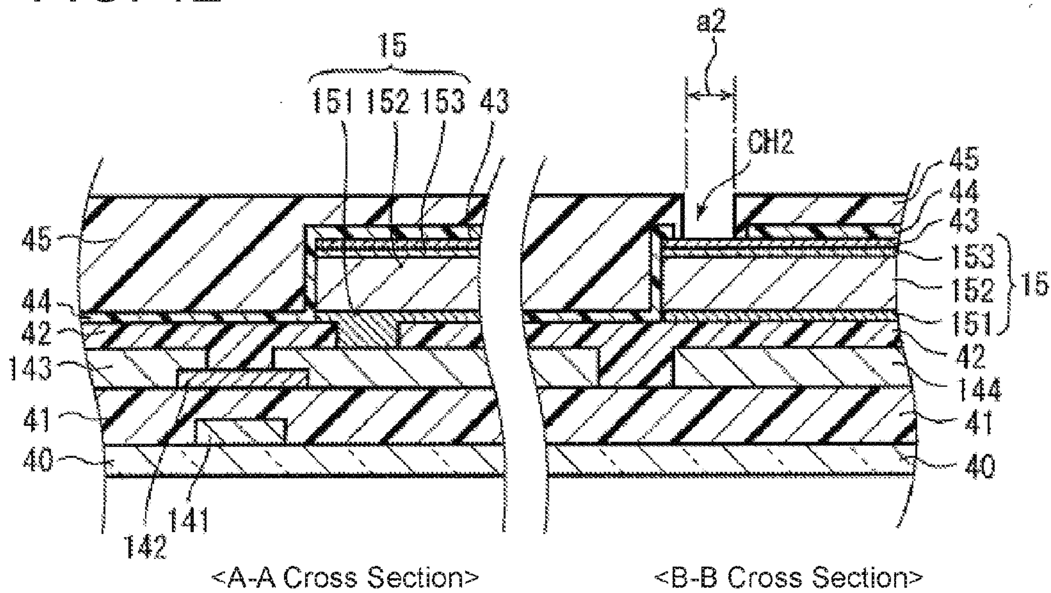


FIG. 11



<A-A Cross Section> <B-B Cross Section>

FIG. 12



<A-A Cross Section> <B-B Cross Section>

FIG. 13

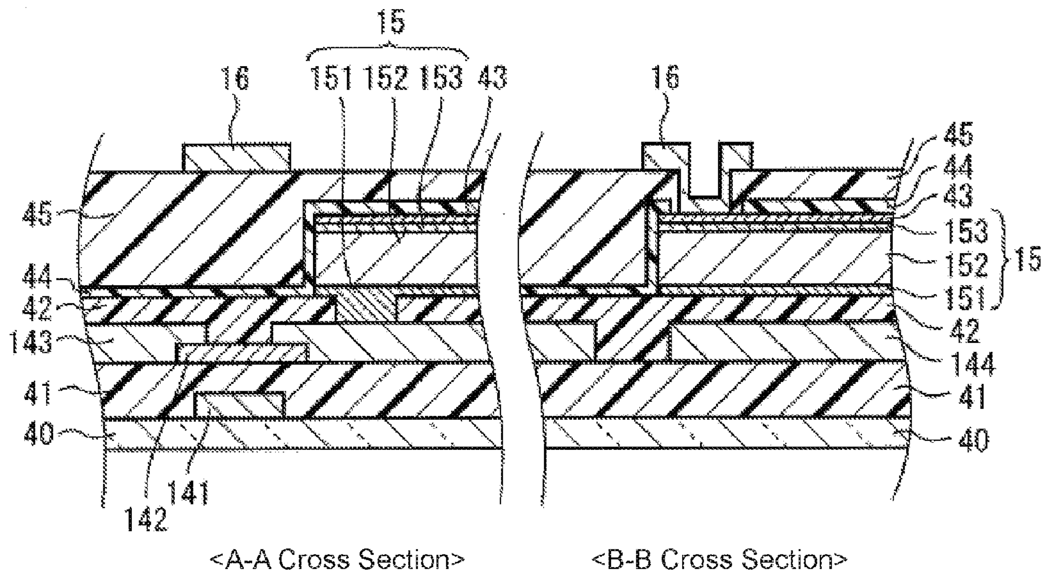


FIG. 14

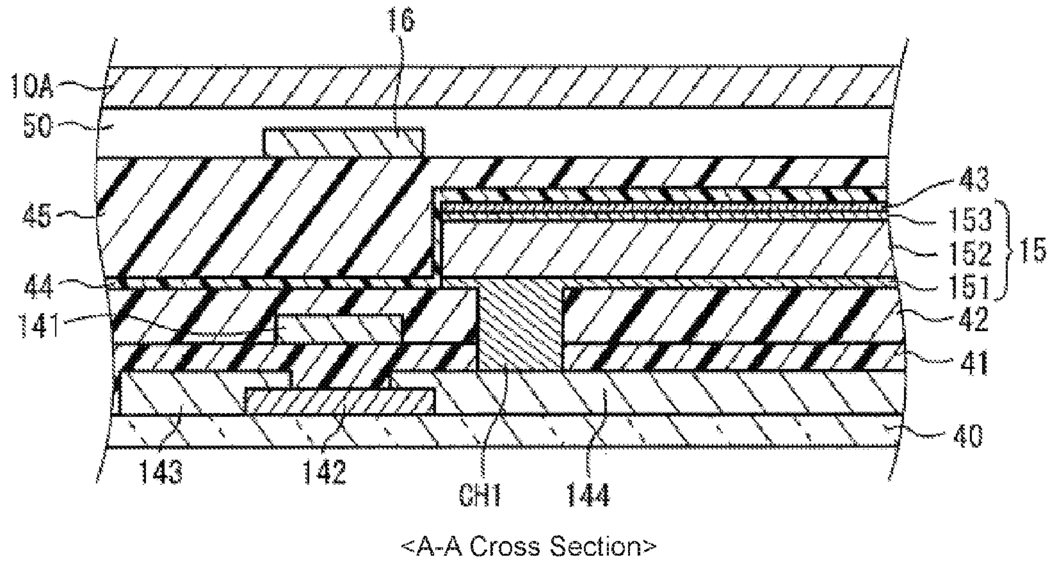
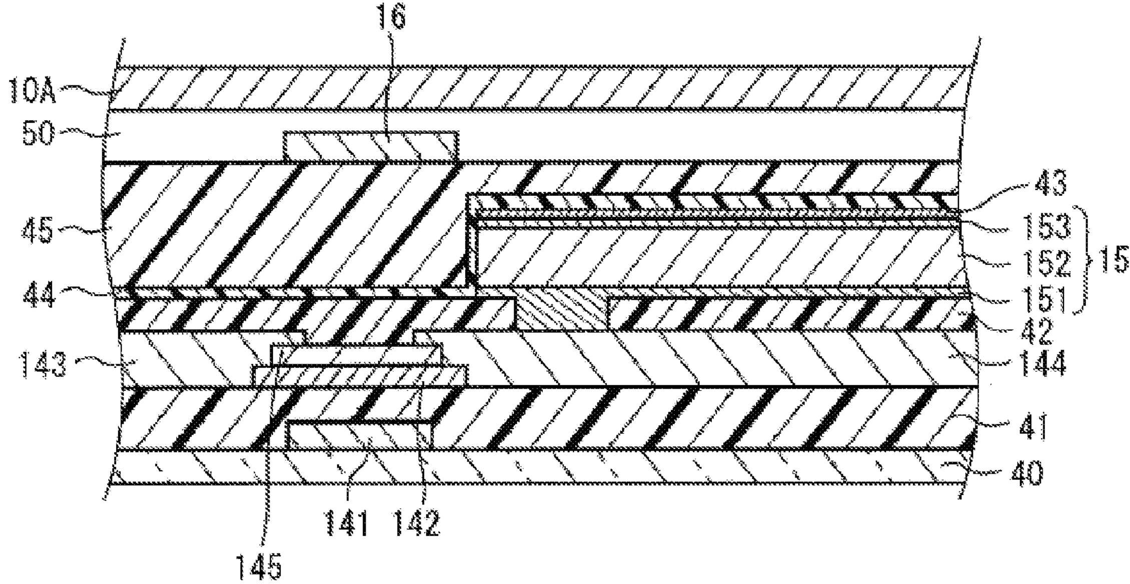


FIG. 15



<A-A Cross Section>

IMAGING PANEL AND X-RAY IMAGING DEVICE

TECHNICAL FIELD

[0001] The present invention relates to an imaging panel and an X-ray imaging device.

BACKGROUND ART

[0002] There are X-ray imaging devices that take X-ray images via an imaging panel having a plurality of pixels. In these types of X-ray imaging devices, photodiodes such as X-ray conversion films made of amorphous selenium (a-Se) convert the radiated X-rays into electric charge, for example. The electric charge that has been thus converted is read out by operating a thin film transistor (hereinafter, also "TFT") included in a pixel. Reading out the electric charge in this manner provides an X-ray image.

[0003] This type of X-ray imaging device is described in Patent Document **1**, which discloses a photoelectric converter constituting an X-ray image detector. Patent Document **1** describes that, in this photoelectric converter, a photodiode element has a photoelectric conversion layer between a bottom electrode and top electrode, and the photoelectric conversion layer has a protective film formed smaller and more inside than the bottom electrode in a manner that covers at least the face of a pattern side wall of the photoelectric conversion layer.

RELATED ART DOCUMENT

Patent Document

[0004] Patent Document 1: Japanese Patent Application Laid-Open Publication No. 2014-78651

SUMMARY OF THE INVENTION

Problems to be Solved by the Invention

[0005] However, the contact hole described in Patent Document 1 has a level difference around the opening of the contact hole between the portion where the protective film opens and a portion where a second protective film opens in a layer above the protective film. Therefore, when a bias wiring line is formed covering the periphery of the opening of the contact hole, the bias wiring line is thinned at this level difference and becomes susceptible to disconnection and the like. This results in a risk of bias signal delays or signal transmission defects.

[0006] The present invention aims at inhibiting the occurrence of thinning or disconnecting of the bias wiring line in an imaging panel and X-ray imaging device, thereby inhibiting signal delays, signal transmission defects, and the like.

MEANS FOR SOLVING THE PROBLEMS

[0007] An imaging panel of the present invention that solves the above-mentioned problems is an imaging panel for generating an image in accordance with scintillation light obtained from X-rays that have passed through a specimen, the imaging panel including: a substrate; a plurality of thin film transistors on the substrate; a first insulating film covering the thin film transistors; a plurality of conversion elements on the first insulating film that convert the scintillation light to electric charge; a second insulating film covering the plurality of conversion elements and the first insulating film; a photosensitive resin layer on the second insulating film; and a bias wiring line respectively connecting to the conversion elements and supplying a bias voltage to the conversion elements, wherein each of the thin film transistors includes: a gate electrode; a gate insulating film in a layer above or a layer below the gate electrode; a semiconductor active layer facing the gate electrode in a thickness direction with the gate insulating film interposed between the semiconductor active layer and the gate electrode; a source electrode electrically connected to the semiconductor active layer; and a drain electrode electrically connected to the semiconductor active layer and separated from the source electrode, wherein the plurality of conversion elements include: a first semiconductor layer electrically connected to the drain electrode via a first contact hole in the first insulating film; a second semiconductor layer over the first semiconductor layer and having a conductivity type that is opposite to the first conductivity type; and an electrode on the second semiconductor layer connected to the bias wiring line via a second contact hole that penetrates the second insulating film and the photosensitive resin layer, and wherein in the second contact hole, an area of a region where the photosensitive resin layer is open is smaller than an area of a region where the second insulating film is open.

EFFECTS OF THE INVENTION

[0008] The present invention makes it possible to inhibit the occurrence of thinning or disconnecting of the bias wiring line in an imaging panel and X-ray imaging device, thereby inhibiting signal delays, signal transmission defects, and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a schematic diagram showing an X-ray imaging device of an embodiment.

[0010] FIG. **2** is a schematic diagram showing a general configuration of the imaging panel in FIG. **1**.

[0011] FIG. **3** is a plan view of a pixel from the imaging panel in FIG. **2**.

[0012] FIG. **4**A is a cross-sectional view of FIG. **3** along the line A-A.

[0013] FIG. **4**B is a cross-sectional view of FIG. **3** along the line B-B.

[0014] FIG. **5** is an enlarged view of primary components showing the contact hole periphery in FIG. **4**B.

[0015] FIG. **6** is a cross-sectional view of a pixel in the manufacturing process of the gate electrode along the line A-A and along the line B-B.

[0016] FIG. **7** is a cross-sectional view during a manufacturing process of a gate insulating film of the pixel shown in FIG. **3** along the line A-A and along the line B-B.

[0017] FIG. **8** is a cross-sectional view during a manufacturing process of a semiconductor active layer of the pixel shown in FIG. **3** along the line A-A and along the line B-B.

[0018] FIG. **9** is a cross-sectional view during a manufacturing process of a source electrode and a drain electrode of the pixel shown in FIG. **3** along the line A-A and along the line B-B.

[0019] FIG. **10** is a cross-sectional view during a manufacturing process of a photodiode of the pixel shown in FIG. **3** along the line A-A and along the line B-B.

[0020] FIG. **11** is a cross-sectional view during a manufacturing process of a second interlayer insulating film of the pixel shown in FIG. **3** along the line A-A and along the line B-B.

[0021] FIG. **12** is a cross-sectional view during a manufacturing process of a photosensitive resin layer of the pixel shown in FIG. **3** along the line A-A and along the line B-B.

[0022] FIG. **13** is a cross-sectional view during a manufacturing process of a photosensitive resin layer and bias wiring line of the pixel shown in FIG. **3** along the line A-A and along the line B-B.

[0023] FIG. **14** is a cross-sectional view of a pixel of an imaging panel having a top-gate TFT according to a modification example.

[0024] FIG. **15** is a cross-sectional view of a modification example of a pixel in the imaging panel including a TFT having an etch-stop layer.

DETAILED DESCRIPTION OF EMBODIMENTS

[0025] An imaging panel of one embodiment of the present invention is an imaging panel for generating an image in accordance with scintillation light obtained from X-rays that have passed through a specimen, the imaging panel including: a substrate; a plurality of thin film transistors on the substrate; a first insulating film covering the thin film transistors; a plurality of conversion elements on the first insulating film that convert the scintillation light to electric charge; a second insulating film covering the plurality of conversion elements and the first insulating film; a photosensitive resin layer on the second insulating film; and a bias wiring line respectively connecting to the conversion elements and supplying a bias voltage to the conversion elements, wherein each of the thin film transistors includes: a gate electrode; a gate insulating film in a layer above or a layer below the gate electrode; a semiconductor active layer facing the gate electrode in a thickness direction with the gate insulating film interposed between the semiconductor active layer and the gate electrode; a source electrode electrically connected to the semiconductor active layer; and a drain electrode electrically connected to the semiconductor active layer and separated from the source electrode, wherein the plurality of conversion elements include: a first semiconductor layer electrically connected to the drain electrode via a first contact hole in the first insulating film; a second semiconductor layer over the first semiconductor layer and having a conductivity type that is opposite to the first conductivity type; and an electrode on the second semiconductor layer connected to the bias wiring line via a second contact hole that penetrates the second insulating film and the photosensitive resin layer, and wherein in the second contact hole, an area of a region where the photosensitive resin layer is open is smaller than an area of a region where the second insulating film is open (first configuration).

[0026] According to the first configuration, the second contact hole is formed penetrating the second insulating film and the photosensitive resin layer, and the area of the region where the photosensitive resin layer opens is smaller than the area of the region where the second insulating film opens. Thus, the portion where the second insulating film is opened does not form a level difference at the inner side face of the second contact hole. Accordingly, the opening peripheral section of the second contact hole only has a level difference at the portion where the photosensitive resin layer opens, which inhibits disconnecting, thinning, etc. of the bias wiring line at the second contact hole. As a result, it is possible to inhibit the occurrence of bias signal delay or signal transmission defects.

[0027] A second configuration is the first configuration, in which it is preferable that, in the second contact hole, a periphery of the opening in the second insulating film be covered by the photosensitive resin layer.

[0028] A third configuration is the first or second configuration, in which the gate insulating film may be in a layer above the gate electrode.

[0029] A fourth configuration is the third configuration, in which the configuration may further include an etch-stop layer on the semiconductor active layer.

[0030] A fifth configuration is the first or second configuration, in which the gate insulating film may be in a layer below the gate electrode.

[0031] An X-ray imaging device of one embodiment of the present invention includes the imaging panel according to any one of the first to fifth configurations; a controller controlling respective gate voltages of the plurality of thin film transistors and reading out data signals that correspond to electric charge converted by the conversion elements; an X-ray light source radiating X-rays; and a scintillator converting the X-rays to scintillation light (sixth configuration).

[0032] Embodiments of the present invention will be described in detail below with reference to the drawings. Portions in the drawings that are the same or similar are assigned the same reference characters and descriptions thereof will not be repeated.

[0033] (Configuration)

[0034] FIG. **1** is a schematic diagram showing an X-ray imaging device of an embodiment. An X-ray imaging device **1** includes an imaging panel **10** and a controller **20**. X-rays from the X-ray source **30** irradiate a specimen S, and the X-rays that have passed through the specimen S are converted to fluorescent light (hereinafter, scintillator light) by the scintillator **10**A at the top of the imaging panel **10**. The X-ray imaging device **1** captures X-ray images by the scintillator light being imaged by the imaging panel **10** and the controller **20**.

[0035] FIG. **2** is a schematic diagram showing a general configuration of the imaging panel **10**. As shown in FIG. **2**, a plurality of gate lines **11** and a plurality of data lines **12** intersecting the plurality of gate lines **11** are formed on the imaging panel **10**. The imaging panel **10** has a plurality of pixels **13** defined by the gate lines **11** and data lines **12**. FIG. **2** shows an example that has **16** (four rows and four columns) pixels **13**, but the number of pixels in the imaging panel **10** is not limited to this.

[0036] Each of the pixels **13** has a TFT **14** connected to the gate line **11** and data line **12**, and a photodiode **15** connected to the TFT **14**. Furthermore, while not shown in FIG. **2**, each of the pixels **13** has a bias line **16** (see FIG. **3**) that supplies bias voltage to the photodiode **15**, and this bias line is disposed roughly parallel to the data line **12**.

[0037] In each of the pixels **13**, the scintillation light, or namely the converted X-rays that have passed through the specimen S, is converted by the photodiode **15** into an electric charge that corresponds to the intensity of the scintillation light.

[0038] Each of the gate lines **11** in the imaging panel **10** is switched to a sequentially selectable state by the gate controller **20**A, and the TFT **14** connected to the gate line **11**

in the selected state turns ON. When the TFT **14** turns ON, a data signal corresponding to the electric charge converted by the photodiode **15** is output via the data line **12**.

[0039] Next, a specific configuration of the pixel **13** will be described. FIG. **3** is a plan view of the pixel **13** from the imaging panel **10** shown in FIG. **2**. FIG. **4**A is a cross-sectional view of the pixel **13** shown in FIG. **3** along the line A-A, and FIG. **4**B is a cross-sectional view of the pixel **13** shown in FIG. **3** along the line B-B.

[0040] As shown in FIG. **4**A and FIG. **4**B, the pixel **13** is formed on a substrate **40**. The substrate **13** is an insulating substrate such as a glass substrate, silicon substrate, a heat-resistant plastic substrate, a resin substrate, or the like, for example. In particular, for a plastic substrate or resin substrate, polyethyleneterephthalate (PET), polyethylene naphthalate (PEN), polyethersulfone (PES), acrylic, polyimide, or the like may be used.

[0041] The TFT **14** includes a gate electrode **141**, semiconductor active layer **142** disposed on the gate electrode **141** with a gate insulating film **41** therebetween, and a source electrode **143** and drain electrode **144** connected to the semiconductor active layer **142**.

[0042] The gate electrode **141** is formed contacting one surface (hereinafter, main surface) of the substrate **40** in the thickness direction. The gate electrode **141** is made of a metal such as aluminum (Al), tungsten (W), molybdenum (Mo), tantalum (Ta), chromium (Cr), titanium (Ti), or copper (Cu), or is an alloy of these metals or a metal nitride of these, for example. The gate electrode **141** may also be constituted by a plurality of metal films layered together, for example. In the present embodiment, the gate electrode **141** has a layered structure in which an aluminum metal film and titanium metal film are layered together in this order.

[0043] As shown in FIG. **4**A, the gate insulating film **41** is formed on the substrate **40** and covers the gate electrode **141**. The gate insulating film **41** may be silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), silicon nitrogen oxide (SiN_xO_y) (x>y), or the like, for example.

[0044] In order to prevent diffusion of impurities or the like from the substrate **40**, the gate insulating film **41** may be a multilayer structure. For example, the lower layer may be silicon nitride (SiN_x), silicon nitrogen oxide (SiN_xO_y) (x>y), etc., and the upper layer may be silicon oxide (SiO_x), silicon oxynitride (SiO_xN_y) (x>y), etc. Moreover, in order to form a compact gate insulating film that has little gate leakage current at low formation temperatures, a noble gas such as Argon may be included in the reactive gas so as to be mixed into the insulating film. In the present embodiment, the gate insulating film **41** has a multilayer structure in which the bottom layer is a 100 nm-400 nm silicon nitride film formed with a reactant gas of SiH_4 and NH_3, and the top layer is a 50 nm-100 nm silicon oxide film.

[0045] As shown in FIG. **4**A, the semiconductor active layer **142** is formed contacting the gate insulating film **41**. The semiconductor active layer **142** is made of an oxide semiconductor. The oxide semiconductor may be an amorphous oxide semiconductor or the like containing $InGaO_3(ZnO)_5$, magnesium zinc oxide ($Mg_xZn_{1-x}O$), cadmium zinc oxide ($Cd_xZn_{1-x}O$), cadmium oxide (CdO), or containing prescribed proportions of indium (In), gallium (Ga), and zinc (Zn), for example. The semiconductor active layer **142** may be a ZnO amorphous material doped with one or more impurity elements selected among group **1** elements, group **13** elements, group **14** elements, group **15** elements, group **17** elements, and the like, or a polycrystalline material. Alternatively, the semiconductor active layer be a microcrystalline material (a mix of amorphous and polycrystalline states), or a material that has had no impurities added.

[0046] As shown in FIG. **4**A and FIG. **4**B, the source electrode **143** and drain electrode **144** are formed contacting the semiconductor active layer **142** and the gate insulating film **41**. As shown in FIG. **3**, the source electrode **143** is connected to the data line **12**. As shown in FIG. **4**A, the drain electrode **144** is connected to a photodiode **15** via a first contact hole CH**1**. The source electrode **143**, data line **12**, and drain electrode **144** are formed on the same layer.

[0047] The source electrode **143**, data line **12**, and drain electrode **144** are made of a metal such as aluminum (Al), tungsten (W), molybdenum (Mo), tantalum (Ta), chromium (Cr), titanium (Ti), or copper (Cu), or are an alloy of these metals or a metal nitride of these, for example. Alternatively, the source electrode **143**, data line **12**, and drain electrode **144** may be a transmissive material such as indium tin oxide (ITO), indium zinc oxide (IZO), indium tin oxide containing silicon oxide (ITSO), indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), titanium nitride, or the like, or may be a combination of these.

[0048] The source electrode **143**, data line **12**, and drain electrode **144** may be constituted by a plurality of metal films layered together, for example. In the present embodiment, the source electrode **143**, data line **12**, and drain electrode **144** have a multilayer structure in which a titanium metal film, aluminum metal film, and titanium metal film are layered together in this order.

[0049] As shown in FIGS. **4**A and **4**B, the first interlayer insulating film **42** covers the semiconductor active layer **142**, source electrode **143**, data line **12**, and drain electrode **144**. The first interlayer insulating film **42** may be a single layer structure made of silicon oxide (SiO_2) or silicon nitride (SiN), or a multilayer structure in which silicon nitride (SiN) and silicon oxide (SiO_2) are layered together in this order.

[0050] As shown in FIG. **4**A and FIG. **4**B, the photodiode **15** is formed on the first interlayer insulating film **42** contacting the drain electrode **144**. The photodiode **15** includes at least a first semiconductor layer having a first conductivity type, and a second semiconductor layer having a second conductivity type that is opposite to the first conductivity type. In the present embodiment, the photodiode **15** includes an n-type amorphous silicon layer **151** (first semiconductor layer), intrinsic amorphous silicon layer **152**, and a p-type amorphous silicon layer **153** (second semiconductor layer).

[0051] The n-type amorphous silicon layer **151** is made of amorphous silicon that has been doped with an n-type impurity (phosphorous, for example). The n-type amorphous silicon layer **151** is formed contacting the drain electrode **144**. The thickness of the n-type amorphous silicon layer **151** is 20 nm to 100 nm, for example.

[0052] The intrinsic amorphous silicon layer **152** is made of intrinsic amorphous silicon. The intrinsic amorphous silicon layer **152** is formed contacting the n-type amorphous silicon layer **151**. The thickness of the intrinsic amorphous silicon layer is 200 nm to 2000 nm, for example.

[0053] The p-type amorphous silicon layer **153** is made of amorphous silicon that has been doped with a p-type impurity (boron, for example). The p-type amorphous silicon layer **153** is formed contacting the intrinsic amorphous

silicon layer **152**. The thickness of the p-type amorphous silicon layer **153** is 10 nm to 50 nm, for example.

[0054] The drain electrode **144** functions as the drain electrode of the TFT **14** and the bottom electrode of the photodiode **15**. Furthermore, the drain electrode **144** also functions as a reflective film that reflects scintillation light that has passed through the photodiode **15** back toward the photodiode **15**.

[0055] As shown in FIG. **4**A and FIG. **4**B, an electrode **43** is formed on top of the photodiode **15** and functions as the top electrode of the photodiode **15**. The electrode **43** is made of indium zinc oxide (IZO), for example.

[0056] The second interlayer insulating film **44** is formed contacting the first interlayer insulating film **42** and electrode **43**. The second interlayer insulating film **44** may be a single layer structure made of silicon oxide (SiO_2) or silicon nitride (SiN), or a multilayer structure in which silicon nitride (SiN) and silicon oxide (SiO_2) are layered together in this order.

[0057] A photosensitive resin layer **45** is formed on top of the second interlayer insulating film **44**. The photosensitive resin layer **45** is made of an organic resin material or an inorganic resin material.

[0058] As shown in FIGS. **3**, **4**A, and **4**B, the bias wiring line **16** is formed on the photosensitive resin layer **45** substantially parallel to the data line **12**. Specifically, as shown in FIGS. **4**A and **4**B, the bias wiring line **16** is formed on top of the photosensitive resin layer **45** so as to overlap the TFT **14** and be near an edge portion of the photodiode **15** near the data line **12**. The bias wiring line **16** is connected to a voltage controller **20**D (see FIG. **1**). Furthermore, as shown in FIG. **4**B, the bias wiring line **16** is connected to the electrode **43** via a second contact hole CH**2** and applies a bias voltage received from the voltage controller **20**D to the electrode **43**. The bias wiring line **16** has a multilayer structure in which indium zinc oxide (IZO) and molybdenum (Mo) are layered together, for example.

[0059] FIG. **5** is an enlarged view of primary components showing the second contact hole CH**2** periphery in FIG. **4**B. In the second contact hole CH**2**, the area of the open region of the second interlayer insulating film (the region shown by al in FIG. **5**) is greater than the area of the open region of the photosensitive resin layer **45** (the region shown by a**2** in FIG. **5**). Thus, the hole peripheral section **44***a* near where the second interlayer insulating film **44** opens is completely covered by the hole peripheral section **45***a* near where the photosensitive resin layer **45** opens. In other words, a side face CH**2***a* inside the second contact hole CH**2** is covered by the photosensitive resin layer **45**.

[0060] As shown in FIGS. **4**A and **4**B, a protective layer **50** is formed on top of the imaging panel **10**, or namely on top of the photosensitive resin layer **45**, so as to cover the bias wiring line **16**, and the scintillator **10**A is disposed on top of the protective layer **50**.

[0061] The configuration of the controller **20** will be explained while referring back to FIG. **1**. The controller **20** includes a gate controller **20**A, signal reader **20**B, image processor **20**C, voltage controller **20**D, and timing controller **20**E.

[0062] As shown in FIG. **2**, the gate controller **20**A is connected to a plurality of the gate lines **11**. The gate controller **20**A applies, via the gate lines **11**, a prescribed gate voltage to the TFTs **14** of the pixels **13** connected to the gate lines **11**.

[0063] As shown in FIG. **2**, the signal reader **20**B is connected to the plurality of data lines **12**. The signal reader **20**B, via the respective data lines **12**, reads out data signals that correspond to the electric charge converted by the photodiode **15** of the pixel **13**. The signal reader **20**B generates image signals based on the data signals and outputs the result to the image processor **20**C.

[0064] The image processor **20**C generates X-ray images based on the image signals output from the signal reader **20**B.

[0065] The voltage controller **20**D is connected to the bias wiring line **16**. The voltage controller **20**D applies a prescribed bias voltage to the bias wiring line **16**. This applies a bias voltage to the photodiode **15** via the electrode **43** connected to the bias wiring line **16**.

[0066] The timing controller **20**E controls the operation timing of the gate controller **20**A, signal reader **20**B, and voltage controller **20**D.

[0067] The gate controller **20**A selects one gate line **11** from the plurality of gate lines **11** based on the control signal from the timing controller **20**E. The gate controller **20**A applies, via the selected gate line **11**, a prescribed gate voltage to the TFT **14** of the pixel **13** connected to the corresponding gate line **11**.

[0068] The signal reader **20**B selects one data line **12** from the plurality of data lines **12** based on the control signal from the timing controller **20**E. The signal reader **20**B, via the selected data line **12**, reads out the data signal corresponding to the electric charge converted by the photodiode **15** of the pixel **13**. The pixel **13** where the data signal has been read out is connected to the data line **12** selected by the signal reader **20**B and connected to the gate line **11** selected by the gate controller **20**A.

[0069] When irradiated by X-rays from the X-ray source **30**, the timing controller **20**E outputs a control signal to the voltage controller **20**D, for example. Based on this control signal, the voltage controller **20**D applies a prescribed bias voltage to the electrode **43**.

[0070] (Operation of X-ray Imaging Device **10**)

[0071] First, X-rays are radiated from the X-ray source **30**. At such time, the timing controller **20**E outputs a control signal to the voltage controller **20**D. Specifically, a signal indicating that X-rays have been radiated from the X-ray source **30** is output from a controller that controls operation of the X-ray light source **30** to the timing controller **20**E, for example. When this signal has been received by the timing controller **20**E, the timing controller **20**E outputs a control signal to the voltage controller **20**D. The voltage controller **20**D applies a prescribed voltage (bias voltage) to the bias wiring line **16** based on the control signal from the timing controller **20**E.

[0072] The X-rays radiated from the X-ray source **30** pass through the specimen S and enter the scintillator **10**A. The X-rays that have entered the scintillator **10**A are converted into fluorescent light (scintillation light), and the scintillation light enters the imaging panel **10**.

[0073] When the scintillation light enters the photodiode **15** disposed in the respective pixels **13** in the imaging panel **10**, the photodiode **15** converts the scintillation light into an electric charge that corresponds to the intensity of the scintillation light.

[0074] The data signal that corresponds to the electric charge converted by the photodiode **15** passes through the data line **12** and is read out by the signal reader **20**B when

a gate voltage (plus voltage) received from the gate controller **20**A via the gate line **11** turns ON the TFT **14**. An X-ray image that corresponds to the read-out data signal is generated by the image processor **20**C.

[0075] (Manufacturing Method of Imaging Panel **10**)

[0076] Next, a method of manufacturing the imaging panel **10** will be explained. FIGS. **6** to **13** are cross-sectional views of the pixel **13** along lines A-A and B-B during each manufacturing step of the imaging panel **10**.

[0077] As shown in FIG. **6**, sputtering or the like is used to form an aluminum/titanium layered metal film on the substrate **40**. Thereafter, photolithography is used to pattern this metal film to form the gate electrode **141** and gate line **11**. The thickness of the metal film is 300 nm, for example.

[0078] Next, as shown in FIG. **7**, plasma-enhanced CVD or sputtering etc. is used to form the gate insulating film **41** made of silicon oxide (SiO_x) or silicon nitride (SiN_x) etc. on the substrate **40** so as to cover the gate electrode **141**. The thickness of the gate insulating film **41** is approximately 20-150 nm, for example.

[0079] Next, as shown in FIG. **8**, sputtering etc. is used to form an oxide semiconductor on the gate insulating film **41**, and photolithography is used to pattern the oxide semiconductor to form the semiconductor active layer **142**, for example. After the semiconductor active layer **142** has been formed, a high-temperature heat treatment (350° C. or greater, for example) is performed in an environment containing oxygen (e.g., the atmosphere). In such a case, it is possible to reduce oxygen defects in the semiconductor active layer **142**. The thickness of the semiconductor active layer **142** is 30 nm to 100 nm, for example.

[0080] Next, as shown in FIG. **9**, sputtering or the like used to layer titanium, aluminum, and titanium metal films in this order on the gate insulating film **41** and semiconductor active layer **142**. Thereafter, photolithography is used to pattern this metal film to form the source electrode **143**, data line **12**, and drain electrode **144**. The thickness of the source electrode **143**, data line **12**, and drain electrode **144** is 50 nm to 500 nm, for example. The etching may be either dry etching or wet etching, with dry etching being suitable if the area of the substrate **40** is large. This forms a bottom-gate TFT **14**.

[0081] Next, plasma-enhanced CVD is used to form the silicon oxide (SiO_2) or silicon nitride (SiN) first interlayer insulating film **42** on the source electrode **143**, data line **12**, and drain electrode **144**, for example. Thereafter, a thermal treatment of approximately 350° C. is performed on the entire surface of the substrate **40**, and photolithography is used to pattern the first interlayer insulating film **42** and form the first contact hole CH**1**.

[0082] Next, as shown in FIG. **10**, sputtering or the like is used to form the n-type amorphous silicon layer **151**, intrinsic amorphous silicon layer **152**, and p-type amorphous silicon layer **153** in this order on the first interlayer insulating film **42** and drain electrode **144**. At such time, the drain electrode **144** electrically connects to the n-type amorphous silicon layer **151** via the first contact hole CH**1**. Thereafter, photolithography is used for patterning, and dry etching is performed to form the photodiode **15**.

[0083] Next, sputtering or the like is used to deposit indium zinc oxide (IZO) on the first interlayer insulating film **42** and photodiode **15**, which is patterned by photolithography to form the electrode **43**.

[0084] Next, as shown in FIG. **11**, plasma-enhanced CVD or the like is used to deposit silicon oxide (SiO_2) or silicon nitride (SiN) on the first interlayer insulating film **42** and electrode **43** to form the second interlayer insulating film **44**. Thereafter, photolithography is used for patterning in order to form the opening that serves as the second contact hole CH**2** on the electrode **43**.

[0085] Next, as shown in FIG. **12**, a photosensitive resin is deposited on the second interlayer insulating film **44** and dried to form the photosensitive resin layer **45**, and then photolithography is used to form an opening. This forms the second contact hole CH**2**, which penetrates the second interlayer insulating film **44** and photosensitive resin layer **45**.

[0086] Then, as shown in FIG. **13**, sputtering or the like is used to deposit indium tin oxide (IZO) and molybdenum (Mo) metal film layers on the photosensitive resin layer **45**, and these are patterned by photolithography to form the bias wiring line **16**.

[0087] In the present embodiment, the second contact hole CH**2** is formed penetrating the second interlayer insulating film **44** and photosensitive resin layer **45**. As shown in FIG. **5**, the area of the region a**2** where the photosensitive resin layer **45** opens has a smaller size than the area of the region a**1** where the second interlayer insulating film **44** opens. Thus, a level difference b**1** constituted by the hole peripheral section **44***a* near where the second interlayer insulating film **44** opens does not affect the shape of the side face CH**2***a* inside the second contact hole CH**2**. This is because the hole peripheral section **44***a* near where the second interlayer insulating film **44** opens is completely covered by the hole peripheral section **45***a* near where the photosensitive resin layer **45** opens. In other words, the shape of the side face CH**2***a* of the second contact hole CH**2** is influenced only by a level difference b**2** constituted by the hole peripheral section **45***a* of the photosensitive resin layer **45**.

[0088] Accordingly, the present embodiment inhibits disconnection, thinning, etc. of the bias wiring line at the second contact hole CH**2** more than if the shape of the side face CH**2***a* of the second contact hole CH**2** were influenced by both of the level differences b**1** and b**2**. As a result, it is possible to inhibit the occurrence of bias signal delay or signal transmission defects.

Modification Examples

[0089] Next, modification examples of the present invention will be explained.

[0090] In the embodiment described above, an example was described in which the bottom-gate TFT **14** is included in the imaging panel **10**, but as shown in FIG. **14**, the TFT may be a top-gate TFT, or a bottom-gate TFT such as that shown in FIG. **15**, for example.

[0091] The parts that differ from the embodiment described above for the method of manufacturing an imaging panel having the top-gate TFT **14** shown in FIG. **14** will be explained below. First, the semiconductor active layer **142** made of an oxide semiconductor is formed on the substrate **40**. Then, titanium, aluminum, and titanium are layered in this order on the substrate **40** and semiconductor active layer **142** to form the source electrode **143**, data line **12**, and drain electrode **144**.

[0092] Next, the silicon oxide (SiO_x) or silicon nitride (SiN_x) etc. gate insulating film **41** is formed on the semiconductor active layer **142**, source electrode **143**, data line

12, and drain electrode **144**. Thereafter, aluminum and titanium are layered on the gate insulating film **41** to form the gate electrode **141** and gate line **11**.

[0093] After the gate electrode **141** is formed, the first interlayer insulating film **42** is formed on the gate insulating film **41** so as to cover the gate electrode **141**, and the first contact hole CH**1** is formed penetrating through to the drain electrode **144**. Then, in a similar manner to the embodiment described above, the photodiode **15** is formed on the first interlayer insulating film **42** and the drain electrode **144**.

[0094] Furthermore, in the case of an imaging panel equipped with a TFT **14** having an etch stop layer **145** as shown in FIG. **15**, then in the above-mentioned embodiment, after the semiconductor active layer **142** is formed, plasma-enhanced CVD or the like is used to deposit silicon oxide (SiO_2) on the semiconductor active layer **142**, for example. Thereafter, photolithography is used to pattern and form the etch stop layer **145**. Then, after the etch stop layer **145** is formed, titanium, aluminum, and titanium may be layered in this order on the semiconductor active layer **142** and the etch stop layer **145** to form the source electrode **143**, data line **12**, and drain electrode **144**.

[0095] An embodiment of the present invention has been described above, but the above embodiment is a mere example of an implementation of the present invention. Thus, the present invention is not limited to the embodiment described above, and can be implemented by appropriately modifying the embodiment described above without departing from the spirit of the present invention.

INDUSTRIAL APPLICABILITY

[0096] The present invention is useful for imaging panels and X-ray imaging devices.

1. An imaging panel for generating an image in accordance with scintillation light obtained from X-rays that have passed through a specimen, the imaging panel comprising:
   - a substrate;
   - a plurality of thin film transistors on the substrate;
   - a first insulating film covering the thin film transistors;
   - a plurality of conversion elements on the first insulating film that convert the scintillation light to electric charge;
   - a second insulating film covering the plurality of conversion elements and the first insulating film, the second insulating film having a contact hole therein;
   - a photosensitive resin layer on the second insulating film and in the contact hole of the second insulating film; and
   - a bias wiring line respectively connecting to the conversion elements and supplying a bias voltage to the conversion elements,

   wherein each of the thin film transistors includes:
   - a gate electrode;
   - a gate insulating film in a layer above or a layer below the gate electrode;
   - a semiconductor active layer facing the gate electrode with the gate insulating film interposed between the semiconductor active layer and the gate electrode;
   - a source electrode electrically connected to the semiconductor active layer; and
   - a drain electrode electrically connected to the semiconductor active layer and separated from the source electrode,

   wherein the plurality of conversion elements each include:
   - a first semiconductor layer electrically connected to the drain electrode via a contact hole in the first insulating film;
   - a second semiconductor layer over the first semiconductor layer and having a conductivity type that is opposite to the first semiconductor layer; and
   - an electrode on the second semiconductor layer, and

   wherein a contact hole is formed in a portion of the photosensitive resin layer that is disposed within said contact hole in the second insulating film, and said electrode on the second semiconductor layer is connected to the bias wiring line via said contact hole in said portion of the photosensitive resin layer.

2. The imaging panel according to claim **1**, wherein, in the contact hole, a periphery of the contact hole in the second insulating film is covered by the photosensitive resin layer.

3. The imaging panel according to claim **1**, wherein the gate insulating film is in a layer above the gate electrode.

4. The imaging panel according to claim **3**, further comprising an etch-stop layer on the semiconductor active layer.

5. The imaging panel according to claim **1**, wherein the gate insulating film is in a layer below the gate electrode.

6. An X-ray imaging device, comprising:
   - the imaging panel according to claim **1**;
   - a controller controlling respective gate voltages of the plurality of thin film transistors and reading out data signals that correspond to electric charge converted by the conversion elements;
   - an X-ray light source radiating X-rays; and
   - a scintillator converting the X-rays to scintillation light.

7. The imaging panel according to claim **2**, wherein the gate insulating film is in a layer above the gate electrode.

8. The imaging panel according to claim **7**, further comprising an etch-stop layer on the semiconductor active layer.

9. The imaging panel according to claim **2**, wherein the gate insulating film is in a layer below the gate electrode.

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