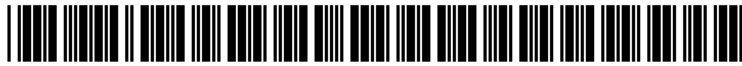

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Lee et al.

(54) **METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES INCLUDING CONDUCTIVE STRUCTURES**

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CPC ***H01L 21/76877*** (2013.01); ***H01L 21/76805*** (2013.01); ***H01L 21/76829*** (2013.01); ***H01L 21/76825*** (2013.01); ***H01L 21/7684*** (2013.01); ***H01L 21/76843*** (2013.01); ***H01L 21/76807*** (2013.01)

(57) **ABSTRACT**

A method of forming a semiconductor device can include forming an insulation layer using a material having a composition selected to provide resistance to subsequent etching process. The composition of the material can be changed to reduce the resistance of the material to the subsequent etching process at a predetermined level in the insulation layer. The subsequent etching process can be performed on the insulation layer to remove an upper portion of the insulation layer above the predetermined level and leave a lower portion of the insulation layer below the predetermined level between adjacent conductive patterns extending through the lower portion of the insulation layer. A low-k dielectric material can be formed on the lower portion of the insulation layer between the adjacent conductive patterns to replace the upper portion of the insulation layer above the predetermined level.

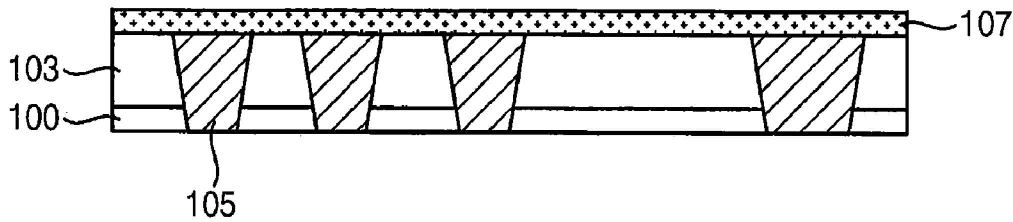


FIG. 1

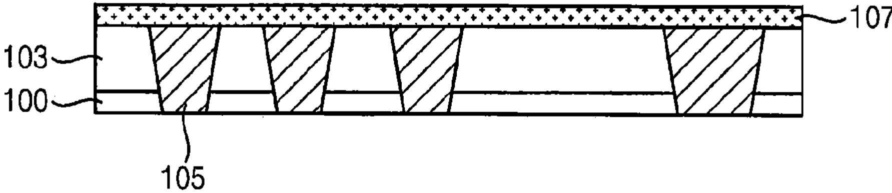


FIG. 2

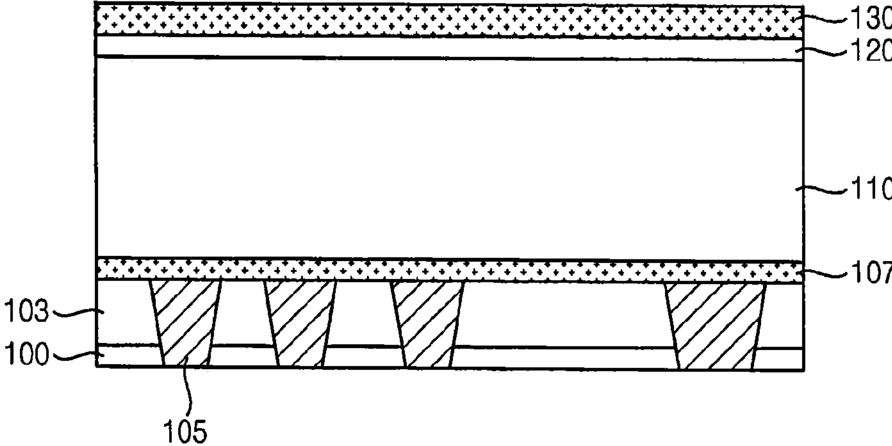


FIG. 3

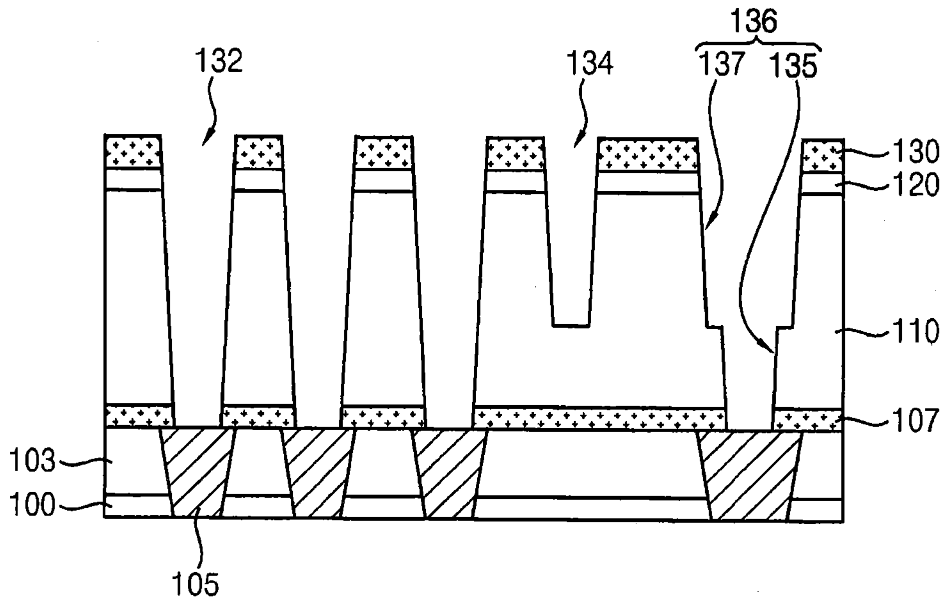


FIG. 4

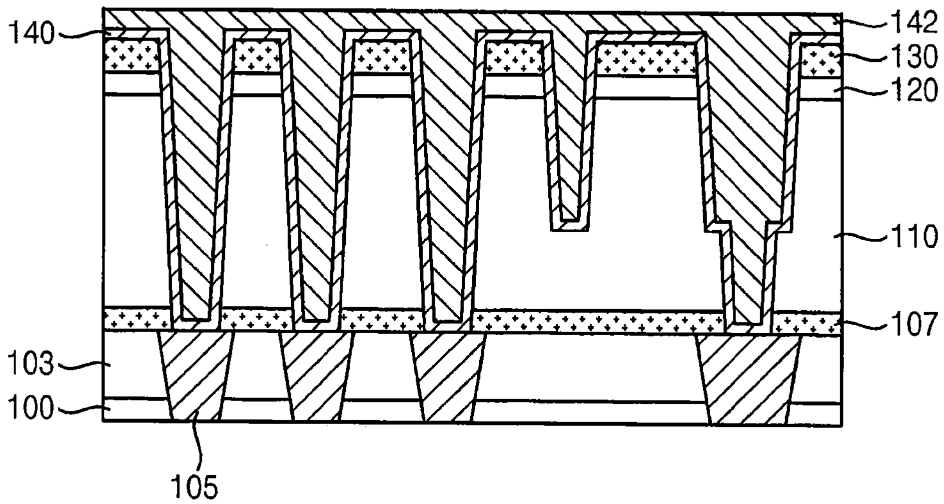


FIG. 5

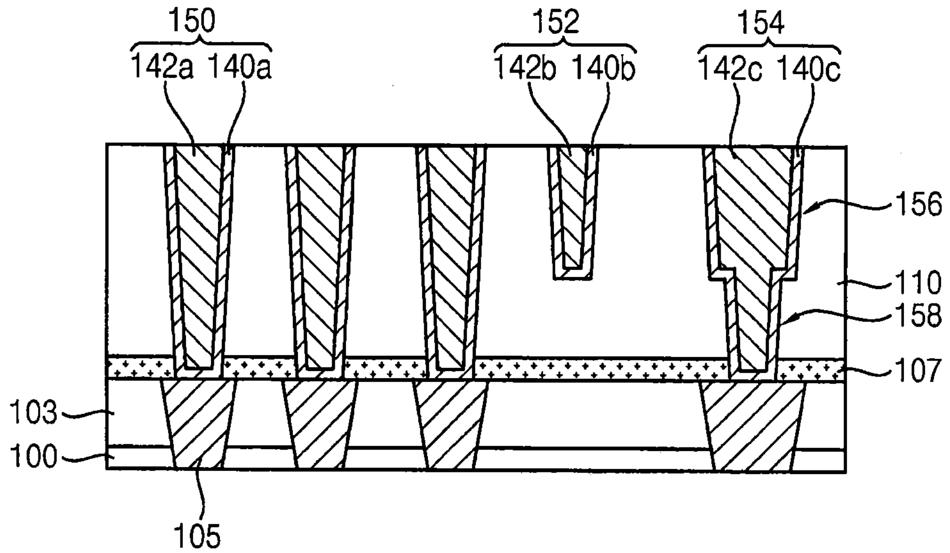


FIG. 6

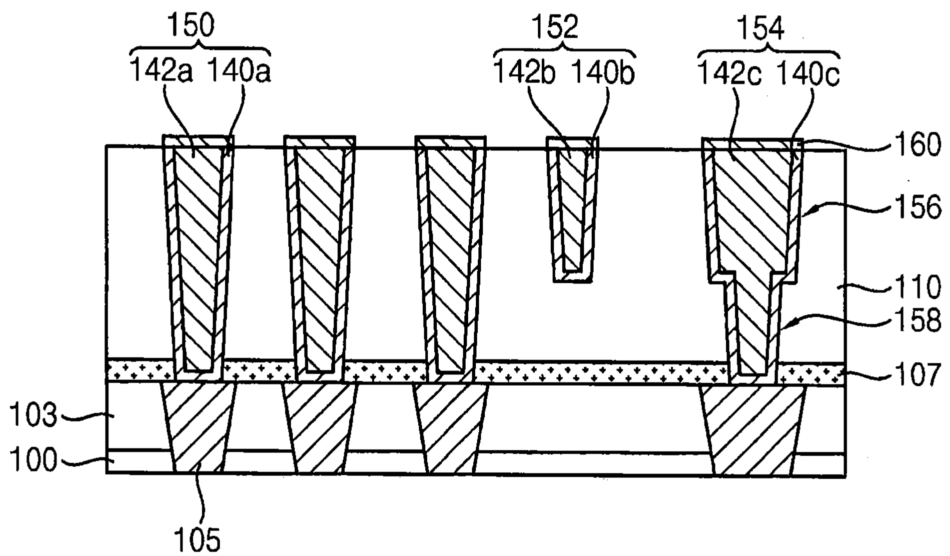


FIG. 7

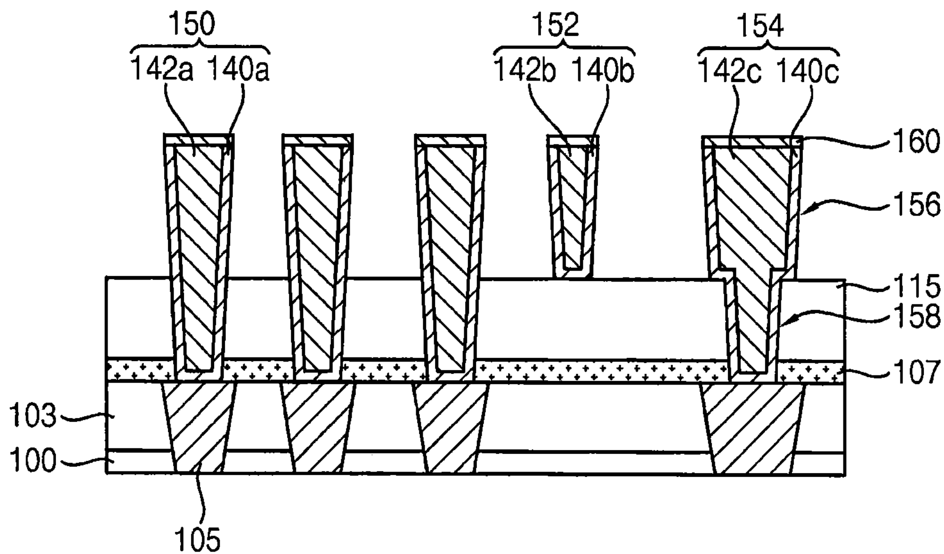


FIG. 8

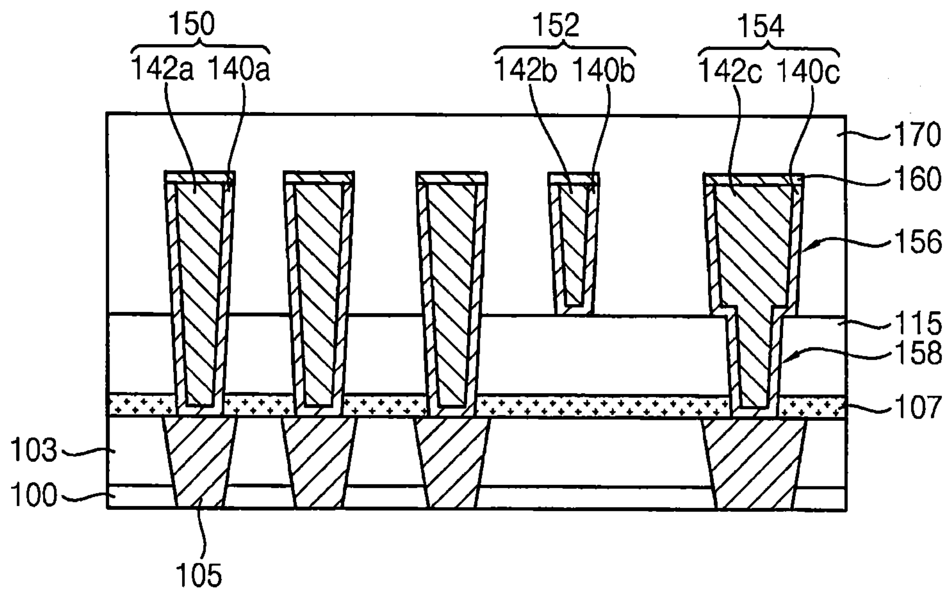


FIG. 9

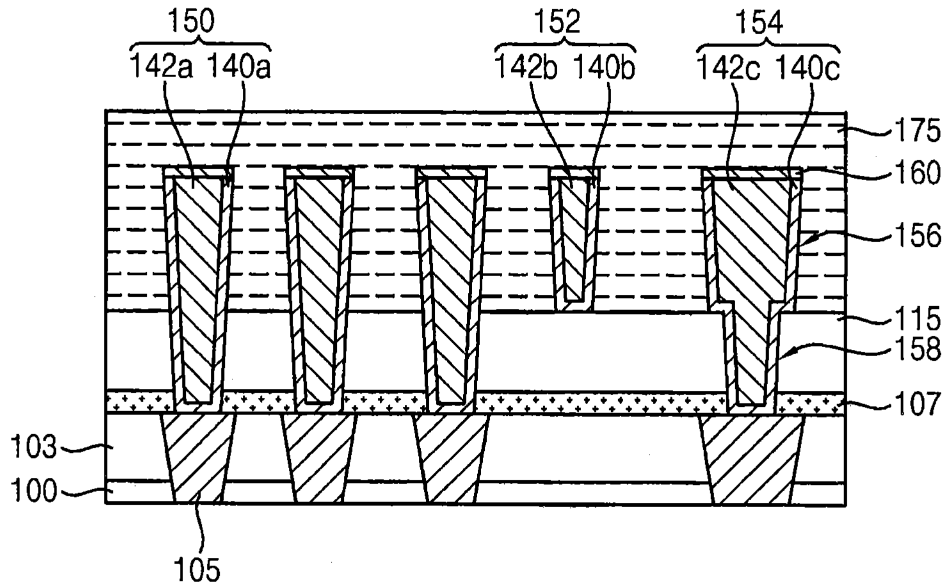


FIG. 10

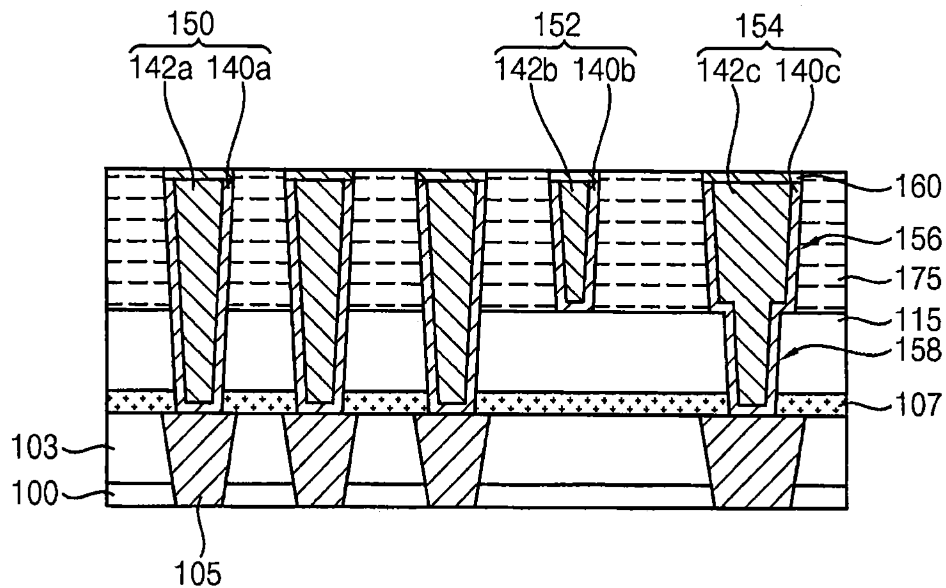


FIG. 11

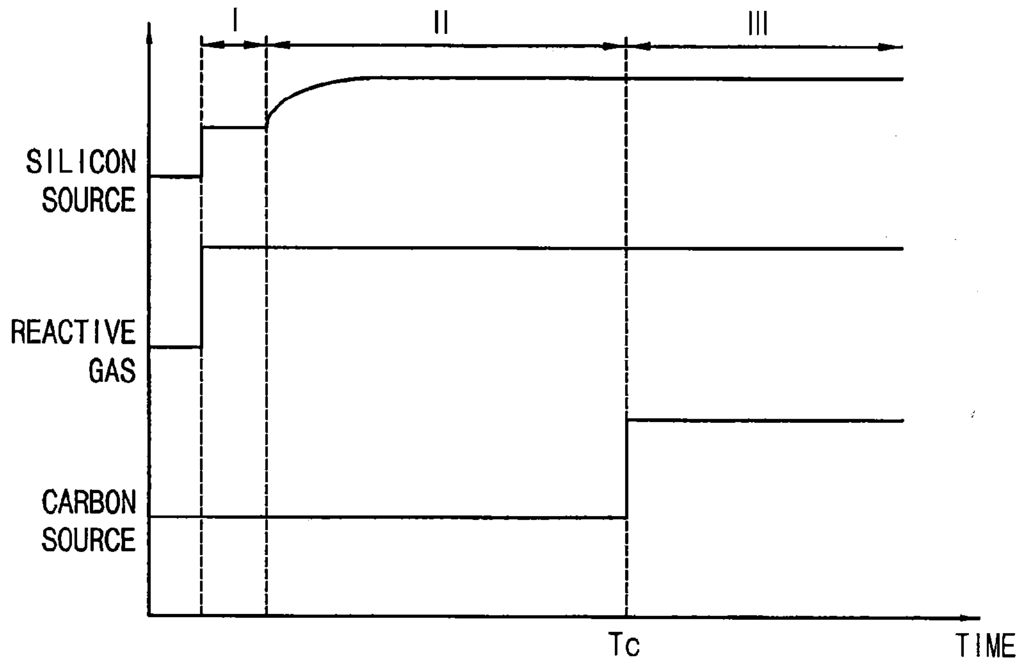


FIG. 12

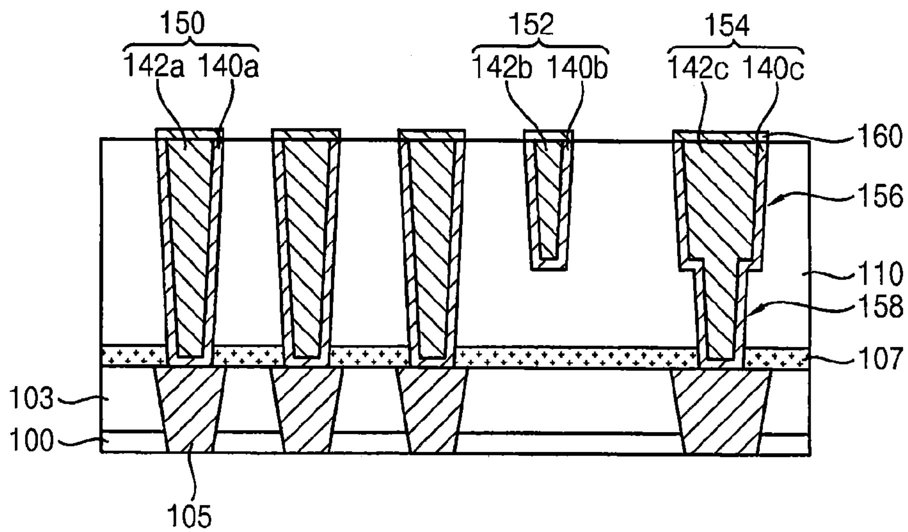


FIG. 13

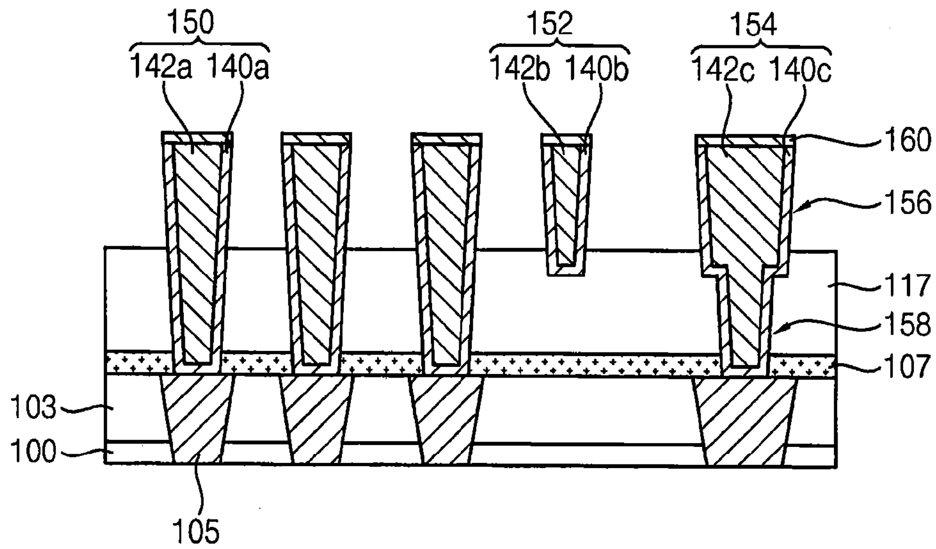


FIG. 14

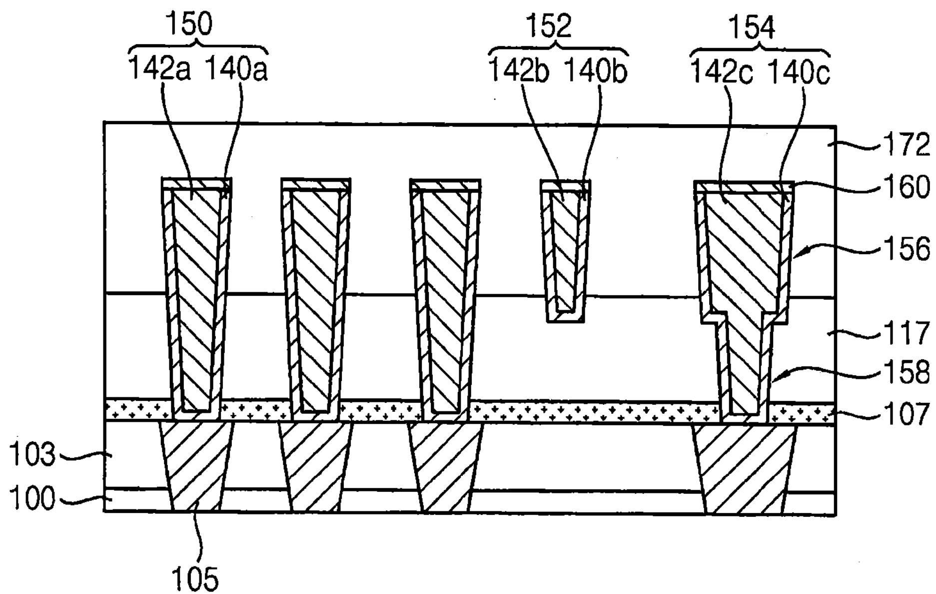


FIG. 15

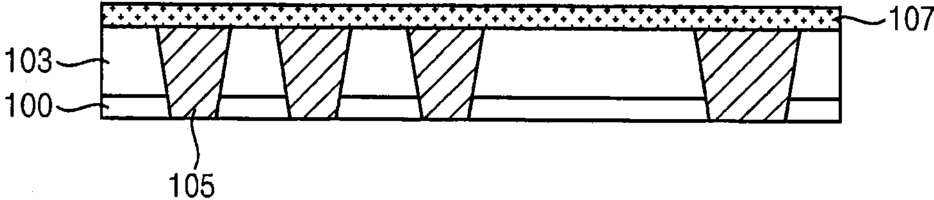


FIG. 16

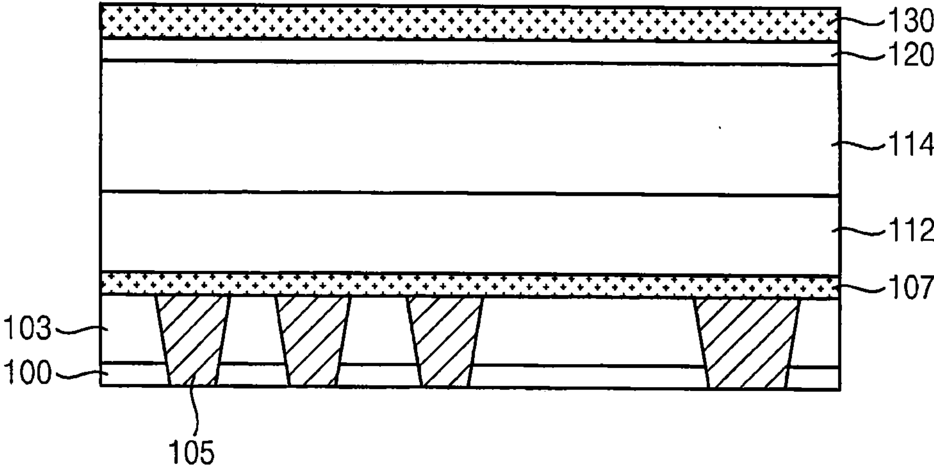


FIG. 17

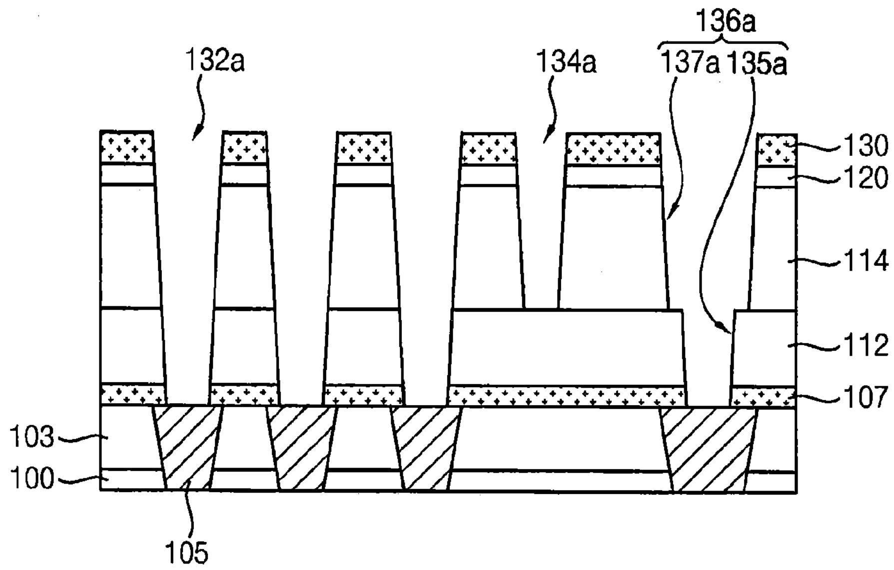


FIG. 18

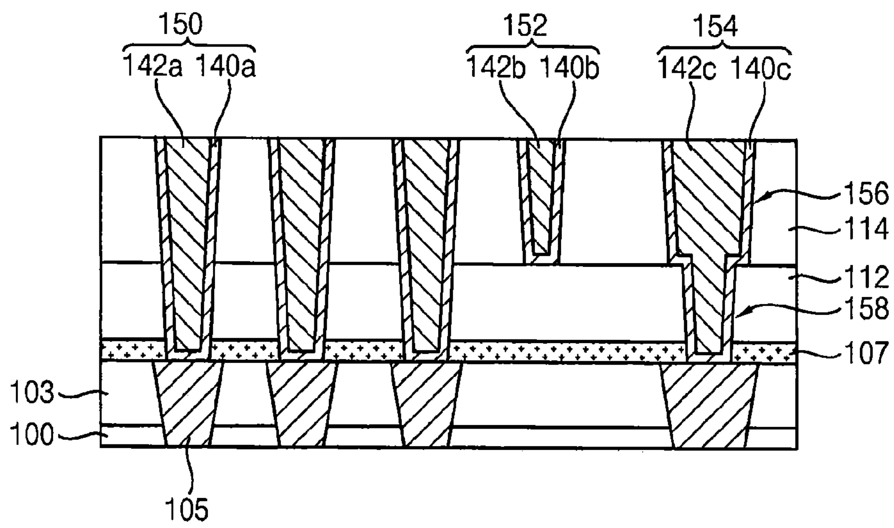


FIG. 19

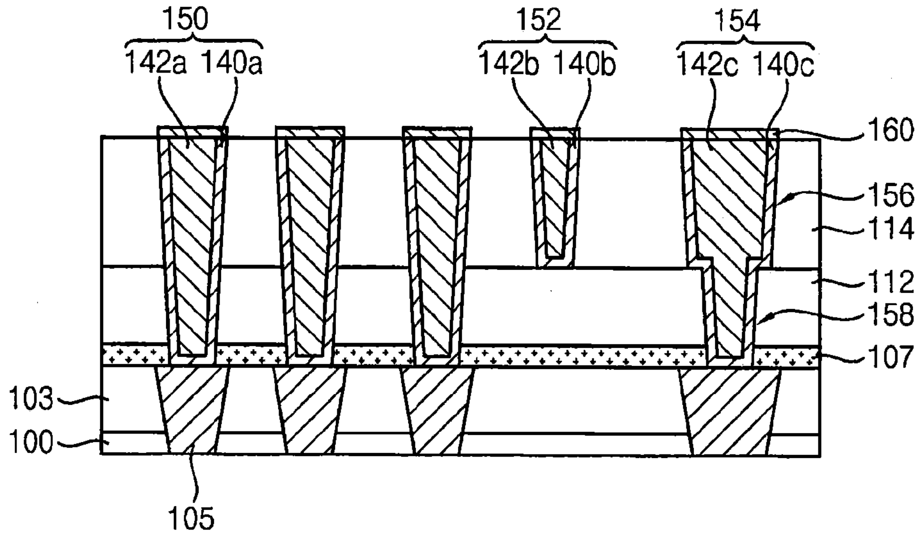


FIG. 20

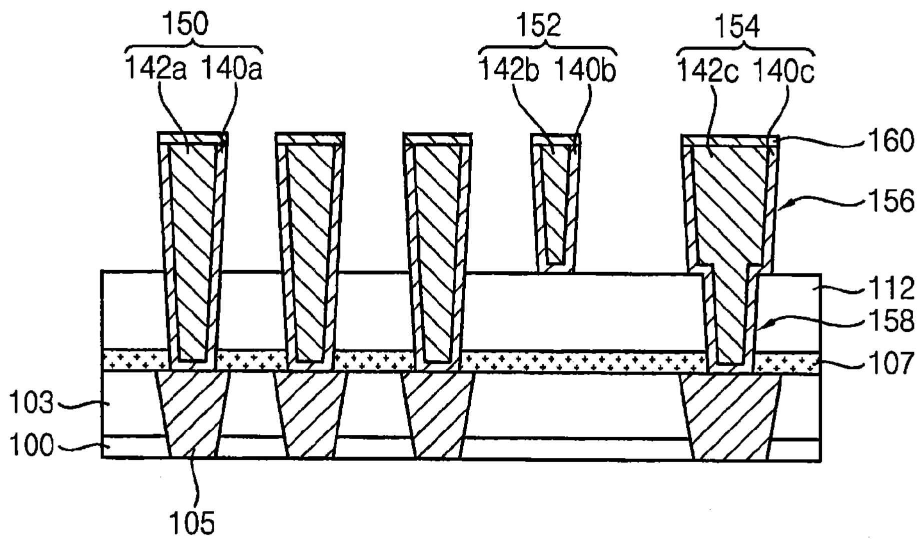


FIG. 21

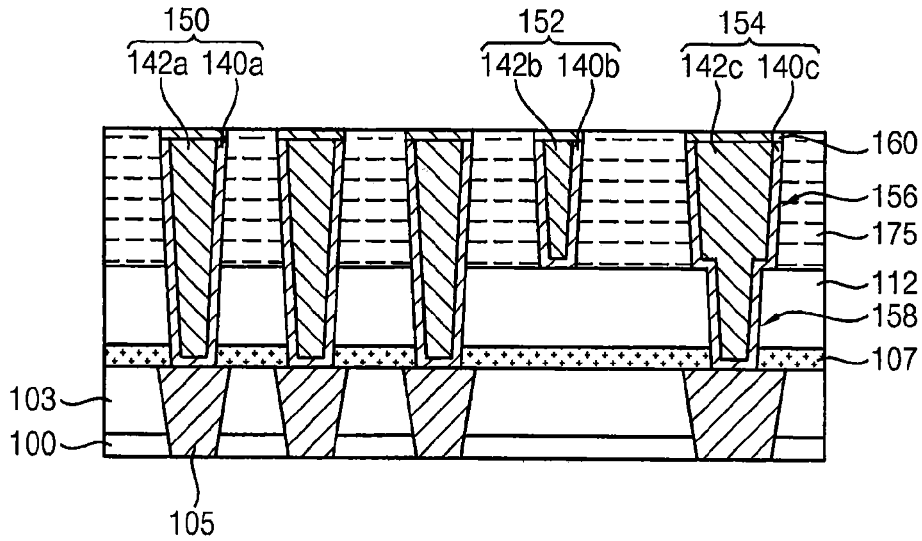


FIG. 22

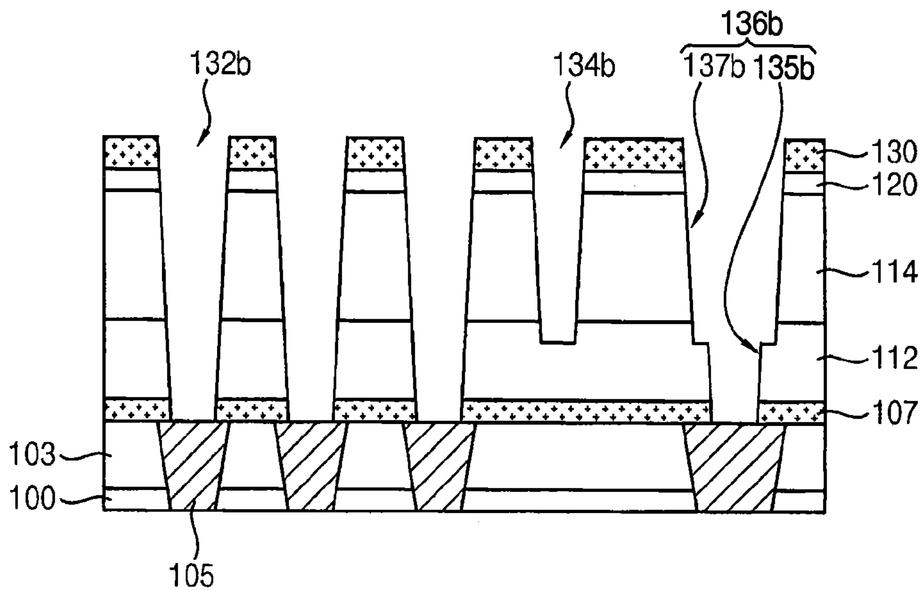


FIG. 23

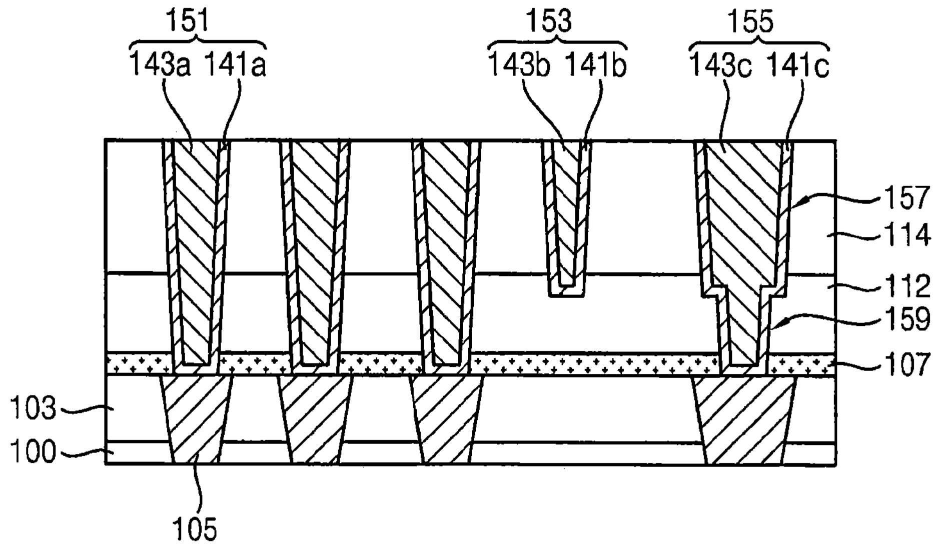


FIG. 24

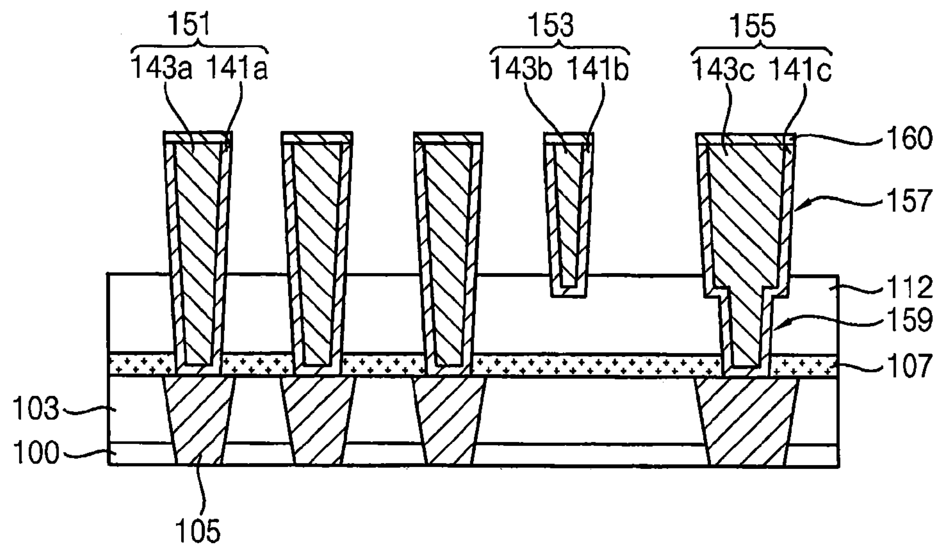


FIG. 25

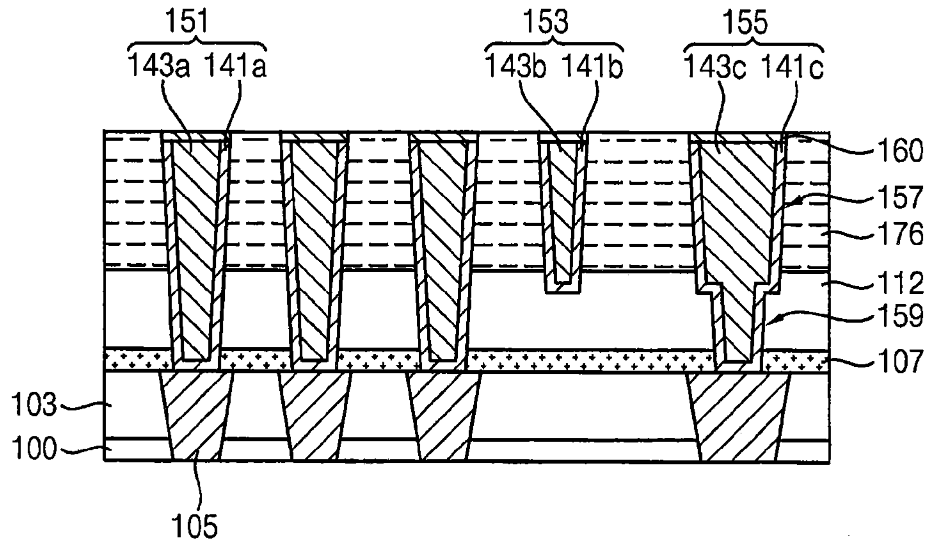


FIG. 26

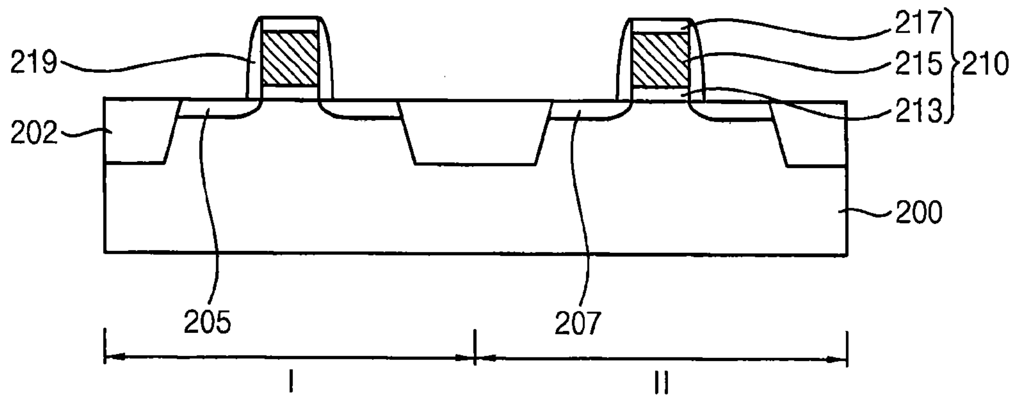


FIG. 27

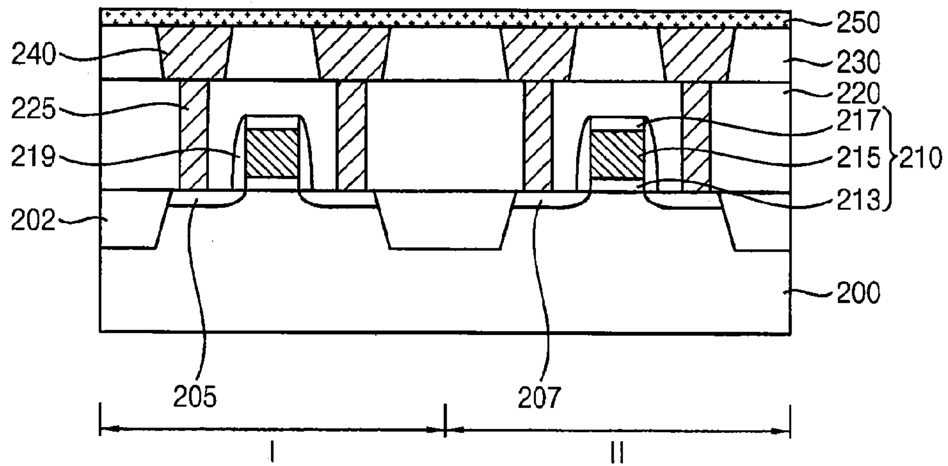


FIG. 28

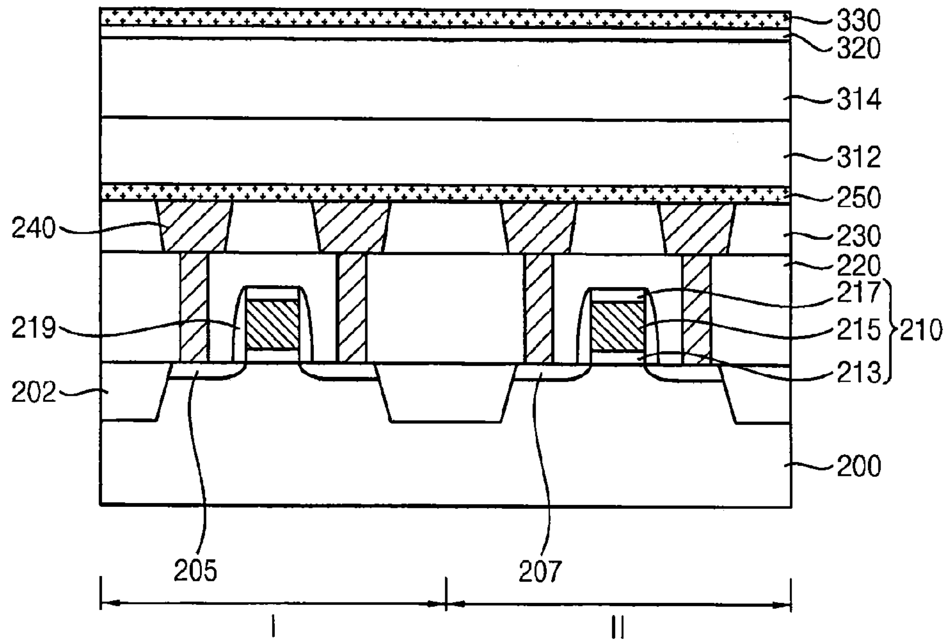


FIG. 29

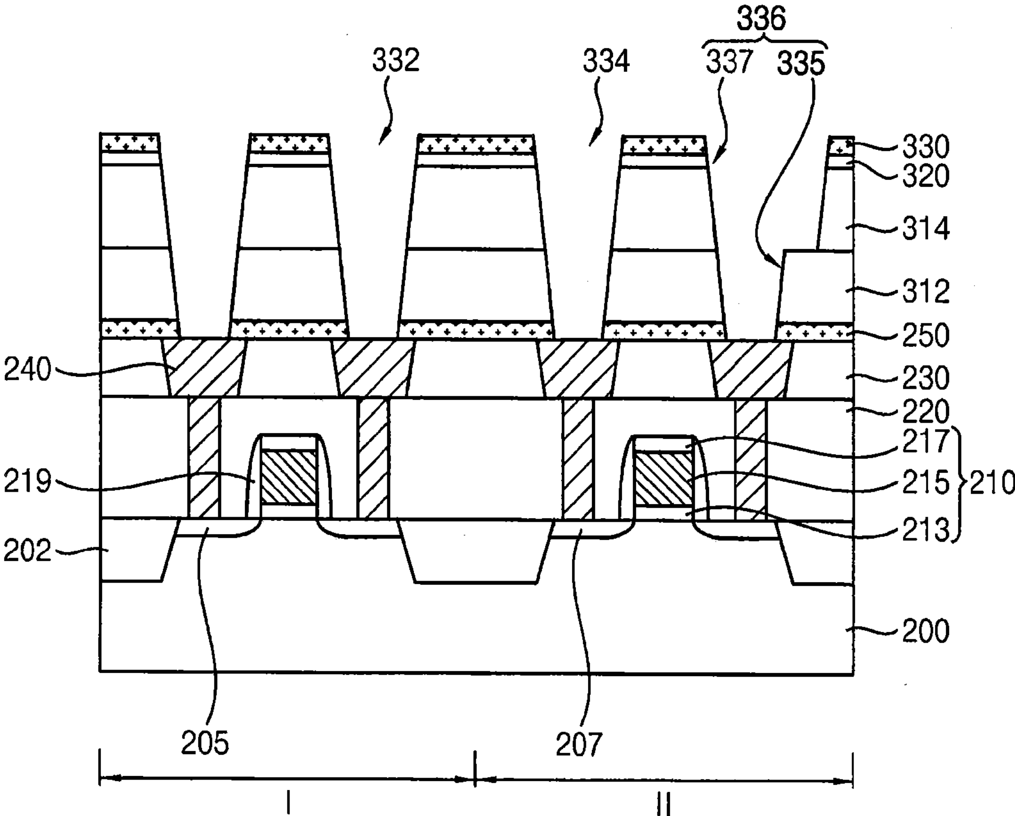


FIG. 30

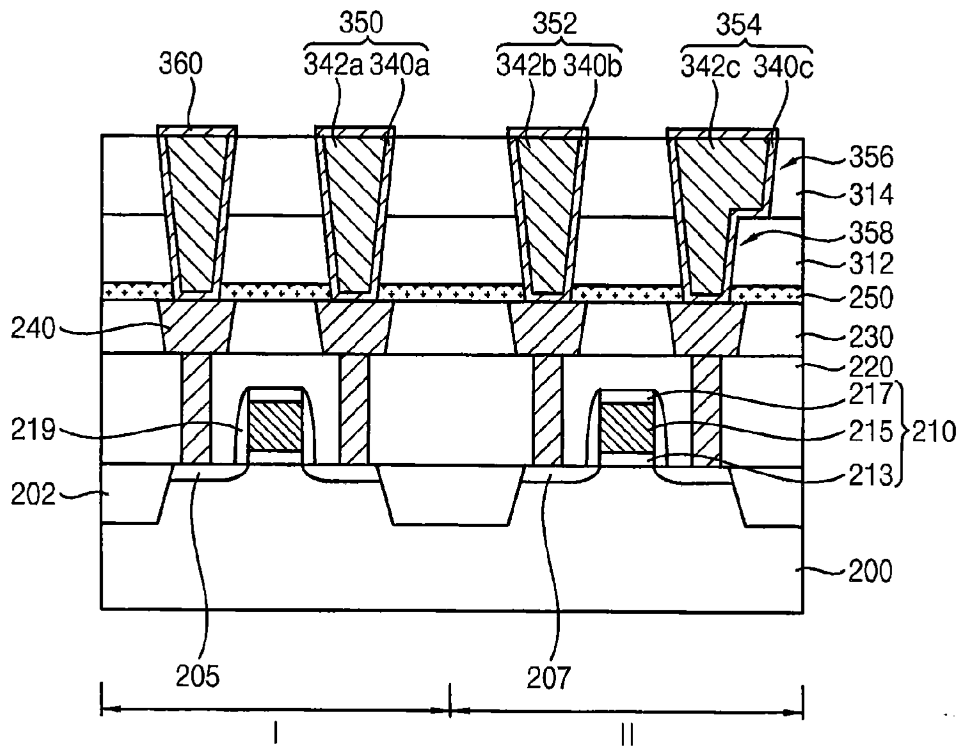


FIG. 31

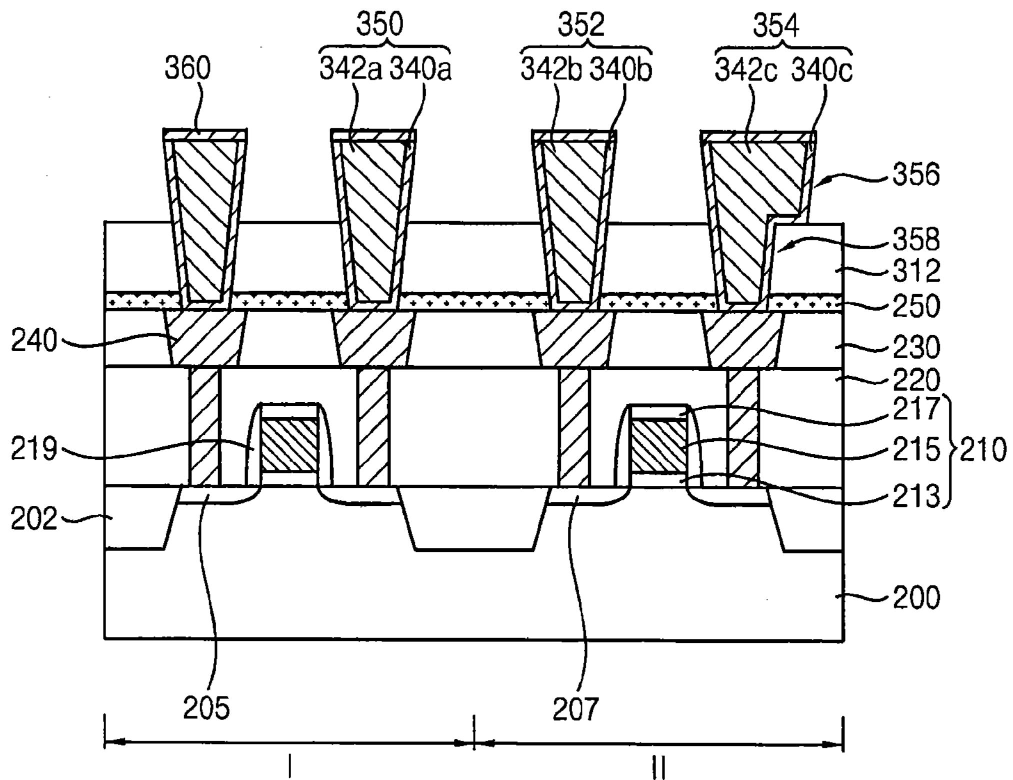


FIG. 32

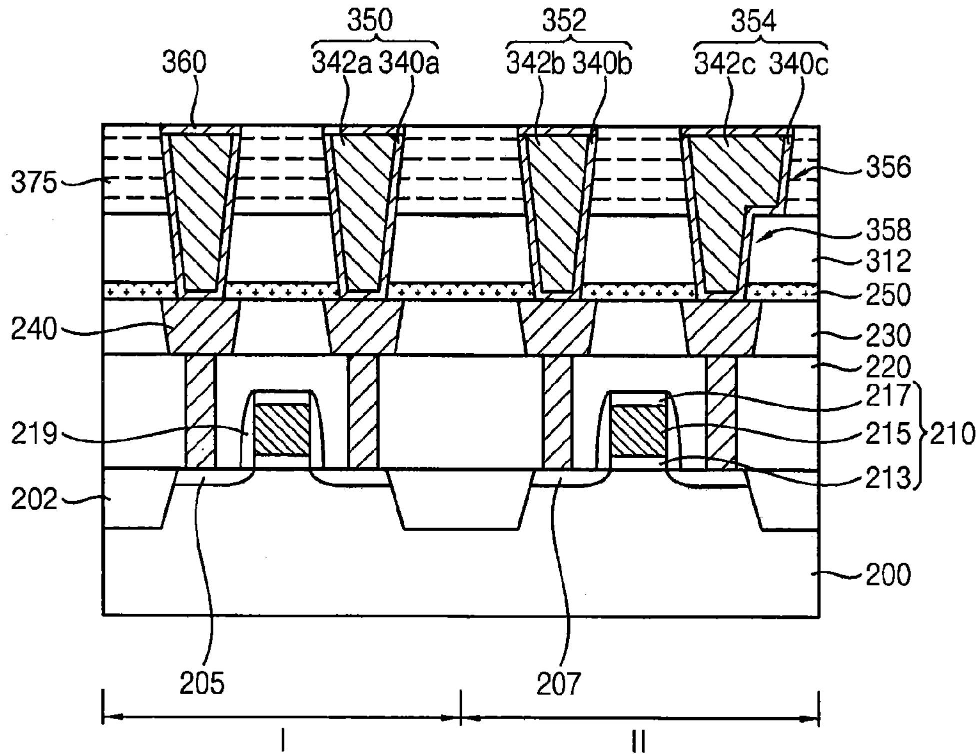


FIG. 33

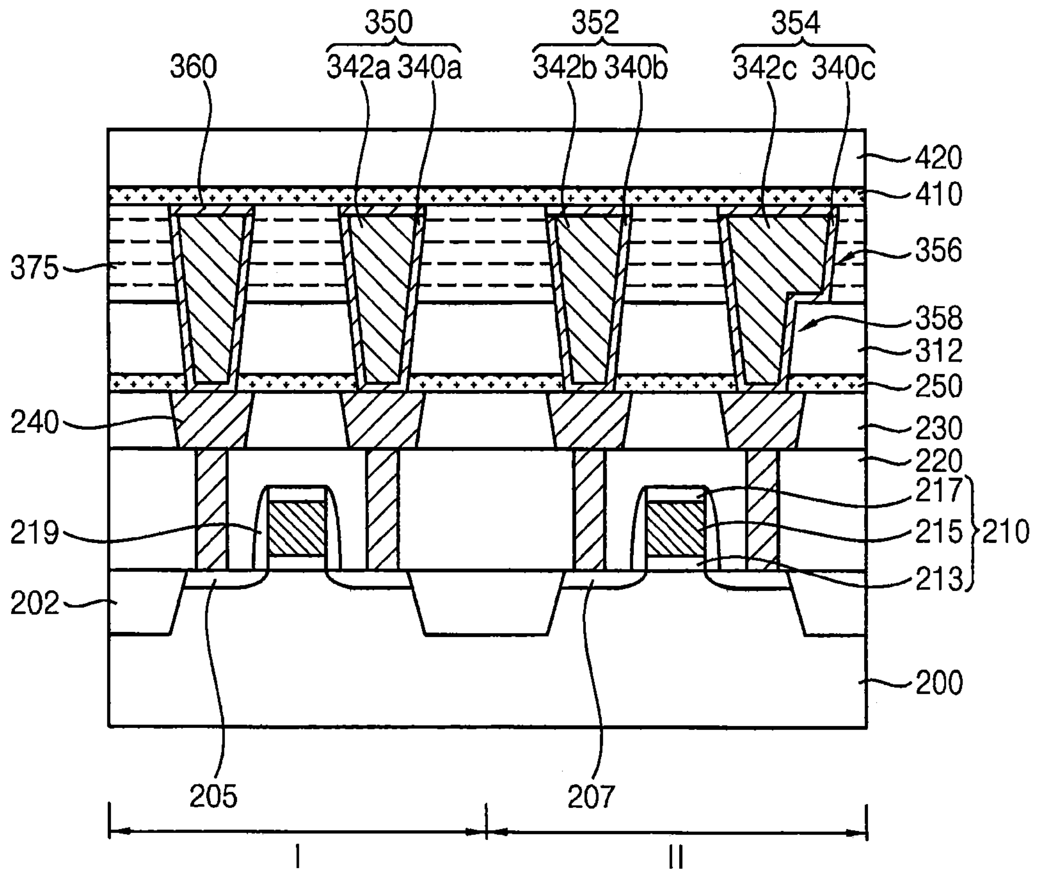


FIG. 34

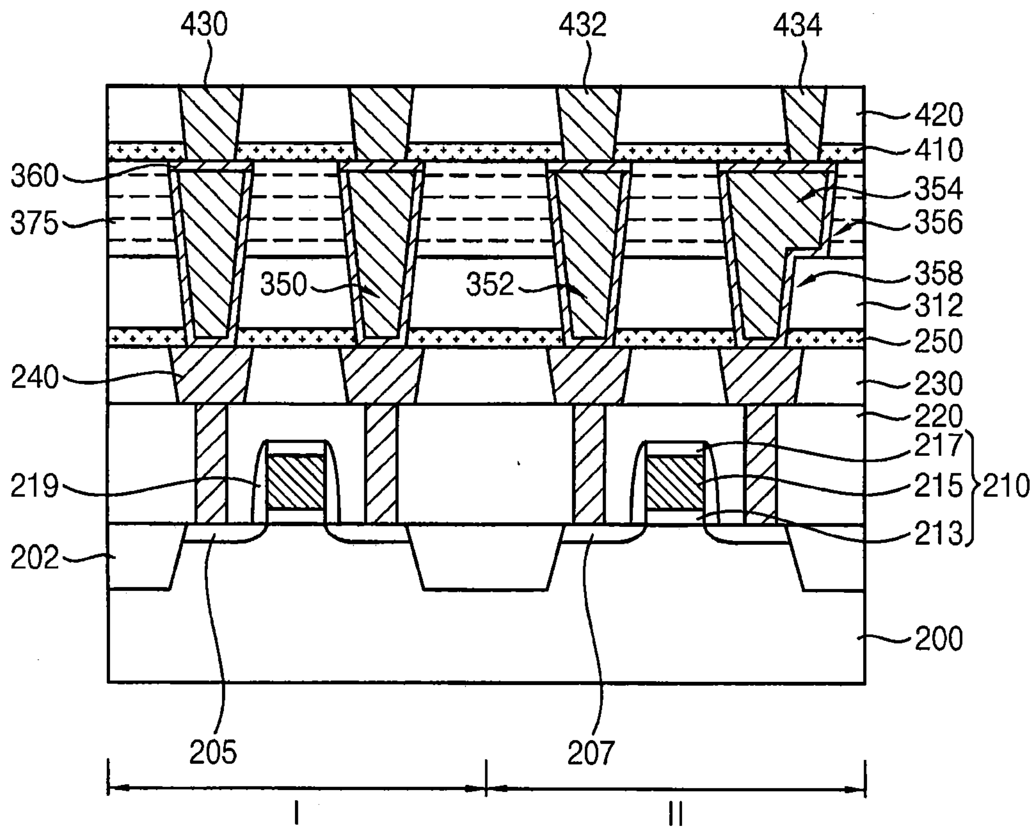
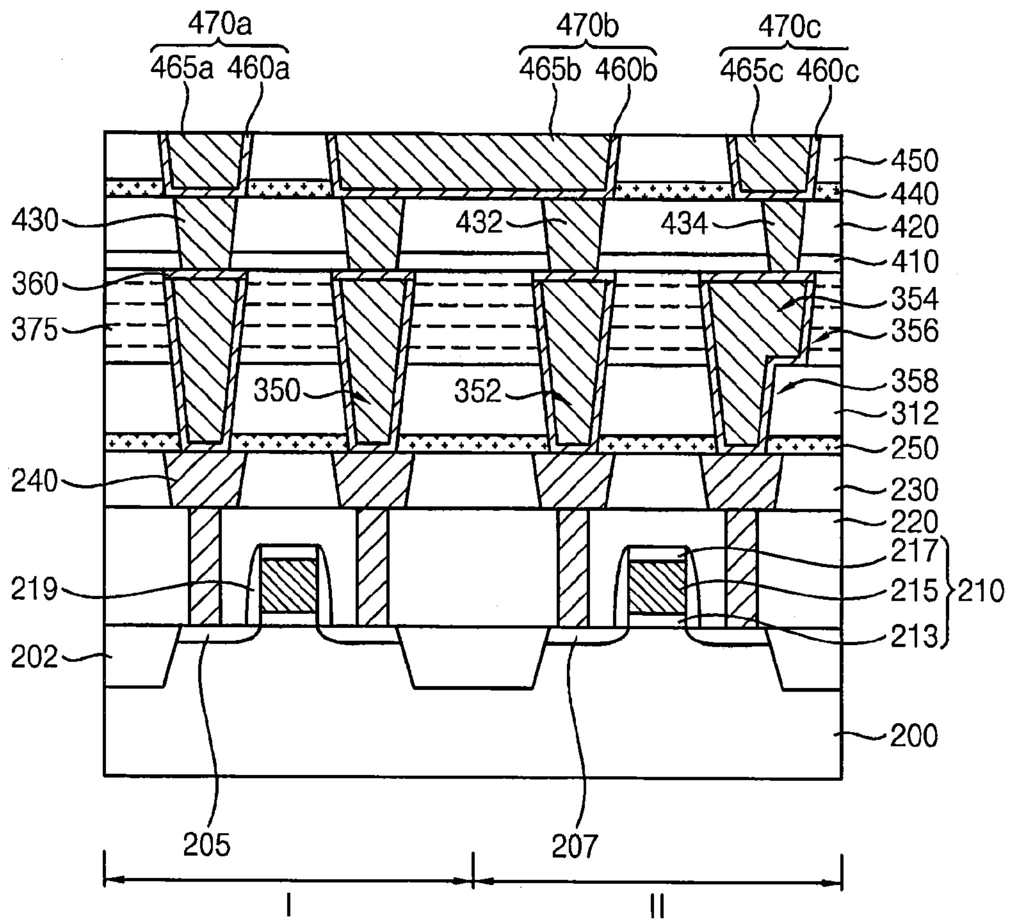


FIG. 35



METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES INCLUDING CONDUCTIVE STRUCTURES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 USC §119 to Korean Patent Application No. 10-2014-0172618, filed on Dec. 4, 2014 in the Korean Intellectual Property Office (KIPO), the contents of which are incorporated by reference herein in their entirety.

FIELD

[0002] Embodiments relate to methods of forming conductive structures buried in a dielectric layer, semiconductor devices including the conductive structures and methods of manufacturing the semiconductor devices.

BACKGROUND

[0003] As a semiconductor device becomes highly integrated, distances between wiring patterns included in the semiconductor device decrease. Thus, a parasitic capacitance between the neighboring wiring patterns may increase, which may reduce the reliability of the semiconductor device.

[0004] Additionally, a low-k insulation layer adjacent to the wiring patterns may be damaged while performing, for example, an etching process or a thermal treatment for the formation of the wiring patterns, and thus the parasitic capacitance may be further increased by the damage to the low-k insulation layer.

SUMMARY

[0005] According to example embodiments, a method of forming a semiconductor device can include forming an insulation layer using a material having a composition selected to provide resistance to a subsequent etching process. The composition of the material can be changed to reduce the resistance of the material to the subsequent etching process at a predetermined level in the insulation layer. The subsequent etching process can be performed on the insulation layer to remove an upper portion of the insulation layer above the predetermined level and leave a lower portion of the insulation layer below the predetermined level between adjacent conductive patterns extending through the lower portion of the insulation layer. A low-k dielectric material can be formed on the lower portion of the insulation layer between the adjacent conductive patterns to replace the upper portion of the insulation layer above the predetermined level.

[0006] According to example embodiments, a method of forming a conductive structure can include forming a sacrificial layer including an inorganic insulative material on a lower contact by an in-situ deposition process, where the sacrificial layer can have a composition at a lower portion and a different composition at an upper portion thereof. A conductive pattern can be formed to extend through the sacrificial layer to electrically connect to the lower contact. The upper portion of the sacrificial layer can be removed such that the conductive pattern is exposed by the lower portion of the sacrificial layer and an insulating interlayer can be formed on the lower portion of the sacrificial layer to cover the conductive pattern.

[0007] According to example embodiments, a method of forming a conductive structure can include forming a supporting layer including a silicon oxide-based material on a lower contact and forming a sacrificial layer including silicon carboxide or carbon-doped silicon oxide on the supporting layer. A conductive pattern can be formed to extend through the sacrificial layer and electrically connect to the lower contact. The sacrificial layer can be removed to expose the conductive pattern above the supporting layer and an insulating interlayer can be formed on the supporting layer to cover the conductive pattern.

[0008] According to example embodiments, a method of manufacturing a semiconductor device can include forming a lower insulation layer covering a semiconductor element on a substrate and forming a lower circuit electrically connected to the semiconductor element through the lower insulation layer. A first etch-stop layer can be formed to cover the lower circuit on the lower insulation layer and a supporting layer can be formed to include a silicon oxide-based material on the first etch-stop layer. A sacrificial layer can including silicon carboxide or carbon-doped silicon oxide can be formed on the supporting layer. A conductive pattern can be formed electrically connected to the lower circuit through the sacrificial layer, the supporting layer and the first etch-stop layer. The sacrificial layer can be removed such that the conductive pattern can be exposed by the supporting layer and a first insulating interlayer can be formed to cover the conductive pattern.

[0009] According to example embodiments, a semiconductor device, can include a lower insulation layer on a substrate and a lower circuit in the lower insulation layer. A supporting layer can be on the lower insulation layer and the lower circuit, where the supporting layer can include a silicon-based inorganic material. An insulating interlayer can be on the supporting layer, where the insulating interlayer can have a density that is less than that of the supporting layer. A conductive pattern can extend through the insulating interlayer and the supporting layer to electrically connect to the lower circuit and a capping layer pattern can be on a top surface of the conductive pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Example embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings. FIGS. **1** to **35** represent non-limiting, example embodiments as described herein.

[0011] FIGS. **1** to **10** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments;

[0012] FIG. **11** is a graph showing a deposition source profile during a formation of a sacrificial layer in accordance with example embodiments;

[0013] FIGS. **12** to **14** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments;

[0014] FIGS. **15** to **21** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments;

[0015] FIGS. **22** to **25** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments; and

[0016] FIGS. **26** to **35** are cross-sectional views illustrating a method of manufacturing a semiconductor device in accordance with example embodiments.

DESCRIPTION OF EMBODIMENTS

[0017] Various example embodiments will be described more fully hereinafter with reference to the accompanying drawings, in which some example embodiments are shown. The present inventive concept may, however, be embodied in many different forms and should not be construed as limited to the example embodiments set forth herein. Rather, these example embodiments are provided so that this description will be thorough and complete, and will fully convey the scope of the present inventive concept to those skilled in the art. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity.

[0018] It will be understood that when an element or layer is referred to as being "on," "connected to" or "coupled to" another element or layer, it can be directly on, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present. Like numerals refer to like elements throughout. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0019] It will be understood that, although the terms first, second, third, fourth etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present inventive concept.

[0020] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0021] The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting of the present inventive concept. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0022] Example embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of idealized example embodiments (and intermediate structures). As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, example embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of the present inventive concept.

[0023] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this inventive concept belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0024] FIGS. **1** to **10** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments.

[0025] Referring to FIG. **1**, a lower contact **105** extending through a lower insulation layer **103** may be formed. A plurality of the lower contacts **105** may be formed in the lower insulation layer **103**.

[0026] In example embodiments, the lower insulation layer **103** may be formed on a passivation layer **100**, and a contact hole extending through the lower insulation layer **103** and the passivation layer **100** may be formed. The lower contact **105** may be formed by forming a conductive layer in the contact hole by a deposition process or a plating process.

[0027] The lower insulation layer **103** may be formed of an insulative material such as silicon oxide or silicon oxynitride. For example, the lower insulation layer **103** may be formed of a silicon oxide-based material such as plasma enhanced oxide (PEOX), tetraethyl orthosilicate (TEOS), boro tetraethyl orthosilicate (BTEOS), phosphorous tetraethyl orthosilicate (PTEOS), boro phospho tetraethyl orthosilicate (BPTEOS), boro silicate glass (BSG), phospho silicate glass (PSG), boro phospho silicate glass (BPSG), or the like.

[0028] The passivation layer **100** may be formed of silicon nitride. The conductive layer may be formed of a metal such as aluminum (Al), tungsten (W) or copper (Cu), or a metal nitride.

[0029] In some embodiments, the lower contact **105** may be electrically connected to a circuit device or a lower wiring formed on a semiconductor substrate. Damages to the circuit device or the lower wiring while forming the contact hole may be prevented by the passivation layer **100**.

[0030] A first etch-stop layer **107** covering the lower contacts **105** may be formed on the lower insulation layer **103**. The first etch-stop layer **107** may be formed of silicon nitride, silicon oxynitride, silicon carbonitride or a metal. The first etch-stop layer **107** may be formed as a single layer including one of the materials, or as a multi-layered structure including at least two of the materials.

[0031] For example, the first etch-stop layer **107** may be formed by a at least one process of a chemical vapor deposition (CVD) process, a plasma enhanced chemical vapor deposition (PECVD) process, a low pressure chemical vapor deposition (LPCVD) process, a high density plasma chemical vapor deposition (HDP-CVD) process, a spin coating process, a sputtering process, an atomic layer deposition (ALD) process, and a physical vapor deposition (PVD) process.

[0032] Referring to FIG. **2**, a sacrificial layer **110**, a buffer layer **120** and a second etch-stop layer **130** may be sequentially formed on the first etch-stop layer **107**.

[0033] In example embodiments, the sacrificial layer **110** may be formed of a silicon oxide-based material doped with carbon. For example, the sacrificial layer **110** may be formed of a silicon oxide-based material including hydrocarbon groups such as alkyl groups. In some embodiments, the sacrificial layer **110** may be formed of a TEOS-based silicon oxide including, for example, TEOS, BTEOS, PTEOS or BPTEOS, or polysiloxane including alkyl substituents.

[0034] In some embodiments, the sacrificial layer **110** may be substantially formed of silicon carboxide (SiOC or SiOC:H).

[0035] In example embodiments, the sacrificial layer **110** may have different compositions at an upper portion and a lower portion thereof. For example, a carbon amount or concentration at the upper portion of the sacrificial layer **110** (adjacent the buffer layer **120**) may be greater than a carbon amount or concentration at the lower portion of the sacrificial layer **110** (adjacent the first etch-stop layer **107**). In some embodiments, the lower portion of the sacrificial layer **110** may include silicon oxide substantially devoid of carbon, and the upper portion of the sacrificial layer **110** may include silicon oxide doped or combined with carbon. Accordingly, a layer density at the upper portion of the sacrificial layer **110** may be less than a layer density at the lower portion of the sacrificial layer **110**.

[0036] An adjustment of the composition of the sacrificial layer **110** is described in further detail with reference to FIG. **11**.

[0037] The buffer layer **120** may be formed of, e.g., silicon oxynitride. The second etch-stop layer **130** may be formed as a single-layered or multi-layered structure including silicon nitride, silicon carbonitride, silicon oxynitride and/or a metal. A stress from the second etch-stop layer **130** may be absorbed or alleviated by the buffer layer **120**.

[0038] The sacrificial layer **110**, the buffer layer **120** and the second etch-stop layer **130** may be formed by a CVD process, a PECVD process, a sputtering process such as an ion-beam sputtering, a spin coating process, or the like.

[0039] Referring to FIG. **3**, the second etch-stop layer **130**, the buffer layer **120** and the sacrificial layer **110** may be sequentially and partially etched to form openings.

[0040] For example, a photoresist layer may be formed on the second etch-stop layer **130**, and then the photoresist layer may be partially removed by exposure and developing processes to form a mask pattern. The second etch-stop layer **130**, the buffer layer **120** and the sacrificial layer **110** may be partially removed by, e.g., a dry etching process using the mask pattern to form the openings. The buffer layer **120** may also serve as an anti-reflective layer while performing the exposure process.

[0041] In some embodiments, the mask pattern may be formed using a carbon-based or silicon-based spin on hardmask (SOH) material, or a silicon oxynitride-based hardmask material.

[0042] In example embodiments, the openings may include a first opening **132**, a second opening **134** and a third opening **136**.

[0043] In some embodiments, the first openings **132** may extend through the sacrificial layer **110** and the first etch-stop layer **107** to expose the lower contact **105**. The second opening **134** may extend through an upper portion of the sacrificial layer **110**, and may not extend to a top surface of the first etch-stop layer **107**. For example, the second opening **134** may have a trench shape formed at the upper portion of the sacrificial layer **110**.

[0044] The third opening **136** may extend through the sacrificial layer **110** and the first etch-stop layer **107** to expose the lower contact **105**, and may have a non-linear (or stepped) sidewall profile. For example, the third opening **136** may be formed by a dual damascene process. Accordingly, the third opening **136** may include a via hole **135** through which the lower contact **105** is exposed, and a trench **137** connected to an upper portion of the via hole **135**.

[0045] In some embodiments, the via hole **135** extending through the sacrificial layer **110** and the first etch-stop layer **107** may be formed substantially together with the first opening **132**, and a portion of the sacrificial layer **110** adjacent to an upper portion of the via hole **135** may be further etched to form the trench **137** having a width expanded from a width of the via hole **135**.

[0046] For example, the second opening **134** and the trench **137** may be formed, and then the second opening **134** may be covered by a mask such that a portion of the trench **134** and a region in which the first opening **132** is formed may be exposed by the mask. Next, the first opening **132** and the via hole **135** under the trench **137** may be formed by etching the sacrificial layer **110** exposed by the mask. The trench **137** may be merged with the via hole **135**.

[0047] After the formation of the openings, the mask pattern may be removed by an ashing process and/or a strip process.

[0048] Referring to FIG. **4**, a conductive layer filling the openings may be formed on the second etch-stop layer **130**.

[0049] In example embodiments, a barrier layer **140** may be formed conformally along a top surface of the second etch-stop layer **130**, and sidewalls and bottoms of the first to third openings **134**, **134** and **136**. A conductive layer **142** sufficiently filling the first to third openings **132**, **134** and **136** may be formed on the barrier layer **140**.

[0050] The barrier layer **140** may be formed of a metal nitride such as titanium nitride (TiNx) or tungsten nitride (WNx). The barrier layer **140** may prevent a metal ingredient included in the conductive layer **142** from being diffused into the sacrificial layer **110**. The barrier layer **140** may also provide an adhesion for the formation of the conductive layer **142**. The barrier layer **140** may be formed by, e.g., a sputtering process or an ALD process.

[0051] The conductive layer **142** may be formed by, e.g., an electroplating process. In this case, a seed layer may be formed conformally on the barrier layer **140** by a sputtering process using a copper target. A plating solution such as a copper sulfate solution may be prepared, and a current may be applied using the seed layer and the plating solution as a cathode and an anode, respectively. Thus, the conductive

layer **142** including copper may be grown or precipitated on the seed layer through an electrochemical reaction.

[0052] In some embodiments, an annealing process may be further performed after performing the electroplating process so that a chemical structure in the conductive layer **142** may be stabilized.

[0053] In some embodiments, the conductive layer **142** may be formed by a sputtering process using a metal target such as copper, tungsten or aluminum, or an ALD process.

[0054] Referring to FIG. **5**, upper portions of the conductive layer **142** and the barrier layer **140** may be planarized to form conductive patterns.

[0055] In example embodiments, the upper portions of the conductive layer **142** and the barrier layer **140** may be planarized by, e.g., a chemical mechanical polish (CMP) process until a top surface of the sacrificial layer **110** is exposed. The second etch-stop layer **130** and the buffer layer **120** may be also removed by the planarization process.

[0056] Accordingly, a first conductive pattern **150**, a second conductive pattern **152** and a third conductive pattern **154** may be formed in the first opening **132**, the second opening **134** and the third opening **136**, respectively.

[0057] The first conductive pattern **150** may include a first barrier layer pattern **140*a*** and a first conductive layer pattern **142*a***, the second conductive pattern **152** may include a second barrier layer pattern **140*b*** and a second conductive layer pattern **142*b***, and the third conductive pattern **154** may include a third barrier layer pattern **140*c*** and a third conductive layer pattern **142*c***.

[0058] The first and third conductive patterns **150** and **154** may extend through the sacrificial layer **110** and the first etch-stop layer **107** to be in contact with the respective lower contacts **105**. The second conductive pattern **152** may be buried in the upper portion of the sacrificial layer **110** and may not contact a lower contact **105**.

[0059] The third conductive pattern **154** may have a non-linear (or stepped) sidewall profile. For example, a lower portion of the third conductive pattern **154** may be defined as a via portion **158**, and an upper portion of the third conductive pattern **154** may be defined as an expanded portion **156** having a width greater than that of the via portion **158**. For example, the expanded portion **156** may be integral with the via portion **158** (to form a unitary structure), and may extend laterally.

[0060] A stepped surface at which the sidewall profile of the third conductive pattern **154** may be non-linearly changed may be defined to be at a boundary between the via portion **158** and the expanded portion **156**.

[0061] In some embodiments, a cleaning process may be further performed to remove a metal residue on the top surface of the sacrificial layer **110**. In some embodiments, an ashing process may be further performed to remove the second etch-stop layer **130** and the buffer layer **120**.

[0062] Referring to FIG. **6**, a capping layer pattern **160** covering an upper surface of each conductive pattern may be formed.

[0063] The capping layer pattern **160** may include a metal which may be more chemically stable than the metal included in the first to third conductive patterns **150**, **152** and **154** and may be formed by, e.g., a sputtering process or an ALD process. For example, the capping layer pattern **160** may be formed using cobalt (Co) or molybdenum (Mo). The capping layer pattern **160** may be formed of a nitride of the metal.

[0064] In example embodiments, while performing a deposition process using, e.g., cobalt or cobalt nitride, the capping layer pattern **160** may be substantially self-aligned or self-assembled with the first to third conductive patterns **150**, **152** and **154** due to an affinity between metallic materials. Thus, the capping layer pattern **160** covering the first to third conductive patterns **150**, **152** and **154** may be formed without an additional etching process.

[0065] In some embodiments, the capping layer pattern **160** may fully cover the upper surface of each of the first to third conductive patterns **150**, **152** and **154**, and may partially cover the top surface of the sacrificial layer **110**. In some embodiments, an upper surface of the capping layer pattern **160** may have a curved shape or a dome shape due to properties of the self-aligned or self-assembled metallic materials

[0066] In some embodiments, before the formation of the capping layer pattern **160**, upper portions of the conductive patterns **150**, **152** and **154** may be partially removed by, e.g., an etch-back process to form recesses. In this case, the capping layer pattern **160** may fill each recess.

[0067] Referring to FIG. **7**, an upper portion of the sacrificial layer **110** may be removed such that upper portions of the first to third conductive patterns **150**, **152** and **154** may be exposed.

[0068] In some embodiments, the upper portion of the sacrificial layer **110** may be removed by a wet etching process using, e.g., a hydrofluoric acid solution or a buffer oxide etchant (BOE) solution. In some embodiments, the upper portion of the sacrificial layer **110** may be removed by an ashing process, a dry etching process using a fluoro hydrocarbon gas such as CF_4, CHF_3, or CH_2F_2, or a plasma etching process. In some embodiments, the removal process is defined to be one that is configured to selectively etch the sacrificial layer based on the concentration of carbon in the sacrificial layer **110**.

[0069] As described above, the sacrificial layer **110** may have different compositions at the upper and lower portions thereof. For example, the upper portion of the sacrificial layer **110** may have a carbon amount (or concentration) greater than that in the lower portion. In this case, the upper portion of the sacrificial layer **110** may be easily damaged by various processes used to form the conductive patterns **150**, **152** and **154** including CMP, annealing, cleaning and/or ashing processes. For example, carbon ingredients included in the upper portion of the sacrificial layer **110** may be substantially combusted so that chemical structures therein may be damaged.

[0070] Therefore, the upper portion of the sacrificial layer **110** may be selectively removed by the wet etching process or the dry etching process.

[0071] The remaining lower portion of the sacrificial layer **110** may be defined as a supporting layer **115**.

[0072] In some embodiments, while removing the upper portion of the sacrificial layer **110**, a bottom of the second conductive pattern **152** and/or the stepped surface of the third conductive pattern **154** may substantially serve as an etching end-point. In this case, the second conductive pattern **152** may be disposed on a top surface of the supporting layer **115**, and the via portion **158** of the third conductive pattern **154** may be buried in the supporting layer **115**.

[0073] Thus, bending or leaning of the first to third conductive patterns **152**, **154** and **156** may be prevented by the supporting layer **115**. For example, a bottom of the expanded portion **156** included in the third conductive pattern **156** may

be in contact with the top surface of the supporting layer **115** so that a structural stability may be improved.

[0074] Referring to FIG. **8**, an insulating interlayer **170** covering (and between) the conductive patterns **150**, **152** and **154**, and the capping layer pattern **160** may be formed on the supporting layer **115**.

[0075] The insulating interlayer **170** may be formed of silicon oxide-based or siloxane-based materials having a low dielectric constant (low-k). For example, the insulating interlayer **170** may be formed of the silicon oxide-based material such as PEOX, TEOS, BTEOS, PTEOS, BPTEOS, BSG, PSG or BPSG.

[0076] In some embodiments, while performing a deposition process for the formation of the insulating interlayer **170**, a porogen material may be provided together with a reactive gas. Accordingly, the insulating interlayer **170** may have a net structure in which oxygen atoms and carbon atoms may be combined with silicon atoms.

[0077] In some embodiments, the insulating interlayer **170** may be formed by a flowable chemical vapor deposition (FCVD) process or an ALD process having an improved gap-fill property.

[0078] Referring to FIG. **9**, a modification treatment may be performed on the insulating interlayer **170** so that the insulating interlayer **170** may be converted into a modified insulating interlayer **175**.

[0079] For example, the modification treatment may include an ultraviolet (UV) irradiation or a plasma treatment. In this case, the porogen material combined or incorporated in the insulating interlayer **170** may be substantially removed so that pores may be created in the insulating interlayer **170**. Thus, the modified insulating interlayer **175** may have a porous structure including the pores therein. Therefore, the dielectric constant of the insulating interlayer may be further reduced.

[0080] In some embodiments, if the conductive patterns **150**, **152** and **154** are provided as uppermost wiring structures, an additional etching process or thermal treatment may not be performed so that etching damage of the insulating interlayer **170** may be avoided. Thus, a chemical structure of the insulating interlayer **170** may be intentionally modified by the above modification treatment so that a low-k insulation structure may be achieved.

[0081] Referring to FIG. **10**, an upper portion of the modified insulating interlayer **175** may be planarized by, e.g., a CMP process such that the capping layer pattern **160** may be exposed.

[0082] In some embodiments, top surfaces of the modified insulating interlayer **175** and the capping layer pattern **160** may be substantially coplanar with each other after the planarizing process. In some embodiments, the top surface of the modified insulating interlayer **175** may be lower than the top surface of the capping layer pattern **160** after the planarizing process.

[0083] According to example embodiments as described above, the sacrificial layer **110** may be formed, and then the conductive patterns **150**, **152** and **154** may be formed in the sacrificial layer **110**. A damaged upper portion of the sacrificial layer **110** may be removed, and a new insulating interlayer may be formed in a space from which the upper portion of the sacrificial layer **110** was removed. Thus, a low-k insulation structure free of an etching damage or a thermal damage may be formed between the conductive patterns **150**, **152** and **154**. Additionally, the compositions at upper and lower portions of the sacrificial layer **110** may be differentiated so that the upper portion of the sacrificial layer **110** may be selectively removed. The lower portion of the sacrificial layer **110** may remain to prevent the conductive patterns **150**, **152** and **154** from bending, leaning or collapsing.

[0084] In some embodiments, additional wiring structure may be formed on the conductive patterns **150**, **152** and **154**. In this case, the conductive patterns **150**, **152** and **154** may serve as an interconnection structure connecting upper and lower wirings to each other.

[0085] In some embodiments, as described above, the conductive patterns **150**, **152** and **154** may serve as the uppermost wiring structures.

[0086] FIG. **11** is a graph showing a deposition source profile during a formation of a sacrificial layer in accordance with example embodiments.

[0087] Referring to FIG. **11**, the structure illustrated in FIG. **1** may be loaded in a deposition process, and a deposition source may be introduced into the deposition chamber to form the sacrificial layer **110**.

[0088] The deposition source may include a silicon source, a reactive gas and a carbon source. The silicon source may include a silicon precursor such as silane (SiH_4), disilane (Si_2H_6) or dichlorosilane (SiH_2Cl_2). The reactive gas may include, e.g., oxygen (O_2), ozone (O_3), or the like. The carbon source may include methane (CH_4), ethane (C_2H_6), or the like.

[0089] At an initial phase (e.g., a phase I shown in FIG. **11**), a slight amount of the silicon source and the reactive gas may be introduced together so that a silicon oxide layer may be formed on the first etch-stop layer **107**. After a specific period (e.g., from a phase II), an amount of the silicon source may be gradually increased to form a transition layer. After the formation of the transition layer, a flow rate of the silicon source may be steadily maintained. A flow rate of the reactive gas may be steadily maintained from the initial phase.

[0090] At a time Tc (e.g., at the beginning of phase III), the carbon source may be first initiated. Accordingly, carbon may be doped in the silicon oxide layer, or silicon carboxide may be created so that the sacrificial layer **110** may be formed.

[0091] In some embodiments, after the time Tc, flow rates of the silicon source, the reactive gas and the carbon source may be constantly and uniformly provided.

[0092] In some embodiments, an introduction of the carbon source may be initiated together with the reactive gas, and the flow rate of the carbon source may be gradually increased. In this case, a carbon concentration in the sacrificial layer **110** may be increased from a lower portion to an upper portion.

[0093] As described above, the time at which the carbon source may be introduced may be controlled, so that the composition of the sacrificial layer **110** may be adjusted at the lower and upper portions thereof. Further, a thickness or a height of the upper portion that may be removed may be controlled by an adjustment of the time Tc.

[0094] FIGS. **12** to **14** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments. Detailed descriptions on processes and/or materials substantially the same as or similar to those illustrated with reference to FIGS. **1** to **10** may be omitted herein.

[0095] Referring to FIG. **12**, processes substantially the same as or similar to FIGS. **1** to **6** may be performed.

[0096] In example embodiments, a sacrificial layer **110** covering a lower insulation layer **103** and lower contacts **105**

may be formed on a first etch-stop layer **107**, and first to third conductive patterns **150**, **152** and **154** may be formed in the sacrificial layer **110**. The first and third conductive patterns **150** and **154** may be formed through the sacrificial layer **110** and the first etch-stop layer **107** to be in contact with the respective lower contacts **105**. The second conductive pattern **152** may be buried in an upper portion of the sacrificial layer **110** so as not to contact the lower contact **105**. The third conductive pattern **154** may include a via portion **158** and an expanded portion **156**. A capping layer pattern **160** covering an upper surface of each of the conductive patterns **150**, **152** and **154** may be formed.

[0097] Referring to FIG. **13**, a process substantially similar to that illustrated with reference to FIG. **7** may be performed. In example embodiments, an upper portion of the sacrificial layer **110** may be removed such that upper portions of the first to third conductive patterns **150**, **152** and **154** may be exposed. A remaining portion of the sacrificial layer **110** may be defined as a supporting layer **117**.

[0098] In example embodiments, a lower portion of the second conductive pattern **152**, the via portion **158** of the third conductive pattern **154**, and a lower portion of the expanded portion **156** may be buried in the supporting layer **117**. In this case, the sacrificial layer **110** may be removed such that a bottom of the second conductive pattern **152** and/or a stepped surface of the third conductive pattern **154** may not be exposed. Thus, an upper surface of the supporting layer **117** may be higher than the bottom of the second conductive pattern **152** and/or the stepped surface of the third conductive pattern **154**.

[0099] Accordingly, the second conductive pattern **152** and the expanded portion **156** of the third conductive pattern **154** may be partially buried in the supporting layer **117**. Therefore, a structural stability of the second conductive pattern **152** and the third conductive pattern **154** may be further improved.

[0100] Referring to FIG. **14**, a process substantially the same as or similar to that illustrated with reference to FIG. **8** may be performed. Thus, an insulating interlayer **172** covering (and between) the conductive patterns **150**, **152** and **154**, and the capping layer pattern **160** may be formed on the supporting layer **117**.

[0101] Subsequently, as illustrated with reference to FIGS. **9** and **10**, the insulating interlayer **172** may be converted into a modified insulating interlayer through a modification treatment. The modified insulating interlayer may be planarized until the capping layer pattern **160** may be exposed.

[0102] FIGS. **15** to **21** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments. Detailed descriptions on processes and/or materials substantially the same as or similar to those illustrated with reference to FIGS. **1** to **10** may be omitted herein.

[0103] Referring to FIG. **15**, and as also illustrated with reference to FIG. **1**, a lower insulation layer **103** may be formed on the passivation layer **100**, and lower contacts **105** extending through the lower insulation layer **103** and the passivation layer **100** may be formed. A first etch-stop layer **107** covering the lower contacts **105** may be formed on the lower insulation layer **103**.

[0104] Referring to FIG. **16**, a supporting layer **112** and a sacrificial layer **114** may be sequentially formed on the first etch-stop layer **107**. A buffer layer **120** and a second etch-stop layer **130** may be sequentially formed on the sacrificial layer **114**.

[0105] In example embodiments, the supporting layer **112** may be formed of a low-k silicon oxide-based or siloxane-based material. The sacrificial layer **114** may be formed of silicon oxide doped with carbon or silicon carboxide.

[0106] In some embodiments, the supporting layer **112** and the sacrificial layer **114** may be formed in-situ in a deposition chamber for a CVD process or an ALD process. For example, as illustrated in FIG. **11**, a silicon source and a reactive gas may be provided in the deposition chamber to form the supporting layer **112** substantially including silicon oxide.

[0107] A time at which the formation of the supporting layer **112** is completed may be set as a time Tc, and a carbon source may be provided after the time Tc. Thus, the sacrificial layer **114** substantially including silicon carboxide or silicon oxide doped with carbon may be obtained.

[0108] Referring to FIG. **17**, a process substantially the same as or similar to that illustrated with reference to FIG. **3** may be performed to form first to third openings **132*a***, **134*a*** and **136*a***.

[0109] In example embodiments, the first and third openings **132*a*** and **136*a*** may extend through the second etch-stop layer **130**, the buffer layer **120**, the sacrificial layer **114**, the supporting layer **112** and the first etch-stop layer **107**. A top surface of the lower contact **105** may be exposed through the first and third openings **132*a*** and **136*a***.

[0110] The second opening **134*a*** may extend through the second etch-stop layer **130**, the buffer layer **120** and the sacrificial layer **114**. A top surface of the supporting layer **112** may be exposed through second opening **134*a***.

[0111] The third opening **136*a*** may include a via hole **135*a***, and a trench **137*a*** expanded from an upper portion of the via hole **135*a***. In example embodiments, a boundary between the via hole **135*a*** and the trench **137** may be defined substantially by the top surface of the supporting layer **112**.

[0112] In example embodiments, the top surface of the supporting layer **112** may substantially serve as an etch-stop surface while performing an etching process for the formation of the second opening **134*a*** and the trench **137*a***. For example, a plasma etching process may be performed for the formation of the second opening **134*a*** and the trench **137*a***. The sacrificial layer **114** having a relatively great amount of carbon may be easily damaged and etched by the plasma etching process. Thus, the etching process may be performed until the supporting layer **112** which may have a relatively small amount of carbon, or may be substantially carbon-free is exposed.

[0113] Referring to FIG. **18**, processes substantially the same as or similar to those illustrated with reference to FIGS. **4** and **5** may be performed.

[0114] Accordingly, a first conductive pattern **150**, a second conductive pattern **152** and a third conductive pattern **154** may be formed in the first opening **132*a***, the second opening **134*a*** and the third opening **136*a***, respectively. The first conductive pattern **150** may include a first barrier layer pattern **140*a*** and a first conductive layer pattern **142*a***. The second conductive pattern **152** may include a second barrier layer pattern **140*b*** and a second conductive layer pattern **142*b***. The third conductive pattern **154** may include a third barrier layer pattern **140*c*** and a third conductive layer pattern **142*c***.

[0115] In example embodiments, the first conductive pattern **150** and the third conductive pattern **154** may extend

through the sacrificial layer **114**, the supporting layer **112** and the first etch-stop layer **107** to be in contact with the respective lower contact **105**. The second conductive pattern **152** may extend through the sacrificial layer **114**, and may be in contact with the top surface of the supporting layer **112**. For example, the second conductive pattern **152** may be landed on the top surface of the supporting layer **112**.

[0116] The third conductive pattern **154** may include a via portion **158** and an expanded portion **156**. A stepped surface between the via portion **158** and the expanded portion **156** may be defined by the top surface of the supporting layer **112**.

[0117] Referring to FIG. **19**, a process substantially the same as or similar to that illustrated with reference to FIG. **6** may be performed to form a capping layer pattern **160** covering a top surface of each conductive pattern **150**, **152** and **154**.

[0118] Referring to FIG. **20**, the sacrificial layer **114** may be removed such that upper portions of the conductive patterns **150**, **152** and **154** may be exposed. After the removal of the sacrificial layer **114**, the top surface of the supporting layer **112** may be also exposed.

[0119] For example, the sacrificial layer **114** may be removed by an ashing process, a dry etching process using a fluoro hydrocarbon gas such as CF_4, CHF_3, or CH_2F_2, a plasma etching process, or a wet etching process using hydrofluoric acid solution or a BOE solution. The sacrificial layer **114** may be damaged during the processes for the formation of the conductive patterns **150**, **152** and **154** and/or the capping layer pattern **160**, and thus may be easily removed.

[0120] In some embodiments, before the removal of the sacrificial layer **114**, a plasma treatment may be further performed on the sacrificial layer **114**. For example, a reductive reaction gas such as ammonia (NH_3), nitrogen (N_2) or hydrogen (H_2) may be used as part of a reductive plasma treatment of the sacrificial layer **114**.

[0121] In this case, carbon ingredients in the sacrificial layer **114** may be reduced so that an inner structure of the sacrificial layer **114** may be damaged. Thus, the sacrificial layer **114** may be removed more easily by the etching process.

[0122] As illustrated in FIG. **20**, the bottom of the second conductive pattern **152** may be supported by the top surface of the supporting layer **112**. The via portion **158** of the third conductive pattern **154** may be buried in the supporting layer **112** so that a structural stability of the third conductive pattern **154** may be enhanced.

[0123] Referring to FIG. **21**, processes substantially the same as or similar to those illustrated with reference to FIGS. **8** to **10** may be performed.

[0124] In example embodiments, an insulating interlayer covering the conductive patterns **150**, **152** and **154** may be formed, and the insulating interlayer may be converted into a modified insulating interlayer **175**. Accordingly, a dielectric constant of an insulation structure between the conductive patterns **150**, **152** and **154** may be further reduced. An upper portion of the modified insulating interlayer **175** may be planarized until a top surface of the capping layer pattern **160** is exposed.

[0125] FIGS. **22** to **25** are cross-sectional views illustrating a method of forming a conductive structure in accordance with example embodiments.

[0126] Detailed descriptions on processes and/or materials substantially the same as or similar to those illustrated with reference to FIGS. **1** to **10**, or FIGS. **15** to **21** may be omitted herein.

[0127] Referring to FIG. **22**, processes substantially the same as or similar to FIGS. **15** to **17** may be performed to form first to third openings **132*b***, **134*b*** and **136*b***.

[0128] The first opening **132*b*** may have a shape or a structure substantially the same as that of the first opening **132*a*** illustrated in FIG. **17**.

[0129] The second opening **134*b*** may extend through a second etch-stop layer **130**, a buffer layer **120** and a sacrificial layer **114**, and may extend in an upper portion of a supporting layer **112**.

[0130] The third opening **136*b*** may include a via hole **135*b*** and a trench **137*b***. The trench **137*b*** may extend through the second etch-stop layer **130**, the buffer layer **120** and the sacrificial layer **114**, and may extend in the upper portion of the supporting layer **112** to be integrally connected to the via hole **135*b***.

[0131] As described above, the upper portion of the supporting layer **112** may be additionally etched while forming the second opening **134*b*** and the trench **137*b*** such that heights of the second opening **134*b*** and the trench **137*b*** may be increased.

[0132] Referring to FIG. **23**, processes substantially the same as or similar to those illustrated with reference to FIGS. **4** and **5**, or FIG. **18** may be performed. Accordingly, a first conductive pattern **151**, a second conductive pattern **153** and a third conductive pattern **155** may be formed in the first opening **132*b***, the second opening **134*b*** and the third opening **136*b***, respectively.

[0133] The first conductive pattern **151** may include a first barrier layer pattern **141*a*** and a first conductive layer pattern **143*a***. The second conductive pattern **153** may include a second barrier layer pattern **141*b*** and a second conductive layer pattern **143*b***. The third conductive pattern **155** may include a third barrier layer pattern **141*c*** and a third conductive layer pattern **143*c***.

[0134] The first and third conductive patterns **151** and **155** may extend through the sacrificial layer **114**, the supporting layer **112** and a first etch-stop layer **107**, and may be in contact with lower contacts **105**.

[0135] The second conductive pattern **153** may extend through the sacrificial layer **114**, and may be partially inserted or buried in the upper portion of the supporting layer **112**.

[0136] The third conductive pattern **155** may include a via portion **159** and an expanded portion **157**. The via portion **159** may be buried in the supporting layer **112**. The expanded portion **157** may extend through the sacrificial layer **114**, and may extend through the upper portion of the supporting layer **112** to be integrally connected to the via portion **159**.

[0137] Referring to FIG. **24**, processes substantially the same as or similar to those illustrated with reference to FIGS. **19** and **20** may be performed. Accordingly, a capping layer pattern **160** covering each of the conductive patterns **151**, **153** and **155** may be formed, and the sacrificial layer **114** may be removed.

[0138] After the removal of the sacrificial layer **114**, upper portions of the conductive patterns **151**, **153** and **155**, and a top surface of the supporting layer **112** may be exposed. A lower portion of the second conductive pattern **153**, and the expanded portion **157** of the third conductive pattern **155** may be embedded in the supporting layer **112**, so that structural stability of the second and third conductive patterns **153** and **155** may be improved.

[0139] Referring to FIG. **25**, processes substantially the same as or similar to FIGS. **8** to **10**, or FIG. **21** may be performed.

[0140] In example embodiments, an insulating interlayer covering the conductive patterns **151**, **153** and **155** may be formed on the supporting layer **112**. The insulating interlayer may be converted into a modified insulating interlayer **176** through a modification treatment. Accordingly, a dielectric constant of an insulation structure between the conductive patterns **151**, **153** and **155** may be further reduced. An upper portion of the modified insulating interlayer **176** may be planarized until a top surface of the capping layer pattern **160** is exposed.

[0141] FIGS. **26** to **35** are cross-sectional views illustrating a method of manufacturing a semiconductor device in accordance with example embodiments. Detailed descriptions on processes and/or materials substantially the same as or similar to those illustrated with reference to FIGS. **1** to **10**, FIGS. **12** to **14**, FIGS. **15** to **21** and/or FIGS. **22** to **25** are omitted herein.

[0142] Referring to FIG. **26**, a front-end-of-line (FEOL) process may be performed on a substrate **200**.

[0143] In example embodiments, a gate structure **210** may be formed on a substrate **200**, and impurity regions **205** and **207** may be formed on upper portions of the substrate **200** adjacent to the gate structure **210**.

[0144] The substrate **200** may include a first region I and a second region II. For example, the first region I and the second region II may be provided as an NMOS (n-type metal oxide semiconductor) region and a PMOS (p-type metal oxide semiconductor) region, respectively. In this case, p-type impurities may be implanted in the first region I to form a P-well, and n-type impurities may be implanted in the second region II to form an N-well.

[0145] The substrate **200** may include a semiconductor substrate, e.g., a silicon substrate, a germanium substrate, a silicon-germanium substrate, a silicon-on-insulator (SOI) substrate, a germanium-on-insulator (GOI) substrate, etc. In some embodiments, the substrate **200** may include a group III-V compound such as GaP, GaAs, GaSb, or the like.

[0146] An isolation layer **202** may be formed by a shallow trench isolation (STI) process. The substrate **200** may be divided into an active region and a field region by the isolation layer **202**.

[0147] A gate insulation layer, a gate electrode layer and a gate mask layer may be sequentially formed on the substrate **200**, and may be patterned by a photolithography process to form the gate structure including a gate insulation layer pattern **213**, a gate electrode **215** and a gate mask **217**.

[0148] The gate insulation layer may be formed of silicon oxide or metal oxide. In some embodiments, the gate insulation layer may be formed by performing a thermal oxidation process on a top surface of the substrate **200**. The gate electrode layer may be formed of doped polysilicon, metal, metal nitride or metal silicide. The gate mask layer may be formed of silicon nitride. The gate insulation layer, the gate electrode layer and the gate mask layer may be formed by, e.g., a CVD process, a PVD process, an ALD process, or the like.

[0149] Impurities may be implanted using the gate structure **210** as an ion-implantation mask to form a first impurity region **205** and a second impurity region **207** at upper portions of the substrate **200** in the first region I and the second region II, respectively. In example embodiments, the first impurity region **205** may include n-type impurities such as phosphorous (P) or arsenic (As), and the second impurity region **207** may include p-type impurities such as boron (B).

[0150] In this case, a first photoresist mask covering the second region II of the substrate **200** may be formed, and the n-type impurities may be implanted on the first region I to form the first impurity region **205**. The first photoresist mask may be removed by an ashing process and/or a strip process. A second photoresist mask covering the first region I of the substrate **200** may be formed, the p-type impurities may be implanted on the second region II to form the second impurity region **207**. The second photoresist mask may be removed by an ashing process and/or a strip process.

[0151] Accordingly, an NMOS transistor may be defined by the first impurity region **205** and the gate structure **210** on the first region I. A PMOS transistor may be defined by the second impurity region **207** and the gate structure **210** on the second impurity region II. Thus, a CMOS (complementary metal oxide semiconductor) transistor may be formed on the substrate **200**.

[0152] A gate spacer **219** may be further formed on a sidewall of the gate structure **210**. For example, a spacer layer covering the gate structure **210** may be formed on the substrate **200**. The spacer layer may be anisotropically etched to form the gate spacer **219**. The spacer layer may be formed on silicon nitride by a CVD process or an ALD process.

[0153] Referring to FIG. **27**, a first lower insulation layer **220** covering the transistor may be formed on the substrate **200**, and plugs **225** electrically connected to the impurity regions **205** and **207** may be formed through the first lower insulation layer **220**.

[0154] Subsequently, a back-end-of-line (BEOL) process may be performed to form an interconnection structure electrically connected to the plugs **225**.

[0155] A second lower insulation layer **230** covering the plugs **225** may be formed on the first lower insulation layer **220**, and lower contacts **240** electrically connected to the plugs **225** may be formed in the second lower insulation layer **230**. A first etch-stop layer **250** covering the lower contacts **240** may be formed on the second lower insulation layer **230**.

[0156] The first and second lower insulation layers **220** and **230** may be formed of silicon oxide. The plugs **225** and the lower contacts **240** may be formed of a metal such as copper or tungsten. The first etch-stop layer **250** may be formed of silicon nitride, silicon carbonitride, silicon oxynitride and/or a metal.

[0157] In some embodiments, a passivation layer including, e.g., silicon nitride may be formed between the first and second lower insulation layers **220** and **230**.

[0158] Referring to FIG. **28**, a process substantially the same as or similar to that illustrated with reference to FIG. **16** may be performed.

[0159] Accordingly, a supporting layer **312**, a sacrificial layer **314**, a buffer layer **320** and a second etch-stop layer **330** may be sequentially formed on the first etch-stop layer **250**.

[0160] Referring to FIG. **29**, a process substantially the same as or similar to that illustrated with reference to FIG. **17** may be performed. In example embodiments, a first opening **322**, a second opening **334** and third opening **336** may be formed through the second etch-stop layer **330**, the buffer layer **320**, the sacrificial layer **314**, the supporting layer **312** and the first etch-stop layer **250** such that the respective lower contacts **240** may be exposed.

[0161] For example, the lower contact **240** electrically connected to the first impurity region **205** may be exposed

through the first opening **332**. The lower contact **240** electrically connected to the second impurity region **207** may be exposed through the second opening **334**.

[0162] In some embodiments, the third opening **336** may be formed by a dual damascene process, and may include a via hole **335** and a trench **337**. The trench **337** may be integrally connected to an upper portion of the via hole **335**, and may have a width expanded from a width of the via hole **335**. A boundary between the via hole **335** and the trench **337** may be defined by a top surface of the supporting layer **312**.

[0163] Referring to FIG. **30**, processes substantially the same as or similar to FIGS. **18** and **19** may be performed.

[0164] Accordingly, a first conductive pattern **350**, a second conductive pattern **352** and a third conductive pattern **354** may be formed in the first opening **322**, the second opening **334** and the third opening **336**, respectively.

[0165] The first conductive pattern **350** may include a first barrier layer pattern **340***a* and a first conductive layer pattern **342***a*. The second conductive pattern **352** may include a second barrier layer pattern **340***b* and a second conductive layer pattern **342***b*. The third conductive pattern **354** may include a third barrier layer pattern **340***c* and a third conductive layer pattern **342***c*.

[0166] The third conductive pattern **354** may include a via portion **358** formed in the via hole **335**, and an expanded portion **356** formed in the trench **337**. A boundary or a stepped surface between the via portion **358** and the expanded portion **356** may be defined by the top surface of the supporting layer **312**.

[0167] For example, the expanded portion **356** may serve as a routing wiring extending from the via portion **358**.

[0168] A capping layer pattern **360** may be formed on a top surface of each of the first to third conductive patterns **350**, **352** and **354**.

[0169] Referring to FIG. **31**, a process substantially the same as or similar to that illustrated with reference to FIG. **20** may be performed to remove the sacrificial layer **314**. Accordingly, upper portions of the first to third conductive patterns **350**, **352** and **354** and the top surface of the supporting layer **312** may be exposed.

[0170] Referring to FIG. **32**, processes substantially the same as or similar to FIGS. **8** to **10**, or FIG. **21** may be performed.

[0171] In example embodiments, a first insulating interlayer covering the first to third conductive patterns **350**, **352** and **354**, and the capping layer pattern **360** may be formed on the supporting layer **312**. The first insulating interlayer may be converted into a modified first insulating interlayer **375** by a modification treatment. An upper portion of the modified first insulating interlayer **375** may be planarized such that the capping layer pattern **360** may be exposed.

[0172] According to example embodiments as described above, a semiconductor element including the CMOS transistor may be formed on the substrate **200**, and a conductive structure electrically connected to the semiconductor element may be formed. The conductive structure may include the first to third conductive patterns **350**, **352** and **354**, and an insulation structure therebetween. The insulation structure, e.g., the modified first insulating interlayer **375** may include a low-k material. Thus, a parasitic capacitance between the first to third conductive patterns **350**, **352** and **354** may be reduced, and an RC delay of the semiconductor device may be suppressed.

[0173] In some example embodiments, an additional wiring build-up process may be further performed on the conductive structure as described below.

[0174] Referring to FIG. **33**, a third etch-stop layer **410** may be formed on the modified first insulating interlayer **375**, and a second insulating interlayer **420** may be formed on the third etch-stop layer **410**. For example, the third etch-stop layer **410** and the second insulating interlayer **420** may be formed of silicon nitride and silicon oxide, respectively.

[0175] The third etch-stop layer **410** may prevent a damage of the modified first insulating interlayer **375** by the build-up process.

[0176] Referring to FIG. **34**, upper contacts electrically connected to the first to third conductive patterns **350**, **352** and **354** may be formed through the second insulating interlayer **420** and the third etch-stop layer **410**.

[0177] For example, the upper contacts may include a first upper contact **430**, a second upper contact **432** and a third upper contact **434** in contact with the first conductive pattern **350**, the second conductive pattern **352** and the third conductive pattern **354**, respectively.

[0178] The upper contacts may be formed by a plating process or a deposition process such as a sputtering process using a metal, e.g., copper or tungsten.

[0179] Referring to FIG. **35**, a fourth etch-stop layer **440** and a third insulating interlayer **450** may be formed on the second insulating interlayer **420**. Wirings electrically connected to the upper contacts may be formed through the third insulating interlayer **450** and the fourth etch-stop layer **440**.

[0180] For example, the wirings may include a first wiring **470***a*, a second wiring **470***b* and a third wiring **470***c*. The first to third wirings **470***a*, **470***b* and **470***c* may have a stacked structure including barrier layer patterns **460***a*, **460***b* and **460***c*, and conductive layer patterns **465***a*, **465***b* and **465***c*.

[0181] In some embodiments, the first wiring **470***a* and the third wiring **470***c* may be electrically connected to the first upper contact **430** and the third upper contact **434**, respectively. The second wiring **470***b* may be electrically connected commonly to the first upper contact **430** and the second upper contact **432**. Accordingly, the second wiring **470***b* may be configured to transfer an electrical signal between the first region I and the second region II.

[0182] In some embodiments, the first to third wirings **470***a*, **470***b* and **470***c* may be formed by processes substantially the same as or similar to those for the formation of the first to third conductive patterns **350**, **352** and **354** as illustrated in FIGS. **28** to **32**.

[0183] According to example embodiments of the present inventive concepts, conductive patterns may be formed in a sacrificial layer, and then the damaged sacrificial layer may be removed by an ashing process. Subsequently, an insulating interlayer may be formed between the conductive patterns. Thus, the insulating interlayer having a low-k value without an etching damage may be formed between the conductive patterns. Further, a carbon concentration may be controlled while forming the sacrificial layer, so that a removed thickness or a removed height of the sacrificial layer may be adjusted. For example, a conductive structure including an insulating interlayer that may have a dielectric constant (k) less than about 2.5 or less than about 2.0 may be obtained by the method according to example embodiments. The conductive structure may be implemented in a semiconductor device including, e.g., a nano-scaled wiring.

[0184] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and advantages of the present inventive concept. Accordingly, all such modifications are intended to be included within the scope of the present inventive concept as defined in the claims. Therefore, it is to be understood that the foregoing is illustrative of various example embodiments and is not to be construed as limited to the specific example embodiments disclosed, and that modifications to the disclosed example embodiments, as well as other example embodiments, are intended to be included within the scope of the appended claims.

1. A method of manufacturing a semiconductor device including a conductive structure, comprising:

forming a sacrificial layer including an inorganic insulative material on a lower contact by an in-situ deposition process, the sacrificial layer having a composition at a lower portion and a different composition at an upper portion thereof;

forming a conductive pattern extending through the sacrificial layer to electrically connect to the lower contact;

removing the upper portion of the sacrificial layer such that the conductive pattern is exposed by the lower portion of the sacrificial layer; and

forming an insulating interlayer on the lower portion of the sacrificial layer to cover the conductive pattern.

2. The method of claim **1**, wherein the inorganic insulative material comprises a silicon-oxide based material, the sacrificial layer further including carbon, and

a carbon concentration in the upper portion of the sacrificial layer is greater than a concentration of carbon in the lower portion of the sacrificial layer.

3. The method of claim **2**, wherein the upper portion of the sacrificial layer has a density less than that of the lower portion of the sacrificial layer.

4. The method of claim **2**, wherein forming the sacrificial layer includes:

loading an object including the lower contact into a process chamber;

providing a silicon source and a reactive gas to the process chamber; and

providing a carbon source starting at a predetermined time after providing the silicon source and the reactive gas.

5. The method of claim **1**, further comprising:

forming a first etch-stop layer covering the lower contact; and

sequentially forming a buffer layer and a second etch-stop layer on the sacrificial layer.

6. The method of claim **5**, wherein forming the conductive pattern includes:

forming an opening extending through the second etch-stop layer, the buffer layer and the sacrificial layer;

forming a conductive layer on the second etch-stop layer to fill the opening; and

planarizing an upper portion of the conductive layer, the second etch-stop layer and the buffer layer until the sacrificial layer is exposed.

7. The method of claim **5**, wherein the first etch-stop layer and the second etch-stop layer comprises at least one of silicon nitride, silicon carbonitride, silicon oxynitride and a metal, and

the buffer layer comprises silicon oxynitride.

8. The method of claim **1**, wherein forming the insulating interlayer comprises forming a silicon oxide-based material using a flowable chemical vapor deposition (FCVD) process.

9. The method of claim **1**, further comprising:

performing a modification treatment to convert the insulating interlayer to a modified insulating interlayer.

10. The method of claim **9**, wherein the modification treatment includes an ultraviolet (UV) irradiation or a plasma treatment.

11.-**14**. (canceled)

15. A method of manufacturing a semiconductor device including a conductive structure, comprising:

forming a supporting layer including a silicon oxide-based material on a lower contact;

forming a sacrificial layer including silicon carboxide or carbon-doped silicon oxide on the supporting layer;

forming a conductive pattern extending through the sacrificial layer and being electrically connected to the lower contact;

removing the sacrificial layer to expose the conductive pattern above the supporting layer; and

forming an insulating interlayer on the supporting layer to cover the conductive pattern.

16. The method of claim **15**, wherein the supporting layer is carbon-free, or has a carbon concentration that is less than that of the sacrificial layer.

17. The method of claim **15**, wherein the lower contact is included in a plurality of lower contacts, wherein forming the conductive pattern includes forming a first conductive pattern, a second conductive pattern and a third conductive pattern, the first conductive pattern and the third conductive pattern extending through the sacrificial layer and the supporting layer to electrically contact respective ones of the lower contacts, the second conductive pattern being buried in the sacrificial layer, and electrically isolated from the plurality of the lower contacts; and

wherein forming the third conductive pattern includes performing a dual damascene process.

18. The method of claim **17**, wherein the third conductive pattern includes a via portion in contact with one of the respective lower contacts, and an expanded portion integrally connected to the via portion, the expanded portion having a larger width than that of the via portion, and

a stepped surface is defined to be at boundary between the via portion and the expanded portion.

19. The method of claim **18**, wherein a top surface of the supporting layer, a bottom of the second conductive pattern, and the stepped surface of the third conductive pattern are coplanar with each other.

20. The method of claim **18**, wherein a top surface of the supporting layer is higher than a bottom of the second conductive pattern and the stepped surface of the third conductive pattern.

21. The method of claim **15**, wherein removing the sacrificial layer includes performing a dry etching process using a fluoro hydrocarbon gas or a plasma etching process.

22. The method of claim **21**, before removing the sacrificial layer, further comprising performing a reductive plasma treatment on the sacrificial layer.

23. The method of claim **15**, wherein forming the supporting layer and forming the sacrificial layer are performed in a single process chamber in-situ.

24.-**30**. (canceled)

31. A method of manufacturing a semiconductor device including a conductive structure, comprising:

forming an insulation layer using a material having a composition selected to provide resistance to a subsequent etching process;

changing the composition of the material to reduce the resistance of the material to the subsequent etching process at a predetermined level in the insulation layer;

performing the subsequent etching process on the insulation layer to remove an upper portion of the insulation layer above the predetermined level and leaving a lower portion of the insulation layer below the predetermined level between adjacent conductive patterns extending through the lower portion of the insulation layer; and

forming a low-k dielectric material on the lower portion of the insulation layer between the adjacent conductive patterns to replace the upper portion of the insulation layer above the predetermined level.

32.-**41**. (canceled)

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