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(54) **SYSTEM, METHOD AND APPARATUS FOR LEADLESS SURFACE MOUNTED SEMICONDUCTOR PACKAGE**

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(57) **ABSTRACT**

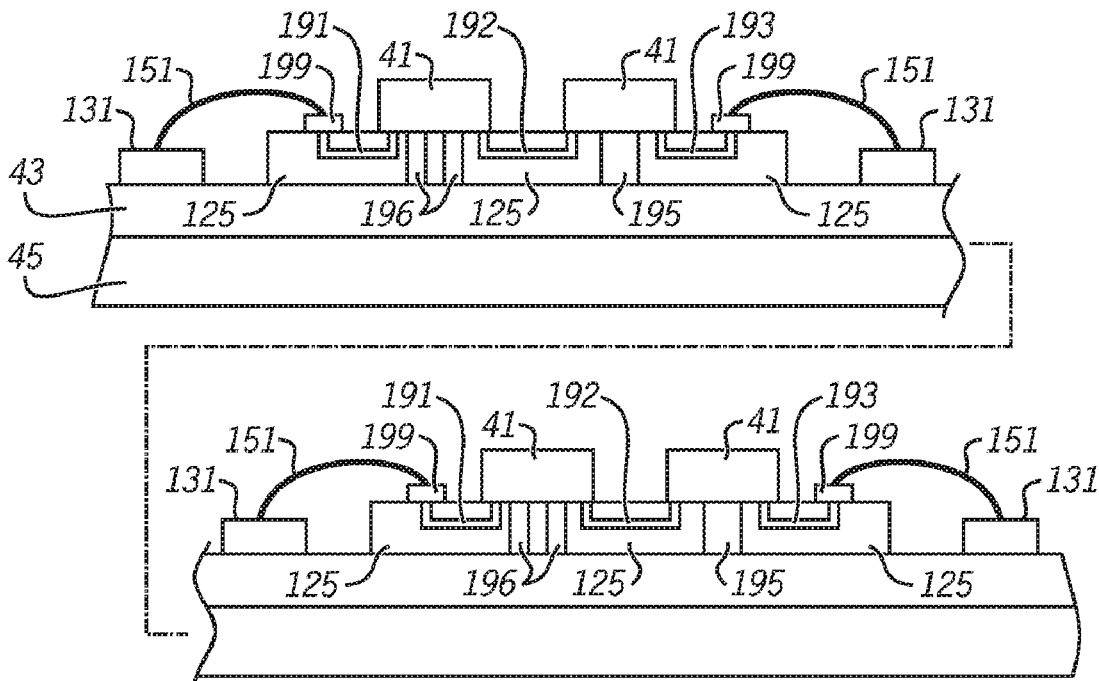
A packaged semiconductor device may include a termination surface having terminations configured as leadless interconnects to be surface mounted to a printed circuit board. A first flange has a first surface and a second surface. The first surface provides a first one of the terminations, and the second surface is opposite to the first surface. A second flange also has a first surface and a second surface, with the first surface providing a second one of the terminations, and the second surface is opposite to the first surface. A die is mounted to the second surface of the first flange with a material having a melting point in excess of 240° C. An electrical interconnect extends between the die and the second surface of the second flange opposite the termination surface, such that the electrical interconnect, first flange and second flange are substantially housed within a body.

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(60) Division of application No. 14/341,292, filed on Jul. 25, 2014, now Pat. No. 9,263,375, which is a continuation of application No. 13/484,664, filed on May 31, 2012, now Pat. No. 8,803,302.



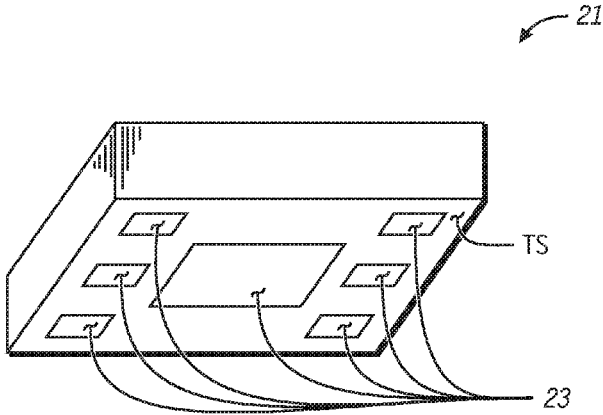


FIG. 1

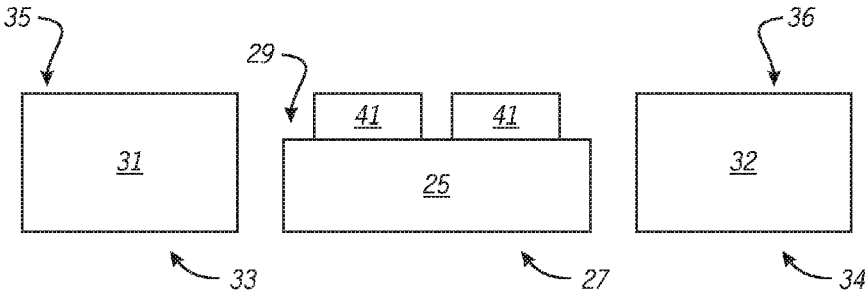


FIG. 2

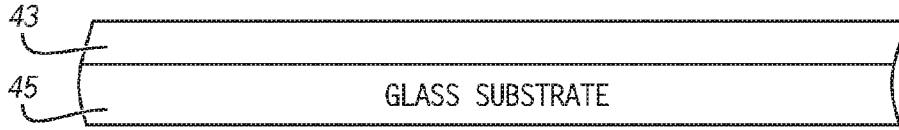


FIG. 3A

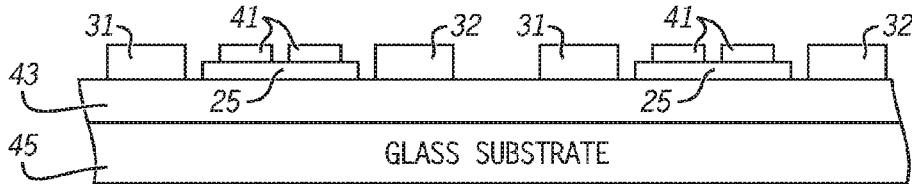


FIG. 3B

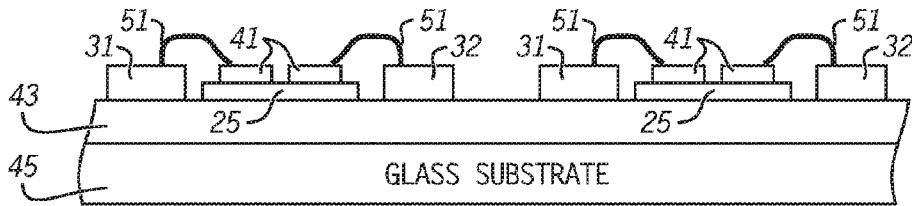


FIG. 3C

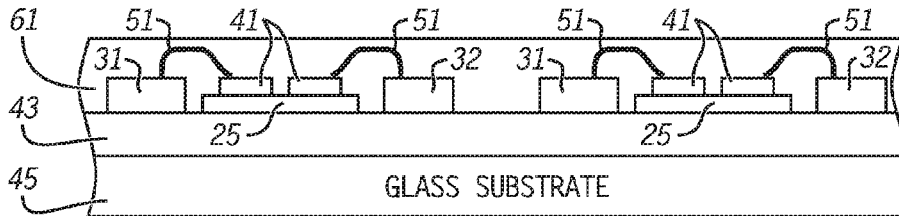


FIG. 3D

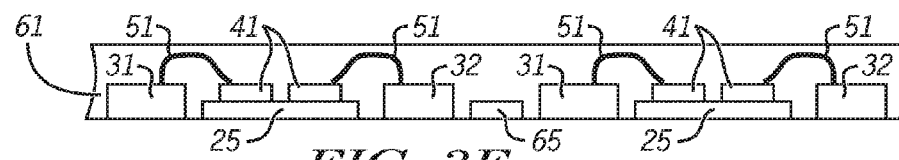


FIG. 3E

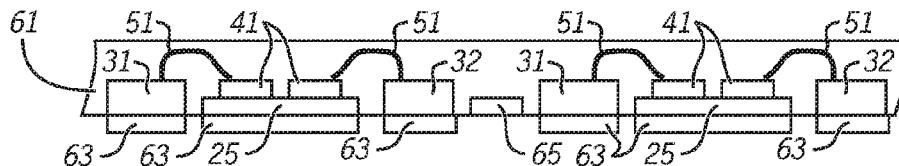


FIG. 3F

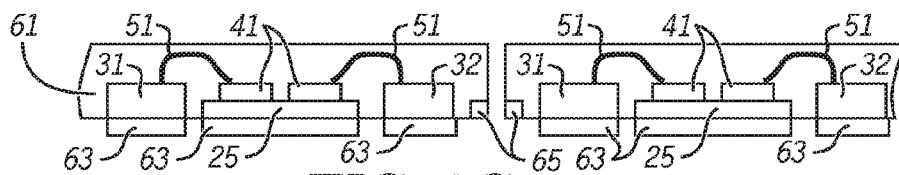


FIG. 3G

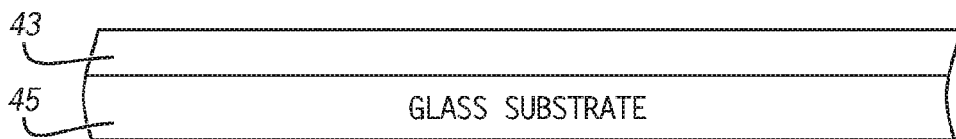


FIG. 4A

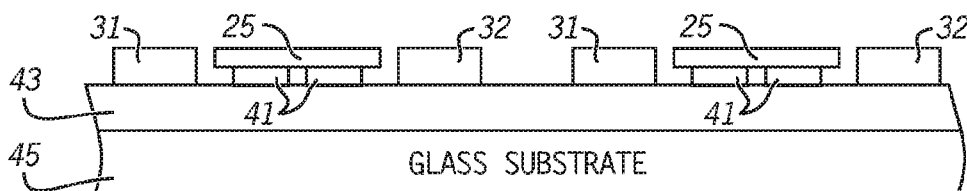


FIG. 4B

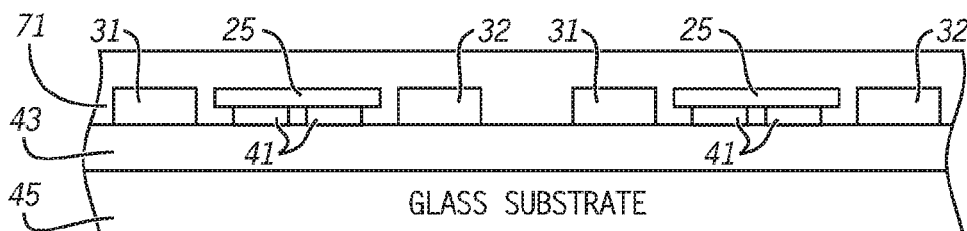


FIG. 4C

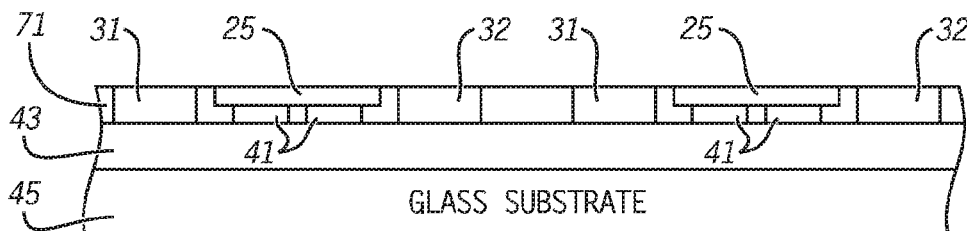


FIG. 4D

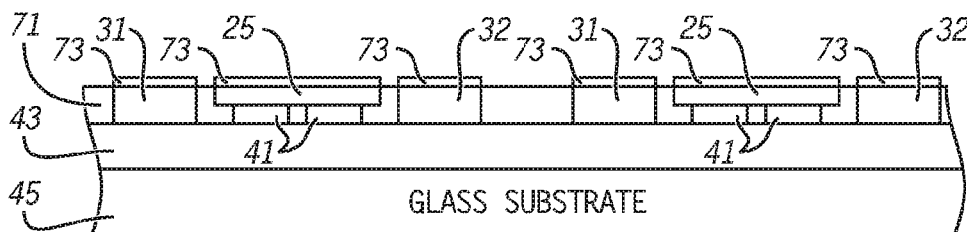


FIG. 4E

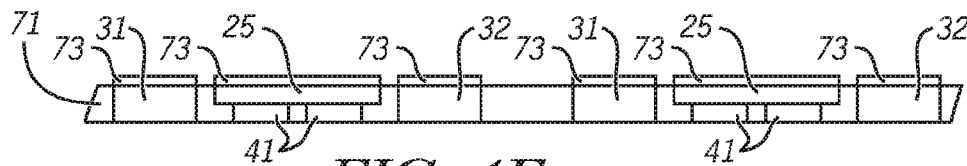
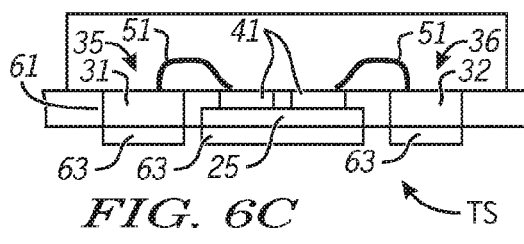
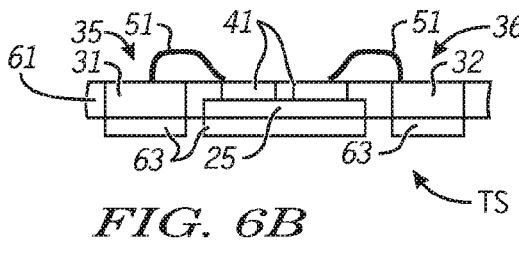
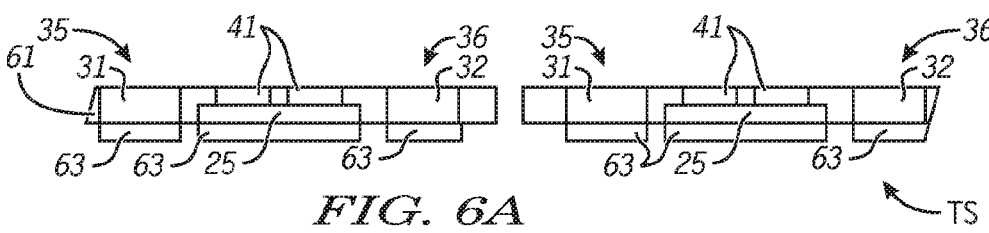
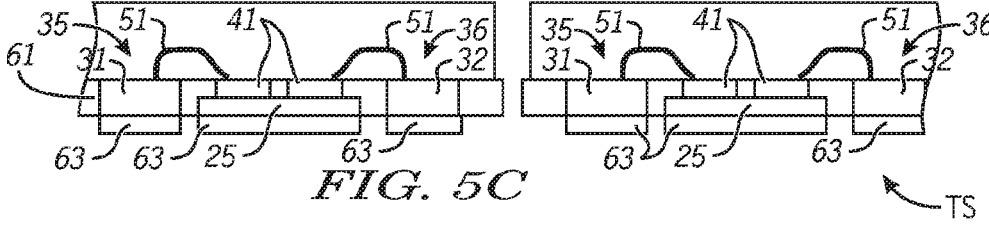
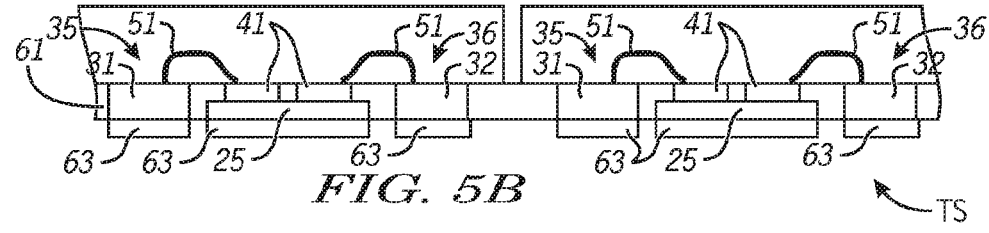
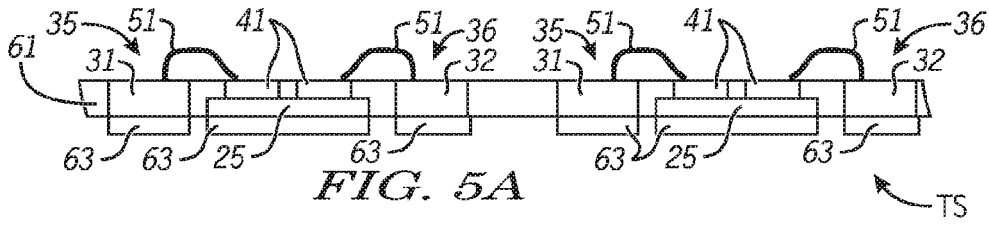


FIG. 4F



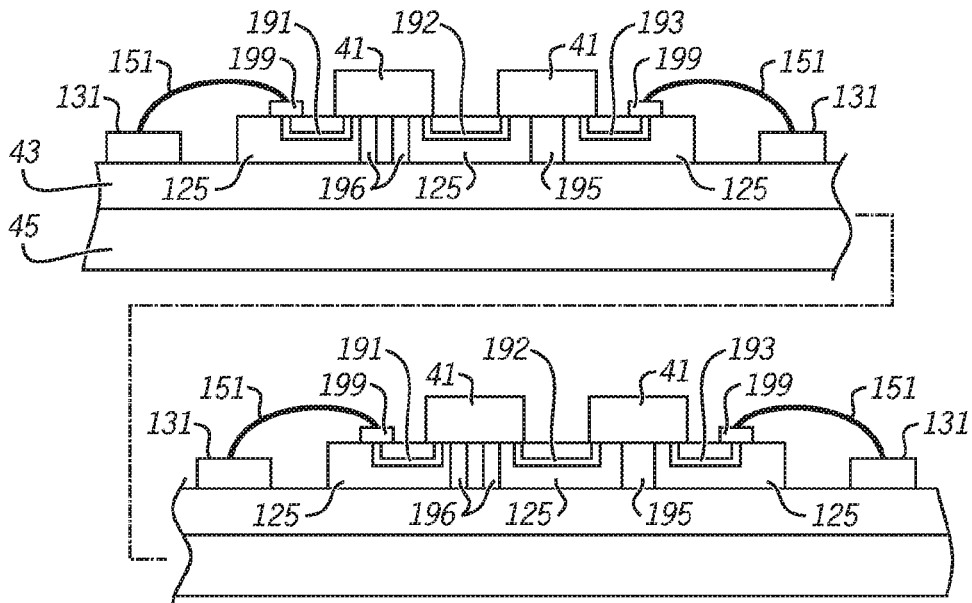


FIG. 7

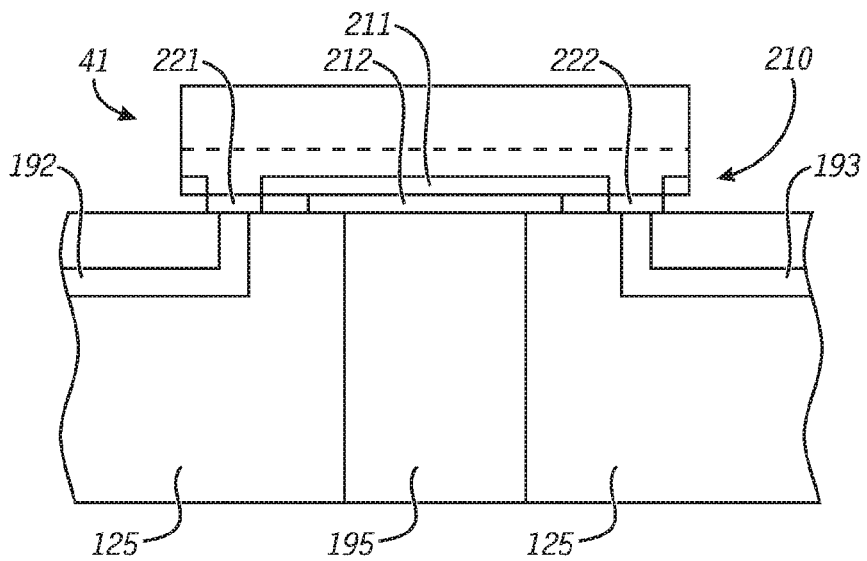


FIG. 8

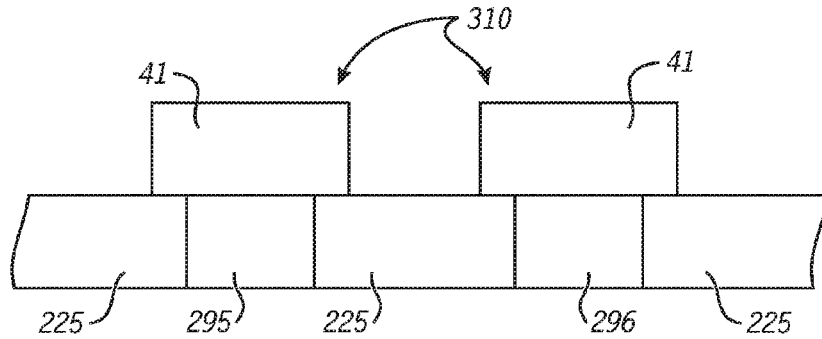


FIG. 9

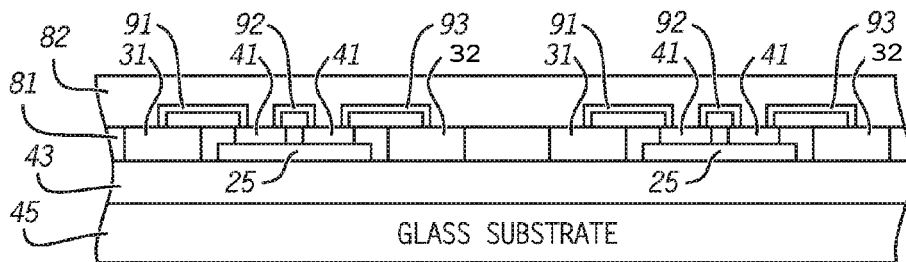


FIG. 10

**SYSTEM, METHOD AND APPARATUS FOR
LEADLESS SURFACE MOUNTED
SEMICONDUCTOR PACKAGE**

CROSS-REFERENCE TO RELATED
APPLICATION(S)

[0001] The present application is divisional patent application of U.S. patent application Ser. No. 14/341,292, entitled "SYSTEM, METHOD AND APPARATUS FOR LEADLESS SURFACE MOUNTED SEMICONDUCTOR PACKAGE" filed on Jul. 25, 2014, which issued as U.S. Pat. No. 9,263,375 on Feb. 16, 2016, which is a continuation of U.S. patent application Ser. No. 13/484,664, entitled "SYSTEM, METHOD AND APPARATUS FOR LEADLESS SURFACE MOUNTED SEMICONDUCTOR PACKAGE" filed on May 31, 2012, which issued as U.S. Pat. No. 8,803,302 on Aug. 12, 2014, the entirety of which are herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Disclosure

[0003] The present invention relates in general to electronic devices, and, in particular, to leadless surface mount semiconductor packages.

[0004] 2. Description of the Related Art

[0005] Semiconductor die are encapsulated in a semiconductor package for protection from damage by external stresses and to provide a system for carrying electrical signals to and from the chips. Many different types of semiconductor packages exist, including dual-in-line packages, pin grid array packages, tape-automated bonding (TAB) packages, multi-chip modules (MCMs), and power packages. One type of power package is a high power package used for a high power semiconductor device that is capable of dissipating greater than ten watts of power.

[0006] A need exists for a package for a high power semiconductor device that has improved thermal conductivity for improved reliability, that is less expensive than ceramic-based packages, and that can be used to package multiple semiconductor die in a single package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] So that the manner in which the features and advantages of the embodiments are attained and can be understood in more detail, a more particular description may be had by reference to the embodiments thereof that are illustrated in the appended drawings. However, the drawings illustrate only some embodiments and therefore are not to be considered limiting in scope as there may be other equally effective embodiments.

[0008] FIG. 1 is a schematic diagram of an embodiment of a packaged semiconductor device (SD);

[0009] FIG. 2 is schematic side view of an embodiment of a partially packaged SD;

[0010] FIGS. 3A-3G depict an embodiment of a sequence of processes for fabricating a packaged SD;

[0011] FIGS. 4A-4F depict another embodiment of a sequence of processes for fabricating a packaged SD;

[0012] FIGS. 5A-5C and 6A-6C depict alternate embodiments of processes for completing fabrication of a packaged SD; and

[0013] FIGS. 7-10 are schematic side views of other embodiments of packaged SDs.

[0014] The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION

[0015] Typically, power packages use relatively high resistivity die attach materials that have a high lead content, a large thickness, and a low thermal conductivity of approximately twenty to thirty watts per meter Kelvin (w/m-K). Each of these characteristics contribute to heat transfer problems during device operation. These power packages also typically have an air cavity enclosed by ceramic components, which are expensive. Furthermore, these power packages are typically limited to a single semiconductor die per package, which requires: (1) matching components to be located on the same chip as the high power semiconductor device and results in lossy devices with poor electrical performance; or (2) matching components to be located on one or more different chips in different packages and requires a larger footprint or a larger amount of space in the final product for multiple packages.

[0016] Specific embodiments described herein entail a leadless packaged device that includes one or more components, such as a semiconductor die, mounted in a package that is suitable for high power applications without the use of a lead frame. The leadless packaged device includes a relatively thick heat sink flange, but some embodiments have no separate lead frame structure, which is typically included to connect the input and output of a device to a circuit board. The components to be packaged can be attached to the heat sink flange using a high temperature die attach process. The flange/component combination can then be housed, such as in an encapsulant (e.g., a plastic material) so that the lower surface of the heat sink flange and the terminal pads remain exposed from the encapsulant to form leadless terminations, e.g., interconnects. As used herein, the term 'housing' can refer to either a solid overmolded structure or an air housing or cavity without encapsulant material.

[0017] Such a technique facilitates packaging flexibility and achieves improvements in wire bond quality. Furthermore, flatness of the packaged semiconductor device and co-planarity of the elements is maintained due to the placement of the relatively thick heat sink flanges, or die attached thereto, onto a thermal tape attached to a carrier substrate. Accordingly, a lower profile package with enhanced performance and improved reliability can be achieved for high power radiofrequency applications.

[0018] Referring to FIG. 1, a packaged semiconductor device (SD) 21, such as a radio frequency (RF) device, comprises a major surface referred to as a termination surface, labeled TS, that comprises a plurality of terminations 23 configured as leadless interconnects to be surface mount attached to a PCB. The PCB is not shown.

[0019] FIG. 2 illustrates a portion of package SD 21, which includes a first flange 25 (or heat sink flange), a second flange 31, and a third flange 32, each of which correspond to the termination surface TS of FIG. 1. The first flange 25 has a first surface 27 and a second surface 29. The first surface 27 includes the larger of the terminations 23 illustrated at FIG. 1. The second surface 29 is opposite the surface 27 and can be substantially parallel to the first surface 27. The second flange 31 has a first surface 33 and a second surface 35. The first surface 33 corresponds to a second one of the plurality of smaller terminations 23 of FIG. 1. The second surface 35 is opposite the second surface 33 and can be substantially par-

allel to the first surface 33. The third flange 32 has a first surface 34 and a second surface 36. The first surface 34 corresponds to a second one of the plurality of smaller terminations 23 of FIG. 1. The second surface 36 is opposite the second surface 33 and can be substantially parallel to the first surface 33. The flanges 25, 31, 32 are electrically and thermally conductive, and each flange 25, 31, 32 may have a thickness of about 30 mils to about 100 mils. In other embodiments the thickness is about 40 mils to about 100 mils. In still other embodiments, the thickness is about 40 mils to about 65 mils.

[0020] Embodiments of the heat sink flanges, e.g., flange 25, illustrated herein may be thermally and electrically conductive copper or a copper laminate material. Individual heat sink flanges are shown for simplicity of illustration. In some embodiments, the heat sink flange may be a single flange, or in an array of interconnected heat sink flanges (not shown), as known to those skilled in the art. The heat sink flange is sized to accommodate one or more semiconductor dies in accordance with the particular design of the semiconductor device. Locations of the flanges may be selectively plated to provide a portion of the surface of the heat sink flange suitable for a subsequent die attach operation.

[0021] One or more semiconductor dies may be coupled to the heat sink flange 25. In an embodiment, the semiconductor dies may be high power, e.g., greater than 30 watts. Radiofrequency semiconductor dies may be attached to a surface of the heat sink flange using a high temperature bonding process, such as a gold-silicon eutectic bonding die attach process. In such an embodiment, the flange thickness of the heat sink flange may be of suitable thickness, for example, at least 30 mils, in order to withstand the high temperatures (e.g., greater than 400° C.) needed for gold-silicon eutectic bonding without damage.

[0022] Unfortunately, a high temperature bonding process may not be suitable for some leadless surface mount packages because of multiple dies, the metallurgical nature of the die attach, and the thermal expansion mismatch between the semiconductor material and Cu can cause warping of the Cu and, thus, the terminations or otherwise damage the semiconductor device.

[0023] One or more dies is mounted to the second surface 29 of the first flange 25. The dies 41 may comprise active or passive components. For example, an active component can include such a semiconductor die that includes transistors, such as a die having microprocessor, a die having memory, and the like. An active component may be a high power (e.g., greater than 30 watts) radio frequency die. A passive component can include a capacitor, inductor, resistor, and the like. Die other than those illustrated can be mounted to other flanges.

[0024] A material, such as a Pb-free metallic system that forms a metallurgical joint, having a melting point in excess of 240° C. may be used for this purpose. Other embodiments may have a melting point in excess of 260° C. For example, the following materials can be used to attach the one or more dies 41 to the second surface: AuSi, AuSn, or Ag. The approximate melting points of these materials are: AuSi, ~360° C.; AuSn, ~280° C.; and Ag, ~800° C. The silver may comprise sintered silver. Each die 41 may have the same or different thickness, which can be about 3 mils to about 5 mils, or about 1 mil to about 10 mils in other embodiments. For AuSi, the bond may be formed by Si in the die mixing with Au on the back of the die and Au on the flange. For AuSn, the

bond may form from the plated AuSn on the back of the die or a combination of Au and Sn plated on the back of the die, or plated selectively on the flange below where the die goes. The Ag bond may be formed by nano-Ag or micro-Ag attach material that is included in the interface. According to an embodiment, radiofrequency semiconductor dies may be attached to a surface of the heat sink flange using a high temperature bonding process, such as a gold-silicon eutectic bonding die attach process. In such an embodiment, the flange thickness of the heat sink flange may be of suitable thickness, for example, at least 30 mils, in order to withstand the high temperatures (e.g., greater than 400° C.) needed for gold-silicon eutectic bonding without damage. Thus, for high power applications, it is desirable to surface mount the one or more semiconductor dies of a semiconductor device using a robust, highly reliable die attach process, for example, a high temperature metallurgical bonding process such as gold-silicon bonding, gold-tin bonding, silver bonding, and so forth. In contrast, lead-free metallurgical die attach materials provide package 100 with a more environmentally-friendly characteristic and the use of a die attach comprising, for example, AuSi, AuSn, or Ag (with no epoxy). In addition, a Cu or other non-ceramic flange provides package 100 with its better thermal conductivity and lowered thermal resistivity, which produces improved reliability characteristics. This is in contrast to typical power packages that use relatively high resistivity die attach materials that have a high lead content, a large thickness, and a low thermal conductivity of approximately 20 to 30 W/m-K. Each of these characteristics contributes to heat transfer problems during device operation.

[0025] FIGS. 3A through 3G illustrate a particular embodiment of forming the SD 21. At FIG. 3A, a double-sided thermal tape 43 (FIG. 3A) may be affixed to a carrier substrate 45 (e.g., a glass substrate) that acts to hold various components during the packaging process that forms a plurality of packaged devices at the same time. The flanges 25, 31, 32 may be picked by automated packaging equipment and placed onto the tape 43 (FIG. 3B). As shown in FIG. 3B, two packages are being contemporaneously formed, each package including a set of corresponding flanges 25, 31, 32. The die 41 and first flange 25 of each package be can be formed having a combined thickness T that is substantially equal to the thickness T of the second flange 31, or different. Because of thermal considerations, die 41 may be attached to flange 25 prior to flange 25 being placed on tape 43.

[0026] As shown in FIG. 3C, one or more electrical interconnects 51 may be formed between the dies 41 and the second surfaces 35, 36 (FIG. 2) of the second flanges 31, 32, respectively. The electrical interconnects 51 may comprise bond wires or other types of interconnects, as will be discussed in greater detail below. Bond wires and wire bonding processes are known by those skilled in the art. In an embodiment, 2 mil gold wires may be utilized, and in another embodiment, 10 mil aluminum wires may be used. However, various known wires of varying materials and diameters may be utilized in accordance with particular design requirements.

[0027] In FIG. 3D, a body 61 is formed using an encapsulating material that (when cured) forms a solid that substantially encapsulates the flanges 25, 31, 32, dies 41 and electrical interconnects 51. The body 61 has been formed to provide support thereto, such that the electrical interconnects 51 and flanges 25, 31, 32 are substantially encapsulated e.g., housed, within body 61 to form a packaged device. In these embodiments, the flanges 25, 31, 32 each have a surface that is

co-planar to a surface of each other flange by virtue of being attached to the carrier substrate by the thermal tape 43. These coplanar surfaces are not covered by the encapsulating material. After encapsulating, the carrier substrate 45 and the thermal tape 43 are removed as indicated at FIG. 3E to expose the coplanar surfaces of the flanges 25, 31, 32.

[0028] At each of the flanges 25, 31, 32, respectively, a metalized surface 63 can be formed, as indicated at FIG. 3F, overlying the exposed coplanar surfaces of the flanges 25, 31, 32. For example, the metalized surfaces 63 may comprise Sn or NiPdAu, which is typically deposited using a plating process. The metalized surfaces 63 form the outermost terminations 23 of the package device. The terminations 23 may be co-planar along the termination surface TS to less than about 0.001 inches.

[0029] The packaged devices being contemporaneously formed are singulated to form individual packages, as indicated at FIG. 3G. Singulation can be performed using mechanical sawing, laser ablation, and the like.

[0030] A metallic film 65 (FIG. 3E) may be encapsulated that resides between the packaged SDs 21. The metallic film 65 may comprise Cu and may have a thickness of about 5 mils. The metallic film may be located at the bottom of the flange (e.g., stuck to the adhesive), coplanar with the bottoms of the terminations. The metallic film 65 may be exposed on at least one of the four sidewalls of each of the packaged SDs 21 when the packaged SDs are singulated (compare FIGS. 3F and 3G). This process is well suited for overmold or encapsulation bodies, rather than the air cavity bodies described below. Note that this feature is not a leadframe that provides an electrically and thermally conductive chassis or frame, and in other embodiments, need not be used.

[0031] In some embodiments, the packaged SD may have a power capacity or power rating of about 30 W to about 400 W. In addition, the packaged SD may be configured to operate at radio frequencies of about 3 kHz to about 100 GHz. Typical sizes of the flanges may comprise 200×200 mils, 400×400 mils, 240×650 mils, 260×650 mils, 800×400 mils, or 1200×500 mils. Power also depends on die technology, voltage used, etc.

[0032] Another embodiment of forming SD 21 is depicted in FIGS. 4A through 4F. FIG. 4A is similar to FIG. 3A and therefore, the same reference numerals are maintained to represent the carrier substrate 45 and thermal tape 43. Furthermore, in the present embodiment, the combined height of the die 41 and flange 25 can be selected to have substantially the same height as flanges 31, 32 to facilitate a subsequent planarization process, as described below. Flanges 31, 32 are attached to the thermal tape 43 as illustrated at FIG. 4B. In addition, the combinations of flange 25/die 41 are attached to the thermal tape 43 with the active side of die 41 in contact with the thermal tape 43.

[0033] At FIG. 4C, encapsulating material 71, which can be the same or similar type encapsulating material as the encapsulating material 61 previously described, is deposited to form a package body that substantially encapsulates the components placed on the thermal tape. A portion of the encapsulating material 71 is removed using a planarization process to expose the backsides of the flanges 25, 31, 32. The planarization process can include a mechanical process, chemical process, the like, and combinations thereof. The exposed backsides of the flanges 25, 31, 32 implement or facilitate formation of the termination surface TS (FIG. 1), e.g., they can form surface mount contacts.

[0034] Subsequently, the backsides of the flanges 25, 31, 32 can be metalized with a material 73 (FIG. 4E) to form surface mount contacts at a final termination surface TS (FIG. 1) to be electrically connected to a substrate, such as a PCB (not illustrated). The thermal tape 43 and carrier 45 are removed, as illustrated at FIG. 4F, thus leaving a plurality of individual package workpieces, e.g., packages that have not been completed. The flanges 31, 32 of the plurality of completed workpieces have not yet been electrically connected to the die 41. Various processing flows can be implemented subsequent to removal of the carrier 45 and thermal tape 43 to complete processing of packaged devices SD 21.

[0035] As a further example, the carrier substrate 45 and thermal tape 4 are illustrated as being removed subsequent to formation of the backside metal at FIG. 4E. It will be appreciated however that the carrier substrate 45 and thermal tape 43 could be removed subsequent to prior steps. For example, the carrier substrate 45 and thermal tape 43 could be removed any time subsequent to formation of the body of the package as illustrated at FIG. 4C. FIG. 5 illustrates a particular embodiment where encapsulation of each package workpiece of a panel occurs prior to singulation of the individual package workpieces. For example, each package workpiece of the panel has electrical interconnects formed between its die 41 and flanges 31, 32, as illustrated at FIG. 5A. In particular, electrical interconnects 51 have been formed between the package workpiece die 41 and the surfaces 35 of the flanges 31 opposite the termination surface TS, and between die 41 and the surface 36 of the flanges 32. The electrical interconnects 51 may comprise a wire bond as illustrated at FIG. 5A, or other types of interconnects as described in greater detail herein.

[0036] As illustrated at FIG. 5B, a housing is formed over each of the individual package workpieces to encapsulate the flanges 25, 31, 32 and electrical interconnect 51 of each package workpiece. The housing can be formed by depositing an encapsulation material, as previously described, or by providing an air housing, e.g. a cover which maintains an air space, overlying the components of each package workpiece. According to a particular embodiment, the particular encapsulation is chosen to support a power capacity of about 30 W to about 400 W. Subsequent to encapsulating the individual package substrates, the panel can be singulated (FIG. 5C) to form individual package devices. FIG. 6 illustrates an alternate embodiment, from that of FIG. 5, for implementing package devices. In particular, as illustrated at FIG. 6A, the panel is singulated prior to encapsulation to form individual package workpieces, one of which is illustrated in FIGS. 6B and 6C. For each singulated package workpiece, as illustrated at FIG. 6B, electrical interconnects 51 are formed between its die 41 and its flange surfaces 35 and 36, which are opposite the termination surface TS. As illustrated at FIG. 6C, the housing is formed over the singulated package workpiece to encapsulate its components. The housing can be formed by depositing encapsulation material, as previously described, or provided by an air housing. The air housing may comprise mounting a lid to the assembly to house the electrical interconnect in an air cavity, such that the electrical interconnect is free of encapsulation material. As discussed previously, the housing is chosen to support power dissipation capacity of between about 30 Watts to about 400 W, and to support high frequency RF applications.

[0037] It will be appreciated, that many alternate embodiments of the described packaging process exist. For example,

instead of a composite structure that includes die **41** attached to a conductive flange **25**, other compound structures may be formed. For example, FIG. 7 illustrates a compound structure that is formed prior to being attached to the thermal tape that includes die **41** attached to a printed circuit board **125** (PCB **125**). The PCB **125** is illustrated to include conductive studs **195** (heat sinks), and interconnects including inter-level interconnects **191-193** and through vias **196**. The conductive studs **195** can be formed from a material that provides greater thermal conductivity than the substrate of the PCB **125**. For example, the conductive studs **195** can include copper, aluminum, other metals, the like, and combinations thereof.

[0038] A particular embodiment of the compound structure that includes the die **41** and the PCB **125** is illustrated in greater detail at FIG. 8, which illustrates the die **41** mounted with its active surface **210** mounted facedown such that die bond pads **221** and **222** have been surface mount attached to the PCB **125**. Interlevel routing **192** and **193** is illustrated as being in electrical contact with the die bond pads **221**, **222**, respectively. As illustrated in FIG. 8, interlevel routing **192** electrically connects the die bond pad **221** to a die bond pad of the adjacent die **41** that is attached to the same PCB board **125**. Interlevel interconnect **193** connects the die bond pad **222** to a PCB bond pad **199** of the printed circuit board **125** as also illustrated at FIG. 7. The conductive stud **195**, which in effect is a sufficiently large heat sink to dissipate heat from die **41**, is in contact with a heat conductive interface **212** (FIG. 8), such as a metallic pad, and extends through the PCB board **125** to an opposing surface that is opposite the surface where the die **41** is mounted. The large heat conductive interface **212** overlies a dielectric region **211** that electrically isolates the heat conductive interface **212** from any underlying conductive features at the active region **210** of the die **41**.

[0039] FIG. 9 illustrates an alternate embodiment of a compound structure that includes the dies **41** and a PCB **225**. In particular, the dies **41** are mounted on conductive studs **295**, **296**, respectively, which themselves are formed through the PCB **225** to provide heat sink functionality. The resulting composite structure can be picked and placed with the die **41** facedown against the thermal tape, or with the die **41** mounted face-up, wherein the conductive studs **195** are in contact with the thermal tape. Though not specifically illustrated, it will be appreciated that additional conductive routing can be implemented using interlevel interconnects formed within the PCB **225**. In particular, bond pads can be formed near the periphery of PCB **225** that can be wire bonded directly to bond pads of die **41** using conventional wire bonding, while other bond pads can be formed near the periphery of PCB **225** that can be wire bonded directly to flanges, similar to flanges **31**, **32** previously described.

[0040] FIG. 10 illustrates an alternate embodiment of providing conductive interconnects between the die **41** and flanges **31**, **32**. In particular, instead of forming conventional wire bonds, additional layers are formed overlying the top side of the package device, e.g., the side opposite the thermal tape, after formation of the body portion **81**. For example, the body portion **81** comprises a dielectric material that is planarized to expose the top surfaces of the die **41** and flanges **31**, **32**. Subsequently, additional conductive and dielectric layers are formed to implement conductive interconnects **91**, **92**, **93** between terminals, e.g., bond pads, of die **41** and flanges **31**, **32**. Formation of inter-level interconnects eliminates the need for conventional wire bonding techniques. The housing **82** can be formed by depositing an encapsulation material, as

previously described, or by providing an air housing, e.g., a cover which maintains an air space, overlying the components of each package workpiece.

[0041] In some embodiments, a packaged semiconductor device (SD) comprises a termination surface comprising a plurality of terminations configured as leadless interconnects to be surface mounted to a circuit board. A first flange may have a first surface and a second surface, the first surface providing a first one of the plurality of terminations, and the second surface is opposite to the first surface. A second flange may have a first surface and a second surface, the first surface providing a second one of the plurality of terminations, and the second surface is opposite to the first surface. A die may be mounted to the second surface of the first flange with a Pb-free, die attach material having a melting point in excess of 240° C. In addition, an electrical interconnect may extend between the die and the second surface of the second flange opposite the termination surface, such that the electrical interconnect, first flange and second flange are substantially housed within a body.

[0042] The packaged SD may be configured to operate at radio frequencies of greater than about 3 kHz to about 100 GHz (e.g., 80 GHz). In other embodiments, it operates at about 3 kHz to about 10 GHz. The electrical interconnect may comprise a wire bond, and the die may have a thickness of about 3 mils to about 5 mils. The electrical interconnect also may comprise at least one interconnect level comprising a conductive layer and a dielectric layer (e.g., a printed circuit board or PCB). The body may comprise a solid body that substantially encapsulates the flanges, die and electrical interconnect to provide support thereto. The die and second flange may have surfaces farthest from the termination surface that are co-planar. The body also may comprise a lid mounted to the packaged SD to house the electrical interconnect in an air cavity, such that the electrical interconnect is free of encapsulation material.

[0043] The flanges may be electrically and thermally conductive and each flange may have a thickness of about 30 mils to about 100 mils. A surface of each of the flanges may further comprise an additional conductive layer of material opposite the die at the termination surface, the additional conductive layers form the terminations, and the terminations are coplanar along the termination surface to less than about 0.001 inches. A panel may comprise a plurality of packaged SDs, including the packaged SD described. The panel may further comprise a metallic film encapsulated between the packaged SDs, such that a metallic portion is exposed on at least one sidewall of each of the packaged SDs when the packaged SDs are singulated. The metallic film may comprise Cu and have a thickness of about 5 mils.

[0044] All of the terminations of the packaged SD may be on the termination surface, and the packaged SD may have no side wall terminations. The termination surface may comprise a first surface area, and the terminations comprise a second surface area that is in a range of about 0.2% to about 20% of the first surface area. The die may comprise a first die of an active component or a passive component, and may further comprise a second die mounted to the second surface of the second flange. The die and first flange may comprise a combined thickness that is substantially equal to a thickness of the second flange. The packaged SD may have a power capacity of greater than about 30 W to about 400 W. Alternatively, at least one of the first and second flanges may be embedded in a circuit board.

[0045] Some embodiments of a method of packaging a semiconductor device (SD) may comprise (a) placing a first component comprising a die mounted to a first flange on an adhesive substrate; (b) placing a second flange on the adhesive substrate adjacent to but spaced apart from the first component; (c) electrically interconnecting the die and the second flange; (d) housing at least portions of the flanges by encapsulation to form an assembly surrounding the flanges; and (e) housing the flanges and electrical interconnect such that the packaged SD has a power capacity of greater than about 30 W.

[0046] The die may be mounted to the first flange with a material having a melting point in excess of 260° C. In some embodiments, (a) comprises placing the first component with the die in contact with the adhesive substrate, such that a surface of the die that is farthest from the adhesive substrate and a surface of a second flange are co-planar. In other embodiments, after (d), the method may further comprise thinning the encapsulant to expose backsides of the flanges adjacent a termination surface. Step (c) may comprise forming a wire bond. Steps (d) and (e) may comprise substantially encapsulating the flanges, die and electrical interconnect in a solid material but not one surface of the flanges. Step (e) may comprise mounting a lid to the assembly to house the electrical interconnect in an air cavity, such that the electrical interconnect is free of encapsulation material.

[0047] In other embodiments, the die has a thickness of about 3 mils to about 5 mils; the flanges are electrically and thermally conductive and each flange has a thickness of about 30 mils to about 100 mils; and the packaged SD is configured to operate at radio frequencies of about 3 kHz to about 100 GHz.

[0048] A surface of each of the flanges may further comprise an additional conductive layer of material opposite the die at a termination surface, and the additional conductive layers of material comprise Sn or NiPdAu and form terminations that are co-planar along the termination surface to less than about 0.001 inches.

[0049] A method of forming a panel may comprise a plurality of packaged semiconductor devices, including the packaged semiconductor device, and (e) occurs before the packaged semiconductor device is singulated from the panel. The method may further comprise placing a metallic film between the packaged SDs before (d), encapsulating the metallic film in (e), and then cutting the panel at the metallic film such that a metallic portion is formed on side walls of each of the packaged SDs when the panel is cut, and the metallic film comprises Cu and has a thickness of about 5 mils. In addition, the terminations of the packaged SD may be at a termination surface, and the packaged SD may have no side wall terminations. The termination surface may comprise a first surface area, and the terminations comprise a second surface area that is in a range of about 0.2% to about 20% of the first surface area. The method may further comprise embedding at least one of the first and second flanges in a printed circuit board.

[0050] In still other embodiments, a method of packaging a semiconductor device (SD) may comprise (a) mounting a die to a first flange to form a first component; (b) placing the die on the adhesive substrate with the first flange extending therefrom; (c) placing a second flange on the adhesive substrate adjacent to but spaced apart from the first component, such that the die and second flange have surfaces that are co-planar; (d) housing at least portions of the die and flanges by encapsulation to form an assembly; (e) electrically interconnecting

the die and the second flange; (f) adding an additional conductive layer of material to surfaces of the flanges opposite the die to form a termination surface with terminations configured to be surface mounted to a circuit board without leads external to the assembly; and (g) housing the flanges and electrical interconnect such that the packaged SD has a power capacity of greater than about 30 W.

[0051] Step (a) may comprise mounting the die to the first flange with a material having a melting point in excess of 240° C. After (d), the method may further comprise thinning the encapsulant to expose backsides of the flanges adjacent the termination surface. Step (d) may occur before (e), and (d) may comprise forming one of a wire bond, and at least one conductive layer and at least one dielectric layer.

[0052] Step (g) may comprise mounting a lid to the assembly to house the electrical interconnect in an air cavity, such that the electrical interconnect is free of encapsulation material, and the die has a thickness of about 3 mils to about 5 mils. The flanges may be electrically and thermally conductive and have a thickness of 30 mils to 100 mils, and the packaged SD may be configured to operate at radio frequencies of greater than about 3 kHz.

[0053] Embodiments of a method of forming a panel may comprise a plurality of packaged semiconductor devices, including the packaged semiconductor device, and may further comprise cutting the panel to form the plurality of packaged semiconductor devices. Step (g) may occur before or after the panel is cut, and may further comprise placing a metallic film between the packaged semiconductor devices before (d), encapsulating the metallic film in (d), and then cutting the panel at the metallic film such that a metallic portion is formed on side walls of each of the packaged SDs when the panel is cut.

[0054] For clarity of illustration, different shading and/or hatching is utilized in the illustrations to distinguish the different elements of the semiconductor device. In addition, a term “horizontal” may be used herein to define a plane parallel to the plane or surface of the semiconductor device, regardless of its orientation. Thus, a term “vertical” refers to a direction perpendicular to the horizontal as defined. Terms, such as “above,” “below,” “top,” “bottom,” “side” (as in “side-wall”), “upper,” “lower,” and so forth are defined with respect to the horizontal plane.

[0055] This written description uses examples to disclose the embodiments, including the best mode, and also to enable those of ordinary skill in the art to make and use the invention. The patentable scope is defined by the claims, and may include other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims if they have structural elements that do not differ from the literal language of the claims, or if they include equivalent structural elements with insubstantial differences from the literal languages of the claims.

[0056] Note that not all of the activities described above in the general description or the examples are required, that a portion of a specific activity may not be required, and that one or more further activities may be performed in addition to those described. Still further, the order in which activities are listed are not necessarily the order in which they are performed.

[0057] In the foregoing specification, the concepts have been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing

from the scope of the invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of invention.

[0058] As used herein, the terms “comprises,” “comprising,” “includes,” “including,” “has,” “having” or any other variation thereof, are intended to cover a non-exclusive inclusion. For example, a process, method, article, or apparatus that comprises a list of features is not necessarily limited only to those features but may include other features not expressly listed or inherent to such process, method, article, or apparatus. Further, unless expressly stated to the contrary, “or” refers to an inclusive-or and not to an exclusive-or. For example, a condition A or B is satisfied by any one of the following: A is true (or present) and B is false (or not present), A is false (or not present) and B is true (or present), and both A and B are true (or present).

[0059] Also, the use of “a” or “an” are employed to describe elements and components described herein. This is done merely for convenience and to give a general sense of the scope of the invention. This description should be read to include one or at least one and the singular also includes the plural unless it is obvious that it is meant otherwise.

[0060] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any feature(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature of any or all the claims.

[0061] After reading the specification, skilled artisans will appreciate that certain features are, for clarity, described herein in the context of separate embodiments, may also be provided in combination in a single embodiment. Conversely, various features that are, for brevity, described in the context of a single embodiment, may also be provided separately or in any subcombination. Further, references to values stated in ranges include each and every value within that range.

What is claimed is:

1. A packaged semiconductor die (SD), comprising:
 - a termination surface comprising a plurality of terminations configured as leadless interconnects to be surface mounted to a circuit board;
 - a first flange having a first surface of the first flange and a second surface of the first flange, the first surface of the first flange providing a first one of the plurality of terminations, wherein the second surface of the first flange is opposite to the first surface of the first flange;
 - a second flange having a first surface of the second flange and a second surface of the second flange, the first surface of the second flange providing a second one of the

plurality of terminations, wherein the second surface of the second flange is opposite to the first surface of the second flange;

a die metallurgically attached to the second surface of the first flange with a Pb-free, die attach material having a melting point in excess of 240° C.; and

an electrical interconnect between the die and the second surface of the second flange opposite the termination surface, wherein the electrical interconnect, the first flange and the second flange are substantially housed within a body.

2. The packaged SD according to claim 1, wherein the body is selected from a group consisting of a solid body that substantially encapsulates the flanges, the die, and the electrical interconnect to provide support thereto and a lid mounted to the packaged SD to house the electrical interconnect in an air cavity with the electrical interconnect being free of encapsulation material.

3. The packaged SD according to claim 1, wherein all of the terminations of the packaged SD are on the termination surface, and the packaged SD has a power capacity of greater than about 30 W.

4. The packaged SD according to claim 1, wherein all of the terminations of the packaged SD are on the termination surface.

5. The packaged SD according to claim 1, wherein the packaged SD has a power capacity of greater than about 30 W.

6. The packaged SD according to claim 1, wherein the body comprises a solid body that substantially encapsulates the flanges, the die, and the electrical interconnect to provide support thereto.

7. The packaged SD according to claim 1, wherein the body comprises a lid mounted to the packaged SD to house the electrical interconnect in an air cavity with the electrical interconnect being free of encapsulation material.

8. The packaged SD according to claim 1, wherein the die and the second flange have surfaces that are co-planar.

9. The packaged SD according to claim 8, with a first surface of the die having been placed, at least temporarily, on an adhesive substrate with the first flange extending from a second surface of the die opposite the first surface.

10. The packaged SD according to claim 9, wherein the die mounted to the second surface of the first flange form a first component, the second flange having been placed, at least temporarily, on the adhesive substrate adjacent to but spaced apart from the first component.

11. The packaged SD according to claim 1, wherein at least portions of the die and the flanges are encapsulated to form an assembly, wherein an additional conductive layer of material is added to surfaces of the flanges opposite the die to form a termination surface with terminations configured to be surface mounted to a circuit board without leads external to the assembly.

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