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(54) **AMPLITUDE MODULATION-PHASE MODULATION (AM-PM) LINEARIZATION IN A POWER AMPLIFIER**

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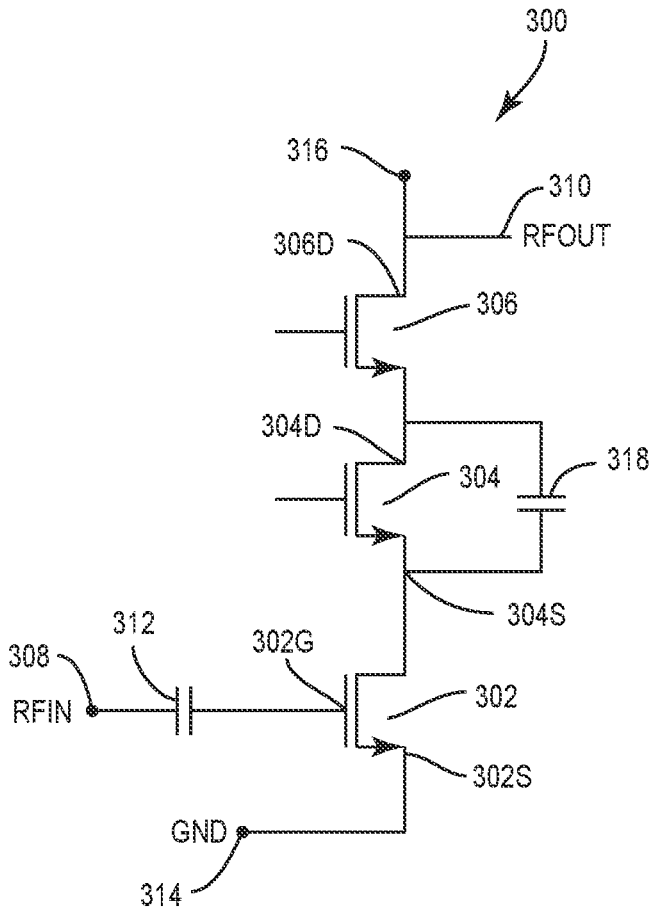
(57) **ABSTRACT**

Amplitude modulation-phase modulation (AM-PM) linearization in power amplifier techniques are disclosed. In one aspect, a fixed capacitor is placed in parallel to a cascode device within a power amplifier. The sum of capacitances from the cascode device and the parallel capacitor may be relatively fixed across voltage swings, allowing for small phase changes across a wide range of signal amplitudes passing through the power amplifier. The small phase changes across voltage swings make it easier to provide compensation for such phase changes resulting in a more efficient device.



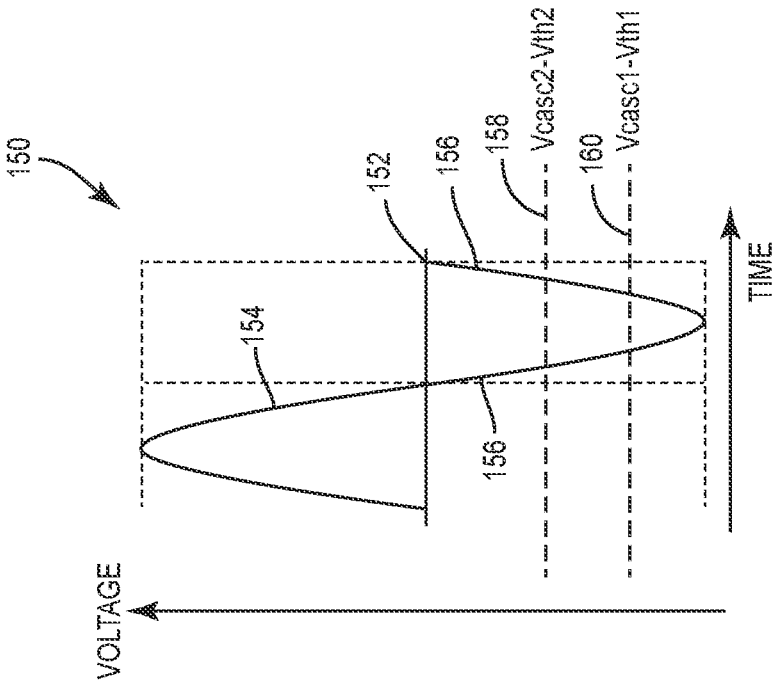

150
VOLTAGE
TIME
152
154
156
156
158
Vcasc2-Vth2
160
Vcasc1-Vth1

FIG. 1B

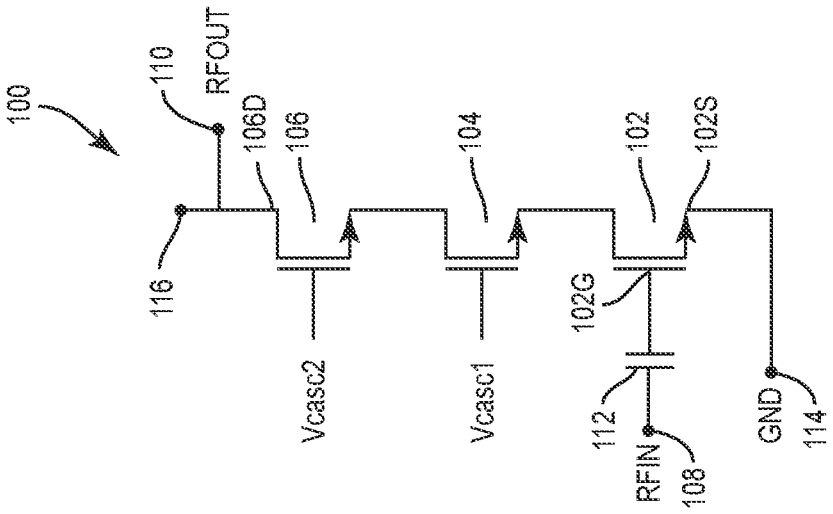

100
110
RFOUT
106D
106
104
102
102S
116
Vcasc2
Vcasc1
102G
112
RFIN
108
GND
114

FIG. 1A

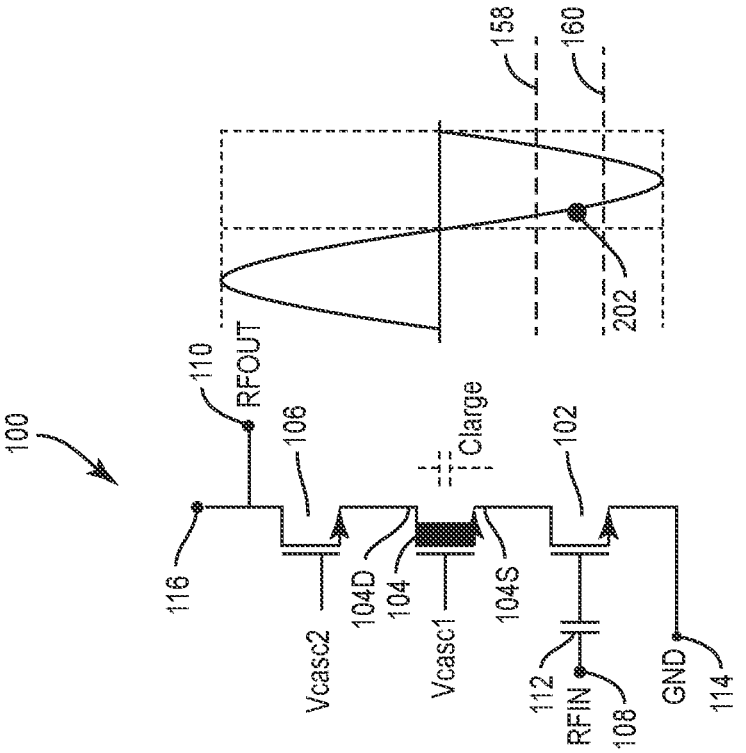

100
110
RFOUT
106
Clarge
102
116
104D
104
104S
Vcasc2
Vcasc1
112
RFIN
108
GND
114
158
160
202

FIG. 2B

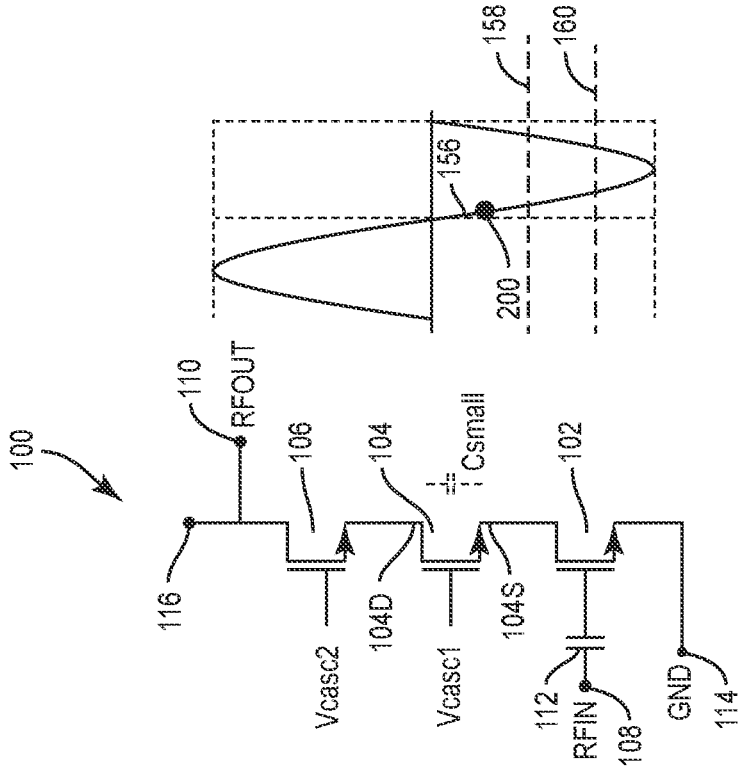

100
110
RFOUT
106
104
Csmall
102
116
104D
104S
Vcasc2
Vcasc1
112
RFIN
108
GND
114
158
160
156
200

FIG. 2A

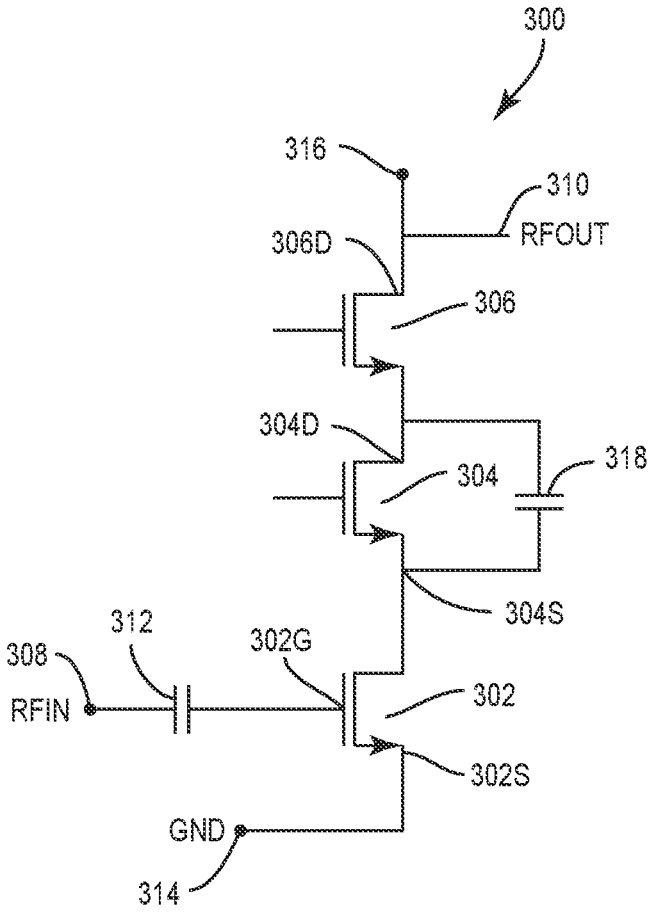

300
316
310
RFOUT
306D
306
304D
304
318
304S
312
308
302G
RFIN
302
302S
GND
314

FIG. 3

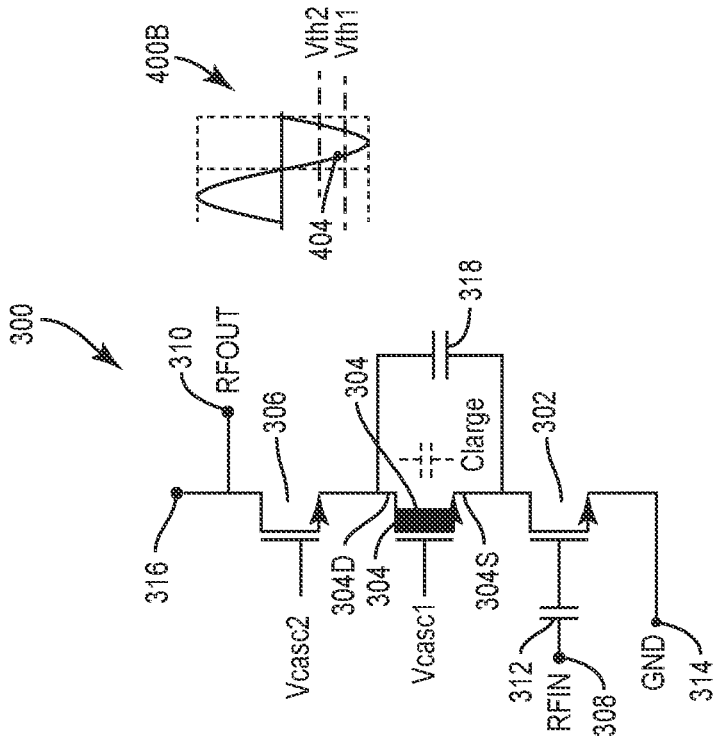

400B
Vth2
Vth1
404
300
310
RFOUT
306
304
318
316
Clarge
302
304D
304
304S
Vcasc2
Vcasc1
312
RFIN
308
GND
314

FIG. 4B

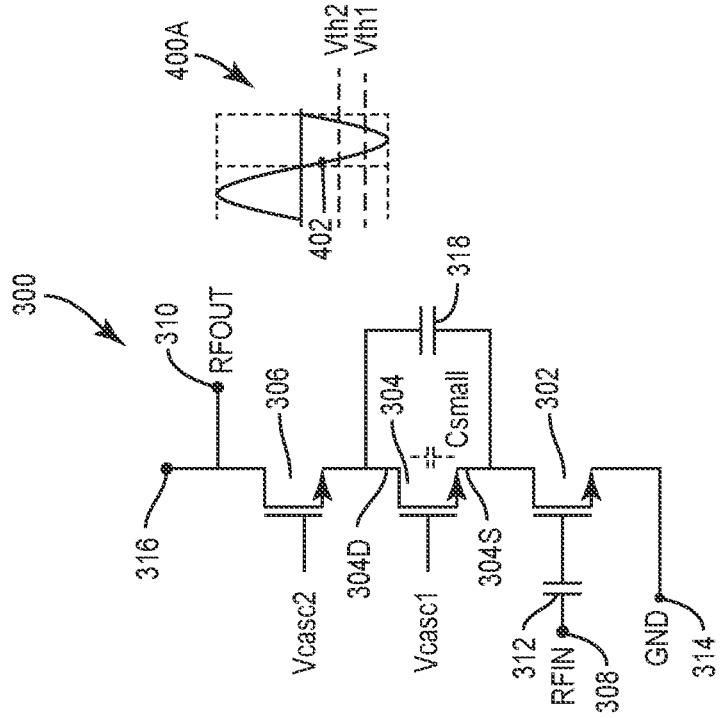

400A
Vth2
Vth1
402
300
310
RFOUT
306
304
318
316
Csmall
302
304D
304S
Vcasc2
Vcasc1
312
RFIN
308
GND
314

FIG. 4A

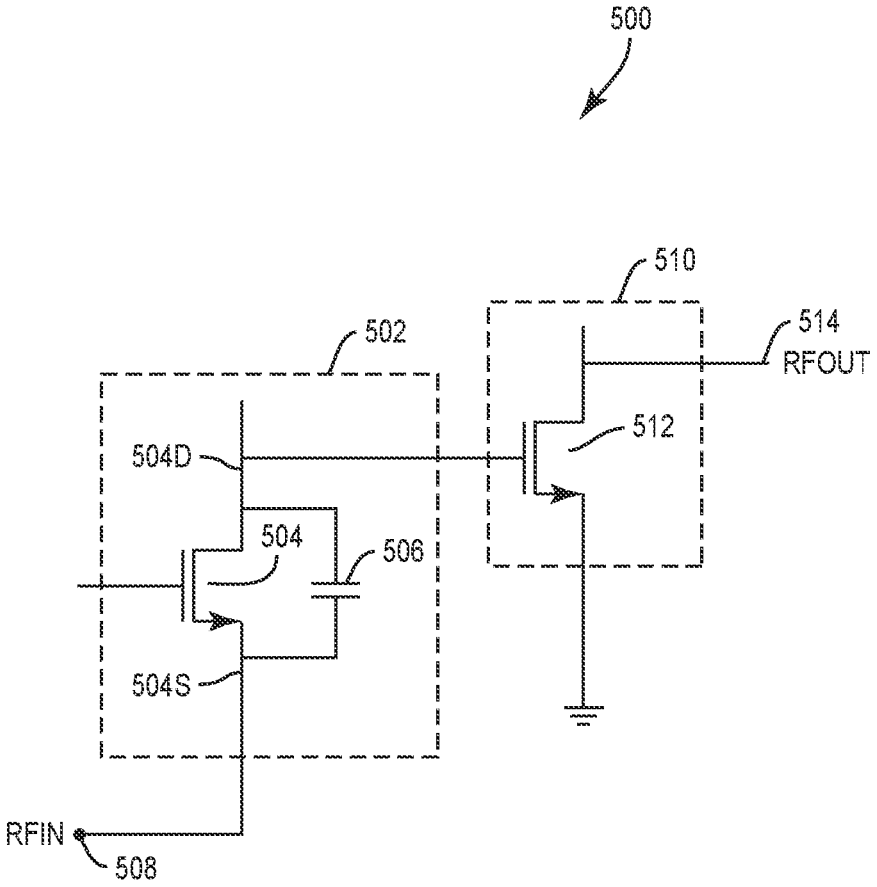


FIG. 5A

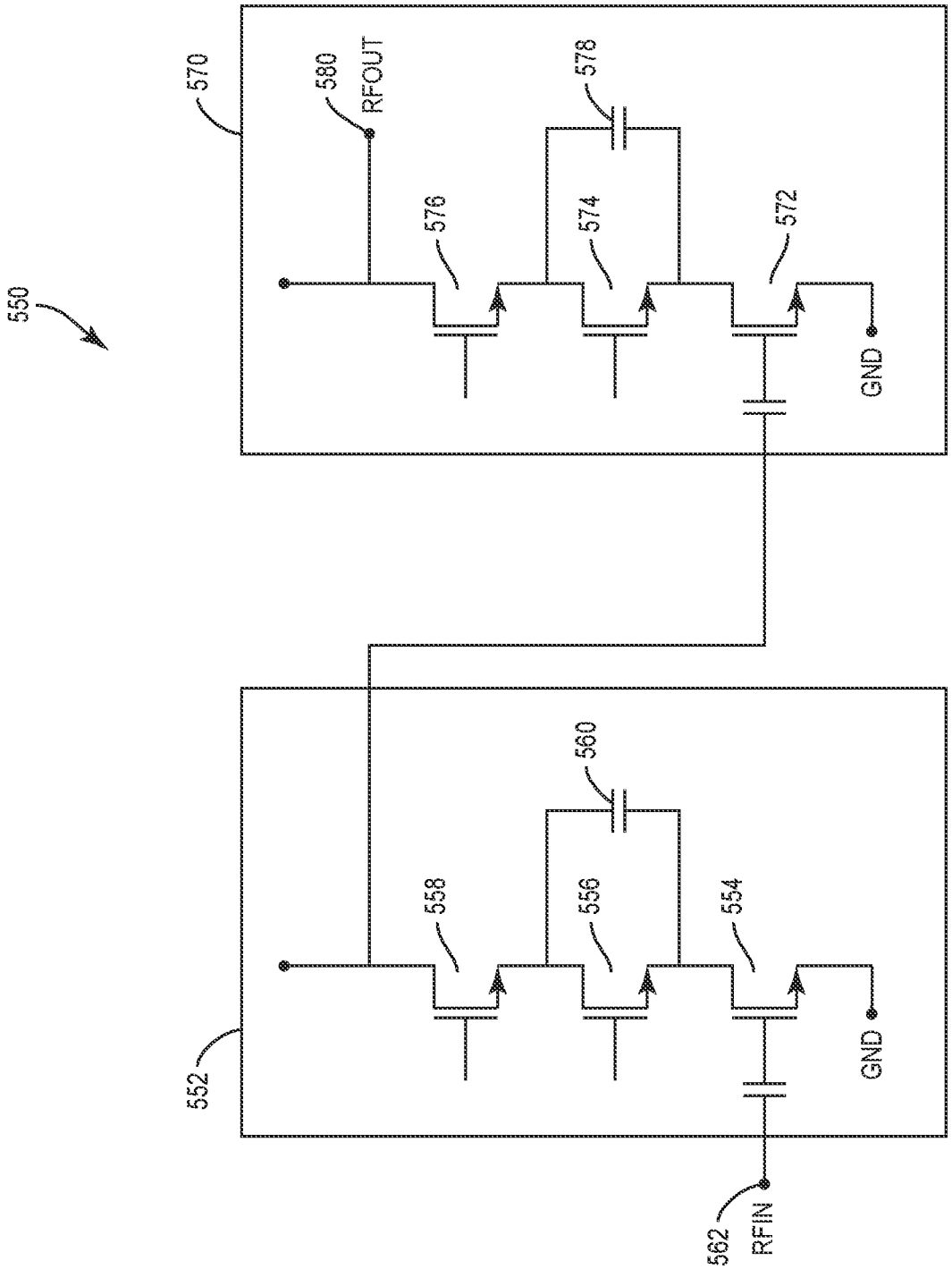

550
570
580
RFOUT
578
576
574
572
GND
552
560
558
556
554
GND
562
RFIN

FIG. 5B

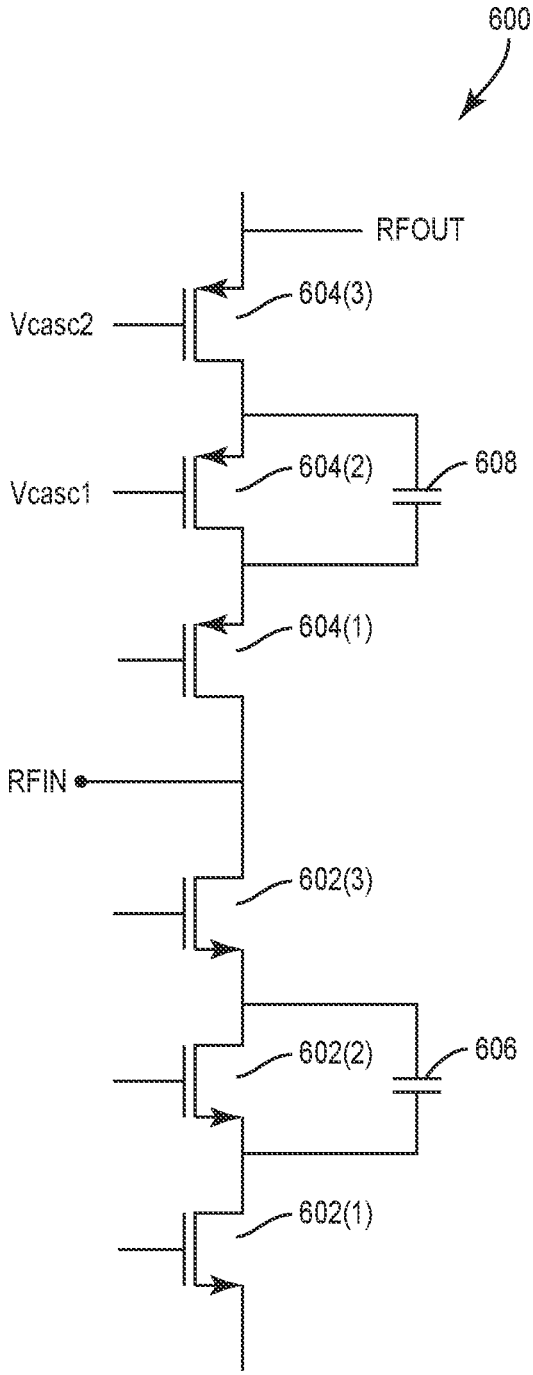

600
RFOUT
604(3)
Vcasc2
604(2)
608
Vcasc1
604(1)
RFIN
602(3)
602(2)
606
602(1)

FIG. 6

AMPLITUDE MODULATION-PHASE MODULATION (AM-PM) LINEARIZATION IN A POWER AMPLIFIER

BACKGROUND

I. Field of the Disclosure

[0001] The technology of the disclosure relates generally to power amplifiers and, more particularly, to power amplifiers with separate transconductance and transimpedance devices that may need improved phase linearity across multiple power levels.

II. Background

[0002] Computing devices abound in modem society, and more particularly, mobile communication devices have become increasingly common. The prevalence of these mobile communication devices is driven in part by the many functions that are now enabled on such devices. Increased processing capabilities in such devices means that mobile communication devices have evolved from pure communication tools into sophisticated mobile entertainment centers, thus enabling enhanced user experiences. The advent of the fifth generation-new radio (5G-NR) cellular standards, and particularly the use of millimeter wave signals creates challenges for power amplifiers used in the transmission chains of such mobile communication devices. Accordingly, there is room for innovation for the power amplifiers.

SUMMARY

[0003] Aspects disclosed in the detailed description include amplitude modulation-phase modulation (AM-PM) linearization in a power amplifier. In particular, exemplary aspects of the present disclosure provide a fixed capacitor in parallel to a cascode device within a power amplifier. The sum of capacitances from the cascode device and the parallel capacitor may be relatively fixed across voltage swings, allowing for small phase changes across a wide range of signal amplitudes passing through the power amplifier. The small phase changes across voltage swings make it easier to provide compensation for such phase changes resulting in a higher linearity power amplifier while also consuming less power, and thus overall being a more efficient device.

[0004] In this regard, in one aspect, a power amplifier stage is disclosed. The power amplifier stage comprises a cascode device. The power amplifier stage also comprises a fixed value capacitor coupled in parallel with the cascode device. The fixed value capacitor is configured to act as a variable capacitor as a function of a radio frequency (RF) signal.

[0005] In another aspect, a power amplifier device is disclosed. The power amplifier device comprises a first stage comprising a first transistor coupled electrically in parallel to a fixed value capacitor. The fixed value capacitor is configured to act as a variable capacitor as a function of an RF signal. The power amplifier device also comprises a second stage comprising a second transistor.

[0006] In another aspect, a power amplifier device is disclosed. The power amplifier device comprises a first stage comprising a first transistor having coupled electrically in parallel a first fixed value capacitor. The first fixed value capacitor is configured to act as a variable capacitor as a function of an RF signal. The power amplifier device also comprises a second stage comprising a second transistor having coupled electrically in parallel a second fixed value capacitor. The second fixed value capacitor is configured to act as a variable capacitor as a function of an RF signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1**A is a circuit diagram of an exemplary conventional cascode power amplifier stage;

[0008] FIG. **1**B is a graph of a power swing versus time showing where cascode transistors typically crush and enter triode mode during operation;

[0009] FIG. **2**A is a circuit diagram showing an effective capacitance of a cascode device within the power amplifier stage at small to medium negative voltages;

[0010] FIG. **2**B is a circuit diagram showing an effective capacitance of the cascode device within the power amplifier stage at large negative voltages;

[0011] FIG. **3** is a circuit diagram of a cascode power amplifier stage with a parallel capacitor added to a cascode device to improve linearity of phase changes according to an exemplary aspect of the present disclosure;

[0012] FIG. **4**A is a circuit diagram showing an effective capacitance of the cascode device and the parallel capacitor within the power amplifier stage of FIG. **3** at small to medium negative voltages;

[0013] FIG. **4**B is a circuit diagram showing an effective capacitance of the cascode device and the parallel capacitor within the power amplifier stage of FIG. **3** at large negative voltages;

[0014] FIG. **5**A is a circuit diagram of a power amplifier device having multiple stages where a first stage is a transimpedance stage with a parallel capacitor and a subsequent stage is a transconductance stage for the power amplifier device;

[0015] FIG. **5**B is a circuit diagram of a power amplifier device having multiple stages where both stages have a middle cascode device with a parallel capacitance to improve phase linearity; and

[0016] FIG. **6** is a circuit diagram of a complementary power amplifier stage having both p-type field effect transistors (FETs) (PFETs) and n-type FETs (NFETs) with parallel capacitors for cascode devices used in both sides of the power amplifier device.

DETAILED DESCRIPTION

[0017] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0018] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be

termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0019] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0020] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0021] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0022] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0023] Aspects disclosed in the detailed description include amplitude modulation-phase modulation (AM-PM) linearization in a power amplifier. In particular, exemplary aspects of the present disclosure provide a fixed capacitor in parallel to a cascode device within a power amplifier. The sum of capacitances from the cascode device and the parallel capacitor may be relatively fixed across voltage swings, allowing for small phase changes across a wide range of signal amplitudes passing through the power amplifier. The small phase changes across voltage swings make it easier to provide compensation for such phase changes resulting in a higher linearity power amplifier while also consuming less power, and thus overall being a more efficient device.

[0024] More specifically, at small to medium negative voltages, the cascode device is active and presents little capacitive loading to the signal path. Accordingly, the parallel capacitor dominates since it has different signals on its two terminals. In contrast, at high negative voltages, the cascode device may be crushed, acting, for example, in a triode mode, causing the parallel capacitor to be bootstrapped (i.e., the parallel capacitor has a low loading effect on the signal path, since both its terminals are effectively seeing the same signal) and allowing an inherent capacitance of the cascode device to dominate. In this fashion, the sum of the capacitances provided by the cascode device and the parallel capacitor remains relatively constant across voltage swings, which in turn causes any phase change (e.g., phase delay) to be small. The small phase change allows for simpler compensation solutions.

[0025] Before addressing particular exemplary aspects of the AM-PM linearization, a brief overview of a source of a phase change is discussed with reference to FIGS. **1**A-**2**B. This induced phase change generated by a non-linear capacitive loading of the signal path leads to non-linear phase behavior, which may require additional circuitry to compensate. The additional circuitry consumes more power and thus decreases overall efficiency and may lead to operation that does not comply with relevant wireless protocols. A discussion of exemplary aspects of the present disclosure begins below with reference to FIG. **3**.

[0026] In this regard, FIG. **1**A is circuit diagram of a power amplifier stage **100** formed from a transconductance device **102**, a middle cascode device **104** and a top cascode transistor **106**. As illustrated, the transconductance device **102**, the middle cascode device **104**, and the top cascode transistor **106** are formed from n-type field effect transistors (FETs) (NFETs). A signal to be amplified (e.g., RFIN) is provided at an input node **108**, and an amplified signal (RFOUT) is provided at an output node **110**. RFIN may pass through a blocking capacitor **112** to a gate **102**G of the transconductance device **102**. The transconductance device **102** provides the primary amplification to RFIN. The middle cascode device **104** and the top cascode transistor **106** are both cascodes relative to the transconductance device **102**. A source **102**S of the transconductance device **102** may be coupled to a ground **114**, and a drain **106**D of the top cascode transistor **106** may be coupled to the output node **110** and a supply voltage **116**.

[0027] In normal use, at low signal swing levels, the transconductance device **102**, the middle cascode device **104**, and the top cascode transistor **106** operate in a saturation mode. However, at peak negative voltages, these devices may be "crushed" or enter a triode mode. This crushing occurs when the drain voltage is less than the gate voltage by more than a device threshold voltage. This concept is better illustrated by graph **150** in FIG. **1**B, where the power amplifier stage **100** operates around a direct current (DC) voltage level **152**. The transconductance device **102**, the middle cascode device **104**, and the top cascode transistor **106** operate in the saturation mode as long as the voltage level of RFOUT is above the DC voltage level **152** (generally shown by curve **154**). Likewise, so long as curve **156** is above line **158**, the transconductance device **102**, the middle cascode device **104**, and the top cascode transistor **106** oper-

ate in the saturation mode. However, at line **158**, the drain voltage of the top cascode transistor **106** is more than a threshold Vth2 below the voltage of the gate voltage of the top cascode transistor **106**, and the top cascode transistor **106** crushes (i.e., enters triode mode of operation). Likewise, when RFOUT passes below line **160**, the drain voltage of the middle cascode device **104** is more than a threshold Vth1 below the voltage of the gate voltage of the middle cascode device **104**, and the middle cascode device **104** crushes.

[0028] Operation in a triode mode also changes the effective capacitance of the middle cascode device **104**. Thus, as shown in FIG. **2**A, when the power amplifier stage **100** is in a saturation mode as shown by dot **200** on line **156**, the loading capacitance between the drain **104**D and the source **104**S is relatively small (Csmall). This capacitance is shown by the dotted capacitor symbol to show its effective existence, even though there is not a specific capacitor element in the circuit. Conversely, when the middle cascode device **104** is crushed and in a triode mode as shown by dot **202** in FIG. **213**, the capacitance between the drain **104**D and the source **104**S is large (Clarge). Again, this capacitance is shown by the dotted capacitor symbol to show its effective existence, even though there is not a specific capacitor element in the circuit. The presence of a non-linear signal level variable capacitance in the power amplifier stage **100** introduces a power dependent phase delay in RFOUT, which constitutes distortion. The presence of a variable capacitance means that the phase delay is non-linear and accordingly harder to correct.

[0029] Exemplary aspects of the present disclosure contemplate adding an effectively variable capacitor in parallel to the middle cascode device. Specifically, a capacitor is added in parallel to the middle cascode device, but bootstrapping by the capacitor makes the equivalent capacitor function like a variable capacitor despite being a fixed capacitor in actuality. Thus, instead of trying to prevent the middle cascode device from crushing, exemplary aspects of the present disclosure embrace the crushed state of the middle cascode device and add an effectively variable capacitor in parallel. The sum of the capacitances loading the signal path from the middle cascode device and the parallel capacitor remains constant over changes in the RFOUT signal level, providing a more constant phase profile over power level. Likewise, the use of a fixed capacitance avoids the need for a variable capacitor such as a varactor, which are notoriously poor at the very high frequencies of interest (e.g., in the millimeter wave signal range common to 5G-NR).

[0030] In this regard, FIG. **3** illustrates a power amplifier stage **300** that includes a cascode structure similar to that of the power amplifier stage **100** and particularly includes a transconductance device **302**, a middle cascode device **304**, and a top cascode transistor **306**. As illustrated, the transconductance device **302**, the middle cascode device **304**, and the top cascode transistor **306** are formed from NFETs. A signal to be amplified (e.g., RFIN) is provided at an input node **308** and an amplified signal (RFOUT) is provided at an output node **310**. RFIN may pass through a blocking capacitor **312** to a gate **302**G of the transconductance device **302**. The transconductance device **302** provides the primary amplification to RFIN. The middle cascode device **304**, and the top cascode transistor **306** are both cascodes relative to the transconductance device **302**. A source **302**S of the transconductance device **302** may be coupled to a ground **314**, and a drain **306**D of the top cascode transistor **306** may be coupled to the output node **310** and a supply voltage **316**.

[0031] A capacitor **318** having a fixed value is placed electrically in parallel to the middle cascode device **304**. Specifically, the capacitor **318** is coupled to the drain **304**D and the source **304**S of the middle cascode device **304**. Depending on the RF signal level, there will be a variable bootstrapping effect, which causes the capacitor **318** to appear to be variable, despite its inherently fixed nature. This variation is illustrated in FIGS. **4**A and **4**B. Specifically, as illustrated in FIG. **4**A, when the middle cascode device **304** operates in a saturation mode (e.g., point **402** on graph **400**A), the associated capacitance of the middle cascode device **304** is relatively small (Csmall) and the voltage difference between the drain **304**D and the source **304**S is relatively large. The Csmall capacitance is shown by the dotted capacitor symbol to show its effective existence, even though there is not a specific capacitor element in the circuit. This large voltage difference between the source **304**S and the drain **304**D means that the capacitor **318** will show its loading capacitive effect to the signal path.

[0032] In contrast, in FIG. **413**, the middle cascode device **304** is crushed (e.g., point **404** in graph **400**B). Accordingly, there is little signal difference between the drain **304**D and the source **304**S and the effective capacitance of the middle cascode device **304** is relatively large (Clarge). Again, this capacitance is shown by the dotted capacitor symbol to show its effective existence, even though there is not a specific capacitor element in the circuit. However, because there is little signal difference between the drain **304**D and the source **304**S, the capacitor **318** is effectively bootstraped to show a very small or negligible capacitance to the signal path. Thus, even though the inherent capacitance of the capacitor **318** is fixed, the capacitor **318** functions as a variable capacitor as a function of the RF signal level.

[0033] While the example of the power amplifier stage **300** is shown using NFETs and a single cascoded stage, the teachings of the present disclosure are not so limited. The teachings of the present disclosure may also be applied to power amplifier stages formed from PFETs, complementary metal oxide semiconductor (CMOS) FET arrangements, bulk CMOS devices, silicon on insulator (SOI) CMOS devices, silicon on sapphire (SOS) CMOS devices, or the like. The SOI CMOS devices may be partially- or fully-depleted. Additionally, the transistors may be junction-gate FETs (JFETs), pseudomorphic high electron mobility transistors (PHEMTs), or the like. While all the examples provided are single-ended devices, it should also be appreciated that the concepts of the present disclosure are applicable to differential, quadrature, or other devices. The stages may be combined in a Doherty, hybrid-combining, or out-phasing fashion.

[0034] Still further, aspects of the present disclosure may be applied to a power amplifier device that has multiple stages and, in particular, has a transimpedance device in a first stage (e.g., a common-gate amplifier) and a transconductance device in a second stage (e.g., common-source amplifier), as better illustrated in FIG. **5**A. In particular, a power amplifier device **500** may include a first stage **502** that includes a transimpedance device **504**. The transimpedance device **504** may be a FET and, as illustrated, is an NFET. The transimpedance device **504** has a capacitor **506** coupled in parallel and thus is analogous to the middle cas-

code device **304** of FIG. **3**. The capacitor **506** may be coupled to a drain **504**D and a source **504**S of the transimpedance device **504**. The first stage **502** includes an input node **508** and couples to a second stage **510**. The second stage **510** includes a transconductance device **512**, which may be a FET. The second stage **510** couples to an output node **514**. In operation, the capacitor **506** operates similarly to the capacitor **318**. The transimpedance device **504** and the transconductance device **512** may be of any type and in any combination (n-type, p-type, complementary-type with both n and p).

[0035] FIG. **5**B shows an alternate embodiment of a multi-stage power amplifier **550** with a first stage **552** that includes a transconductance device **554** and associated middle cascode device **556** and top cascode transistor **558**. The devices **554**, **556**, and **558** may be FETs and, as illustrated, are NFETs. The middle cascode device **556** has a capacitor **560** coupled in parallel and thus is analogous to the middle cascode device **304**. The capacitor **560** may be coupled to a drain and a source of the middle cascode device **556**. The first stage **552** includes an input node **562** and couples to a second stage **570**. The second stage **570** includes a transconductance device **572** and associated middle cascode device **574** and top cascode transistor **576**. The devices **572**, **574**, and **576** may be FETs and, as illustrated, are NFETs. The middle cascode device **574** has a capacitor **578** coupled in parallel and thus is analogous to the middle cascode device **304**. The capacitor **578** may be coupled to a drain and a source of the middle cascode device **574**. The top cascode transistor **576** may be coupled to a gate of the transconductance device **572**, and the top cascode transistor **576** may be coupled to an output **580**.

[0036] More complicated power amplifiers may be implemented, having any number of constituent stages, wherein at least one stage includes a cascode device and/or a transimpedance device that has a parallel capacitance connected to reduce the phase variation over power level, and thus linearize the stage.

[0037] FIG. **6** illustrates a CMOS power amplifier stage **600** that includes NFETs **602**(**1**)-**602**(**3**) and PFETs **604**(**1**)-**604**(**3**) that operate as transconductance, middle cascode, and top cascode transistors as is understood. Capacitors **606** and **608** are placed in parallel to the middle cascode devices **602**(**2**) and **604**(**2**) and function like the capacitor **318**.

[0038] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations. Thus, the disclosure is not intended to be limited to the examples and designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A power amplifier stage comprising:
a cascode device; and
a fixed value capacitor coupled in parallel with the cascode device, wherein the fixed value capacitor is configured to act as a variable capacitor as a function of a radio frequency (RF) signal.

2. The power amplifier stage of claim **1**, wherein the cascode device comprises a field effect transistor (FET).

3. The power amplifier stage of claim **2**, further comprising a transconductance device coupled to the cascode device.

4. The power amplifier stage of claim **1**, further comprising a second cascode transistor coupled to the cascode device.

5. The power amplifier stage of claim **2**, wherein the FET comprises an n-type FET (NFET).

6. The power amplifier stage of claim **2**, wherein the FET comprises a p-type FET (PFET).

7. The power amplifier stage of claim **2** implemented in a bulk complementary metal oxide semiconductor (CMOS) device.

8. The power amplifier stage of claim **2** implemented in a silicon on insulator (SOI) complementary metal oxide semiconductor (CMOS) device.

9. The power amplifier stage of claim **2** implemented in a silicon on sapphire (SOS) complementary metal oxide semiconductor (CMOS) device.

10. The power amplifier stage of claim **2**, wherein the FET comprises a drain and a source and the fixed value capacitor is coupled to the drain and the source.

11. The power amplifier stage of claim **1**, wherein the fixed value capacitor presents a large capacitance when the cascode device operates in a saturation mode.

12. The power amplifier stage of claim **11**, wherein the fixed value capacitor presents a small capacitance when the cascode device operates in a triode mode.

13. A power amplifier device comprising:
a first stage comprising a first transistor coupled electrically in parallel to a fixed value capacitor, wherein the fixed value capacitor is configured to act as a variable capacitor as a function of a radio frequency (RF) signal; and
a second stage comprising a second transistor.

14. The power amplifier device of claim **13**, wherein the first transistor and the second transistor comprise an n-type material or a p-type material.

15. The power amplifier device of claim **13**, wherein the first transistor and the second transistor are implemented as a complementary metal oxide semiconductor (CMOS) device.

16. The power amplifier device of claim **13**, wherein the first transistor and the second transistor are implemented in one of the following technologies: bulk complementary metal oxide semiconductor (CMOS), silicon on insulator (SOI) CMOS, and silicon on sapphire (SOS) CMOS.

17. A power amplifier device comprising:
a first stage comprising a first transistor having coupled electrically in parallel a first fixed value capacitor, wherein the first fixed value capacitor is configured to act as a variable capacitor as a function of a radio frequency (RF) signal; and
a second stage comprising a second transistor having coupled electrically in parallel a second fixed value capacitor, wherein the second fixed value capacitor is configured to act as a variable capacitor as a function of an RF signal.

18. The power amplifier device of claim **17**, wherein the first transistor and the second transistor are implemented with one of the following types of devices: n-type, p-type, or complementary (both n-type and p-type).

19. The power amplifier device of claim **17**, wherein the first transistor and the second transistor are implemented in one of the following technologies: bulk complementary metal oxide semiconductor (CMOS), silicon on insulator (SOI) CMOS, and silicon on sapphire (SOS) CMOS.

20. The power amplifier stage of claim **17**, wherein the first transistor and the second transistor are implemented with different types of devices, one n-type and the other p-type.

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