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(54) **THIN FILM TRANSISTOR, METHOD FOR MANUFACTURING THE SAME, AND ARRAY SUBSTRATE**

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(57) **ABSTRACT**

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The embodiments of present disclosure provide a thin film transistor, a method for manufacturing the same, and an array substrate. The thin film transistor comprises an active layer provided on a substrate, the active layer including a middle channel region, a first high resistance region and a second high resistance region provided respectively on external sides of the middle channel region, a source region provided on an external side of the first high resistance region and a drain region provided on an external side of the second high resistance region, wherein a base material of the active layer is diamond single crystal. According to the thin film transistor, the method for manufacturing the same, and the array substrate provided in the embodiments of present disclosure, by providing high resistance regions on external sides of the middle channel region of the active layer, the carrier mobility is reduced and the leakage current of the thin film transistor made of single crystalline diamond is effectively suppressed.

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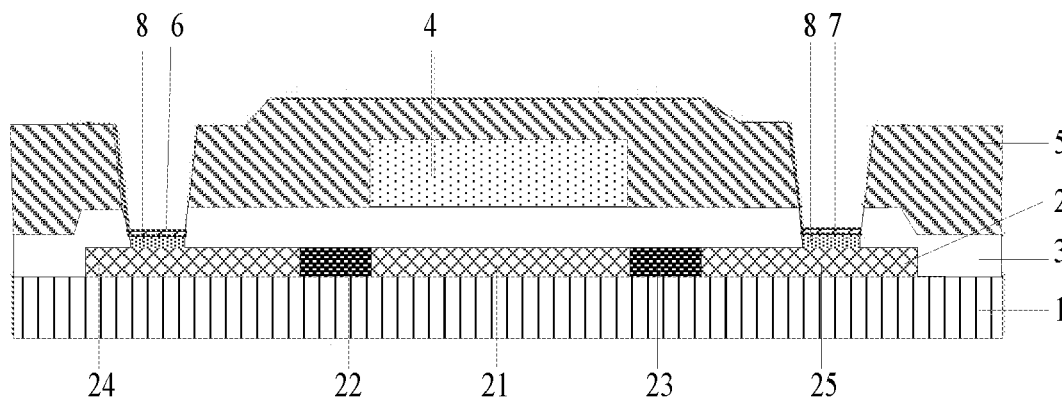
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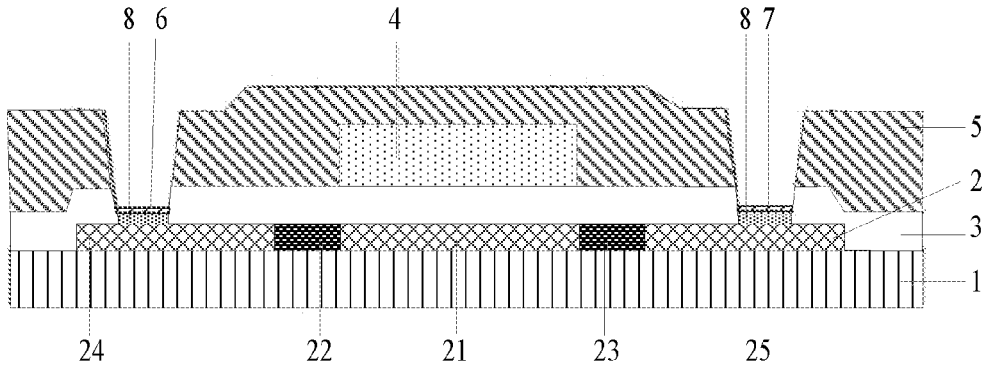


Fig. 1

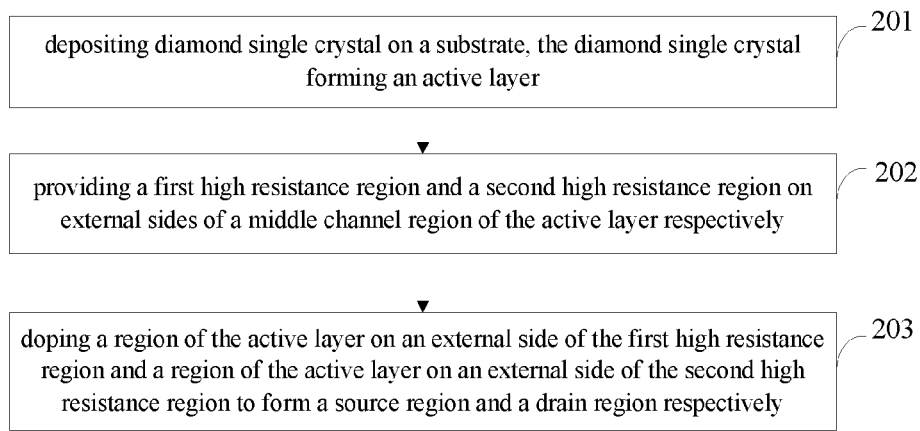


Fig. 2

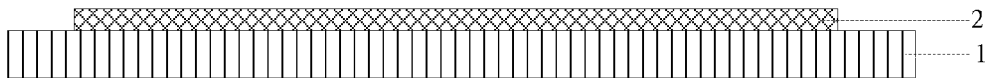


Fig. 3A

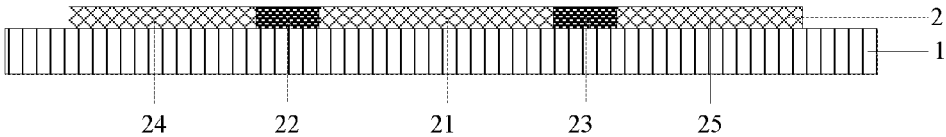


Fig. 3B

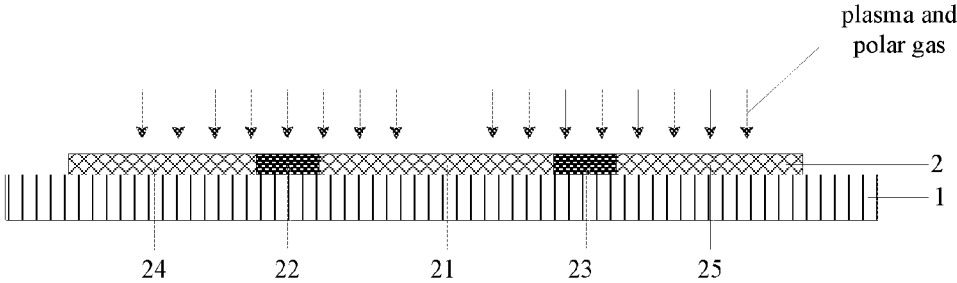


Fig. 3C

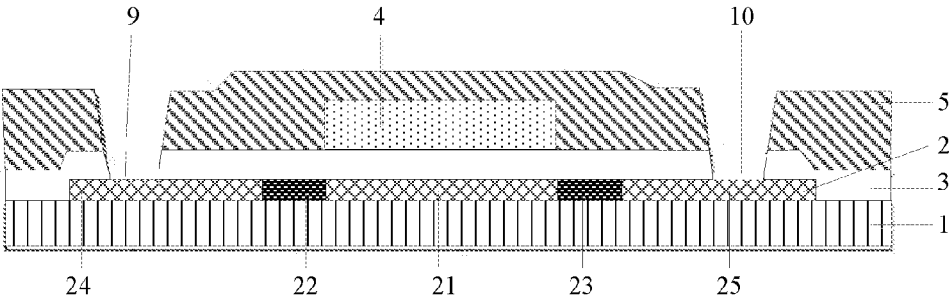


Fig. 3D

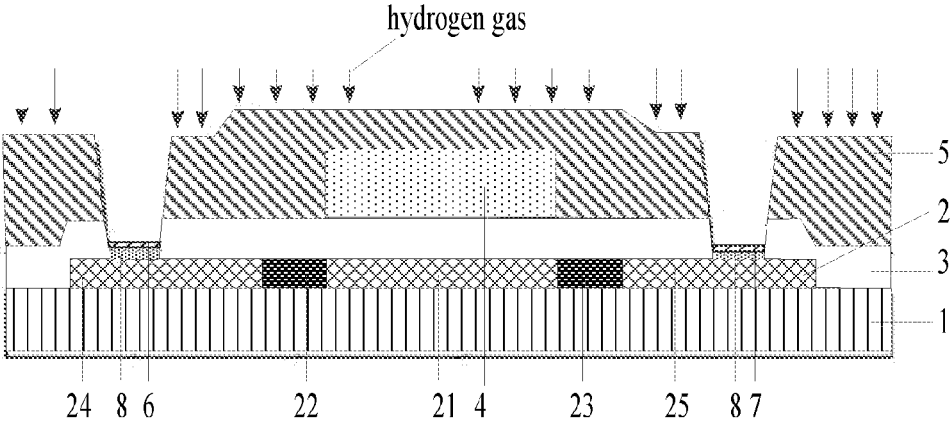


Fig. 3E

**THIN FILM TRANSISTOR, METHOD FOR
MANUFACTURING THE SAME, AND ARRAY
SUBSTRATE**

CROSS-REFERENCE TO RELATED
APPLICATIONS

[0001] This application claims priority of Chinese Patent Application No. 201510125633.X filed on Mar. 20, 2015, the entire disclosure of which is incorporated herein by reference as a part of this application.

TECHNICAL FIELD

[0002] Embodiments of present disclosure relate to a thin film transistor, a method for manufacturing the same, and an array substrate.

BACKGROUND

[0003] Commonly used flat display panels include Liquid Crystal Display (LCD) panels and Organic Light-Emitting Diode (OLED) display panels. An LCD display panel or an OLED display panel includes an array substrate. The array substrate includes a plurality of pixel circuits arranged in an array and consisting of thin film transistors (TFTs), and each pixel circuit corresponds to one subpixel unit. Thin film transistor, as a control switch of a display panel pixel, is directly related to a developing trend for high-performance flat display panels.

[0004] Currently, a thin film transistor in an array substrate includes a gate, a source and a drain as well as an active layer formed between the source/drain and the gate. In order to improve performance of a display panel, it is necessary to improve carrier mobility of the active layer as much as possible. Diamond single crystal has a high carrier mobility and good TFT properties, and is a potentially excellent material for the next-generation TFTs. However, due to the high mobility of this material, leakage current of the TFT device is large, which has an adverse impact on operation characteristics of the TFT device. If such an impact lasts for a long period of time, TFT characteristics will deteriorate and quality of products will decline.

SUMMARY OF THE INVENTION

[0005] Embodiments of present disclosure provide a thin film transistor, a method for manufacturing the same, and an array substrate, so as to reduce leakage current of the thin film transistor.

[0006] In a first aspect, the embodiments of present disclosure provide a thin film transistor, comprising an active layer provided on a substrate, the active layer including a middle channel region, a first high resistance region and a second high resistance region provided respectively on external sides of the middle channel region, a source region provided on an external side of the first high resistance region, and a drain region provided on an external side of the second high resistance region, wherein a base material of the active layer is diamond single crystal.

[0007] Those skilled in the art can understand that the "external side" herein is relative to a center of the thin film transistor.

[0008] Further, a base material of the middle channel region, the source region and the drain region is (111)-face diamond single crystal, and a base material of the first high

resistance region and the second high resistance region is (100)-face diamond single crystal.

[0009] Further, the active layer has been treated with plasma and polar gas.

[0010] Further, the thin film transistor further comprises a source electrode provided on the source region, a drain electrode provided on the drain region, and a carbonized metal layer provided between the source electrode and the source region and between the drain electrode and the drain region.

[0011] Further, the thin film transistor further comprises a gate insulating layer and a gate electrode, wherein the gate insulating layer is provided on the active region and the gate electrode is provided on the gate insulating layer; the gate insulating layer is provided with a first via-hole exposing the source region and a second via-hole exposing the drain region; the source electrode and the drain electrode are formed in the first via-hole of the source region and the second via-hole of the drain region, respectively.

[0012] In a second aspect, the embodiments of present disclosure further provide an array substrate comprising above thin film transistor.

[0013] In a third aspect, the embodiments of present disclosure further provide a method for manufacturing a thin film transistor, comprising:

[0014] depositing diamond single crystal on a substrate, the diamond single crystal forming an active layer;

[0015] providing a first high resistance region and a second high resistance region on external sides of a middle channel region of the active layer respectively; and

[0016] doping a region of the active layer on an external side of the first high resistance region and a region of the active layer on an external side of the second high resistance region to form a source region and a drain region respectively.

[0017] Further, the deposited diamond single crystal is (111)-face diamond single crystal; and

[0018] the providing a first high resistance region and a second high resistance region on external sides of a middle channel region of the active layer respectively comprises:

[0019] etching away (111)-face diamond single crystal in a predetermined first high resistance region and a predetermined second high resistance region, and depositing (100)-face diamond single crystal in the predetermined first high resistance region and the predetermined second high resistance region.

[0020] Further, the method further comprises:

[0021] forming a gate insulating layer on the active layer, and forming a gate electrode on the gate insulating layer; and

[0022] etching a first via-hole and a second via-hole in the source region and the drain region respectively, and depositing metal in the first via-hole and the second via-hole respectively to form a source electrode and a drain electrode.

[0023] Further, the method further comprises:

[0024] performing a rapid thermal annealing treatment on the source electrode and the drain electrode to form a carbonized metal layer between the source electrode and the source region and between the drain electrode and the drain region respectively.

[0025] Further, the depositing diamond single crystal on a substrate comprises:

[0026] depositing (111)-face diamond single crystal on the substrate, wherein a deposition temperature is 780-850° C., a deposition pressure is 16-18 KPa, a flow ratio of methane

to hydrogen gas is 0.5%-1%, a deposition power is 3-5 KW, a deposition rate is 0.01-0.02 $\mu\text{m}/\text{min}$, and a deposition period is 10-15 mins.

[0027] Further, a deposition condition for the depositing (100)-face diamond single crystal in the predetermined first high resistance region and the predetermined second high resistance region includes a deposition temperature of 900-1000° C., a deposition pressure of 21-23 KPa, a flow ratio of methane to hydrogen gas of 3%-4%, a deposition power of 5-7 KW, a deposition rate of 0.1-0.2 $\mu\text{m}/\text{min}$, and a deposition period of 2-3 mins.

[0028] As can be seen from the technical solutions above, the embodiments of present disclosure provide a thin film transistor, a method for manufacturing the same, and an array substrate, wherein the thin film transistor is provided with high resistance regions on external sides of the middle channel region of the active layer, thereby reducing the carrier mobility and effectively suppressing the leakage current of the thin film transistor made of single crystal diamond.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] For the sake of illustrating the technical solutions of the embodiments of present disclosure more clearly, a brief introduction to drawings of the embodiments is made as follows. Apparently, the following drawings merely relate to some embodiments of present disclosure, and do not limit present disclosure.

[0030] FIG. 1 is a structural diagram of a thin film transistor provided in an embodiment of present disclosure;

[0031] FIG. 2 is a flow diagram of a method for manufacturing a thin film transistor provided in an embodiment of present disclosure; and

[0032] FIGS. 3A-3E are structural diagrams of a process for manufacturing a thin film transistor provided in an embodiment of present disclosure.

DETAILED DESCRIPTION OF THE INVENTION

[0033] The technical solutions of the embodiments of the present invention will be described clearly and thoroughly hereinafter in conjunction with the drawings in respective embodiments in order to make the objects, technical solutions and advantages of the embodiments of the disclosure more clear. Obviously, the embodiments described are only some rather than all of the embodiments of the disclosure. All other embodiments obtained by one ordinary person skilled in the art based on the described embodiments in the disclosure without creative work are within the scope of the present disclosure.

[0034] In the description of the present disclosure, it should be noted that the oriental or positional relationship indicated by the terms "upper", "lower", "top", "bottom" or the like is the oriental or positional relationship shown in the drawings, and such terms are used only for the purpose of description and simplifying the description rather than indicating or suggesting that the device or element indicated must be in a specific orientation, be structured and operated in a specific orientation. Such terms shall not be deemed to limit the scope of the present invention.

[0035] Diamond single crystal has high thermal conductivity, wide bandgap, high carrier mobility ($>1300 \text{ V}\cdot\text{S}/\text{cm}^2$) and other excellent properties. Therefore diamond can be

used as a material for both active devices and passive devices in the field of semiconductor technology. However, due to the high carrier mobility of the diamond single crystal, a semiconductor device made of it has high carrier mobility and thus the leakage current at zero Volt is large (10^{-10} - 10^{-7} mA). In addition, since a source electrode and a drain electrode are used for current input and output of the semiconductor device, they are generally made of metal. If the diamond single crystal is used as an active layer of a transistor, the contact between electrodes and semiconductor layers is substantially a contact between the metal and the diamond single crystal. A resistance of contact between the metal and the diamond single crystal directly affects the current-voltage (IV) characteristics of the thin film transistor. The larger the contact resistance is, the larger the parasitic resistance between the source and the drain of the device is, which will not only increase power consumption and noise of the circuit but also affect the speed of the circuit. That is, a desired ohmic contact cannot be formed between the diamond single crystal and the metal.

[0036] By making use of advantages of the diamond single crystal, the embodiments of present disclosure provide a semiconductor device made with the diamond single crystal, thereby reducing the leakage current of the semiconductor device made of the diamond single crystal.

[0037] FIG. 1 shows a structural diagram of a thin film transistor provided in an embodiment of present disclosure. As shown in FIG. 1, the thin film transistor comprises an active layer 2 provided on a substrate 1. The active layer 2 includes a middle channel region 21, a first high resistance region 22 and a second high resistance region 23 provided respectively on external sides of the middle channel region 21, a source region 24 provided on an external side of the first high resistance region 22, and a drain region 25 provided on an external side of the second high resistance region 23. The high resistance region refers to a region whose resistivity is higher than those of the middle channel region, the source region and the drain region.

[0038] A base material of the active layer 2 of aforesaid thin film transistor is diamond single crystal. By providing the first high resistance region 22 and the second high resistance region 23 on external sides of the middle channel region 21 of the active layer 2, the carrier mobility is reduced and the leakage current of the thin film transistor can be effectively suppressed.

[0039] In the present embodiment, the first high resistance region 22 and the second high resistance region 23 are provided on external sides of the middle channel region 21, the source region 24 is provided on the external side of the first high resistance region 22, and the drain region 25 is provided on the external side of the second high resistance region 23. In this way, when electrons are transmitted in the source region, the channel region and the drain region, they must pass through the first high resistance region 22 and the second high resistance region 23, thereby decreasing a transmission speed and kinetic energy of the electrons and reaching the goal of suppressing leakage current.

[0040] Specifically, a base material of the middle channel region, the source region and the drain region is (111)-face diamond single crystal, and a base material of the first high resistance region and the second high resistance region is (100)-face diamond single crystal. On one hand, the use of the diamond single crystals having different crystal orientations reduces the migration of the carriers and suppresses

the leakage current of the thin film transistor; on the other hand, the (100)-face diamond single crystal can also be used as a buffer zone due to its low carrier mobility.

[0041] It is understandable that a length of the first high resistance region and a length of the second high resistance region are not restricted in this embodiment. The length of the first high resistance region and the length of the second high resistance region can be preset in accordance with actual needs to reduce leakage current while ensuring the conductive property of the thin film transistor to be stable.

[0042] In an exemplary embodiment of present disclosure, in order to improve stability of the thin film transistor, the (100)-face diamond single crystal and the (111)-face diamond single crystal in the active layer, i.e., the (111)-face diamond single crystal as a base body of above-described middle channel region, source region and drain region and the (100)-face diamond single crystal as a base body of the first high resistance region and the second high resistance region, are treated with plasma and polar gas. The plasma may be oxygen plasma, and the polar gas may include gas such as N_2 , NH_3 or the like.

[0043] In an exemplary embodiment of present disclosure, the thin film transistor further comprises a source electrode **6** provided on the source region **24**, a drain electrode **7** provided on the drain region **25**, and a carbonized metal layer **8** provided between the source electrode **6** and the source region **24** and between the drain electrode **7** and the drain region **25**. By providing the carbonized metal layer between the source electrode **6** and the source region **24** and between the drain electrode **7** and the drain region **25**, it is facilitated to form a good ohmic contact between the source electrode and the source region and between the drain electrode and the drain region, thereby improving the stability of the thin film transistor.

[0044] In an exemplary embodiment of present disclosure, the thin film transistor further comprises a gate insulating layer **3** and a gate electrode **4**, wherein the gate insulating layer **3** is provided on the active region **2** and the gate electrode **4** is provided on the gate insulating layer **3**; the gate insulating layer **3** is provided with a first via-hole exposing the source region and a second via-hole exposing the drain region; the source electrode and the drain electrode are formed in the first via-hole of the source region and the second via-hole of the drain region respectively.

[0045] In an exemplary embodiment of present disclosure, in order to achieve the electrical insulation between conductor areas and metals inside the thin film transistor and the isolative protection from the surroundings, an interlayer dielectric (ILD) layer **5** is provided on the gate electrode **4**. As with the gate insulating layer **3**, the interlayer dielectric layer **5** is provided with via-holes at positions of the first via-hole exposing the source region and the second via-hole exposing the drain region in the gate insulating layer **3**, and the via-holes are provided at the same positions as the first via-hole and the second via-hole.

[0046] In above thin film transistor, by providing high resistance regions on external sides of the middle channel region of the active layer, diamond single crystals having different crystal orientations are used in the high resistance regions and other regions of the active layer, thereby reducing the carrier mobility and effectively suppressing the leakage current of the thin film transistor. Further, the active layer is treated with plasma and polar gas to form a stable channel region. Further, by providing a carbonized metal

layer between the source electrode and the source region and between the drain electrode and the drain region, it is facilitated to form a good ohmic contact between the source electrode and the source region and between the drain electrode and the drain region, thereby improving the stability of the thin film transistor.

[0047] FIG. 2 shows a flow diagram of a method for manufacturing a thin film transistor provided in an embodiment of present disclosure. As shown in FIG. 2, the method comprises the following steps:

[0048] Step **201**: depositing diamond single crystal on a substrate, the diamond single crystal forming an active layer;

[0049] Step **202**: providing a first high resistance region and a second high resistance region on external sides of a middle channel region of the active layer respectively; and

[0050] Step **203**: doping a region of the active layer on an external side of the first high resistance region and a region of the active layer on an external side of the second high resistance region to form a source region and a drain region respectively.

[0051] The deposited diamond single crystal may be (111)-face diamond single crystal.

[0052] By providing the first and second high resistance regions on external sides of the middle channel region of the active layer, aforesaid method reduces the carrier mobility and effectively suppresses the leakage current of the thin film transistor.

[0053] It is noted that the structure of the thin film transistor provided in present embodiment may be an NMOS structure or a PMOS structure. For the sake of convenience of explanation, the following description is made by taking the NMOS structure as an example.

[0054] Hereinafter a detailed description to the method for manufacturing a thin film transistor is presented in conjunction with FIGS. 3A-3E.

[0055] Step **201** may specifically comprise depositing (111)-face diamond single crystal on a substrate through a process such as Microwave Plasma Chemical Vapor Deposition (MPCVD), the diamond single crystal forming an active layer, as shown in FIG. 3A.

[0056] In an exemplary embodiment, the (111)-face diamond single crystal is deposited on the substrate, wherein a deposition temperature is 780-850° C., a deposition pressure is 16-18 KPa, a flow ratio of methane to hydrogen gas is 0.5%-1%, a deposition power is 3-5 KW, a deposition rate is 0.01-0.02 $\mu\text{m}/\text{min}$, and a deposition period is 10-15 mins.

[0057] The selection of the substrate material primarily depends on the following factors: structural properties, interface properties, chemical stability, thermal properties, electrical conductivity, optical properties and mechanical properties, and these factors need to be taken into consideration when a substrate and a corresponding epitaxial layer are selected. Since silicon is a good heat conductor, a device made of silicon has a good heat conductivity so as to prolong a service life of the device. Therefore in this embodiment, description is made by taking single crystalline silicon substrate as an example. It is noted that in addition to silicon, the substrate material may be silicon carbide (SiC), gallium nitride (GaN), gallium arsenide (GaAs) or the like.

[0058] Step **202** may specifically comprise etching away, through a dry etching process, the (111)-face diamond single crystal from the lightly doped source and drain regions of the active layer, i.e., the (111)-face diamond single crystal in a

predetermined first high resistance region and a predetermined second high resistance region, and depositing (100)-face diamond single crystal in the predetermined first high resistance region and the predetermined second high resistance region, as shown in FIG. 3B. Due to the use of diamond single crystals having different crystal orientations, the migration of the carriers slows down, thereby suppressing the leakage current of the thin film transistor.

[0059] In an exemplary embodiment of present disclosure, the (100)-face diamond single crystal is deposited in the predetermined first high resistance region and the predetermined second high resistance region at a deposition temperature of 900-1000° C., a deposition pressure of 21-23 KPa, a flow ratio of methane to hydrogen gas of 3%-4%, a deposition power of 5-7 KW, a deposition rate of 0.1-0.2 μm/min for a deposition period of 2-3 mins.

[0060] After Step 202, in order to improve the stability of the diamond thin film, in an exemplary embodiment of present disclosure, the diamond base body may be firstly treated with oxygen plasma to form C-O bonds on the surface thereof, and then polar gas (e.g., N₂, or NH₃ or the like) is introduced into the OVEN chamber so that nitrogen atoms or hydrogen atoms are combined with oxygen. At this time, a stable P channel region is formed below the surface of diamond, thereby enhancing the stability of the device, as shown in FIG. 3C.

[0061] In Step 203, a region of the active layer on an external side of the first high resistance region and a region of the active layer on an external side of the second high resistance region are doped to increase the electrical conductivity of these regions. For example, by ion implantation, if the thin film transistor is an N-type one, a region of the active layer on the external side of the first high resistance region and a region of the active layer on the external side of the second high resistance region are doped with a pentavalent impurity element such as phosphorus, arsenic or the like, thereby forming the source region and the drain region respectively.

[0062] In another exemplary embodiment of present disclosure, if the thin film transistor is a P-type one, a region of the active layer on the external side of the first high resistance region and a region of the active layer on the external side of the second high resistance region are doped with a trivalent impurity element such as boron, gallium or the like, thereby forming the source region and the drain region respectively.

[0063] In an exemplary embodiment of present disclosure, aforesaid method further comprises Step 204 not shown in FIG. 2.

[0064] Step 204: forming a gate insulating layer on the active layer and forming a gate electrode on the gate insulating layer; performing implantation of atoms such as B atoms in the source region and the drain region; depositing an ILD layer; and etching a first via-hole and a second via-hole in the source region and the drain region respectively, as shown in FIG. 3D.

[0065] In an exemplary embodiment of present disclosure, aforesaid method further comprises Step 205 not shown in FIG. 2.

[0066] Step 205: depositing, through a self-aligning process, metal on a surface of the source region in the first via-hole 9 and a surface of the drain region in the second via-hole 10 to form a source electrode and a drain electrode, and performing a rapid thermal annealing (RTA) treatment

on the source electrode and the drain electrode to form a carbonized metal layer between the source electrode and the source region and between the drain electrode and the drain region respectively, as shown in FIG. 3E.

[0067] In an exemplary embodiment of present disclosure, the metal deposited on the surface of the source region and the surface of the drain region may be one or more of W, Ti, Mo and the like, and the rapid thermal annealing (RTA) treatment is performed at a temperature of 450-500° C. for 1-2 hours.

[0068] In an exemplary embodiment of present disclosure, Step 205 further comprises hydrotreating above the ILD layer to obtain a better stability of electrical characteristics.

[0069] By forming a carbonized metal layer between the source electrode and the source region and between the drain electrode and the drain region in above steps, a good ohmic contact is formed between the source electrode and the source region and between the drain electrode and the drain region, thereby improving the stability of the thin film transistor.

[0070] The embodiments of present disclosure further provide an array substrate comprising the thin film transistor according to above embodiments.

[0071] The aforesaid embodiments are only exemplary embodiments of the disclosure, and do not intend to limit the scope of the disclosure. The scope of the disclosure is defined by the appended claims.

1. A thin film transistor, comprising an active layer provided on a substrate, the active layer including a middle channel region, a first high resistance region and a second high resistance region provided respectively on external sides of the middle channel region, a source region provided on an external side of the first high resistance region, and a drain region provided on an external side of the second high resistance region, wherein

a base material of the active layer is diamond single crystal.

2. The thin film transistor according to claim 1, wherein a base material of the middle channel region, the source region and the drain region is (111)-face diamond single crystal, and a base material of the first high resistance region and the second high resistance region is (100)-face diamond single crystal.

3. The thin film transistor according to claim 1, wherein the active layer has been treated with plasma and polar gas.

4. The thin film transistor according to claim 1, further comprising a source electrode provided on the source region and a drain electrode provided on the drain region, and a carbonized metal layer provided between the source electrode and the source region and between the drain electrode and the drain region.

5. The thin film transistor according to claim 4, further comprising a gate insulating layer and a gate electrode, wherein

the gate insulating layer is provided on the active region and the gate electrode is provided on the gate insulating layer; the gate insulating layer is provided with a first via-hole exposing the source region and a second via-hole exposing the drain region; and the source electrode and the drain electrode are formed in the first via-hole of the source region and the second via-hole of the drain region respectively.

6. An array substrate, comprising the thin film transistor according to claim 1.

7. A method for manufacturing a thin film transistor, comprising:

depositing diamond single crystal on a substrate, the diamond single crystal forming an active layer;
 providing a first high resistance region and a second high resistance region on external sides of a middle channel region of the active layer respectively; and
 doping a region of the active layer on an external side of the first high resistance region and a region of the active layer on an external side of the second high resistance region to form a source region and a drain region respectively.

8. The method for manufacturing a thin film transistor according to claim 7, wherein the deposited diamond single crystal is (111)-face diamond single crystal; and

the providing a first high resistance region and a second high resistance region on external sides of a middle channel region of the active layer respectively comprises:

etching away the (111)-face diamond single crystal in a predetermined first high resistance region and a predetermined second high resistance region, and depositing (100)-face diamond single crystal in the predetermined first high resistance region and the predetermined second high resistance region.

9. The method for manufacturing a thin film transistor according to claim 7, further comprising:

forming a gate insulating layer on the active layer, and forming a gate electrode on the gate insulating layer; and

etching a first via-hole and a second via-hole in the source region and the drain region respectively, and depositing metal in the first via-hole and the second via-hole respectively to form a source electrode and a drain electrode.

10. The method for manufacturing a thin film transistor according to claim 9, further comprising:

performing a rapid thermal annealing treatment on the source electrode and the drain electrode to form a carbonized metal layer between the source electrode and the source region and between the drain electrode and the drain region respectively.

11. The method for manufacturing a thin film transistor according to claim 7, wherein the depositing diamond single crystal on a substrate comprises:

depositing (111)-face diamond single crystal on the substrate, wherein a deposition temperature is 780-850° C., a deposition pressure is 16-18 KPa, a flow ratio of methane to hydrogen gas is 0.5%-1%, deposition power is 3-5 KW, a deposition rate is 0.01-0.02 $\mu\text{m}/\text{min}$, and a deposition period is 10-15 mins.

12. The method for manufacturing a thin film transistor according to claim 8, wherein a deposition condition for the depositing (100)-face diamond single crystal in the predetermined first high resistance region and the predetermined second high resistance region include a deposition temperature of 900-1000° C., a deposition pressure of 21-23 KPa, a flow ratio of methane to hydrogen gas of 3%-4%, a deposition power of 5-7 KW, a deposition rate of 0.1-0.2 $\mu\text{m}/\text{min}$, and a deposition period of 2-3 mins.

13. The thin film transistor according to claim 2, wherein the active layer has been treated with plasma and polar gas.

14. An array substrate, comprising the thin film transistor according to claim 2.

15. An array substrate, comprising the thin film transistor according to claim 3.

16. An array substrate, comprising the thin film transistor according to claim 4.

17. An array substrate, comprising the thin film transistor according to claim 5.

18. An array substrate, comprising the thin film transistor according to claim 13.

19. The method for manufacturing a thin film transistor according to claim 8, further comprising:

forming a gate insulating layer on the active layer, and forming a gate electrode on the gate insulating layer; and

etching a first via-hole and a second via-hole in the source region and the drain region respectively, and depositing metal in the first via-hole and the second via-hole respectively to form a source electrode and a drain electrode.

20. The method for manufacturing a thin film transistor according to claim 19, further comprising:

performing a rapid thermal annealing treatment on the source electrode and the drain electrode to form a carbonized metal layer between the source electrode and the source region and between the drain electrode and the drain region respectively.

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