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(54) **SEMICONDUCTOR DEVICE**

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CPC ***H01L 23/5223*** (2013.01); ***H01L 27/0886*** (2013.01); ***H01L 23/5283*** (2013.01); ***H01L 29/41791*** (2013.01)

(57) **ABSTRACT**

A semiconductor device includes a substrate, a gate structure on the substrate and a first conductive connection group on the gate structure. The gate structure includes a gate spacer and a gate electrode. The first conductive connection group includes a ferroelectric material layer. At least a part of the ferroelectric material layer is disposed above an upper surface of the gate spacer. And the ferroelectric material layer forms a ferroelectric capacitor having a negative capacitance in the first conductive connection group.

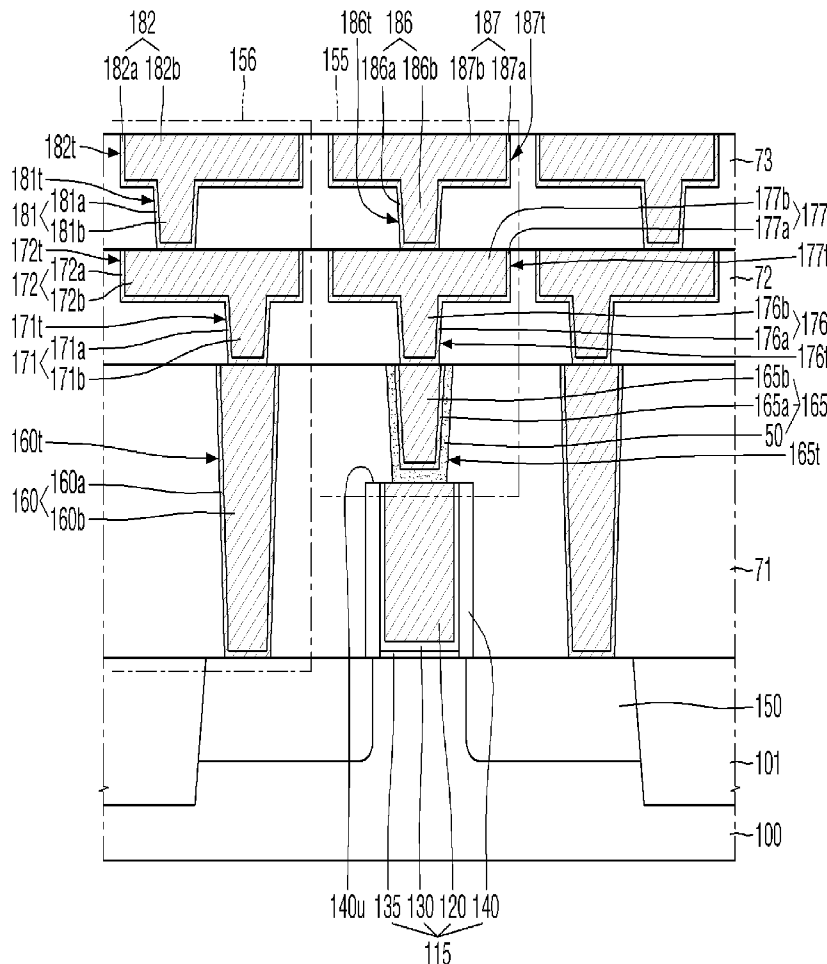


FIG. 1

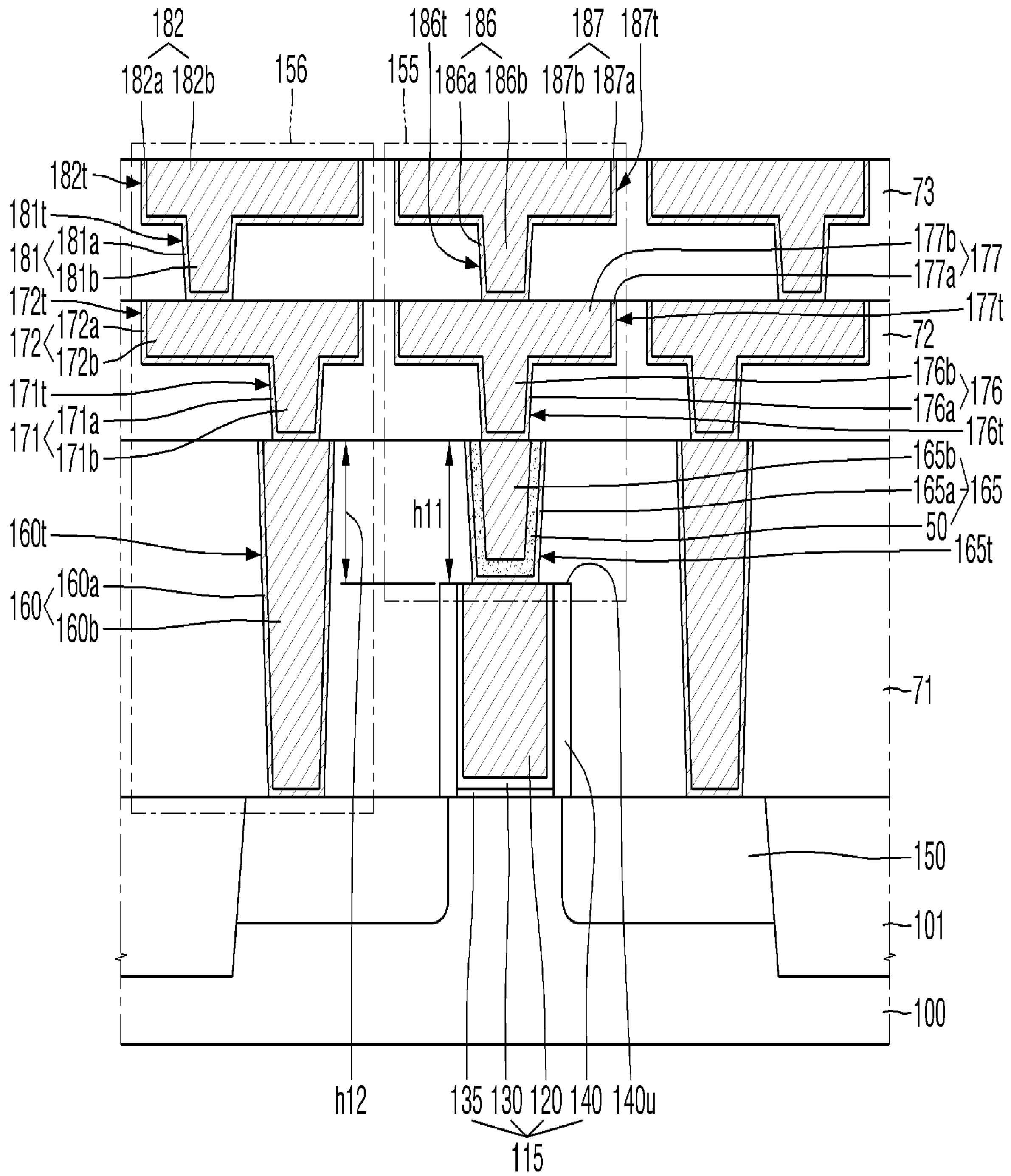


FIG. 2

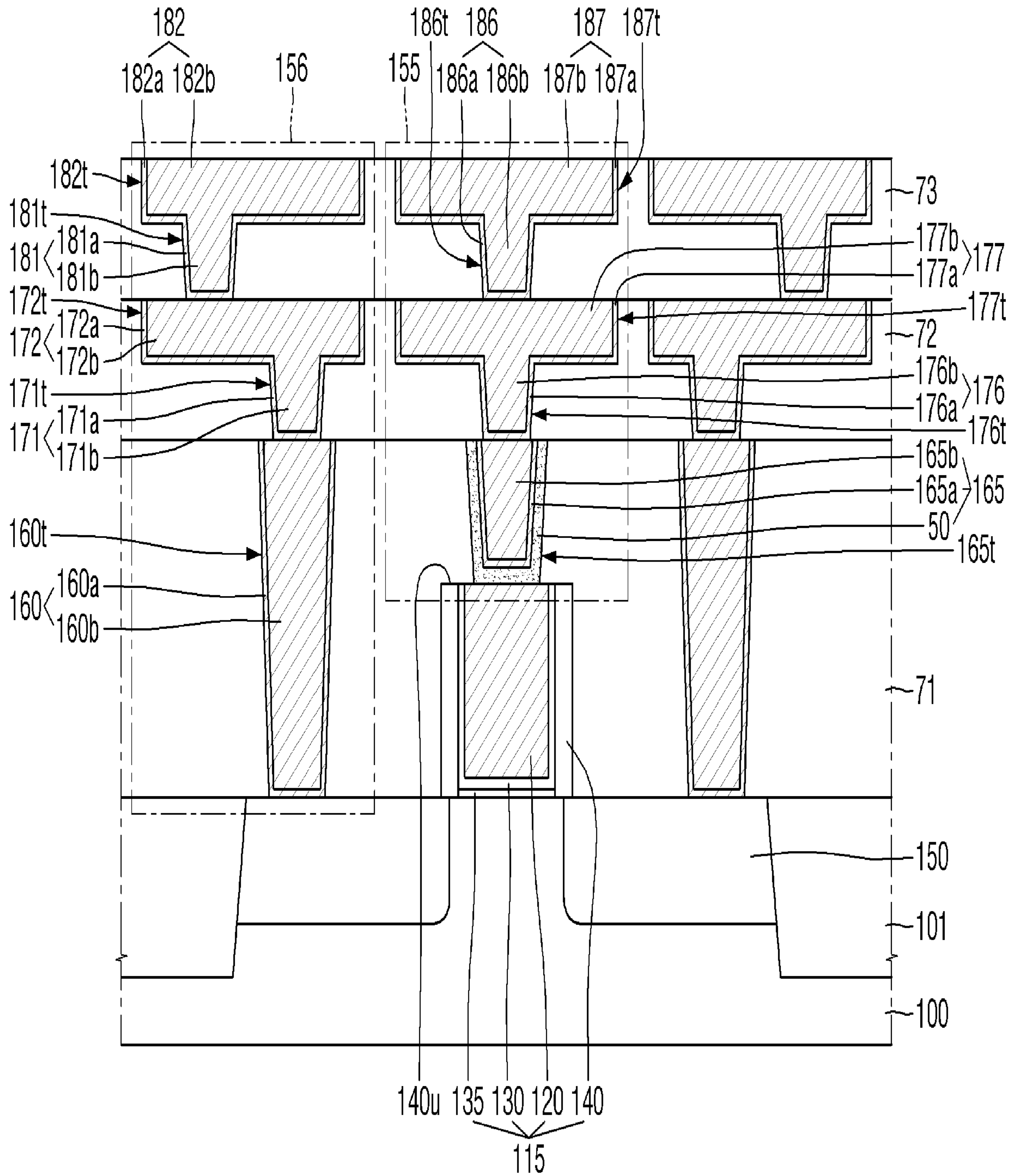


FIG. 3

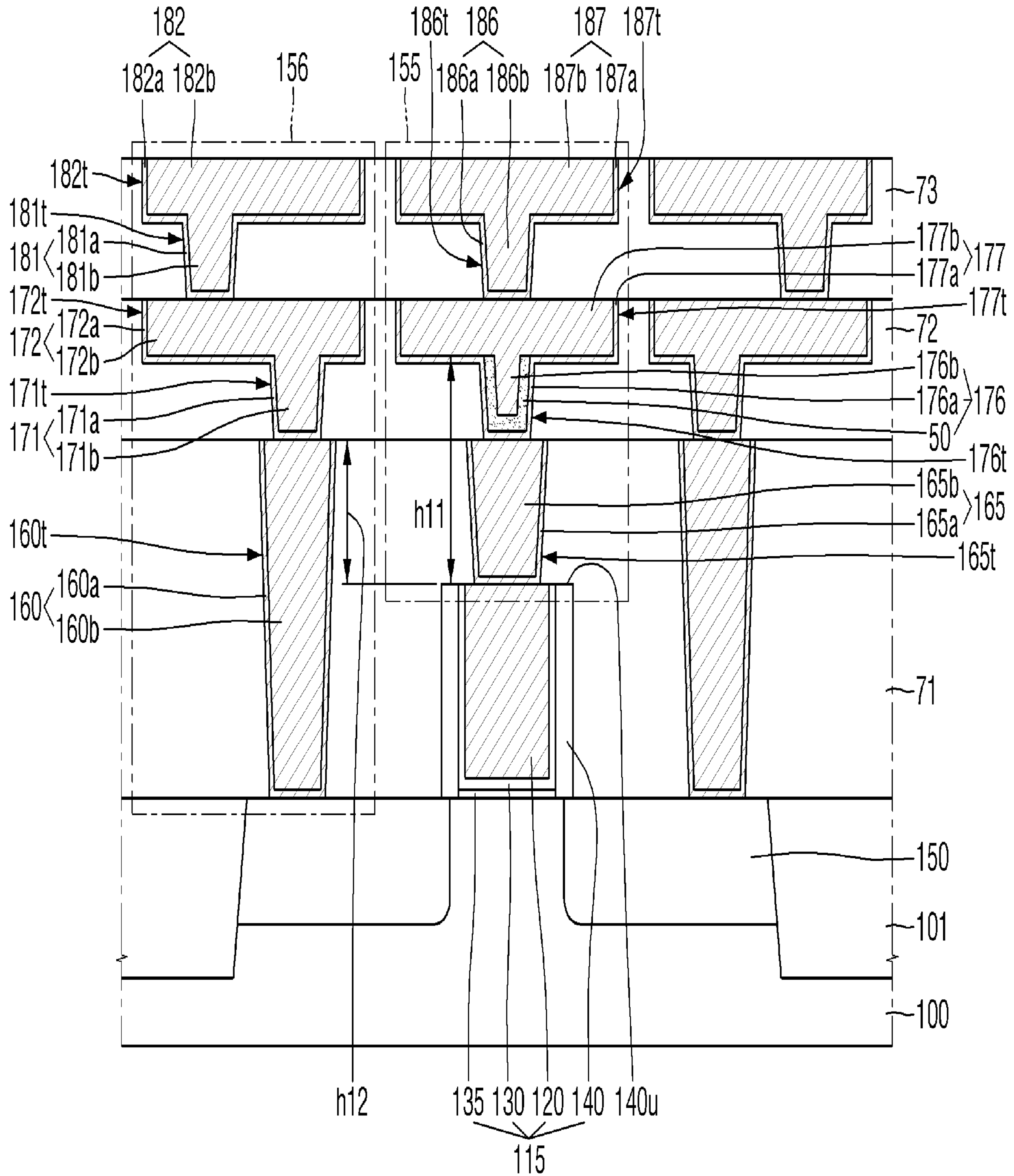


FIG. 4

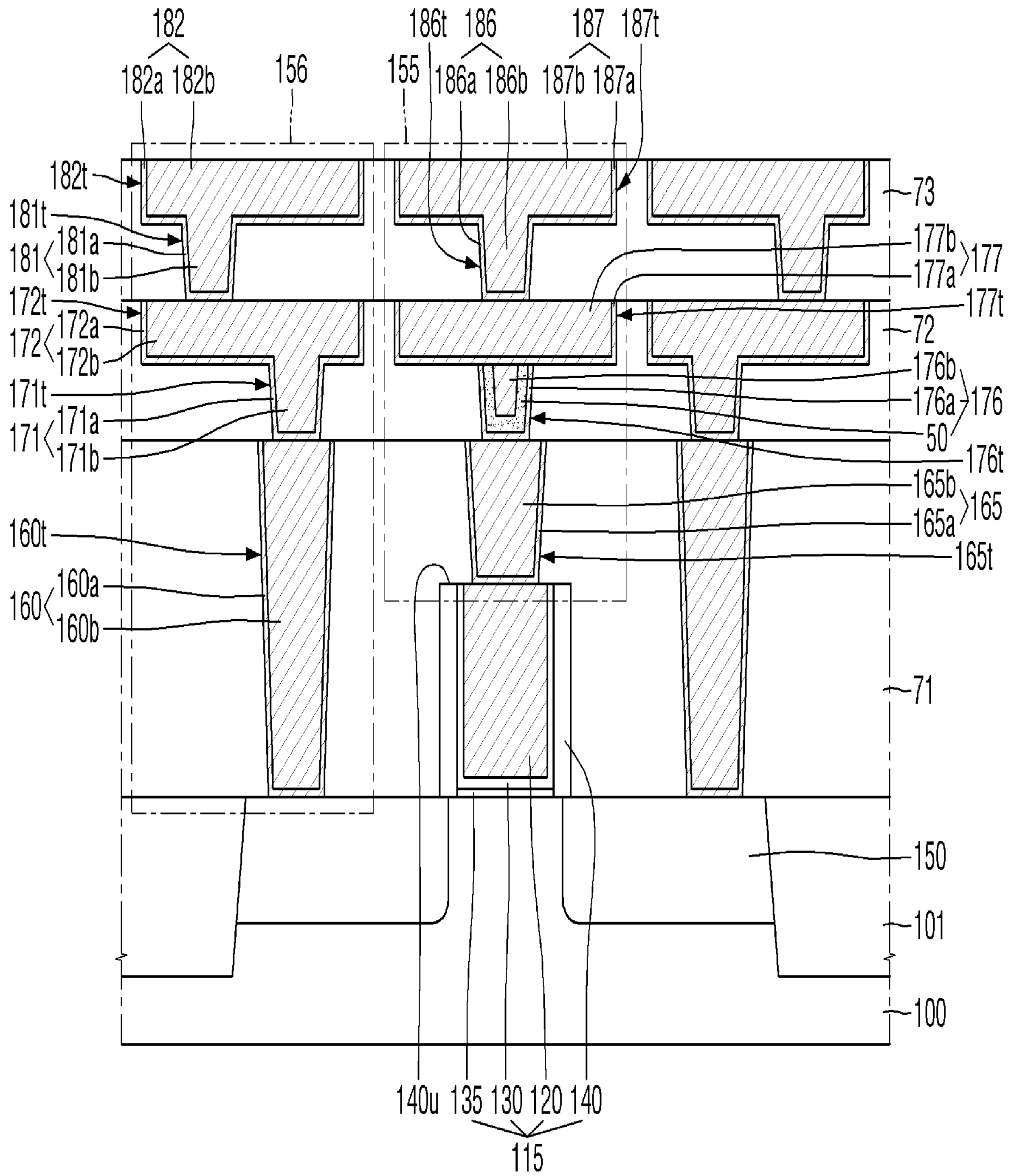


FIG. 5

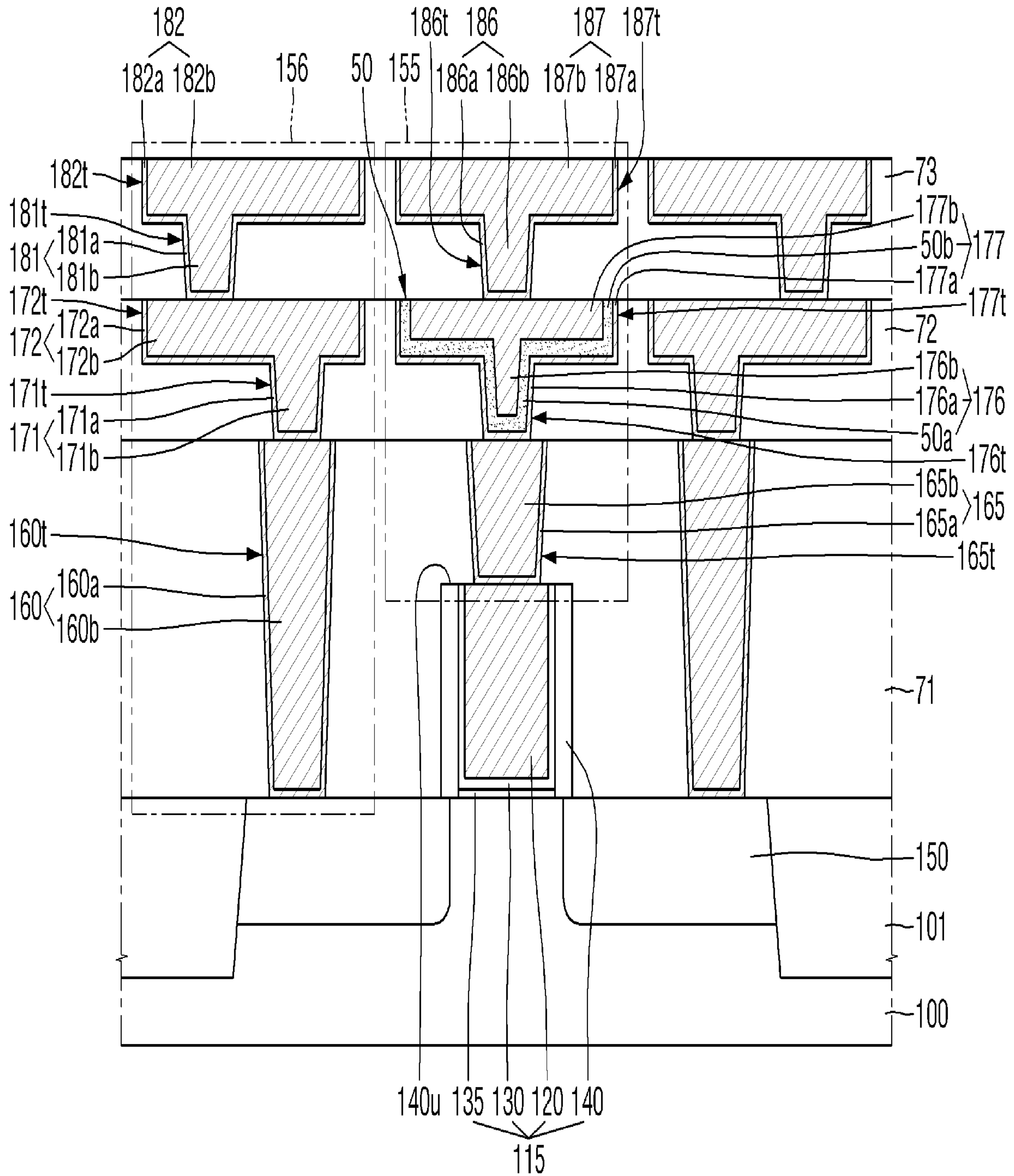


FIG. 6

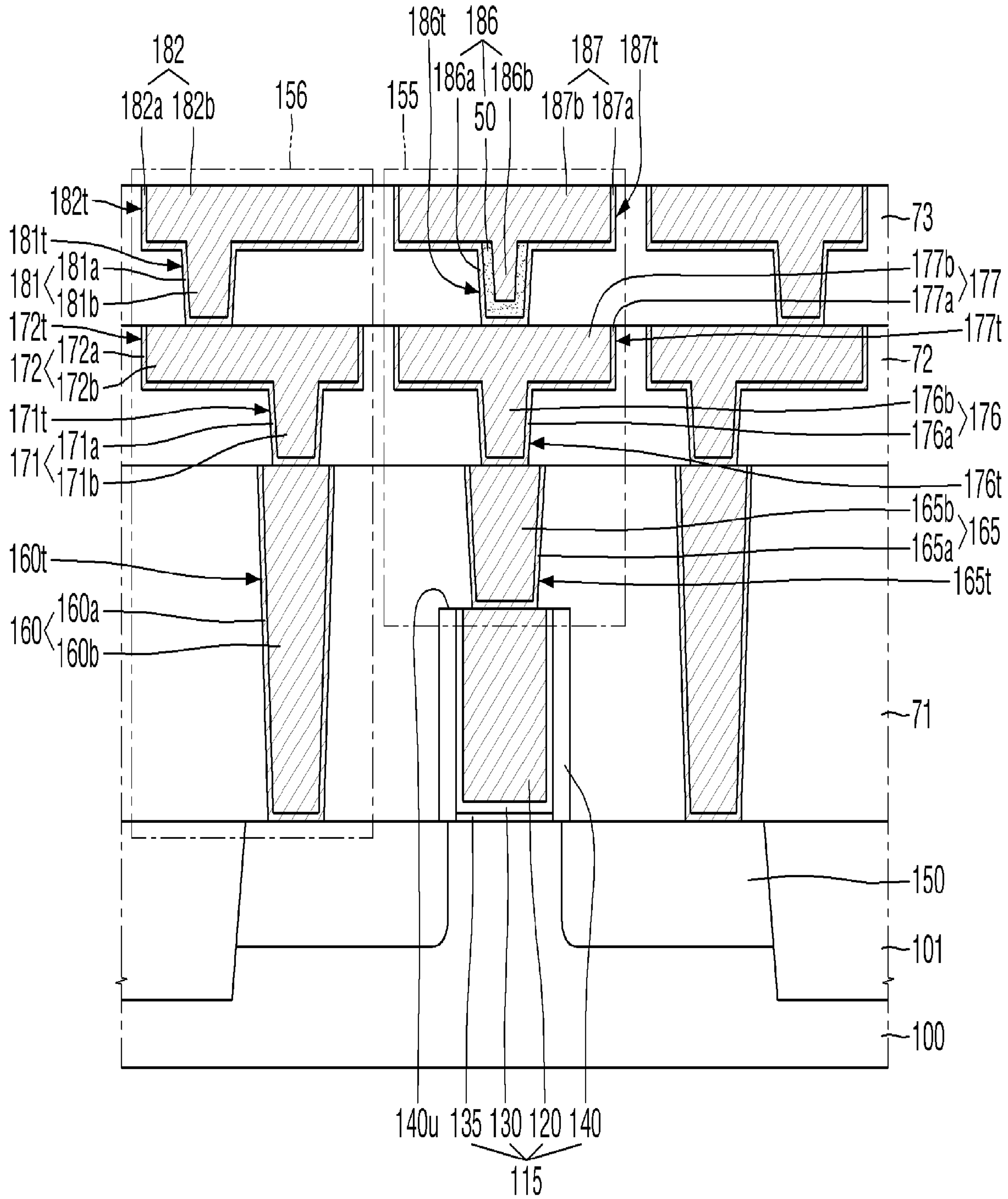


FIG. 7

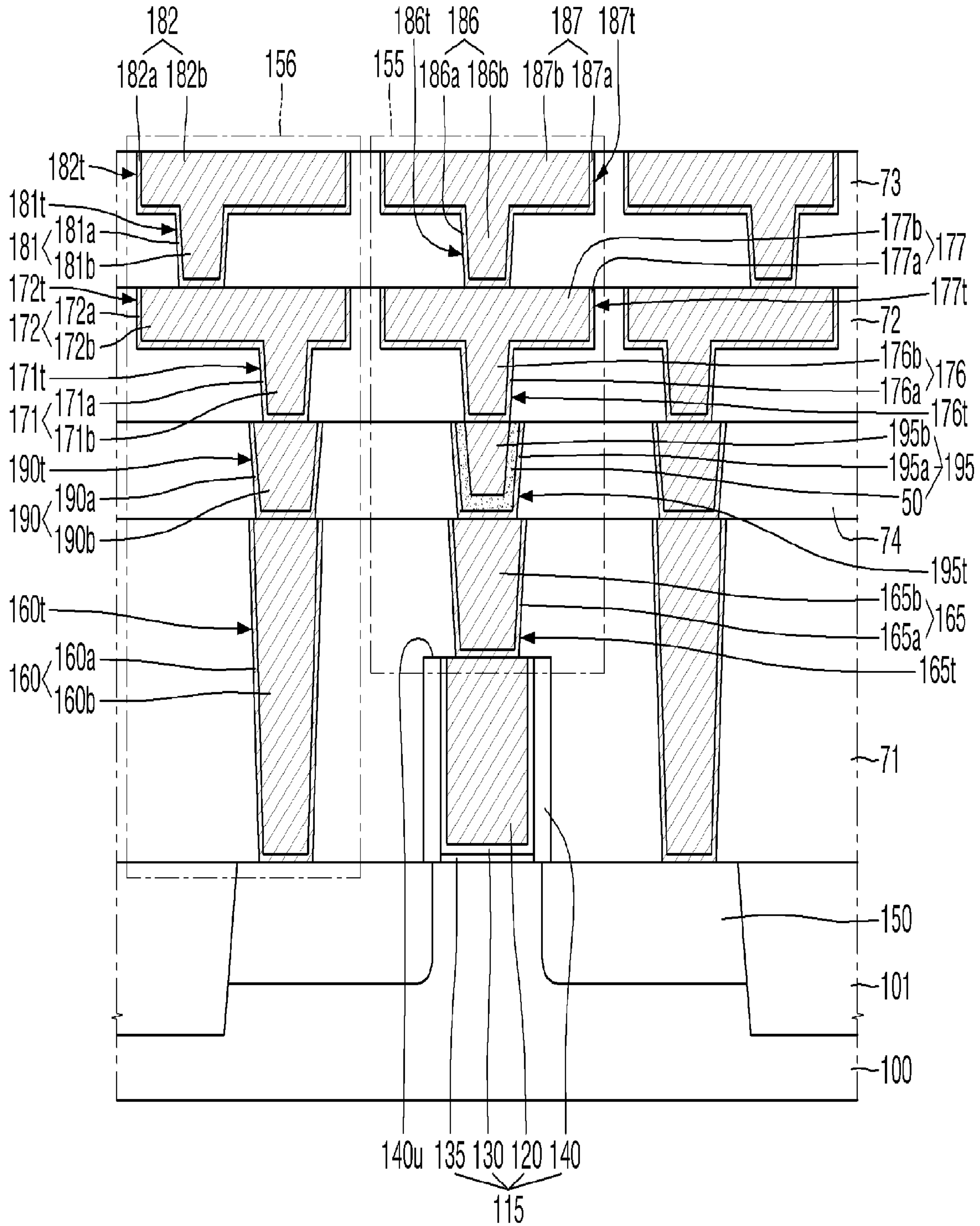


FIG. 8

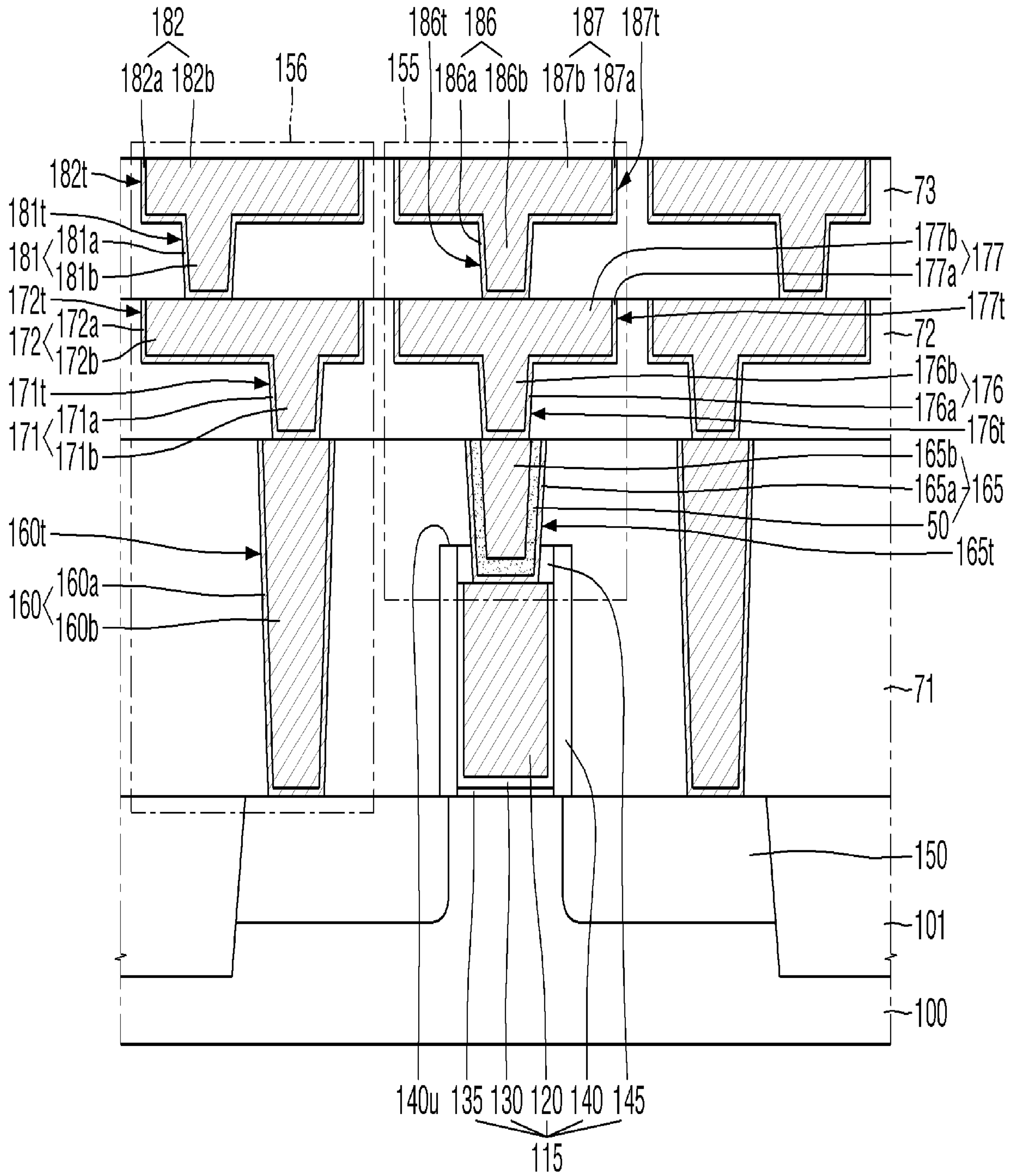


FIG. 9

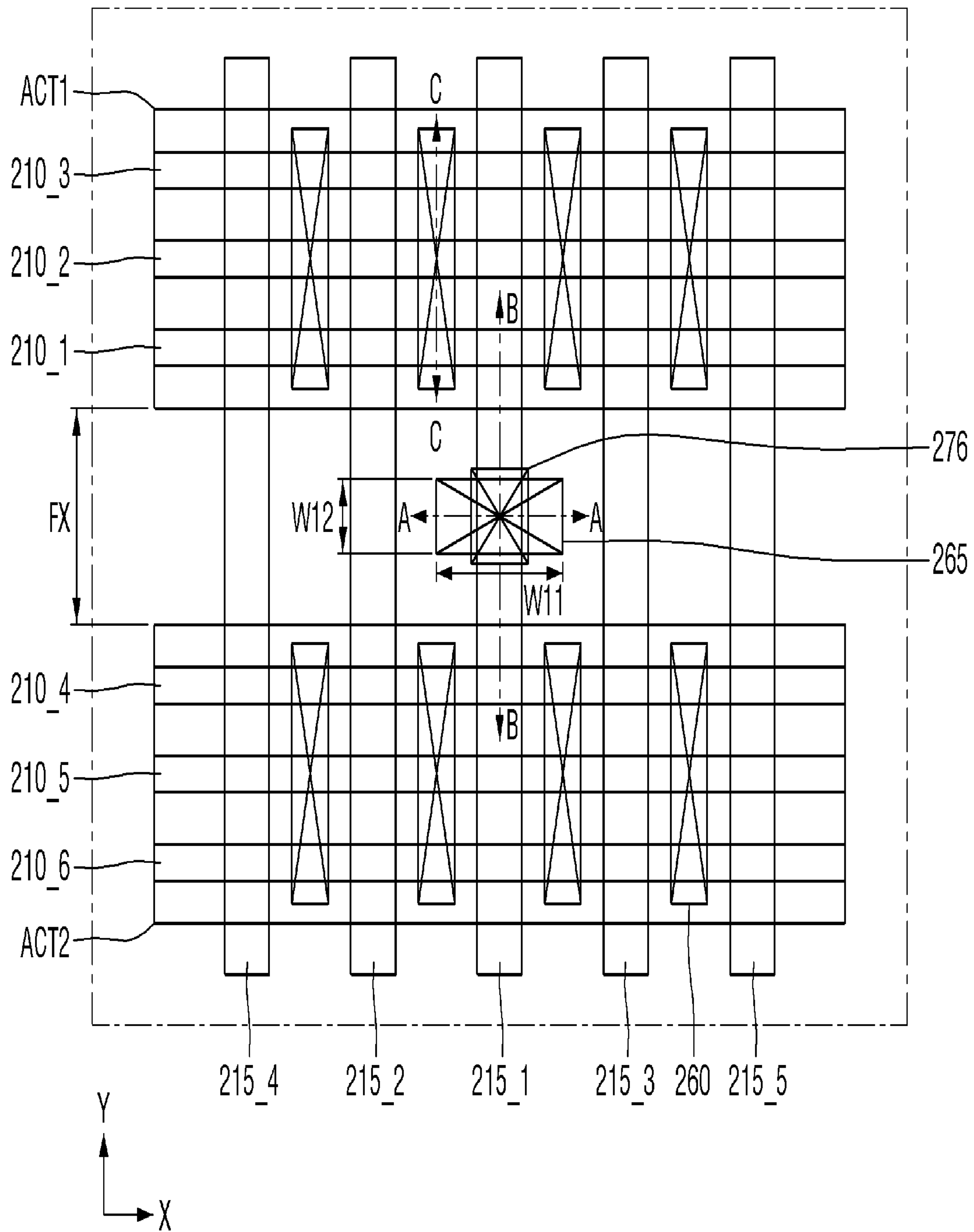


FIG. 10

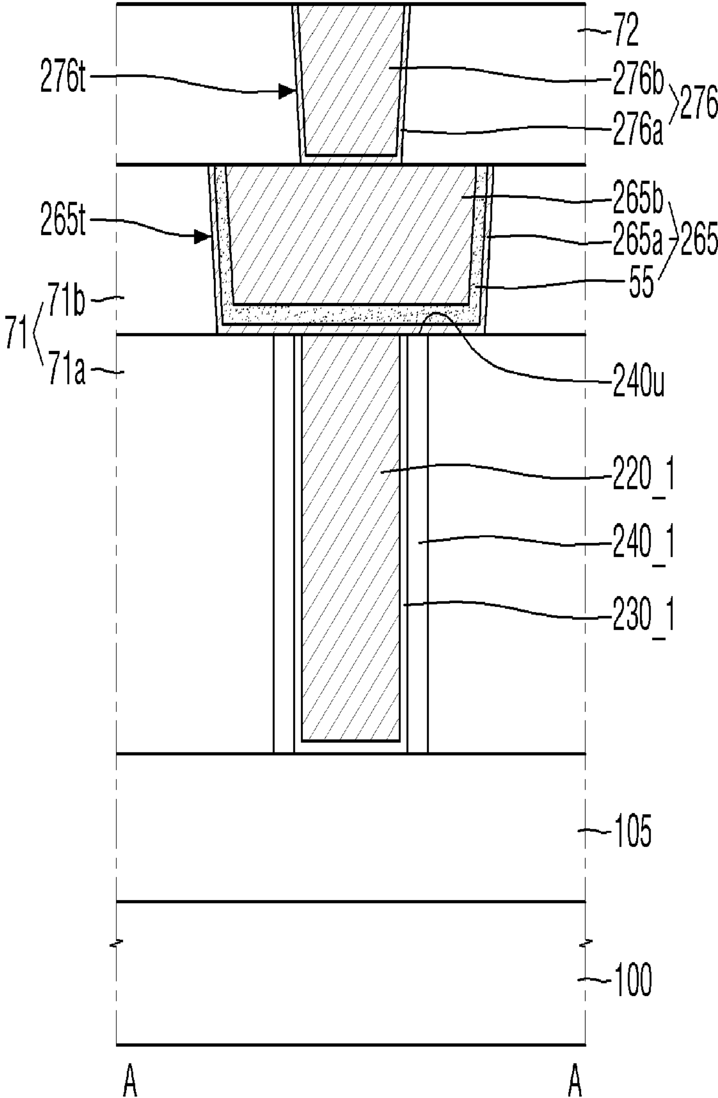


FIG. 11

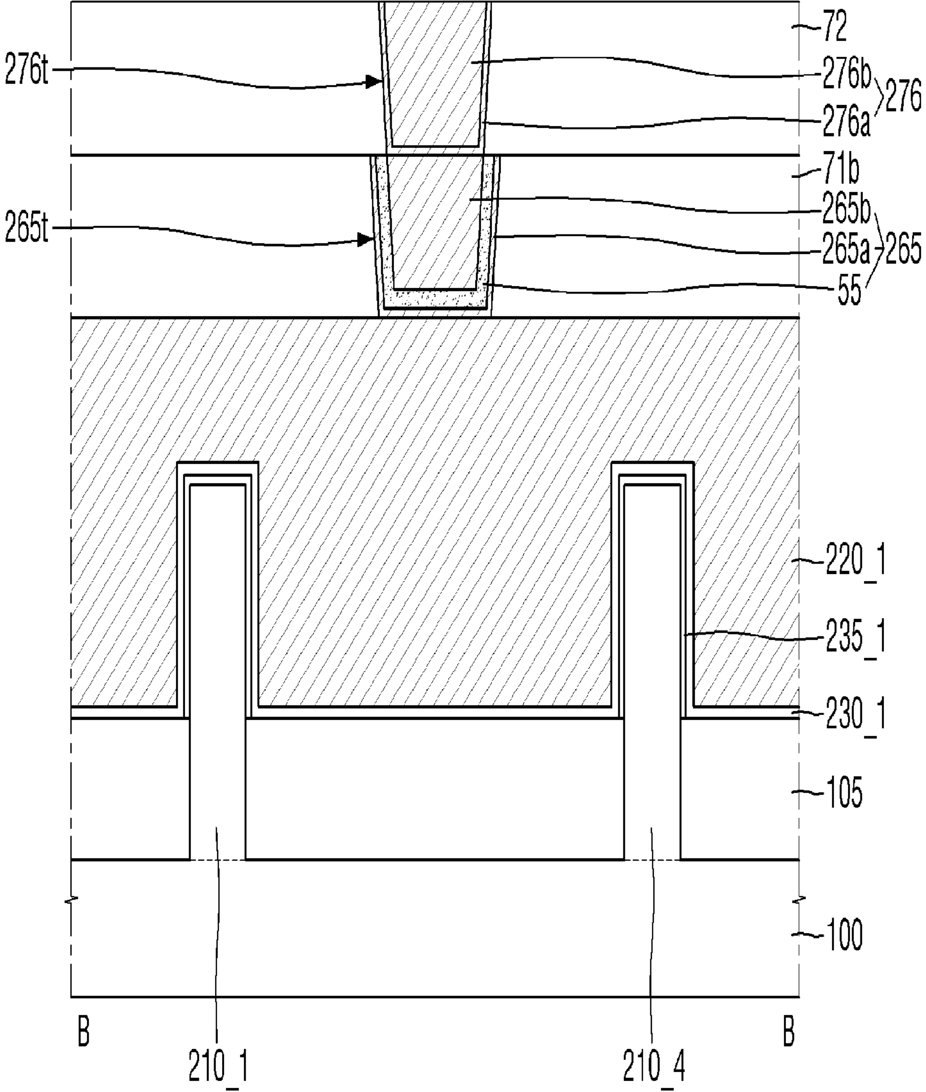


FIG. 12

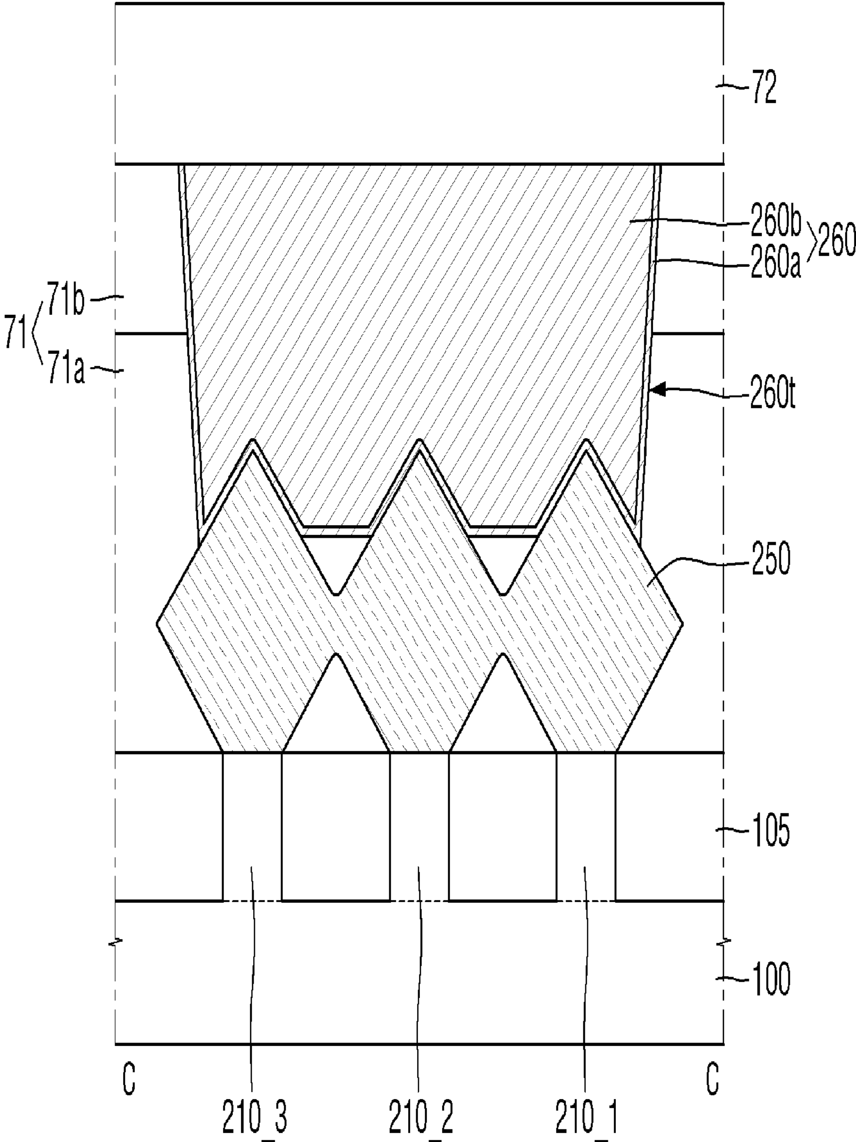


FIG. 13a

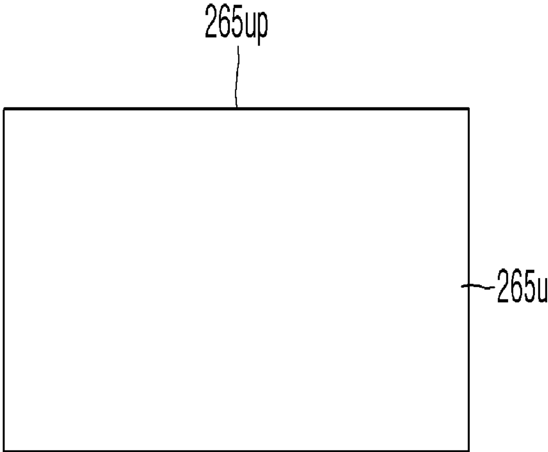


FIG. 13b

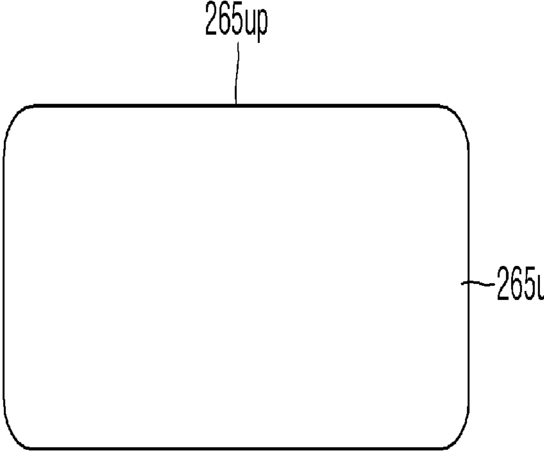


FIG. 13c

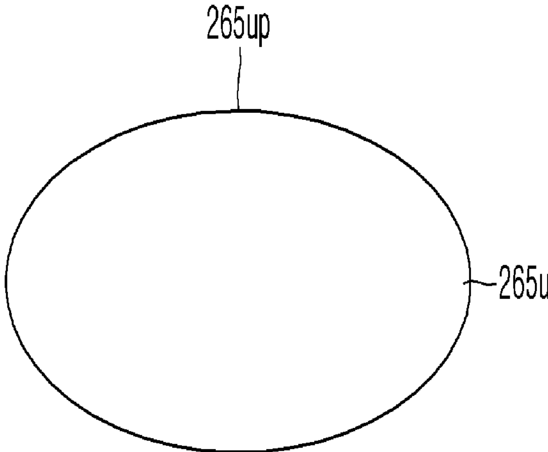


FIG. 13d

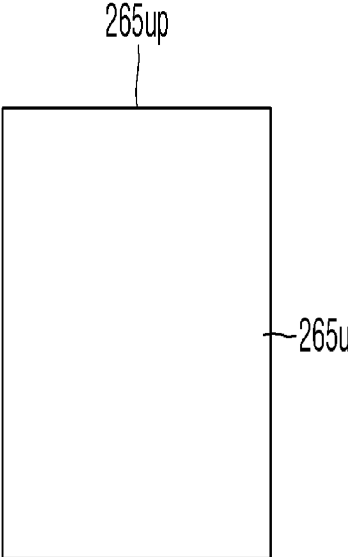


FIG. 13e

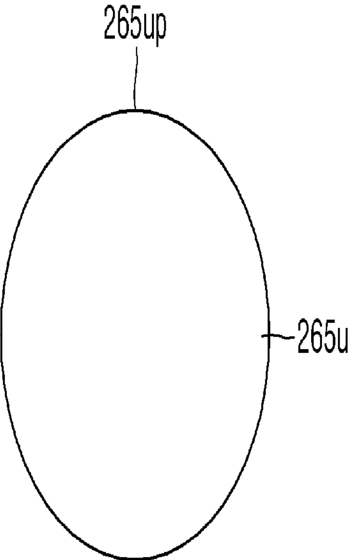


FIG. 14

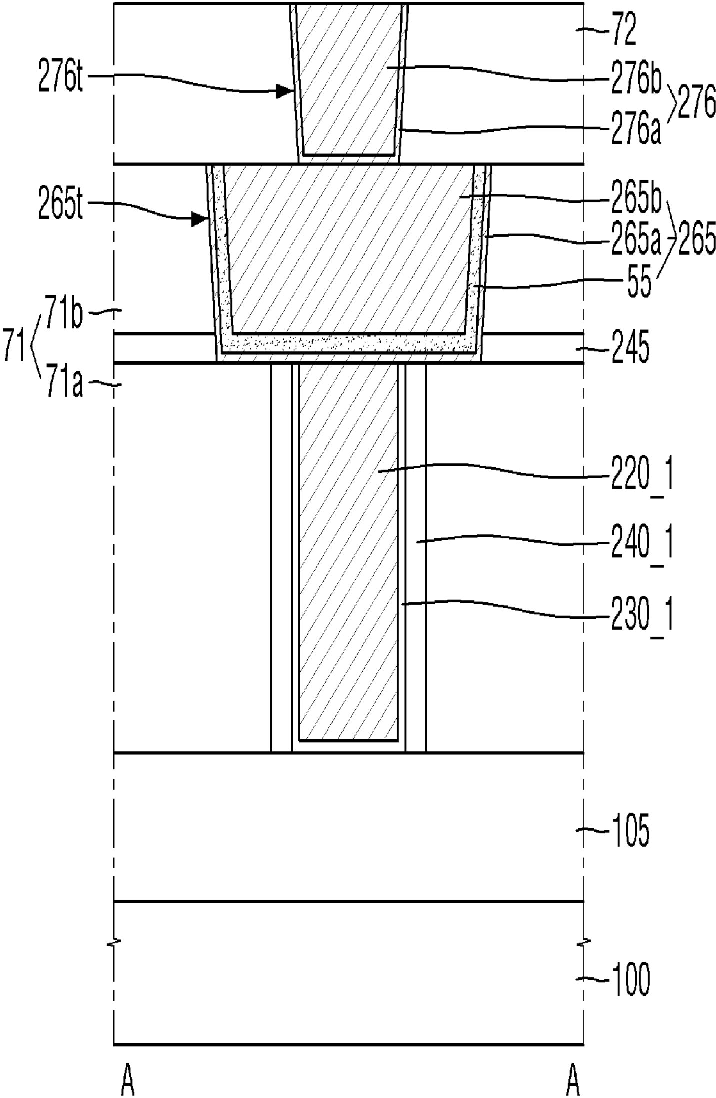


FIG. 15

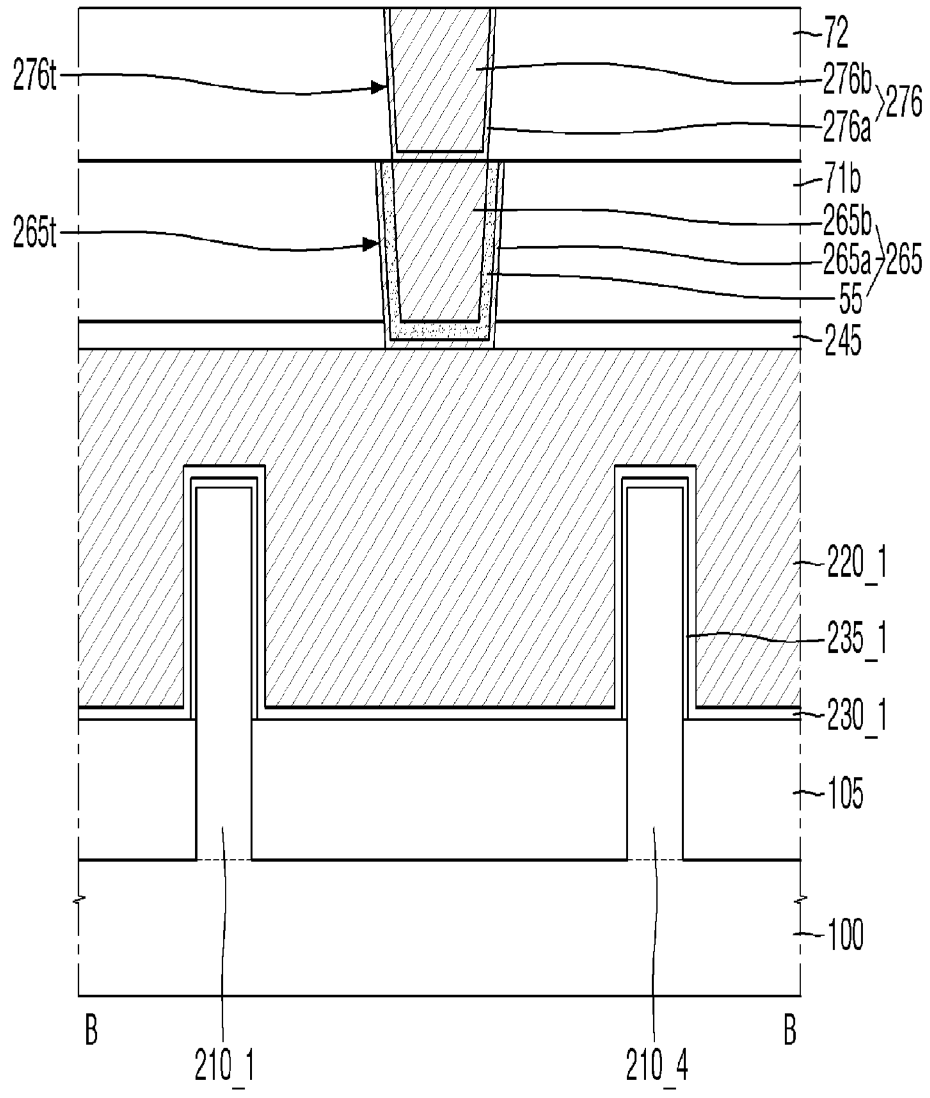


FIG. 16

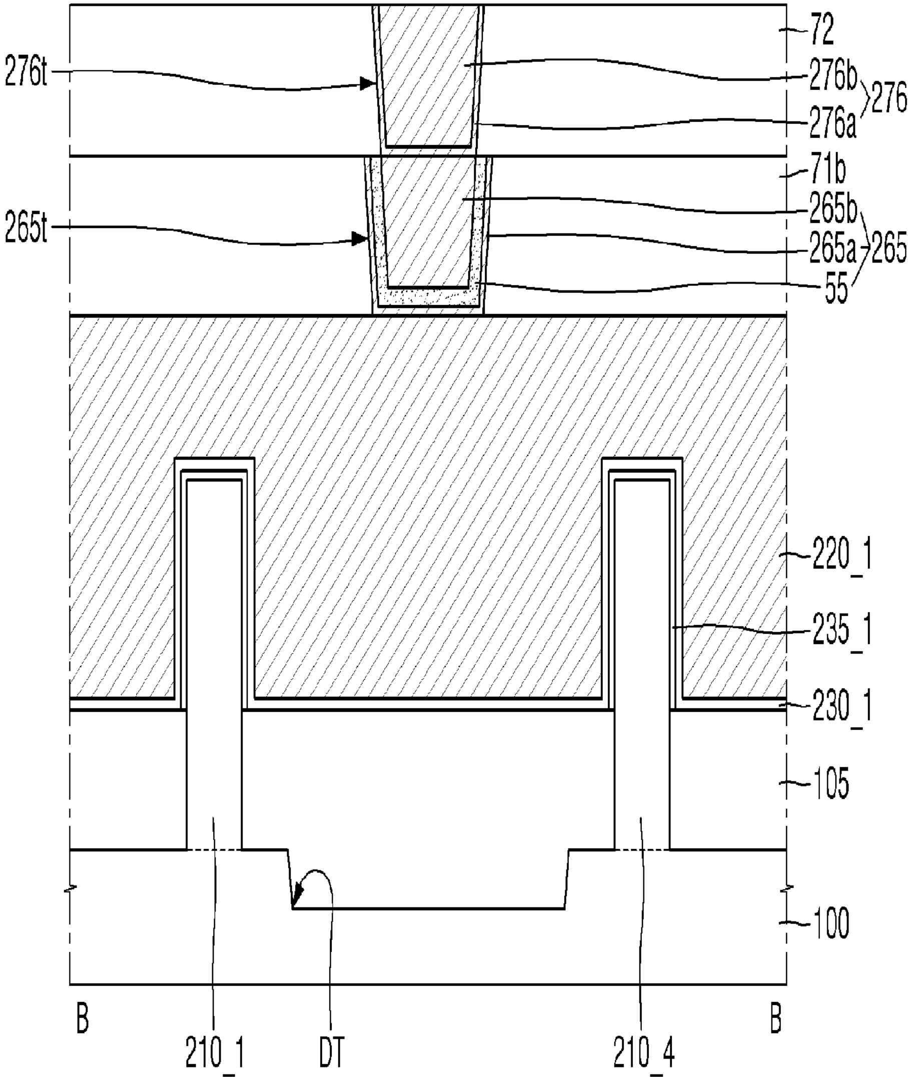


FIG. 17

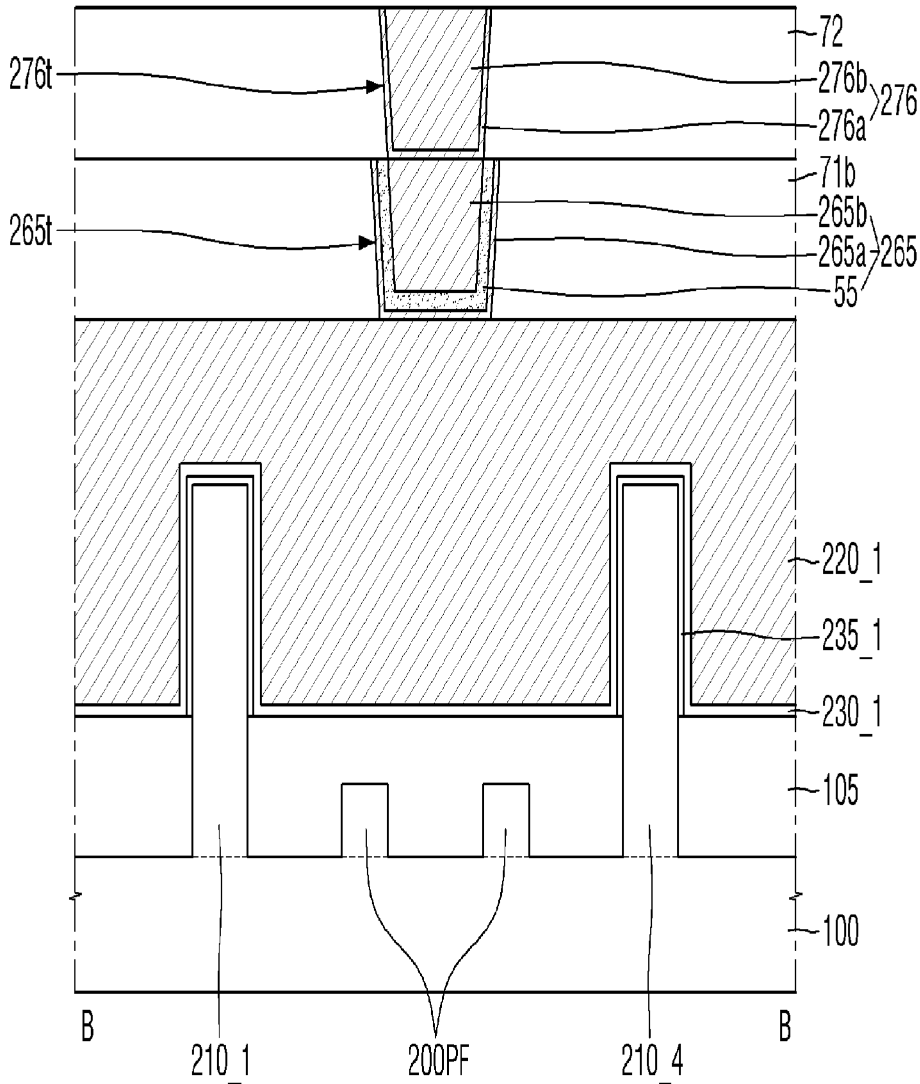


FIG. 18

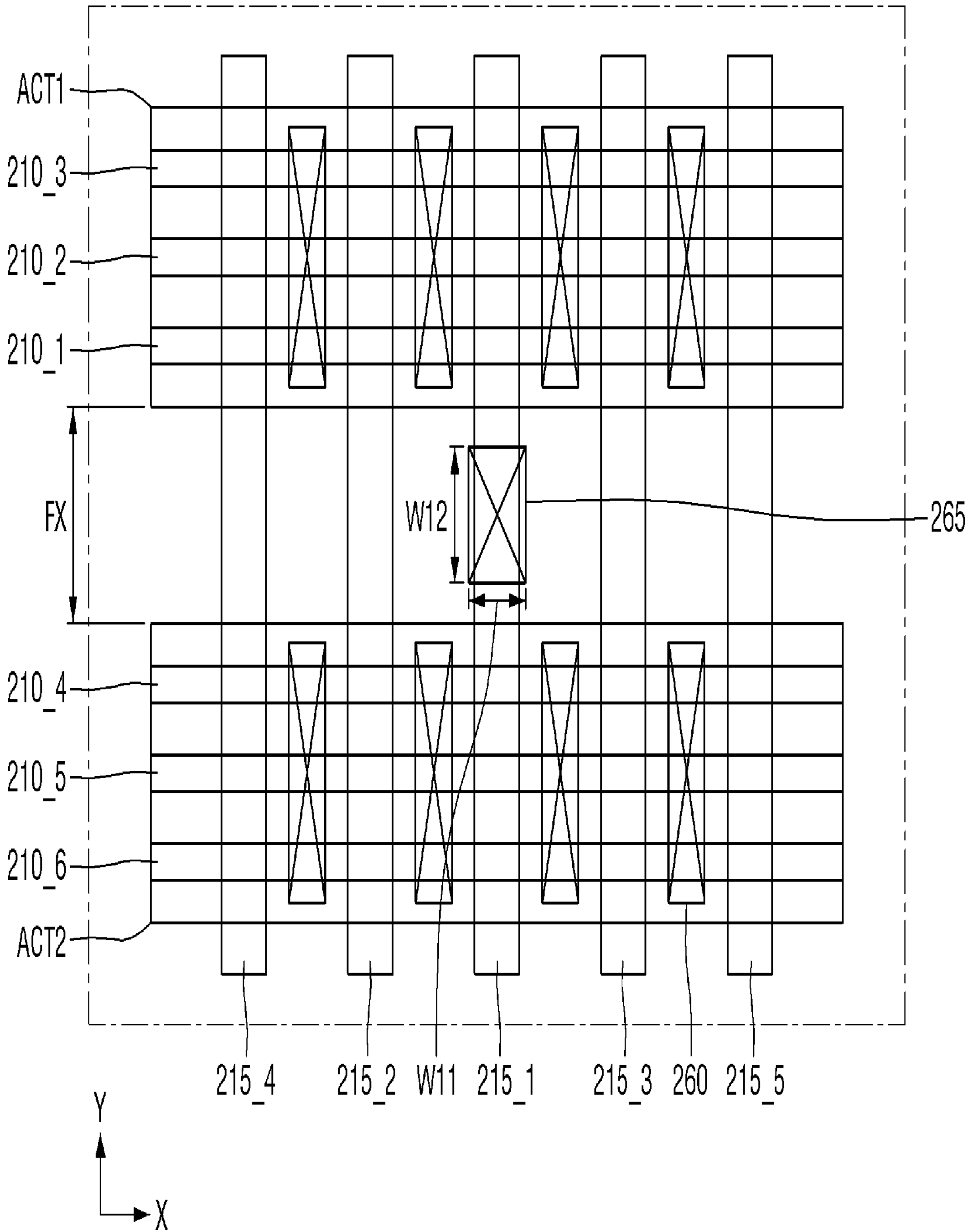


FIG. 19

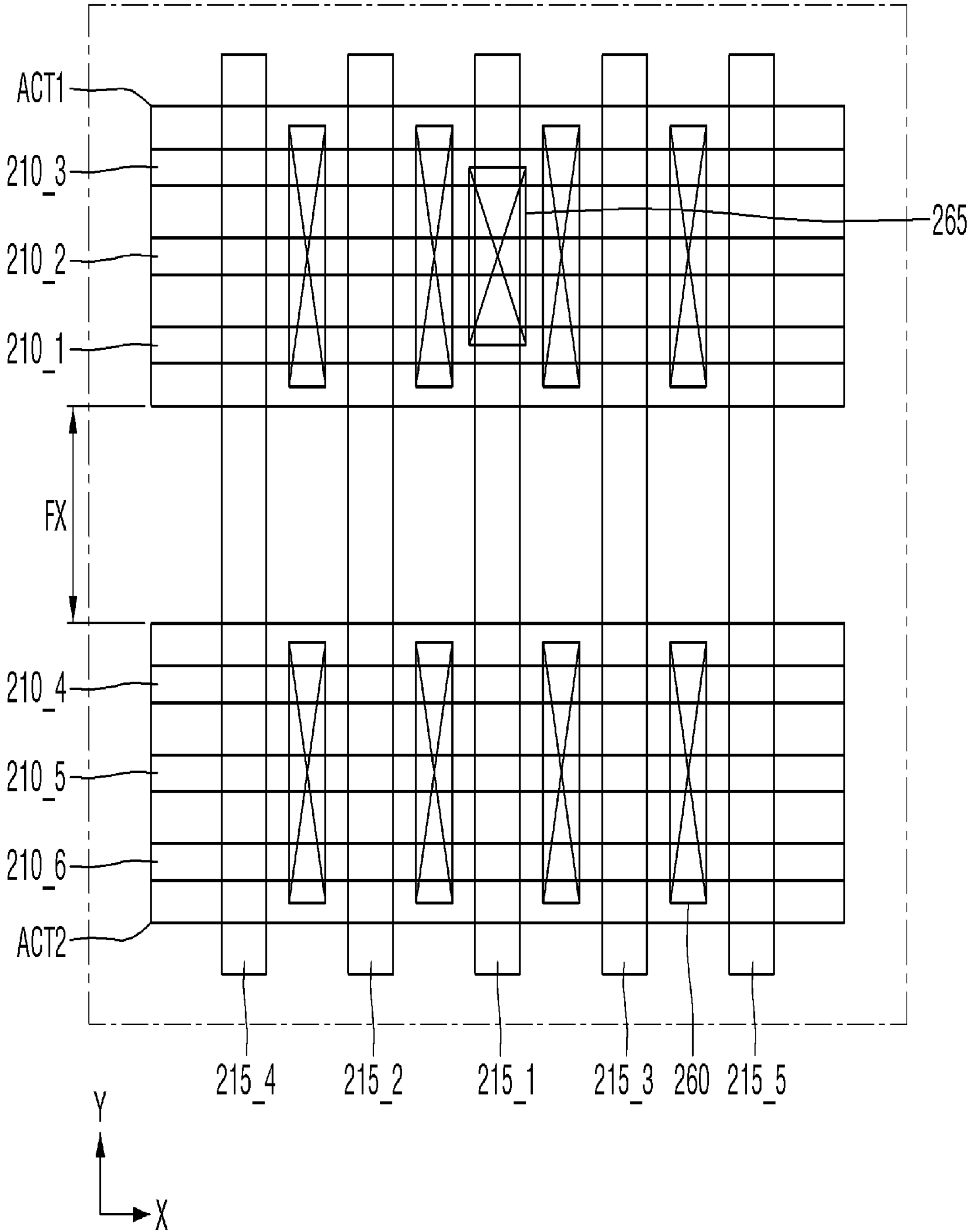


FIG. 20

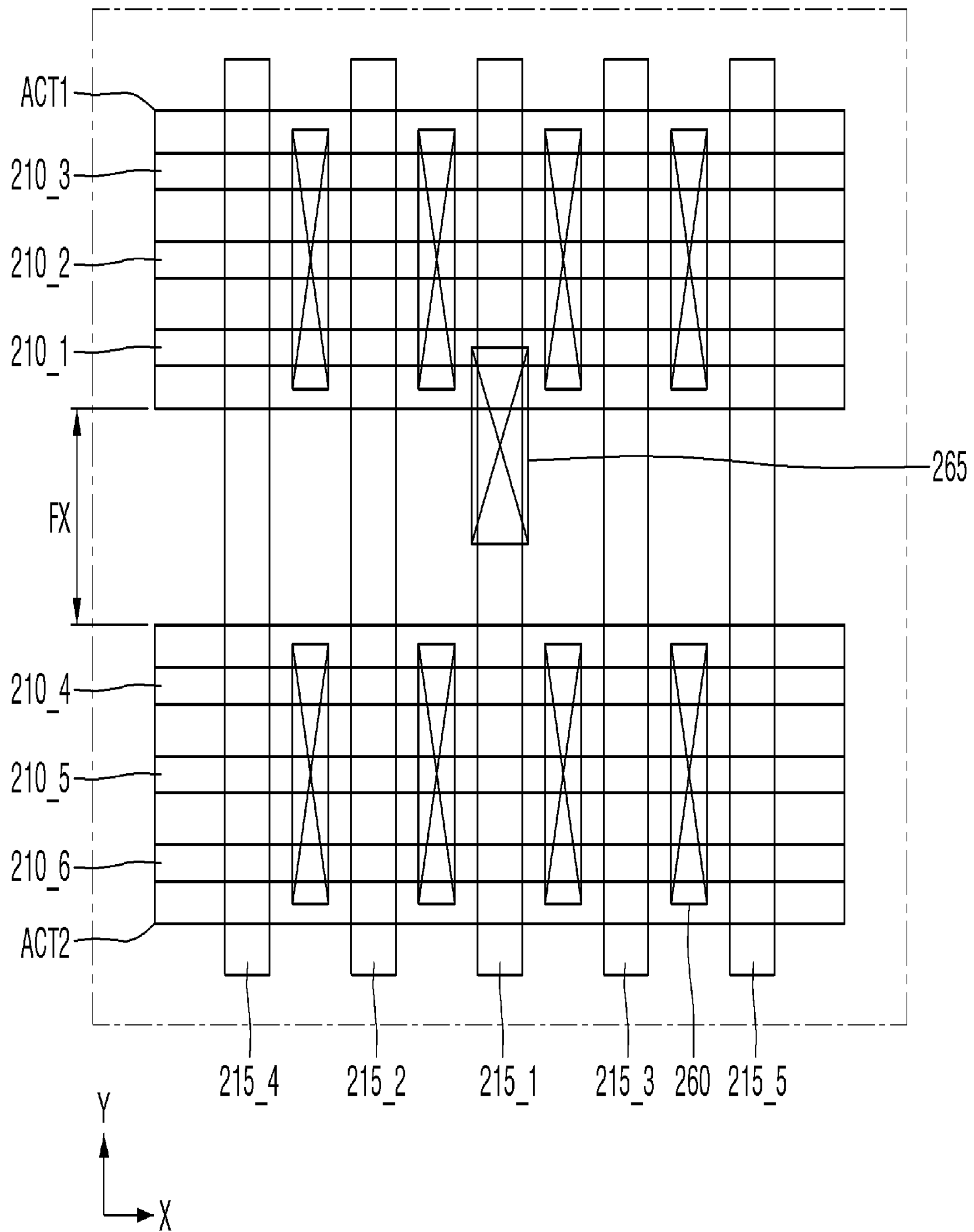


FIG. 21

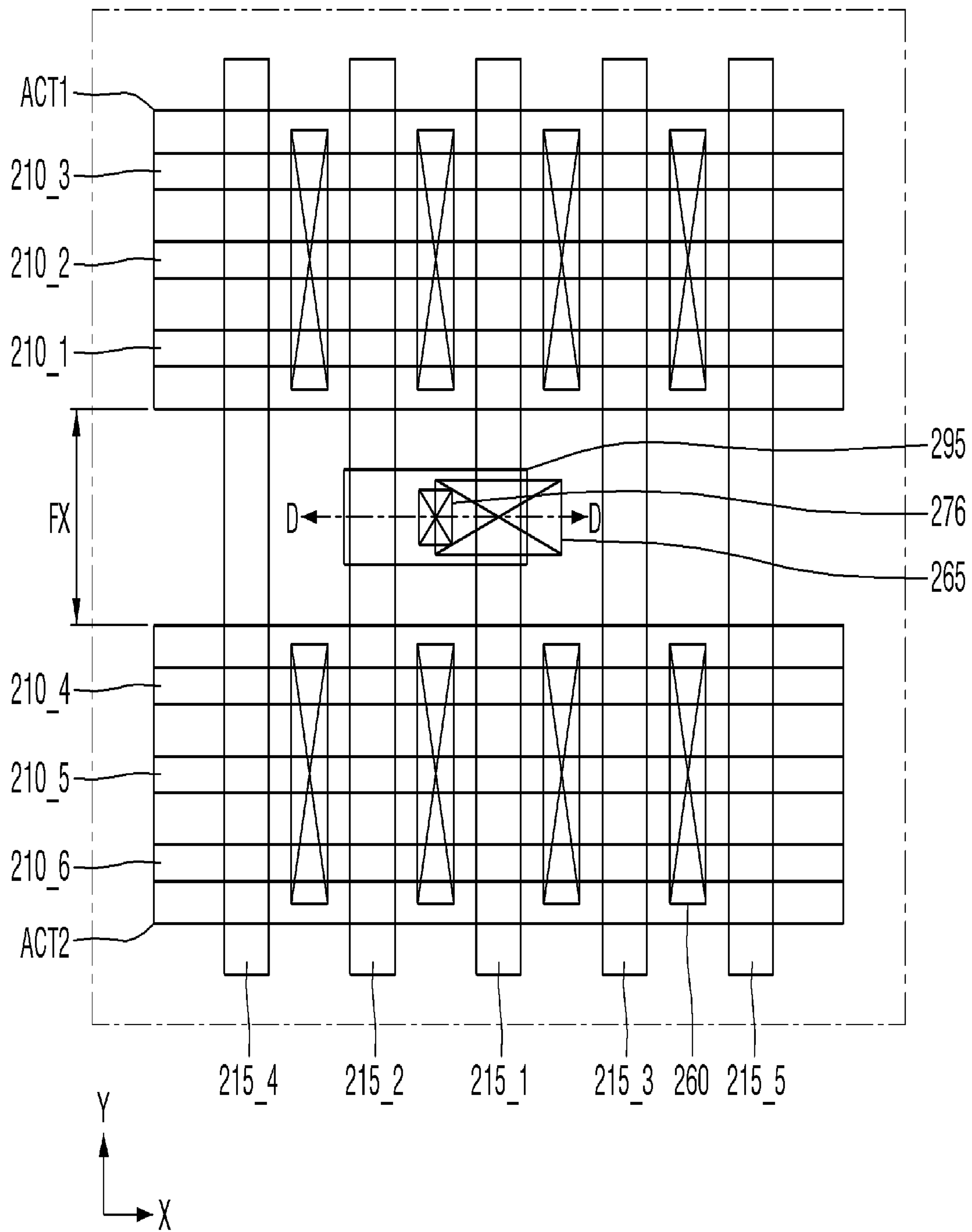


FIG. 22

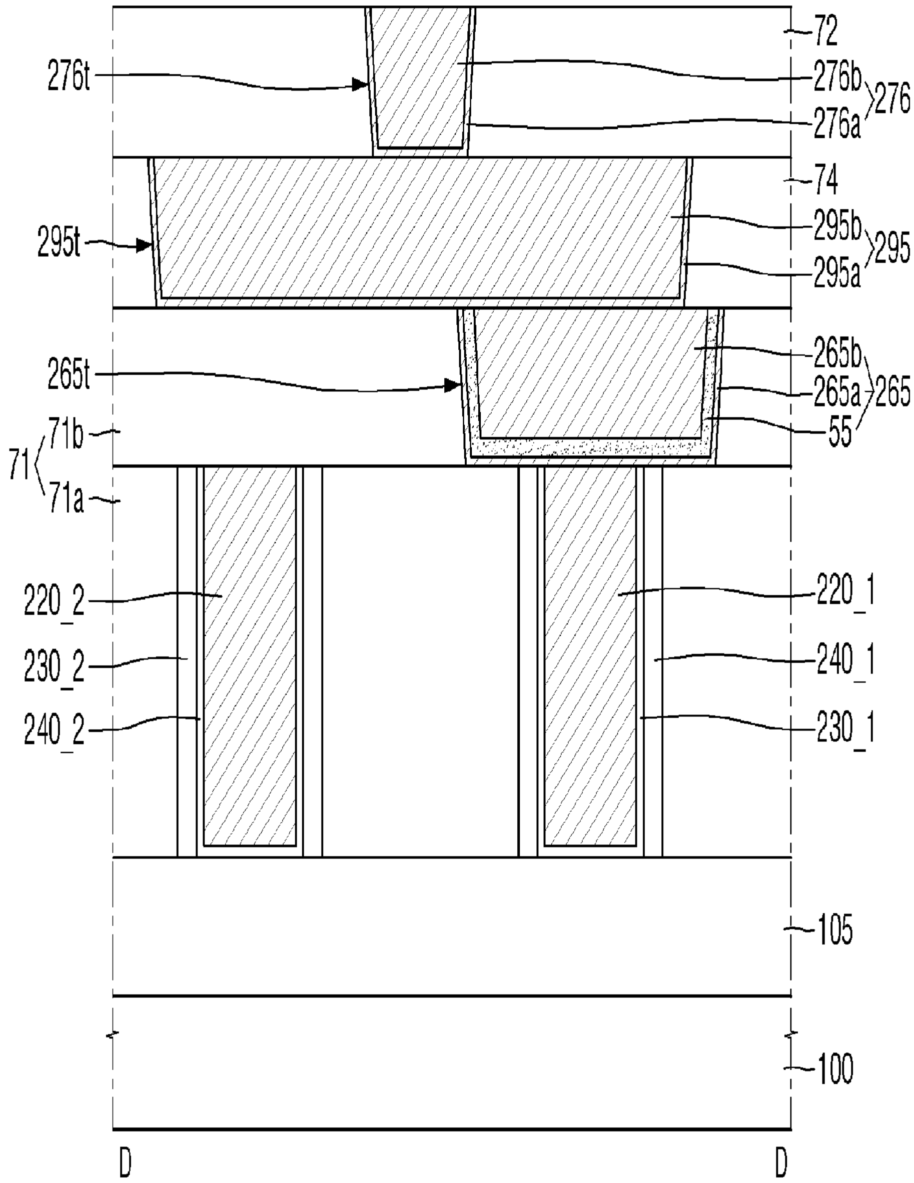


FIG. 23

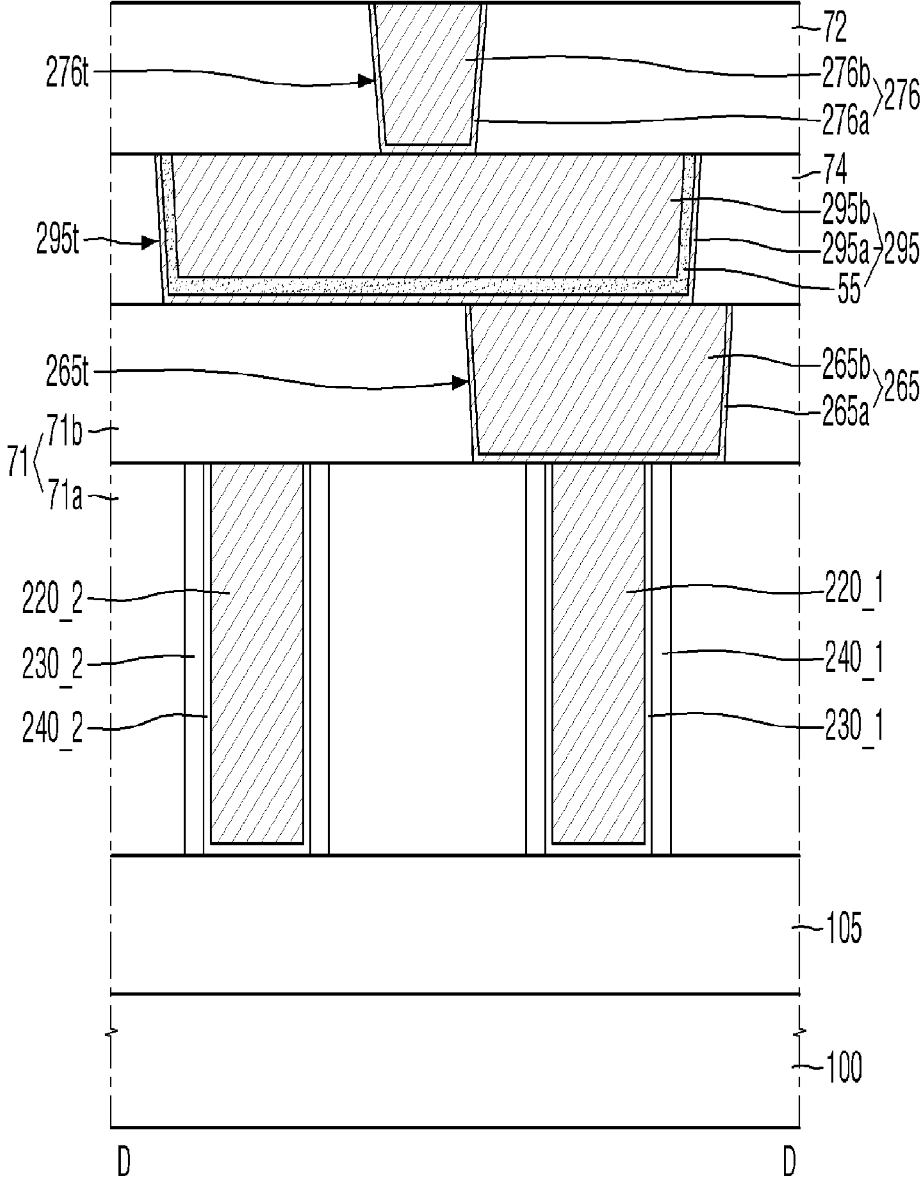


FIG. 24

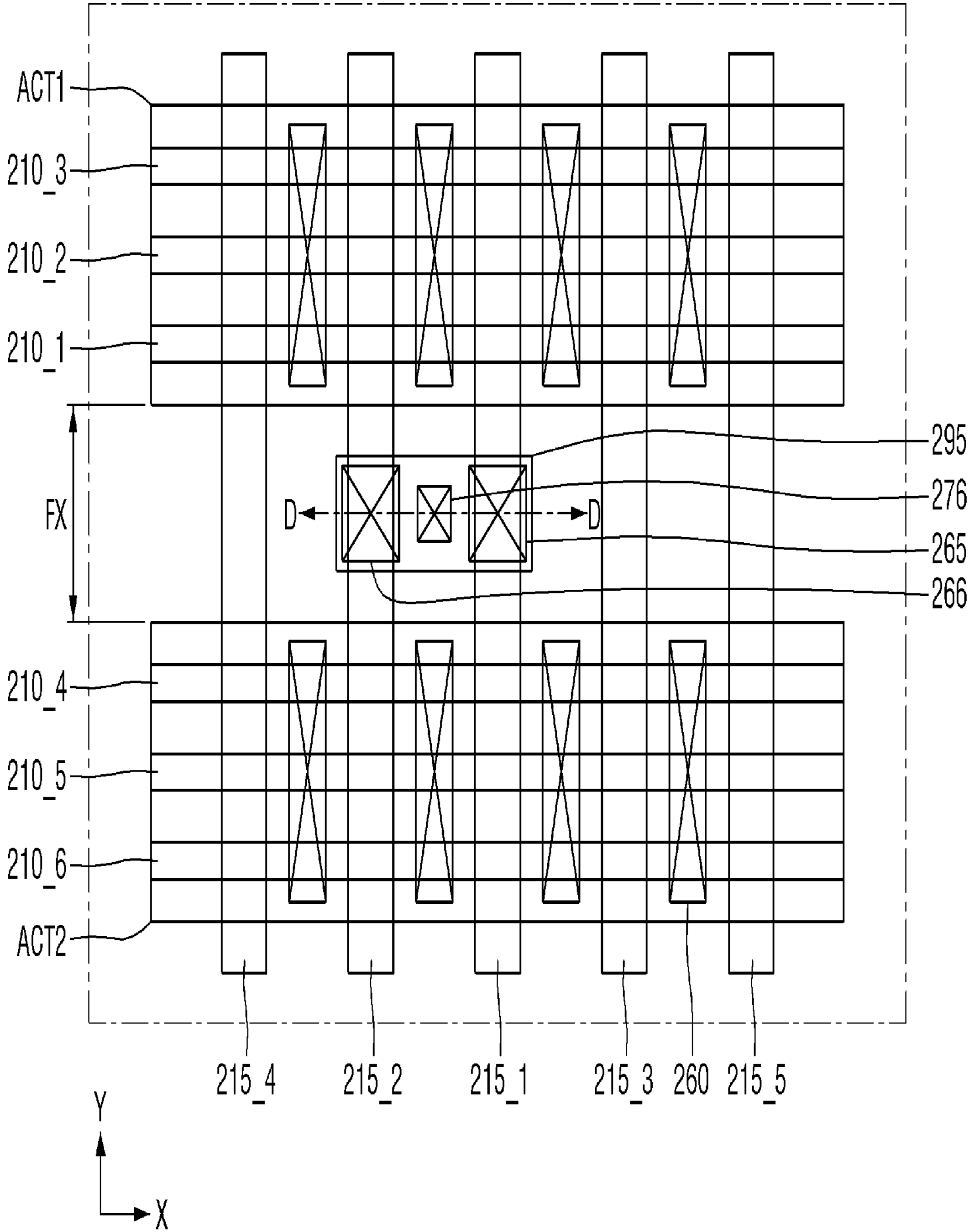
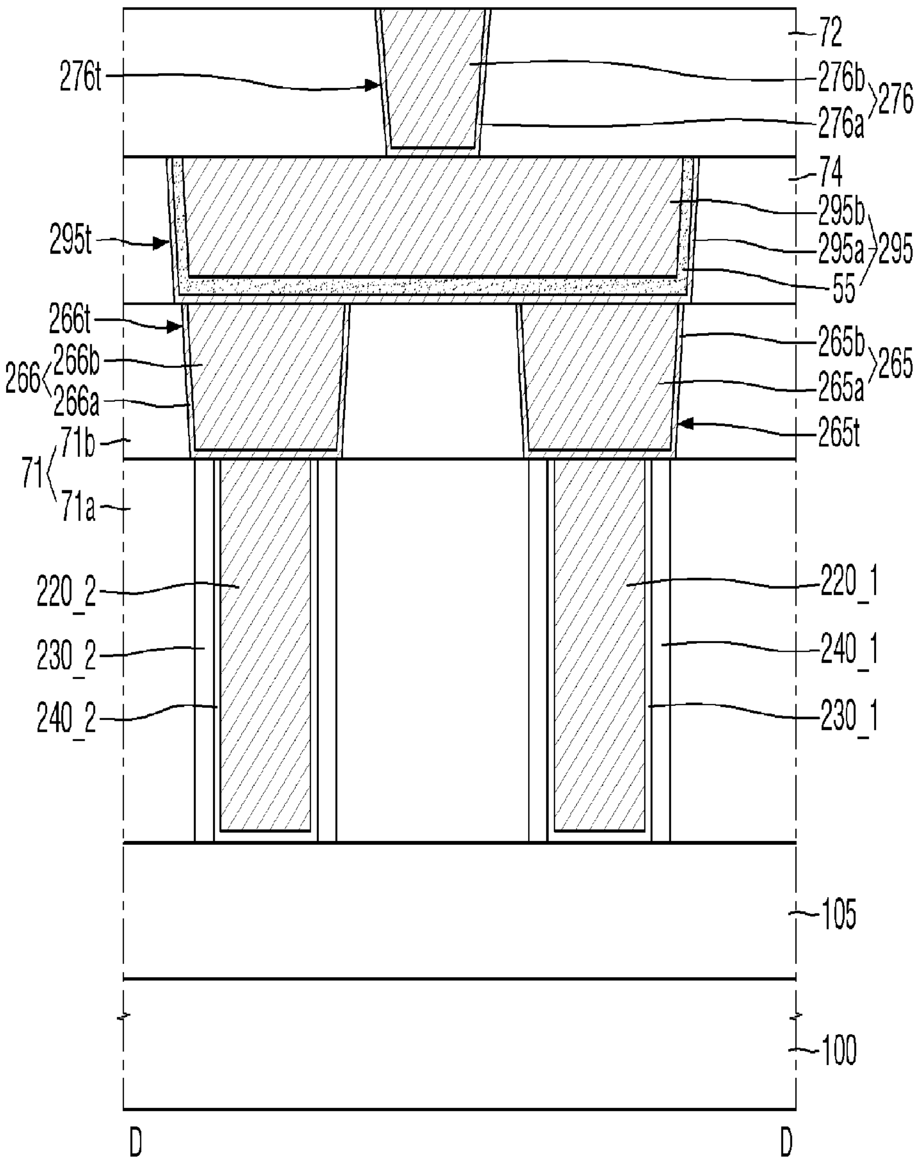


FIG. 25



SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2018-0078671, filed on Jul. 6, 2018, and Korean Patent Application No. 10-2018-0133386, filed on Nov. 2, 2018, in the Korean Intellectual Property Office, the disclosures of which are incorporated herein in their entirety by reference.

BACKGROUND

1. Field of the Disclosure

[0002] The present disclosure relates to a semiconductor device, and more specifically, to a semiconductor device which includes a negative capacitor having a negative capacitance using a ferroelectric material.

2. Description of the Related Art

[0003] After development of metal oxide semiconductor field effect transistors (MOSFETs), the degree of integration of integrated circuits has continuously increased. For example, the degree of integration of the integrated circuit shows a tendency that the total number of transistors per unit chip area is doubled every two years. In order to increase the degree of integration of the integrated circuit, the size of the individual transistor has continuously decreased. In addition, semiconductor technologies for improving the performance of miniaturized transistors have appeared.

[0004] In such semiconductor technologies, there may be a high-K metal gate (HKMG) technology which improves a gate capacitance and reduces a leakage current, and a FinFET technology capable of improving a SCE (short channel effect) in which potential of a channel region is affected by a drain voltage.

[0005] However, as compared with the miniaturization of the transistor size, lowering of a drive voltage of the transistor was not greatly improved. As a result, a power density of a complementary metal oxide (CMOS) transistor increases exponentially. In order to reduce the power density, a decrease in the power of the drive voltage is necessarily required. However, because a silicon-based MOSFET has thermal emission-based physical operating characteristics, it is difficult to achieve a very low supply voltage.

[0006] For this reason, the necessity of development of a transistor having a subthreshold swing below 60 mV/decade or less, which is known as a physical limit of the subthreshold swing (SS) at normal temperature, has emerged.

SUMMARY

[0007] According to an exemplary embodiment of the present inventive concept, a semiconductor device includes a substrate, a gate structure on the substrate and a first conductive connection group on the gate structure. The gate structure includes a gate spacer and a gate electrode. The first conductive connection group includes a ferroelectric material layer. At least a part of the ferroelectric material layer is disposed above an upper surface of the gate spacer. And the ferroelectric material layer forms a ferroelectric capacitor having a negative capacitance in the first conductive connection group.

[0008] According to an exemplary embodiment of the present inventive concept, a semiconductor device includes a substrate, a gate structure including a gate electrode on the substrate, a source/drain region disposed in a region of the substrate adjacent to at least one side of the gate structure, a first conductive connection group disposed on the gate electrode and connected to the gate electrode, and a second conductive connection group connected to the source/drain region and disposed on the source/drain region. The first conductive connection group includes a ferroelectric material layer. The first conductive connection group includes a gate contact plug being in contact with the gate electrode. The second conductive connection group includes a source/drain contact plug being in contact with the source/drain region. An upper surface of the gate contact plug is positioned at substantially the same height as an upper surface of the source/drain contact plug from an upper surface of the substrate. A height from an upper surface of the gate structure to an uppermost surface of the ferroelectric material layer is equal to or greater than a height from the upper surface of the gate structure to the upper surface of the source/drain contact plug.

[0009] According to an exemplary embodiment of the present inventive concept, a semiconductor device includes a substrate including an active region and a field region, a first gate electrode on the substrate, the first gate electrode extending over the active region and the field region in a first direction, and a first gate contact plug on the first gate electrode, the first gate contact plug being connected to the first gate electrode and including a ferroelectric material layer. A width of the first gate contact plug in the first direction being smaller than a length of the first gate electrode in the first direction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The above and other aspects and features of the present disclosure will become more apparent by describing in detail example embodiments thereof with reference to the attached drawings, in which:

[0011] FIG. **1** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0012] FIG. **2** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0013] FIG. **3** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0014] FIG. **4** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0015] FIG. **5** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0016] FIG. **6** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0017] FIG. **7** is a cross-sectional view for explaining a semiconductor device according to some embodiments of the present disclosure;

[0018] FIG. **8** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0019] FIG. **9** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0020] FIGS. **10** to **12** are cross-sectional views taken along lines A-A, B-B and C-C of FIG. **9**;

[0021] FIGS. **13**_a_ to **13**_e_ are diagrams for explaining an example shape that an upper surface of a second gate contact plug may have;

[0022] FIGS. **14** and **15** are diagrams for explaining a semiconductor device according to some embodiments of the present disclosure;

[0023] FIG. **16** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0024] FIG. **17** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0025] FIG. **18** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0026] FIG. **19** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0027] FIG. **20** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0028] FIG. **21** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0029] FIG. **22** is a cross-sectional view taken along line D-D of FIG. **21**;

[0030] FIG. **23** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure;

[0031] FIG. **24** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure; and

[0032] FIG. **25** is a cross-sectional view taken along line D-D of FIG. **24**.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0033] In the drawings of the semiconductor device according to some embodiments of the present disclosure, a fin type transistor (FinFET) including a fin type pattern-shaped channel region or a planar transistor is exemplarily illustrated, but the disclosure is not limited thereto. It is a matter of course that the semiconductor device according to some embodiments of the present disclosure may include a tunneling FET, a transistor including a nanowire, a transistor including a nanosheet or a three-dimensional (3D) transistor. In addition, the semiconductor device according to some embodiments of the present disclosure may include a bipolar junction transistor, a lateral double diffused transistor (LDMOS) or the like.

[0034] FIG. **1** is a diagram for explaining the semiconductor device according to some embodiments of the present disclosure.

[0035] Referring to FIG. **1**, the semiconductor device according to some embodiments of the present disclosure may include a first gate structure **115**, a first source/drain region **150**, a first conductive connection group **155**, and a second conductive connection group **156**.

[0036] The substrate **100** may be a bulk silicon substrate or a silicon-on-insulator (SOI) substrate. Alternatively, the substrate **100** may be a silicon substrate or may include, but is not limited to, other materials, for example, silicon germanium, silicon germanium on insulator (SGOI), indium antimonide, lead tellurium compound, indium arsenide, phosphide indium, gallium arsenide or gallium antimonide.

[0037] An element isolation film **101** may be formed in the substrate **100**. The element isolation film **101** may define an active region. The element isolation film **101** may include, for example, at least one of silicon oxide, silicon oxynitride and silicon nitride.

[0038] The first gate structure **115** may be formed on the substrate **100**. The first gate structure **115** may include a first gate spacer **140**, a first gate electrode **120**, a first interfacial layer **135**, and a first gate insulating layer **130**.

[0039] The first gate spacer **140** may be formed on the substrate **100**. The first gate spacer **140** may define a space in which the first interfacial layer **135**, the first gate insulating layer **130** and the first gate electrode **120** are formed.

[0040] The first gate spacer **140** may include, for example, at least one of silicon nitride (SiN), silicon oxynitride (SiON), silicon oxide (SiO_2), and silicon oxycarbonitride (SiOCN).

[0041] The first interfacial layer **135** may be formed on the substrate **100**. The first interfacial layer **135** may be formed between two first gate spacers of the first gate spacer **140**. Although the first interfacial layer **135** is illustrated as being formed only on the upper surface of the substrate **100**, the disclosure is not limited thereto. Depending on the fabricating method, the first interfacial layer **135** may extend along the sidewalls of the first gate spacer **140**.

[0042] When the substrate **100** contains silicon, the first interfacial layer **135** may include at least one of a silicon oxide layer, a silicon oxynitride layer and a silicon nitride layer.

[0043] The first gate insulating layer **130** may be formed on the first interfacial layer **135**. The first gate insulating layer **130** may extend along the upper surface of the substrate **100** and the sidewalls of the first gate spacer **140**.

[0044] The first gate insulating layer **130** may include, for example, one or more of hafnium oxide, hafnium silicon oxide, hafnium aluminum oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide or lead zinc niobate.

[0045] Unlike the illustrated case, the first gate insulating layer **130** may be formed only on the upper surface of the substrate **100** without extending along the sidewalls of the first gate spacer **140**.

[0046] Also, unlike the illustrated case, the first gate insulating layer **130** may not be formed on the first interfacial layer **135**. In addition, the first interfacial layer **135** may not be formed between the first gate insulating layer **130** and the substrate **100**. For example, the first interfacial layer **135** may be omitted so that the first gate insulating layer **130** may be in contact with the upper surface of the substrate **100**.

[0047] The first gate electrode **120** may be formed on the first gate insulating layer **130**. The first gate electrode **120** may fill a space defined by the first gate spacer **140**. For

example, the upper surface of the first gate electrode **120** may be placed on the same plane as the upper surface of the first gate spacer **140**.

[0048] The first gate electrode **120** may include, for example, at least one of titanium nitride (TiN), tantalum carbide (TaC), tantalum nitride (TaN), titanium silicon nitride (TiSiN), tantalum silicon nitride (TaSiN), tantalum titanium nitride (TaTiN), titanium aluminum nitride (TiAlN), tantalum aluminum nitride (TaAlN), tungsten nitride (WN), ruthenium (Ru), titanium aluminum (TiAl), titanium aluminum carbonitride (TiAlC—N), titanium aluminum carbide (TiAlC), titanium carbide (TiC), tantalum carbonitride (TaCN), tungsten (W), aluminum (Al), copper (Cu), cobalt (Co), titanium (Ti), tantalum (Ta), nickel (Ni), platinum (Pt), nickel platinum (Ni—Pt), niobium (Nb), niobium nitride (NbN), niobium carbide (NbC), molybdenum (Mo), molybdenum nitride (MoN), molybdenum carbide (MoC), tungsten carbide (WC), rhodium (Rh), palladium (Pd), iridium (Ir), osmium (Os), silver (Ag), gold (Au), zinc (Zn), vanadium (V), and combinations thereof.

[0049] A first source/drain region **150** may be formed on at least one side of the first gate structure **115**. As an example, the first source/drain region **150** may be formed by implanting impurities into the substrate **100**. As another example, the first source/drain region **150** may include an epitaxial pattern. The epitaxial pattern may fill recesses formed in the substrate **100**.

[0050] Although not illustrated, the first source/drain region **150** may also include a metal silicide layer.

[0051] A first interlayer insulating layer **71** may be formed on the substrate **100**. The first interlayer insulating layer **71** may cover the first source/drain region **150** and the first gate structure **115**. Although the first interlayer insulating layer **71** is illustrated as a single layer, the present disclosure is not limited thereto. For example, the first interlayer insulating layer **71** may be a plurality of insulating layers formed in different processes with reference to an upper surface **140*u*** of the first gate spacer.

[0052] A second interlayer insulating layer **72** and a third interlayer insulating layer **73** may be sequentially formed on the first interlayer insulating layer **71**.

[0053] Each of the first interlayer insulating layer **71**, the second interlayer insulating layer **72** and the third interlayer insulating layer **73** may include, but is not limited to, for example, silicon oxide, silicon nitride, silicon oxynitride, FOX (Flowable Oxide), TOSZ (Tonen SilaZene), USG (Undoped Silica Glass), BSG (Borosilica Glass), PSG (PhosphoSilica Glass), BPSG (BoroPhosphoSilica Glass), PETEOS (Plasma Enhanced Tetra Ethyl Ortho Silicate), FSG (Fluoride Silicate Glass), CDO (Carbon Doped Silicon Oxide), Xerogel, Aerogel, Amorphous Fluorinated Carbon, OSG (Organo Silicate Glass), Parylene, BCB (bis-benzocyclobutenes), SiLK, polyimide, porous polymeric material or combinations thereof.

[0054] A first conductive connection group **155** may be formed on the substrate **100**. The first conductive connection group **155** may be connected to the first gate electrode **120**.

[0055] The first conductive connection group **155** may include a first gate contact plug **165**, a first lower via plug **176**, a first lower interlayer wiring **177**, a first upper via plug **186**, and a first upper interlayer wiring **187**. The first lower interlayer wiring **177** is formed at a metal level different from that of the first upper interlayer wiring **187**. For example, the metal level of the first lower interlayer wiring **177** is lower than that of the first upper interlayer wiring **187**.

[0056] The first gate contact plug **165** may be formed on the first gate structure **115**. The first gate contact plug **165** may be connected to the first gate electrode **120**. The first gate contact plug **165** may be in contact with the first gate electrode **120**.

[0057] The first gate contact plug **165** may be formed in a first gate contact hole **165*t*** inside the first interlayer insulating layer **71**. The first gate contact hole **165*t*** may expose the first gate electrode **120**.

[0058] The first gate contact plug **165** may include a first gate contact barrier layer **165*a***, a first ferroelectric material layer **50** and a first gate contact filling layer **165*b*** on the first gate electrode **120**. An upper surface of the first gate contact plug **165** is higher than an upper surface of the first gate structure **115**.

[0059] The first gate contact barrier layer **165*a*** may extend along sidewalls and a bottom surface of the first gate contact hole **165*t***.

[0060] The first ferroelectric material layer **50** may be formed on the first gate contact barrier layer **165*a***. The first ferroelectric material layer **50** may extend along sidewalls and a bottom surface of the first gate contact hole **165*t***. At least a part of the first ferroelectric material layer may be disposed above the upper surface **140*u*** of the first gate spacer. In an example embodiment, an uppermost surface of the first ferroelectric material layer **50** is higher than the upper surface **140*u*** of the first gate spacer.

[0061] The first gate contact filling layer **165*b*** may be formed on the first ferroelectric material layer **50**. The first gate contact filling layer **165*b*** may fill the first gate contact hole **165*t***.

[0062] The first lower via plug **176** may be formed on the first gate contact plug **165**. The first lower via plug **176** may be connected to the first gate contact plug **165**. The first lower via plug **176** may be in contact with the first gate contact plug **165**.

[0063] The first lower via plug **176** may be formed in a first lower via hole **176*t*** inside the second interlayer insulating layer **72**. The first lower via hole **176*t*** may expose the first gate contact plug **165**.

[0064] The first lower via plug **176** may include a first lower via barrier layer **176*a*** and a first lower via filling layer **176*b*** on the first gate contact plug **165**.

[0065] The first lower via barrier layer **176*a*** may be formed along sidewalls and a bottom surface of the first lower via hole **176*t***. The first lower via filling layer **176*b*** may be formed on the first lower via barrier layer **176*a***. The first lower via filling layer **176*b*** may fill the first lower via hole **176*t***.

[0066] The first lower interlayer wiring **177** may be formed on the first lower via plug **176**. The first lower interlayer wiring **177** may be connected to the first lower via plug **176**. The first lower interlayer wiring **177** may be in contact with the first lower via plug **176**.

[0067] The first lower interlayer wiring **177** may be formed in a first lower wiring trench **177*t*** inside the second interlayer insulating layer **72**. The first lower via hole **176*t*** may be formed on the bottom surface of the first lower wiring trench **177*t***. For example, the first lower via hole **176*t*** may be connected to the bottom surface of the first lower wiring trench **177*t***.

[0068] The first lower interlayer wiring **177** may include a first lower wiring barrier layer **177***a* and a first lower wiring filling layer **177***b* on the first lower via plug **176**.

[0069] The first lower wiring barrier layer **177***a* may be formed along sidewalls and a bottom surface of the first lower wiring trench **177***t*. The first lower wiring filling layer **177***b* may be formed on the first lower wiring barrier layer **177***a*. The first lower wiring filling layer **177***b* may fill the first lower wiring trench **177***t*.

[0070] The first lower wiring barrier layer **177***a* and the first lower via barrier layer **176***a* may be formed by the same fabricating process, and the first lower wiring filling layer **177***b* and the first lower via filling layer **176***b* may be formed by the same fabricating process. For example, the first lower interlayer wiring **177** and the first lower via plug **176** may be integrally formed using a dual-damascene process. As a result, the first lower via plug **176** and the first lower interlayer wiring **177** may achieve an integral structure.

[0071] The first upper via plug **186** may be formed on the first lower interlayer wiring **177**. The first upper via plug **186** may be connected to the first lower interlayer wiring **177**.

[0072] The first upper via plug **186** may be formed in a first upper via hole **186***t* inside the third interlayer insulating layer **73**. The first upper via plug **186** may include a first upper via barrier layer **186***a* and a first upper via filling layer **186***b* on the first lower interlayer wiring **177**.

[0073] The first upper via barrier layer **186***a* may be formed along sidewalls and a bottom surface of the first upper via hole **186***t*. The first upper via filling layer **186***b* may be formed on the first upper via barrier layer **186***a*. The first upper via filling layer **186***b* may fill the first upper via hole **186***t*.

[0074] The first upper interlayer wiring **187** may be formed on the first upper via plug **186**. The first upper interlayer wiring **187** may be connected to the first upper via plug **186**. The first upper interlayer wiring **187** may be contact with the first upper via plug **186**.

[0075] The first upper interlayer wiring **187** may be formed in a first upper wiring trench **187***t* inside the third interlayer insulating layer **73**. The first upper via hole **186***t* may be formed on the bottom surface of the first upper wiring trench **187***t*. For example, the first upper via hole **186***t* may be connected to the bottom surface of the first upper wiring trench **187***t*.

[0076] The first upper interlayer wiring **187** may include a first upper wiring barrier layer **187***a* and a first upper wiring filling layer **187***b* on the first upper via plug **186**.

[0077] The first upper wiring barrier layer **187***a* may be formed along sidewalls and a bottom surface of the first upper wiring trench **187***t*. The first upper wiring filling layer **187***b* may be formed on the first upper wiring barrier layer **187***a*. The first upper wiring filling layer **187***b* may fill the first upper wiring trench **187***t*.

[0078] The first upper wiring barrier layer **187***a* and the first upper via barrier layer **186***a* may be formed by the same fabricating process, and the first upper wiring filling layer **187***b* and the first upper via filling layer **186***b* may be formed by the same fabricating process. For example, the first upper interlayer wiring **187** and the first upper via plug **186** may be integrally formed using a dual-damascene process. As a result, the first upper via plug **186** and the first upper interlayer wiring **187** may achieve an integrated structure.

[0079] Unlike the illustrated case, other via plugs and interlayer wirings may be further formed between the first upper via plug **186** and the first lower interlayer wiring **177**.

[0080] The second conductive connection group **156** may be formed on the substrate **100**. The second conductive connection group **156** may be connected to the first source/drain region **150**.

[0081] The second conductive connection group **156** may include a first source/drain contact plug **160**, a second lower via plug **171**, a second lower interlayer wiring **172**, a second upper via plug **181**, and a second upper interlayer wiring **182**. The second lower interlayer wiring **172** is formed at a metal level different from that of the second upper interlayer wiring **182**. The first lower interlayer wiring **177** and the second lower interlayer wiring **172** may be formed at the same metal level, and the first upper interlayer wiring **187** and the second upper interlayer wiring **182** may be formed at the same metal level.

[0082] The first source/drain contact plug **160** may be formed on the first source/drain region **150**. The first source/drain contact plug **160** may be connected to the first source/drain region **150**. The first source/drain contact plug **160** may be in contact with the first source/drain region **150**.

[0083] The first source/drain contact plug **160** may be formed in a first source/drain contact hole **160***t* inside the first interlayer insulating layer **71**. The first source/drain contact hole **160***t* may expose the first source/drain region **150**.

[0084] The first source/drain contact plug **160** may include a first source/drain contact barrier layer **160***a* and a first source/drain contact filling layer **160***b* on the first source/drain region **150**.

[0085] The first source/drain contact barrier layer **160***a* may extend along sidewalls and a bottom surface of the first source/drain contact hole **160***t*. The first source/drain contact filling layer **160***b* may be formed on the first source/drain contact barrier layer **160***a*. The first source/drain contact filling layer **160***b* may fill the first source/drain contact hole **160***t*.

[0086] The upper surface of the first source/drain contact plug **160** is higher than the upper surface of the first gate structure **115**. The upper surface of the first source/drain contact plug **160** may be placed on the same plane as the upper surface of the first gate contact plug **165**.

[0087] In the semiconductor device according to some embodiments of the present disclosure, a height h**11** from the upper surface of the first gate structure **115** to the uppermost surface of the first ferroelectric material layer **50** may be the same as or greater than a height h**12** from the upper surface of the first gate structure **115** to the upper surface of the first source/drain contact plug **160**. For example, the uppermost surface of the first ferroelectric material layer **50** may be positioned at the same as or higher than the upper surface of the first source/drain contact plug **160** in a vertical direction perpendicular to the upper surface of the substrate **100**.

[0088] For example, the height h**11** from the upper surface of the first gate structure **115** to the uppermost surface of the first ferroelectric material layer **50** may be substantially the same as the height h**12** from the upper surface of the first gate structure **115** to the upper surface of the first source/drain contact plug **160**.

[0089] The second lower via plug **171** may be formed on the first source/drain contact plug **160**. The second lower via plug **171** may be connected to the first source/drain contact

plug **160**. The second lower via plug **171** may be in contact with the first source/drain contact plug **160**.

[0090] The second lower via plug **171** may be formed in a second lower via hole **171***t* inside the second interlayer insulating layer **72**. The second lower via hole **171***t* may expose the first source/drain contact plug **160**.

[0091] The second lower via plug **171** may include a second lower via barrier layer **171***a* and a second lower via filling layer **171***b* on the first source/drain contact plug **160**.

[0092] The second lower via barrier layer **171***a* may be formed along sidewalls and a bottom surface of the second lower via hole **171***t*. The second lower via filling layer **171***b* may be formed on the second lower via barrier layer **171***a*. The second lower via filling layer **171***b* may fill the second lower via hole **171***t*.

[0093] The second lower interlayer wiring **172** may be formed on the second lower via plug **171**. The second lower interlayer wiring **172** may be connected to the second lower via plug **171**. The second lower interlayer wiring **172** may be in contact with the second lower via plug **171**.

[0094] The second lower interlayer wiring **172** may be formed in a second lower wiring trench **172***t* inside the second interlayer insulating layer **72**. The second lower via hole **171***t* may be formed on the bottom surface of the second lower wiring trench **172***t*. For example, the second lower via hole **171***t* may be connected to the bottom surface of the second lower wiring trench **172***t*.

[0095] The second lower interlayer wiring **172** may include a second lower wiring barrier layer **172***a* and a second lower wiring filling layer **172***b* on the second lower via plug **171**.

[0096] The second lower wiring barrier layer **172***a* may be formed along sidewalls and the bottom surface of the second lower wiring trench **172***t*. The second lower wiring filling layer **172***b* may be formed on the second lower wiring barrier layer **172***a*. The second lower wiring filling layer **172***b* may fill the second lower wiring trench **172***t*.

[0097] The second lower wiring barrier layer **172***a* and the second lower via barrier layer **171***a* may be formed by the same fabricating process, and the second lower wiring filling layer **172***b* and the second lower via filling layer **171***b* may be formed by the same fabricating process. For example, the second lower via plug **171** and the second lower interlayer wiring **172** may be integrally formed using a dual-damascene process. Therefore, the second lower via plug **171** and the second lower interlayer wiring **172** may achieve an integrated structure.

[0098] A second upper via plug **181** may be formed on the second lower interlayer wiring **172**. The second upper via plug **181** may be connected to the second lower interlayer wiring **172**.

[0099] The second upper via plug **181** may be formed in the second upper via hole **181***t* inside the third interlayer insulating layer **73**. The second upper via plug **181** may include a second upper via barrier layer **181***a* and a second upper via filling layer **181***b* on the second lower interlayer wiring **172**.

[0100] The second upper via barrier layer **181***a* may be formed along sidewalls and a bottom surface of the second upper via hole **181***t*. The second upper via filling layer **181***b* may be formed on the second upper via barrier layer **181***a*. The second upper via filling layer **181***b* may fill the second upper via hole **181***t*.

[0101] The second upper interlayer wiring **182** may be formed on the second upper via plug **181**. The second upper interlayer wiring **182** may be connected to the second upper via plug **181**. The second upper interlayer wiring **182** may be in contact with the second upper via plug **181**.

[0102] The second upper interlayer wiring **182** may be formed in a second upper wiring trench **182***t* inside the third interlayer insulating layer **73**. The second upper via hole **181***t* may be formed on the bottom surface of the second upper wiring trench **182***t*. For example, the second upper via hole **181***t* may be connected to the bottom surface of the second upper wiring trench **182***t*.

[0103] The second upper interlayer wiring **182** may include a second upper wiring barrier layer **182***a* and a second upper wiring filling layer **182***b* on the second upper via plug **181**.

[0104] The second upper wiring barrier layer **182***a* may be formed along sidewalls and a bottom surface of the second upper wiring trench **182***t*. The second upper wiring filling layer **182***b* may be formed on the second upper wiring barrier layer **182***a*. The second upper wiring filling layer **182***b* may fill the second upper wiring trench **182***t*.

[0105] The second upper wiring barrier layer **182***a* and the second upper via barrier layer **181***a* may be formed by the same fabricating process, and the second upper wiring filling layer **182***b* and the second upper via filling layer **181***b* may be formed by the same fabricating process. For example, the second upper via plug **181** and the second upper interlayer wiring **182** may be integrally formed using a dual damascene process. Therefore, the second upper via plug **181** and the second upper interlayer wiring **182** may achieve an integrated structure.

[0106] The first ferroelectric material layer **50** may have ferroelectric characteristics. The first ferroelectric material layer **50** may have a thickness enough to have ferroelectric characteristics. For example, the first ferroelectric material layer **50** may have a thickness greater than a critical thickness at which the ferroelectric material layer **50** has ferroelectric characteristics. Since the critical thickness showing the ferroelectric characteristics may vary for a kind of a ferroelectric material of the first ferroelectric material layer **50**, the thickness of the first ferroelectric material layer **50** may vary depending on the kind of the ferroelectric material.

[0107] The first ferroelectric material layer **50** may include, for example, at least one of hafnium oxide, hafnium zirconium oxide, zirconium oxide, barium strontium titanium oxide, barium titanium oxide, and lead zirconium titanium oxide. Here, hafnium zirconium oxide may be a material obtained by doping hafnium oxide with zirconium (Zr), and may be a compound of hafnium (Hf), zirconium (Zr) and oxygen (O).

[0108] The first ferroelectric material layer **50** may further include a doping element doped in the aforementioned material. The doping element may be an element selected from aluminum (Al), titanium (Ti), niobium (Nb), lanthanum (La), yttrium (Y), magnesium (Mg), silicon (Si), calcium (Ca), cerium (Ce), dysprosium (Dy), erbium (Er), gadolinium (Gd), germanium (Ge), scandium (Sc), strontium (Sr) and tin (Sn).

[0109] Each of the barrier layers **160***a*, **165***a*, **171***a*, **172***a*, **176***a*, **177***a*, **181***a*, **182***a*, **186***a* and **187***a* may include, for example, at least one of tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), ruthenium (Ru), cobalt (Co), nickel (Ni), nickel boron (NiB), tungsten (W),

tungsten nitride (WN), tungsten carbonitride (WCN), zirconium (Zr), zirconium nitride (ZrN), vanadium (V), vanadium nitride (VN), niobium (Nb), niobium nitride (NbN), platinum (Pt), iridium (Ir) and rhodium (Rh).

[0110] Each of the filling layers **160***b*, **165***b*, **171***b*, **172***b*, **176***b*, **177***b*, **181***b*, **182***b*, **186***b* and **187***b* may include, for example, at least one of aluminum (Al), copper (Cu), tungsten (W) and cobalt (Co).

[0111] The first conductive connection group **155** connected to the first gate electrode **120** may include the first ferroelectric material layer **50**. However, the second conductive connection group **156** connected to the first source/drain region **150** does not include a ferroelectric material layer.

[0112] A conductive layer is formed on the upper and lower parts of the first ferroelectric material layer **50** included in the first conductive connection group **155**. That is, the first conductive connection group **155** may include a ferroelectric capacitor including the first ferroelectric material layer **50**. In FIG. **1**, by disposing the first ferroelectric material layer **50** between the first gate contact barrier layer **165***a* and the first gate contact filling layer **165***b*, a ferroelectric capacitor may be defined. For example, the layered structure of the first gate contact barrier layer **165***a*, the first ferroelectric material layer **50** and the first gate contact filling layer **165***b* may serve as a ferroelectric capacitor.

[0113] The ferroelectric capacitor may have a negative capacitance. The fact that the ferroelectric capacitor has a negative capacity means that the dipole moment of the molecule may be changed when the ferroelectric material receives an energy greater than a specific external energy. Unlike the ordinary dielectric capacitor, in the ferroelectric capacitor, a section having a negative energy may be generated at the phase transition of the material.

[0114] Therefore, when the ferroelectric material layer having the ferroelectric characteristics is used, a capacitor having a negative capacitance in a specific section may be implemented.

[0115] On the other hand, when the ferroelectric capacitor is connected in series with the gate electrode, the overall capacitance may increase. Therefore, the voltage applied to the gate electrode may be amplified.

[0116] As a result, voltage amplification may be implemented in the gate electrode of the transistor, and the switching speed of the transistor may be improved. That is, a transistor having a subthreshold swing (SS) less than 60 mV/decade at room temperature may be implemented.

[0117] FIG. **2** is a diagram illustrating a semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIG. **1** will be mainly described.

[0118] Referring to FIG. **2**, in the semiconductor device according to some embodiments of the present disclosure, the first gate contact plug **165** may include a first ferroelectric material layer a first gate contact barrier layer **165***a*, and a first gate contact filling layer **165***b* sequentially stacked on the first gate electrode **120**.

[0119] The first gate contact barrier layer **165***a* may be disposed between the first ferroelectric material layer **50** and the first gate contact filling layer **165***b*. For example, the first ferroelectric material layer **50** may be in contact with the first gate electrode **120**.

[0120] The ferroelectric capacitor may be defined by disposing the first ferroelectric material layer **50** between the first gate contact barrier layer **165***a* and the first gate electrode **120**.

[0121] FIG. **3** is a diagram illustrating the semiconductor device according to some embodiments of the present disclosure. FIG. **4** is a diagram illustrating the semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIG. **1** will be mainly described.

[0122] Referring to FIGS. **3** and **4**, in the semiconductor device according to some embodiments of the present disclosure, a first lower via plug **176** may include the first ferroelectric material layer **50**.

[0123] The first lower via plug **176** may include a first lower via barrier layer **176***a*, the first ferroelectric material layer **50**, and a first lower via filling layer **176***b* formed on the first gate contact plug **165**.

[0124] The first ferroelectric material layer **50** may be disposed between the first lower via barrier layer **176***a* and the first lower via filling layer **176***b*. A ferroelectric capacitor may be defined by disposing the first ferroelectric material layer **50** between the first lower via barrier layer **176***a* and the first lower via filling layer **176***b*.

[0125] In an example embodiment, the first lower via barrier layer **176***a* may be disposed between the first ferroelectric material layer **50** and the first lower via filling layer **176***b*.

[0126] The first lower interlayer wiring **177** may not include the first ferroelectric material layer **50**. The first ferroelectric material layer **50** may not extend along the lower surface of the first lower wiring filling layer **177***b*. That is, the first ferroelectric material layer **50** may not extend along the bottom surface of the first lower wiring trench **177***t*.

[0127] A height h**11** from the upper surface of the first gate structure **115** to the uppermost surface of the first ferroelectric material layer **50** is larger than a height h**12** from the upper surface of the first gate structure **115** to the upper surface of the first source/drain contact plug **160**.

[0128] In FIG. **3**, the first lower wiring filling layer **177***b* may be in contact with the first ferroelectric material layer **50**. The first lower wiring filling layer **177***b* may be directly connected to the first lower via filling layer **176***b*.

[0129] In FIG. **4**, the first lower wiring filling layer **177***b* may not be in contact with the first ferroelectric material layer **50**. A first lower wiring barrier layer **177***a* may be disposed between the first lower wiring filling layer **177***b* and the first ferroelectric material layer **50**. The first lower wiring filling layer **177***b* and the first lower via filling layer **176***b* may be separated from each other by the first lower wiring barrier layer **177***a*.

[0130] FIG. **5** is a diagram for explaining the semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIG. **1** will be mainly described.

[0131] Referring to FIG. **5**, in the semiconductor device according to some embodiments of the present disclosure, a first lower via plug **176** and a first lower interlayer wiring **177** may include the first ferroelectric material layer **50**.

[0132] The first ferroelectric material layer **50** may include a first portion **50***a* extending along sidewalls and the bottom

surface of the first lower via hole **176**_t_, and a second portion **50**_b_ extending along sidewalls and the bottom surface of the first lower wiring trench **177**_t_.

[0133] The first lower via plug **176** may include a first lower via barrier layer **176**_a_, a first portion **50**_a_ of the first ferroelectric material layer, and a first lower via filling layer **176**_b_ formed on the first gate contact plug **165**.

[0134] The first lower interlayer wiring **177** may include a first lower wiring barrier layer **177**_a_, a second portion **50**_b_ of the first ferroelectric material layer and a first lower wiring filling layer **177**_b_ formed on the first lower via plug **176**.

[0135] The first ferroelectric material layer **50** may be disposed between the first lower barrier layers **176**_a_ and **177**_a_ and the first lower filling layers **176**_b_ and **177**_b_. A ferroelectric capacitor may be defined by disposing the first ferroelectric material layer **50** between the first lower barrier layers **176**_a_ and **177**_a_ and the first lower filling layers **176**_b_ and **177**_b_.

[0136] FIG. **6** is a diagram for explaining the semiconductor device according to some embodiments of the present disclosure. FIG. **7** is a diagram for explaining the semiconductor device according to some embodiments of the present disclosure. FIG. **8** is a diagram for explaining the semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIG. **1** will be mainly described.

[0137] Referring to FIG. **6**, in the semiconductor device according to some embodiments of the present disclosure, the first upper via plug **186** may include the first ferroelectric material layer **50**.

[0138] The first upper via plug **186** may include a first upper via barrier layer **186**_a_, the first ferroelectric material layer **50** and a first upper via filling layer **186**_b_ formed on the first lower interlayer wiring **177**.

[0139] The first ferroelectric material layer **50** may be disposed between the first upper via barrier layer **186**_a_ and the first upper via filling layer **186**_b_. A ferroelectric capacitor may be defined by disposing the first ferroelectric material layer **50** between the first upper via barrier layer **186**_a_ and the first upper via filling layer **186**_b_.

[0140] Unlike the illustrated case, the first upper via barrier layer **186**_a_ may, of course, be disposed between the first ferroelectric material layer **50** and the first upper via filling layer **186**_b_. The first ferroelectric material layer **50** may be in contact with the first lower wiring filling layer **177**_b_.

[0141] Although it is illustrated that the first upper interlayer wiring **187** does not include the first ferroelectric material layer **50**, the present disclosure is not limited thereto. For example, the first upper interlayer wiring **187** may include the first ferroelectric material layer **50**.

[0142] Referring to FIG. **7**, the semiconductor device according to some embodiments of the present disclosure may further include a first insertion wiring **195** and a second insertion wiring **190**. The first insertion wiring **195** may include the first ferroelectric material layer **50**.

[0143] The first conductive connection group **155** may include a first insertion wiring **195**. The first insertion wiring **195** may be disposed between the first gate contact plug **165** and the first lower via plug **176**.

[0144] The first insertion wiring **195** may be formed on the first gate contact plug **165**. The first insertion wiring **195** may be connected to the first gate contact plug **165**. The first insertion wiring **195** may be in contact with the first gate contact plug **165**.

[0145] The first insertion wiring **195** may be formed in a first insertion wiring trench **195**_t_ inside the insertion interlayer insulating layer **74**. The first insertion wiring trench **195**_t_ may expose the first gate contact plug **165**.

[0146] The first insertion wiring **195** may include a first insertion wiring barrier layer **195**_a_ on the first gate contact plug **165**, the first ferroelectric material layer **50**, and a first insertion wiring filling layer **195**_b_. The first insertion wiring barrier layer **195**_a_ and the first ferroelectric material layer **50** may extend along the sidewalls and the bottom surface of the first insertion wiring trench **195**_t_. The first insertion wiring filling layer **195**_b_ may be formed on the first ferroelectric material layer **50**.

[0147] As illustrated, a ferroelectric capacitor may be defined by disposing the first ferroelectric material layer **50** between the first insertion wiring barrier layer **195**_a_ and the first insertion wiring filling layer **195**_b_.

[0148] On the other hand, unlike the illustrated case above, in a case where the first insertion wiring barrier layer **195**_a_ is disposed between the first ferroelectric material layer **50** and the first insertion wiring filling layer **195**_b_, the first ferroelectric material layer **50** is disposed between the first insertion wiring barrier layer **195**_a_ and the first gate contact plug **165**, thereby defining the ferroelectric capacitor.

[0149] The second conductive connection group **156** may include a second insertion wiring **190**. The second insertion wiring **190** may be disposed between the first source/drain contact plug **160** and the second lower via plug **171**.

[0150] The second insertion wiring **190** may be formed on the first source/drain contact plug **160**. The second insertion wiring **190** may be connected to the first source/drain contact plug **160**. The second insertion wiring **190** may be in contact with the first source/drain contact plug **160**.

[0151] The second insertion wiring **190** may be formed in a second insertion wiring trench **190**_t_ inside the insertion interlayer insulating layer **74**. The second insertion wiring trench **190**_t_ may expose the first source/drain contact plug **160**.

[0152] The second insertion wiring **190** may include a second insertion wiring barrier layer **190**_a_ and a second insertion wiring filling layer **190**_b_ on the first source/drain contact plug **160**.

[0153] Referring to FIG. **8**, in the semiconductor device according to some embodiments of the present disclosure, the first gate structure **115** may further include a first capping pattern **145** on the first gate electrode **120**.

[0154] The upper surface of the first capping pattern **145** may be placed on the same plane as the upper surface **140**_u_ of the first gate spacer.

[0155] A first gate contact hole **165**_t_ may pass through the first capping pattern **145** to expose the first gate electrode **120**.

[0156] FIG. **9** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure. FIGS. **10** to **12** are cross-sectional views taken along lines A-A, B-B and C-C of FIG. **9**. FIGS. **13**_a_ to **13**_e_ are diagrams for explaining example shapes that an upper surface of a second gate contact plug may have.

[0157] For the sake of convenience of explanation, without description of the interlayer wiring, the following

examples will be described, using only the second gate contact plug **265** and a via plug **276** among the conductive connection group connected to a second gate structure **215_1**. Further, explanation will be provided, using only a second source/drain contact plug **260** among the conductive connection group connected to a second source/drain region **250**.

[0158] Further, although FIG. **9** illustrates that one second gate contact plug **265** is formed, it is only for convenience of explanation, and the embodiment is not limited thereto.

[0159] Referring to FIGS. **9** to **12**, the semiconductor device according to some embodiments of the present disclosure may include fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6**, second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5**, the second gate contact plug **265**, and the second source/drain contact plug **260**.

[0160] A substrate **100** may include a first active region ACT**1** and a second active region ACT**2** adjacent to each other, and a field region FX. The field region FX may serve to electrically isolate the first active region ACT**1** and the second active region ACT**2** from each other. Although the field region FX is illustrated as being defined only between the first active region ACT**1** and the second active region ACT**2**, this is for convenience of explanation, and the embodiment is not limited thereto. For example, the field region FX may surround each of the first active region ACT**1** and the second active region ACT**2**.

[0161] The plurality of fin type patterns **210_1**, **201_2** and **210_3** may be formed on the substrate **100** of the first active region ACT**1**. Further, the plurality of fin type patterns **210_4**, **201_5** and **210_6** may be formed on the substrate **100** of the second active region ACT**2**.

[0162] The fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6** may each extend long in a first direction X.

[0163] It is illustrated that the same number of fin type patterns are formed in the first active region ACT**1** and the second active region ACT**2**, but the present disclosure is not limited thereto.

[0164] The fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6** may be a part of the substrate **100**. For example, the fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6** may be epitaxially grown from the substrate **100** or may be formed by patterning the substrate **100**. The fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6** may include silicon or germanium which is an element semiconductor material, respectively.

[0165] Further, the fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6** may include a compound semiconductor, and may include, for example, a group IV-IV compound semiconductor or a group III-V compound semiconductor. The group IV-IV compound semiconductor may be, for example, a binary compound including at least two or more of carbon (C), silicon (Si), germanium (Ge) and tin (Sn), a ternary compound, or a compound obtained by doping these elements with a group IV element. For example, the group III-V compound semiconductor may be, for example, a binary compound, a ternary compound or a quaternary compound formed by combination of at least one of aluminum (Al), gallium (Ga) and indium (In) as a group III element with one of phosphorus (P), arsenic (As) and antimony (Sb) as a group V element.

[0166] A field insulating layer **105** may be formed on the substrate **100**. The field insulating layer **105** may define fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6**. The field insulating layer **105** may be disposed on a part of the sidewalls of the fin type patterns **210_1**, **2102**, **2103**, **2104**, **210_5** and **2106**.

[0167] The field insulating layer **105** may include, for example, at least one of a silicon oxide layer, a silicon nitride layer, and a silicon oxynitride layer.

[0168] The second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5** may be formed on the substrate **100**. The second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5** may extend long in a second direction Y.

[0169] The second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5** may be formed over the first active region ACT**1**, the field region FX and the second active region ACT**2**. The second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5** may be formed on the fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6**. The second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5** may intersect fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6**.

[0170] The second gate structure **215_1** may include a second interfacial layer **235_1**, a second gate insulating layer **230_1**, and a second gate electrode **220_1**. The second gate structure **215_1** may include a second gate spacer **240_1** formed on the sidewalls of the second gate electrode **220_1**.

[0171] The second interfacial layer **235_1** may be formed along the profile of the fin type patterns **210_1** and **210_4** protruding above the upper surface of the field insulating layer **105**. The second gate insulating layer **230_1** may be formed along a profile of fin type patterns **210_1** and **210_4** protruding above the upper surface of the field insulating layer **105**. The second gate electrode **220_1** may be formed on the second gate insulating layer **230_1**.

[0172] The second source/drain region **250** may be formed on the fin type patterns **210_1**, **210_2** and **210_3** disposed in the first active region ACT**1**. A source/drain region may, of course, be formed on the fin type patterns **210_4**, **210_5** and **210_6** disposed in the second active region ACT**2**. Although the second source/drain region **250** is illustrated as having a shape coupled to each other, the embodiment is not limited thereto.

[0173] A first interlayer insulating layer **71** may include a first lower interlayer insulating layer **71***a* and a first upper interlayer insulating layer **71***b*. The first lower interlayer insulating layer **71***a* and the first upper interlayer insulating layer **71***b* may be divided with reference to an upper surface **240***u* of the second gate spacer.

[0174] The second gate contact plug **265** may be formed on the second gate electrode **220_1**. The second gate contact plug **265** may be connected to the second gate electrode **220_1**. The second gate contact plug **265** may be in contact with the second gate electrode **220_1**.

[0175] The second gate contact plug **265** may be formed in a second gate contact hole **265***t* inside the first upper interlayer insulating layer **71***b*. The second gate contact hole **265***t* may expose a part of the second gate electrode **220_1**.

[0176] The second gate contact plug **265** may include a second gate contact barrier layer **265***a*, a second ferroelectric material layer **55**, and a second gate contact filling layer **265***b* on the second gate electrode **220_1**. The upper surface of the second gate contact plug **265** is higher than the upper surface of the second gate structure **215_1**.

[0177] The second gate contact barrier layer **265***a* may extend along sidewalls and a bottom surface of the second gate contact hole **265***t*.

[0178] The second ferroelectric material layer **55** may be formed on the second gate contact barrier layer **265***a*. The second ferroelectric material layer **55** may extend along sidewalls and the bottom surface of the second gate contact hole **265***t*. At least a part of the second ferroelectric material layer **55** may be disposed above the upper surface **240***u* of the second gate spacer. In other ways, the uppermost surface of the second ferroelectric material layer **55** is higher than the upper surface **240***u* of the second gate spacer.

[0179] The second gate contact filling layer **265***b* may be formed on the second ferroelectric material layer **55**. The second gate contact filling layer **265***b* may fill the second gate contact hole **265***t*.

[0180] Unlike the illustrated case, the second gate contact barrier layer **265***a* may be disposed between the second ferroelectric material layer **55** and the second gate contact filling layer **265***b*.

[0181] Since the second gate contact hole **265***t* exposes a part of the second gate electrode **220_1**, a width W12 of the second gate contact plug **265** in the second direction Y is smaller than the width of the second gate electrode **220_1** in the second direction Y.

[0182] The second gate contact plug **265** may extend long in the first direction X. For example, the width W11 of the second gate contact plug **265** in the first direction X may be greater than a width W12 of the second gate contact plug **265** in the second direction Y.

[0183] Further, the width W11 of the second gate contact plug **265** in the first direction X may be greater than not only the width of the second gate electrode **220_1** in the first direction X, but also the width of the second gate structure **215_1** in the first direction X.

[0184] The second gate contact plug **265** may be disposed on the substrate **100** of the field region FX between the first active region ACT**1** and the second active region ACT**2**. The second gate contact plug **265** may be in contact with the second gate electrode **220_1** disposed on the substrate **100** of the field region FX.

[0185] Unlike the illustrated case, the second gate contact plug **265** may be disposed on the substrate **100** rather than the first and second active regions ACT**1** and ACT**2**, while a distal end of the second gate structure **215_1** is located thereon.

[0186] A via plug **276** may be formed on the second gate contact plug **265**. The via plug **276** may be connected to the second gate contact plug **265**. The via plug **276** may be in contact with the second gate contact plug **265**.

[0187] The via plug **276** may be formed in a via hole **276***t* inside the second interlayer insulating layer **72**. The via hole **276***t* may expose the second gate contact plug **265**.

[0188] The via plug **276** may include a via barrier layer **276***a* and a via filling layer **276***b* on the second gate contact plug **265**.

[0189] The via barrier layer **276***a* may be formed along the sidewalls and the bottom surface of the via hole **276***t*. The via filling layer **276***b* may be formed on the via barrier layer **276** *a*. The via filling layer **276***b* may fill the via hole **276***t*.

[0190] The second source/drain contact plug **260** may be formed on the fin type patterns **210_1**, **210_2**, **210_3**, **210_4**, **210_5** and **210_6** between the adjacent second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5**.

[0191] The second source/drain contact plug **260** may be formed on the second source/drain region **250**. The second source/drain contact plug **260** may be connected to the second source/drain region **250**. The second source/drain contact plug **260** may be in contact with the second source/drain region **250**.

[0192] The second source/drain contact plug **260** may be formed in a second source/drain contact hole **260***t* inside the first interlayer insulating layer **71**. The second source/drain contact hole **260***t* may expose the second source/drain region **250**.

[0193] The second source/drain contact plug **260** may include a second source/drain contact barrier layer **260***a* and a second source/drain contact filling layer **260***b* on the second source/drain region **250**.

[0194] The second source/drain contact barrier layer **260***a* may extend along the sidewalls and the bottom surface of the second source/drain contact hole **260***t*. The second source/drain contact filling layer **260***b* may be formed on the second source/drain contact barrier layer **260***a*. The second source/drain contact filling layer **260***b* may fill the second source/drain contact hole **260***t*.

[0195] The upper surface of the second source/drain contact plug **260** may be higher than the upper surface of the second gate structure **215_1**. The upper surface of the second source/drain contact plug **260** may be placed on the same plane as the upper surface of the second gate contact plug **265**.

[0196] A shape of an upper surface **265***u* of the second source/drain contact plug will be described, using FIGS. **13***a* through **13***e*.

[0197] FIGS. **13***a* through **13***c* illustrate a case where the second gate contact plug (**265** of FIG. **9**) extends long in a certain direction. FIGS. **13***d* and **13***e* illustrate a case where the second gate contact plug **265** does not extend long in a specific direction.

[0198] In FIG. **13***a*, a boundary **265**up of the upper surface of the second gate contact plug may have a rectangular shape.

[0199] In FIG. **13***b*, the boundary **265**up of the upper surface of the second gate contact plug may have a rectangular shape with a rounded corner.

[0200] In FIG. **13***c*, the boundary **265**up of the upper surface of the second gate contact plug may have an elliptical shape.

[0201] In FIG. **13***d*, the boundary **265**up of the upper surface of the second gate contact plug may have a square shape.

[0202] In FIG. **13***e*, the boundary **265**up of the upper surface of the second gate contact plug may have a circular shape.

[0203] Unlike the shapes illustrated in FIGS. **13***d* and **13***e*, the boundary **265**up of the upper surface of the second gate contact plug may also be a square shape with rounded corners.

[0204] FIGS. **14** and **15** are diagrams for explaining the semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIGS. **9** to **12** will be mainly described.

[0205] Referring to FIGS. **14** and **15**, in the semiconductor device according to some embodiments of the present dis-

closure, the second gate structure **215_1** may further include a second capping pattern **245** on the second gate electrode **220_1**.

[0206] The second gate contact hole **265*t*** may penetrate a part of the second capping pattern **245** to expose a part of the second gate electrode **220_1**.

[0207] FIG. **16** is a diagram for explaining the semiconductor device according to some embodiments of the present disclosure. FIG. **17** is a diagram for explaining the semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIGS. **9** to **12** will be mainly described.

[0208] Referring to FIG. **16**, in the semiconductor device according to some embodiments of the present disclosure, the first active region ACTT and the second active region ACT**2** may be defined by a deep trench DT.

[0209] In another way, a portion in which the deep trench DT is formed may be a field region FX.

[0210] The deep trench DT is deeper than a trench defining the fin type patterns **210_1** and **210_4**.

[0211] Referring to FIG. **17**, in the semiconductor device according to some embodiments of the present disclosure, a protruding pattern **200**PF protruding from the substrate **100** may be formed in the field region FX.

[0212] The field insulating layer **105** may cover the upper surface of the protruding pattern **200**PF. That is, the upper surface of the protruding pattern **200**PF does not protrude above the upper surface of the field insulating layer **105**.

[0213] FIG. **18** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure. FIG. **19** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure. FIG. **20** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIGS. **9** to **12** will be mainly described, and the via plug (**276** of FIG. **9**) is not illustrated in FIGS. **18** to **20**.

[0214] Referring to FIG. **18**, in the semiconductor device according to some embodiments of the present disclosure, the second gate contact plug **265** may extend long in the second direction Y.

[0215] The width W**11** of the second gate contact plug **265** in the first direction X may be smaller than the width W**12** of the second gate contact plug **265** in the second direction Y.

[0216] Referring to FIG. **19**, in the semiconductor device according to some embodiments of the present disclosure, the second gate contact plug **265** may be formed on the substrate **100** of the first active region ACT**1**.

[0217] The second gate contact plug **265** may be disposed between the second source/drain contact plugs **260** adjacent to each other.

[0218] Referring to FIG. **20**, in the semiconductor device according to some embodiments of the present disclosure, the second gate contact plug **265** may be formed over the first active region ACT**1** and the field region FX.

[0219] A part of the second gate contact plug **265** may be formed on the substrate **100** of the field region FX. The remaining parts of the second gate contact plug **265** may be formed on the substrate **100** of the first active region ACT**1**.

[0220] FIG. **21** is a layout diagram for explaining a semiconductor device according to some embodiments of the present disclosure. FIG. **22** is a cross-sectional view taken along line D-D of FIG. **21**. For the sake of convenience of explanation, differences from those described using FIGS. **9** to **12** will be mainly described.

[0221] Referring to FIGS. **21** and **22**, the semiconductor device according to some embodiments of the present disclosure may further include a third insertion wiring **295**.

[0222] The third insertion wiring **295** may be disposed between the second gate contact plug **265** and the via plug **276**. The third insertion wiring **295** may be connected to the second gate contact plug **265** and the via plug **276**. The third insertion wiring **295** may be in contact with the second gate contact plug **265**.

[0223] The third insertion wiring **295** may be formed in a third insertion wiring trench **295*t*** inside an insertion interlayer insulating layer **74**. The third insertion wiring trench **295*t*** may expose the second gate contact plug **265**.

[0224] The third insertion wiring **295** may include a third insertion wiring barrier layer **295*a*** and a third insertion wiring filling layer **295*b*** on the second gate contact plug **265**. The third insertion wiring barrier layer **295*a*** may extend along the sidewalls and the bottom surface of the third insertion wiring trench **295*t***. The third insertion wiring filling layer **295*b*** may be formed on the third insertion wiring barrier layer **295*a***.

[0225] The third insertion wiring **295** may be formed over at least two or more second gate structures **215_1** and **215_2**. For example, the third insertion wiring **295** may extend onto the upper surface of the second gate structure **215_1** connected to the second gate contact plug **265** and onto the upper surface of the adjacent second gate structure **215_2**. In an example embodiment, a part of the third insertion wiring **295** may extend onto the upper surface of the second gate structure **215_1** connected to the second gate contact plug **265**. Another part of the third insertion wiring **295** may extend onto the upper surface of the adjacent second gate structure **215_2**.

[0226] The via plug **276** may be disposed on the substrate **100** between the second gate structures **215_1** and **215_2** adjacent to each other, but is not limited thereto.

[0227] Unlike the illustrated case, the third insertion wiring **295** may also be formed over three or more second gate structures **215_1**, **215_2**, **215_3**, **215_4** and **215_5**.

[0228] FIG. **23** is a diagram for explaining a semiconductor device according to some embodiments of the present disclosure. For the sake of convenience of explanation, differences from those described using FIG. **21** and FIG. **22** will be mainly described.

[0229] Referring to FIG. **23**, in the semiconductor device according to some embodiments of the present disclosure, the third insertion wiring **295** may include a second ferroelectric material layer **55**.

[0230] A ferroelectric capacitor may be defined by disposing the second ferroelectric material layer **55** between the third insertion wiring barrier layer **295*a*** and the third insertion wiring filling layer **295*b***.

[0231] Unlike the illustrated case, the ferroelectric capacitor may be defined by disposing the second ferroelectric material layer **55** between the third insertion wiring barrier layer **295*a*** and the second gate contact plug **265**.

[0232] FIG. **24** is a layout diagram for explaining a semiconductor device according to some embodiments of

the present disclosure. FIG. **25** is a cross-sectional view taken along line D-D of FIG. **24**. For the sake of convenience of explanation, differences from those described using FIGS. **21** and **23** will be mainly described.

[0233] Referring to FIGS. **24** and **25**, the semiconductor device according to some embodiments of the present disclosure may further include a third gate contact plugs **266** disposed between the third insertion wiring **295** and the second gate structure **215_2**.

[0234] The third gate contact plug **266** may be formed on the second gate electrode **220_2**. The third gate contact plug **266** may be connected to the second gate electrode **220_2**. The third gate contact plug **266** may be in contact with the second gate electrode **220_2**.

[0235] The third gate contact plug **266** may be formed in a third gate contact hole **266***t* inside the first upper interlayer insulating layer **71***b*. The third gate contact hole **266***t* may expose a part of the second gate electrode **220_2**.

[0236] The third gate contact plug **266** may include a third gate contact barrier layer **266***a* and a third gate contact filling layer **266***b* on the second gate electrode **220_2**. The upper surface of the third gate contact plug **266** is higher than the upper surface of the second gate structure **215_2**.

[0237] The third gate contact barrier layer **266***a* may extend along the sidewalls and the bottom surface of the third gate contact hole **266***t*. The third gate contact filling layer **266***b* may be formed on the third gate contact barrier layer **266***a*. The third gate contact filling layer **266***b* may fill the third gate contact hole **266***t*.

[0238] The third gate contact plug **266** may be connected to the third insertion wiring **295**.

[0239] Unlike the case described in FIGS. **9** to **25**, the second ferroelectric material layer **55** may be included in at least one place of the via plug and the interlayer wiring formed in a BEOL process, as described in FIGS. **3** to **6**.

[0240] In concluding the detailed description, those skilled in the art will appreciate that many variations and modifications may be made to the preferred embodiments without substantially departing from the principles of the present disclosure. Therefore, the disclosed preferred embodiments of the disclosure are used in a generic and descriptive sense only and not for purposes of limitation.

1-20. (canceled)

21. A semiconductor device comprising:

a substrate including an active region and a field region defining the active region;

a plurality of fin patterns disposed on the active region of the substrate and extending along in a first direction;

a gate structure on the plurality of fin patterns, the gate structure including a gate spacer and a gate electrode, the gate electrode extending in a second direction and having a first portion on the active region of the substrate and a second portion on the field region of the substrate;

a first conductive connection group on the gate electrode of the gate structure, the first conductive connection group including a ferroelectric material layer;

a source/drain pattern disposed on the plurality of fin patterns; and

a second conductive connection group connected to the source/drain pattern,

wherein at least a part of the ferroelectric material layer is disposed above an upper surface of the gate spacer,

wherein the first conductive connection group includes a gate contact plug being in contact with at least a portion of the first portion of the gate electrode, and

wherein a width of the gate contact plug in the second direction is smaller than a width of the first portion of the gate electrode in the second direction.

22. The semiconductor device of claim **21**, wherein the gate contact plug includes the ferroelectric material layer.

23. The semiconductor device of claim **22**, wherein the gate contact plug further includes a conductive layer, and

the conductive layer is disposed between the ferroelectric material layer and the gate electrode.

24. The semiconductor device of claim **22**, wherein the ferroelectric material layer is in contact with the gate electrode.

25. The semiconductor device of claim **21**, wherein the first conductive connection group further includes a via plug and a interlayer wiring,

the via plug is in contact with the gate contact plug, and the via plug includes the ferroelectric material layer.

26. The semiconductor device of claim **21**, wherein the second conductive connection group does not contain a ferroelectric material layer.

27. The semiconductor device of claim **21**, wherein the width of the gate contact plug in the second direction is smaller than a width of the gate contact plug in the first direction.

28. The semiconductor device of claim **21**, wherein the width of the gate contact plug in the second direction is greater than a width of the gate contact plug in the first direction.

29. The semiconductor device of claim **21**, wherein the entire gate contact plug is in contact with the first portion of the gate electrode.

30. The semiconductor device of claim **21**, wherein the field region of the substrate is a portion in which a deep trench is formed, and

wherein the active region of the substrate is defined by the deep trench.

31. The semiconductor device of claim **21**, wherein the substrate is provided with a protruding pattern disposed in the field region of the substrate and protruding from the substrate.

32. The semiconductor device of claim **31**, further comprising:

a field insulating layer between the substrate and the gate electrode,

wherein the field insulating layer covers an upper surface of the protruding pattern of the substrate.

33. A semiconductor device comprising:

a substrate including an active region and a field region defining the active region;

a plurality of fin patterns disposed on the active region of the substrate and extending along in a first direction;

a gate electrode on the plurality of fin patterns, the gate electrode extending in a second direction and having a first portion on the active region of the substrate and a second portion on the field region of the substrate;

a source/drain pattern disposed on the plurality of fin patterns;

a first conductive connection group on the gate electrode, the first conductive connection group being connected to the gate electrode and including a ferroelectric material layer; and

a second conductive connection group, without connection to the first conductive connection group, connected to the source/drain pattern and disposed on the source/drain pattern,

wherein the first conductive connection group includes a gate contact plug being in contact with at least a portion of the first portion of the gate electrode,

wherein the second conductive connection group includes a source/drain contact plug being in contact with the source/drain pattern,

wherein an upper surface of the gate contact plug is positioned at substantially the same height as an upper surface of the source/drain contact plug relative to an upper surface of the substrate, and

wherein a height from an upper surface of the gate electrode to an uppermost surface of the ferroelectric material layer is equal to or greater than a height from the upper surface of the gate electrode to the upper surface of the source/drain contact plug.

34. The semiconductor device of claim **33**, wherein the second conductive connection group does not include a ferroelectric material layer.

35. The semiconductor device of claim **33**, wherein the gate contact plug includes the ferroelectric material layer.

36. The semiconductor device of claim **33**, wherein the first conductive connection group includes a via plug and an interlayer wiring connected to the gate contact plug, and

the ferroelectric material layer is included in at least one of the via plug and the interlayer wiring.

37. A semiconductor device comprising:

a substrate including an active region and a field region;

a plurality of fin patterns disposed on the active region of the substrate and extending along in a first direction;

a first gate electrode on the plurality of the fin patterns, the first gate electrode extending over the active region and the field region in a second direction and including a first portion on the active region and a second portion on the field region; and

a first gate contact plug on the first portion of the first gate electrode, the first gate contact plug being connected to the first gate electrode and including a ferroelectric material layer,

wherein a first width of the first gate contact plug in the second direction is smaller than a width of the first portion of the first gate electrode in the second direction.

38. The semiconductor device of claim **37**, wherein a second width that the first gate contact plug has in the first direction is different from the first width that the first gate contact plug has in the second direction.

39. The semiconductor device of claim **37**, further comprising:

a via plug on the first gate contact plug; and

an insertion wiring disposed between the first gate contact plug and the via plug.

40. The semiconductor device of claim **39**, further comprising:

a second gate electrode extending over the active region and the field region in the second direction; and

a second gate contact plug on the second gate electrode,

wherein the insertion wiring is further disposed between the second gate contact plug and the via plug and connects the second gate contact plug to the first gate contact plug.

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