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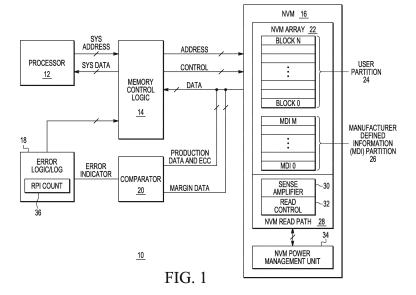
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(54) DATA INTEGRITY CHECK WITHIN A DATA PROCESSING SYSTEM

(57) A memory system includes a memory array, control circuitry, and comparator circuitry. The memory array includes a first section having a first plurality of programmed bitcells having a first threshold voltage distribution and a second section having a second plurality of programmed bitcells having a second threshold voltage distribution which has a lower average threshold voltage than the first threshold voltage distribution. The first plurality and second plurality of programmed bitcells are pro-

grammed with a same set of data values. The control circuitry is configured to provide a read request to the memory array and receive read data in response to the read request, wherein the read data comprises first read data from the first section and second read data from the second section. The comparator circuitry is configured to compare the first read data to the second read data and generate an error indicator in response to the compare.



EP 3 098 816 A3

DOCUMENTS CONSIDERED TO BE RELEVANT

Citation of document with indication, where appropriate,

of relevant passages



Category

EUROPEAN SEARCH REPORT

Application Number

EP 16 16 9875

CLASSIFICATION OF THE APPLICATION (IPC)

Relevant

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EP 3 098 816 A3

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EP 16 16 9875

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