US 20240063199A1

(19) **United States**

(12) **Patent Application Publication**

**Tao et al.**

(10) **Pub. No.: US 2024/0063199 A1**

(43) **Pub. Date: Feb. 22, 2024**

(54) **DIRECT-BONDED OPTOELECTRONIC DEVICES**

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(21) Appl. No.: **18/498,718**

(22) Filed: **Oct. 31, 2023**

**Related U.S. Application Data**

(63) Continuation of application No. 18/206,512, filed on Jun. 6, 2023, which is a continuation of application No. 17/327,169, filed on May 21, 2021, now Pat. No. 11,715,730, which is a continuation of application No. 16/840,245, filed on Apr. 3, 2020, now Pat. No. 11,329,034, which is a continuation of application No. 15/919,570, filed on Mar. 13, 2018, now Pat. No. 10,629,577.

(60) Provisional application No. 62/472,363, filed on Mar. 16, 2017.

**Publication Classification**

(51) **Int. Cl.**

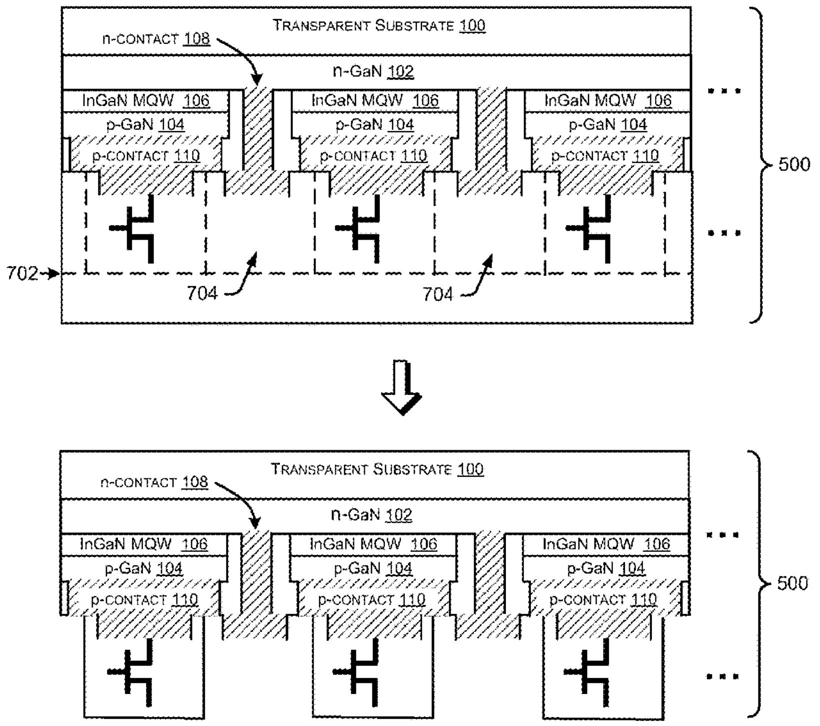
| | |
|---|---|
| ***H01L 25/16*** | (2006.01) |
| ***H01L 33/00*** | (2006.01) |
| ***H01L 25/10*** | (2006.01) |
| ***H01L 27/12*** | (2006.01) |
| ***H01L 27/15*** | (2006.01) |
| ***H01L 25/18*** | (2006.01) |
| ***H01L 21/321*** | (2006.01) |
| ***H01L 21/02*** | (2006.01) |
| ***H01L 23/00*** | (2006.01) |

(52) **U.S. Cl.**

CPC .......... ***H01L 25/167*** (2013.01); ***H01L 33/007*** (2013.01); ***H01L 25/105*** (2013.01); ***H01L 27/1214*** (2013.01); ***H01L 27/156*** (2013.01); ***H01L 25/18*** (2013.01); ***H01L 21/3212*** (2013.01); ***H01L 21/02118*** (2013.01); ***H01L 24/80*** (2013.01); ***H01L 24/08*** (2013.01); ***H01L 33/0093*** (2020.05); *H01L 33/06* (2013.01)

(57) **ABSTRACT**

Direct-bonded LED arrays and applications are provided. An example process fabricates a LED structure that includes coplanar electrical contacts for p-type and n-type semiconductors of the LED structure on a flat bonding interface surface of the LED structure. The coplanar electrical contacts of the flat bonding interface surface are direct-bonded to electrical contacts of a driver circuit for the LED structure. In a wafer-level process, micro-LED structures are fabricated on a first wafer, including coplanar electrical contacts for p-type and n-type semiconductors of the LED structures on the flat bonding interface surfaces of the wafer. At least the coplanar electrical contacts of the flat bonding interface are direct-bonded to electrical contacts of CMOS driver circuits on a second wafer. The process provides a transparent and flexible micro-LED array display, with each micro-LED structure having an illumination area approximately the size of a pixel or a smallest controllable element of an image represented on a high-resolution video display.



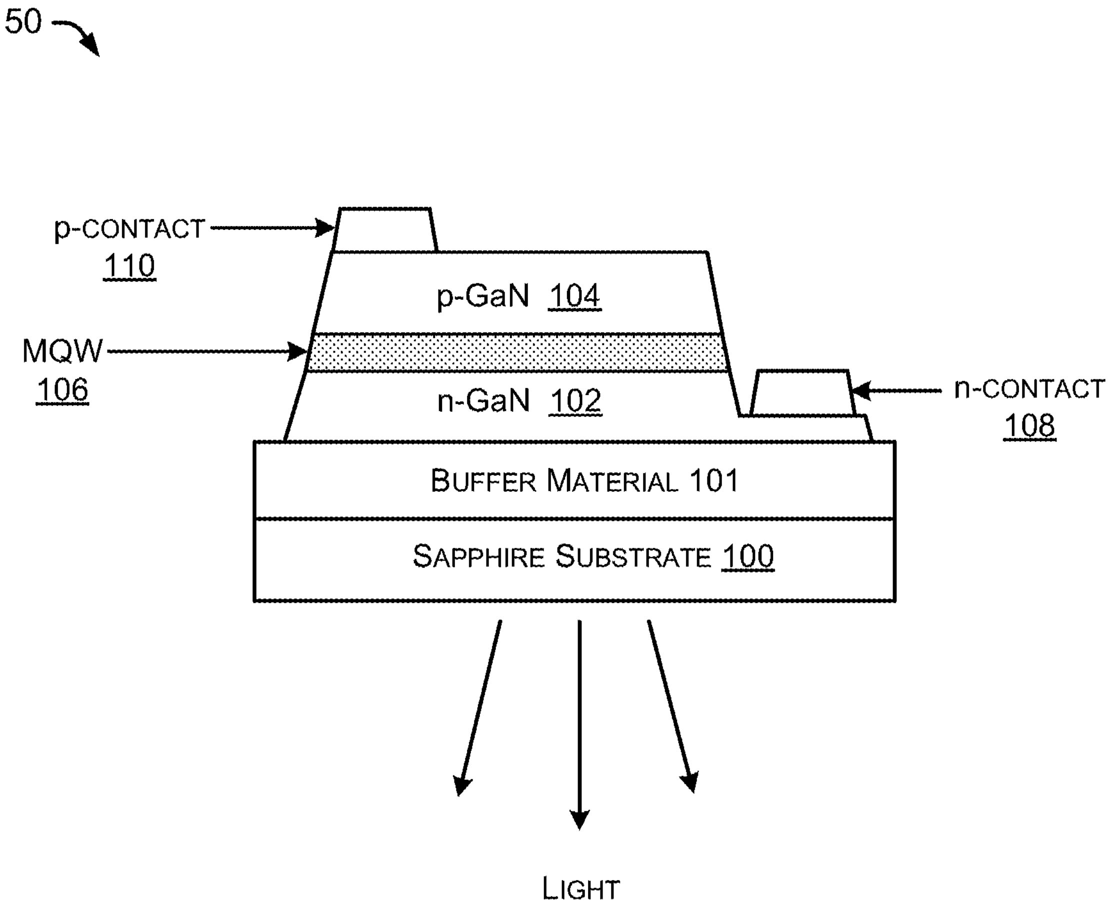


FIG. 1
(PRIOR ART)

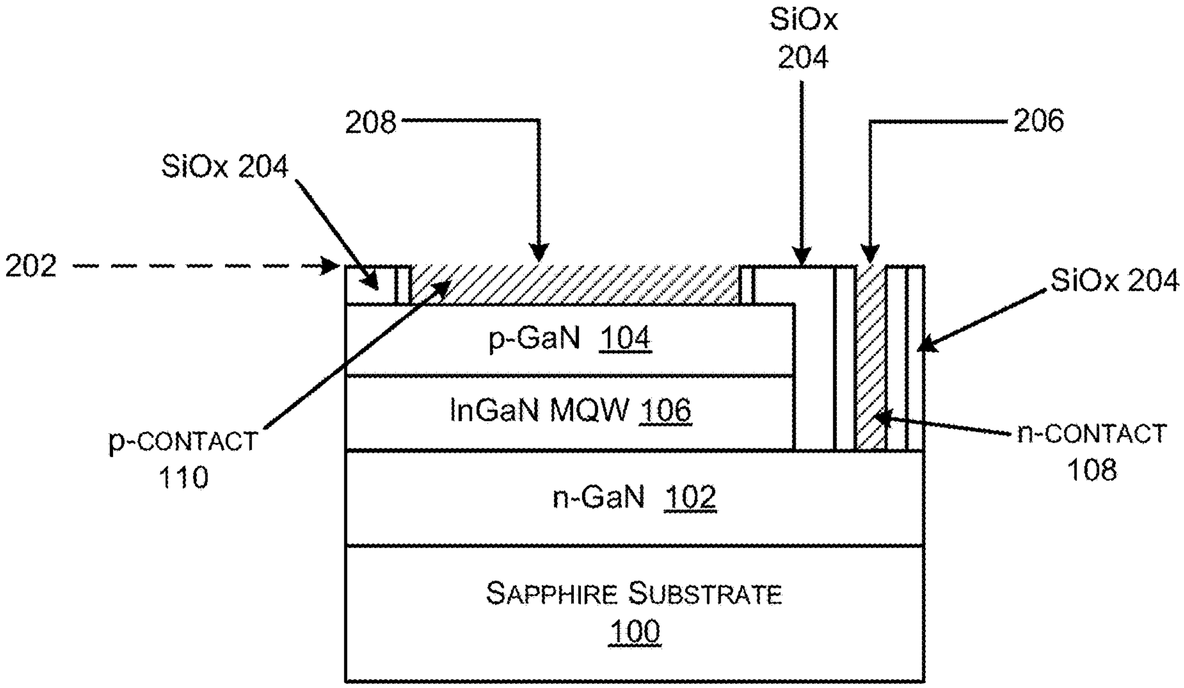

SiOx
204
208
206
SiOx 204
202
SiOx 204
p-GaN 104
InGaN MQW 106
p-CONTACT
110
n-CONTACT
108
n-GaN 102
SAPPHIRE SUBSTRATE
100

FIG. 2

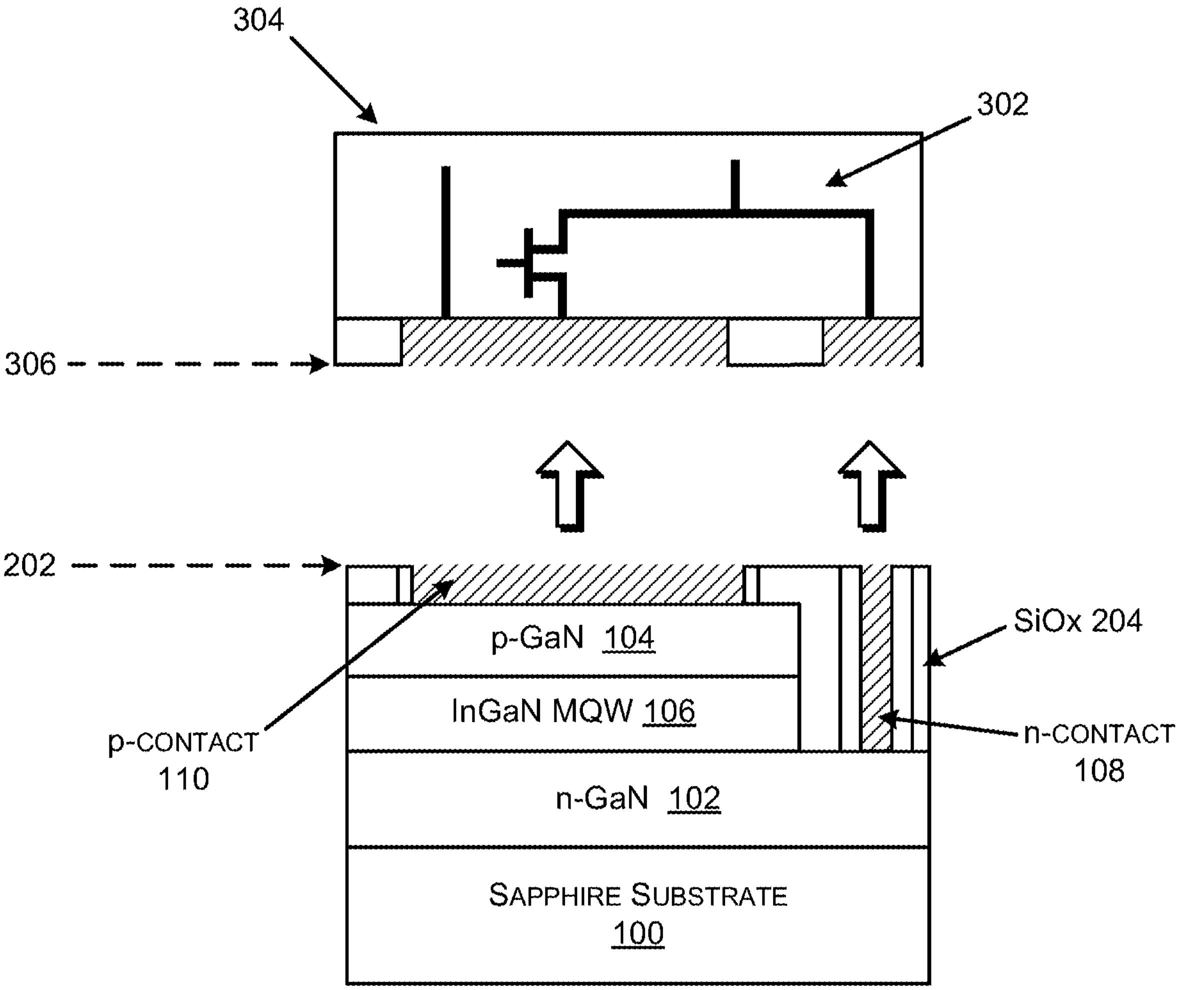

304
302
306
202
SiOx 204
p-GaN 104
InGaN MQW 106
n-CONTACT 108
p-CONTACT 110
n-GaN 102
SAPPHIRE SUBSTRATE 100

FIG. 3

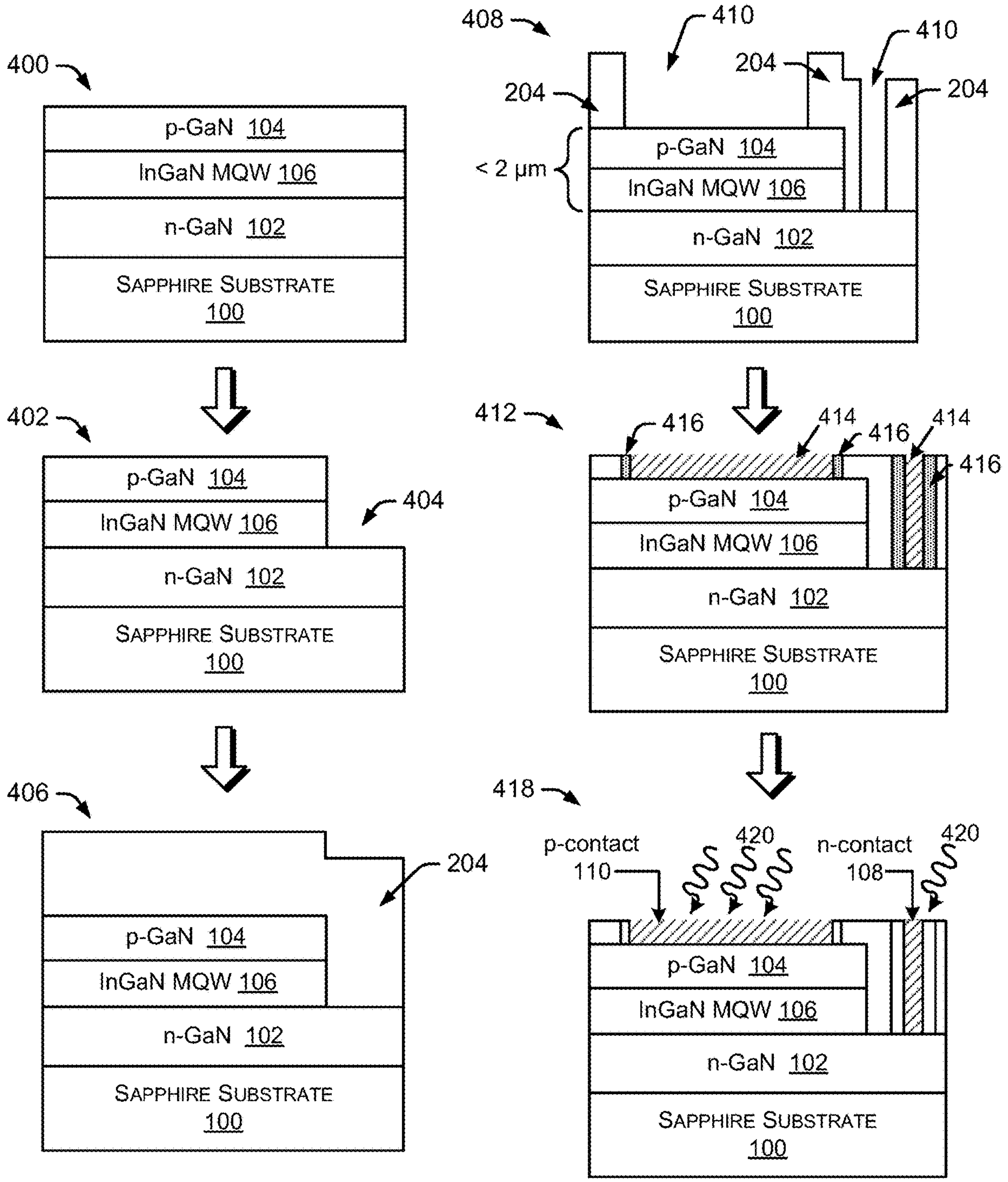

400
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE 100
402
404
406
204
408
410
204
410
204
< 2 μm
412
416
414
416
414
416
418
p-contact 110
420
n-contact 108
420

FIG. 4

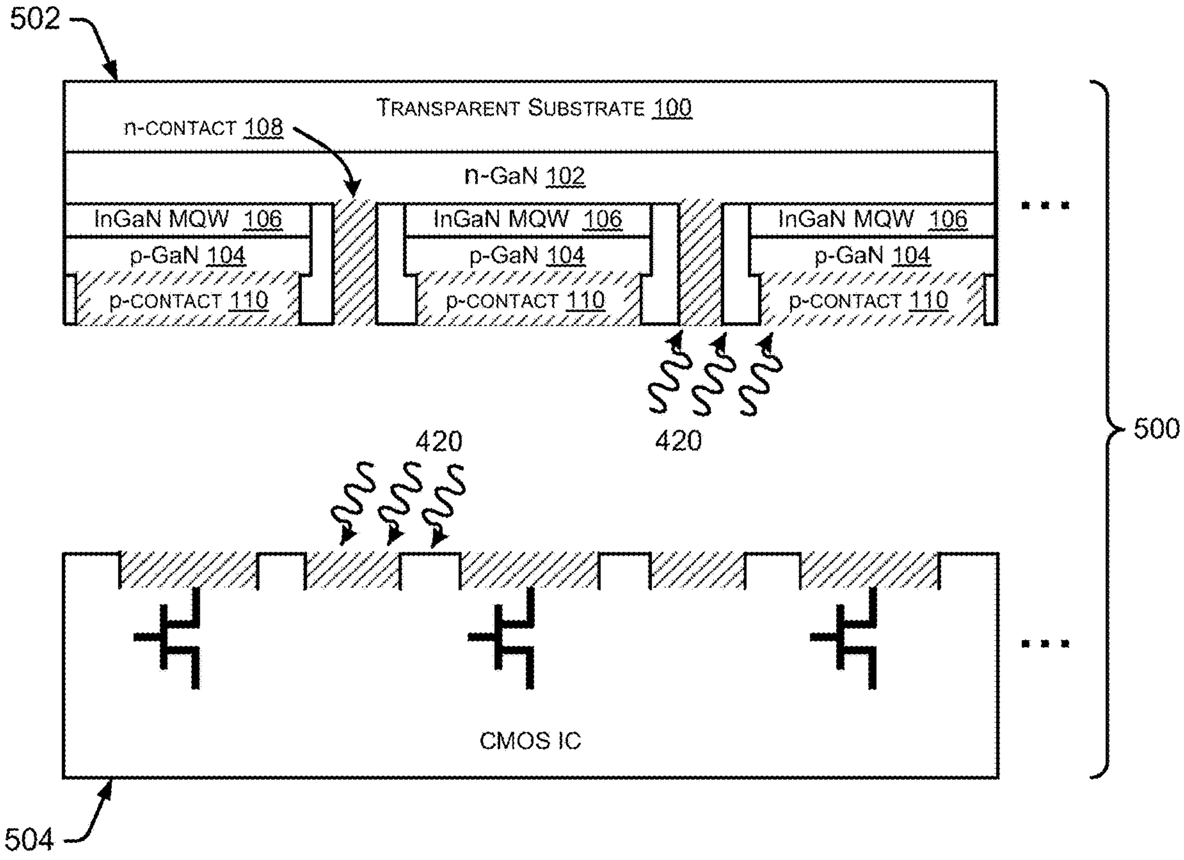

502
TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
420
420
500
CMOS IC
504

FIG. 5

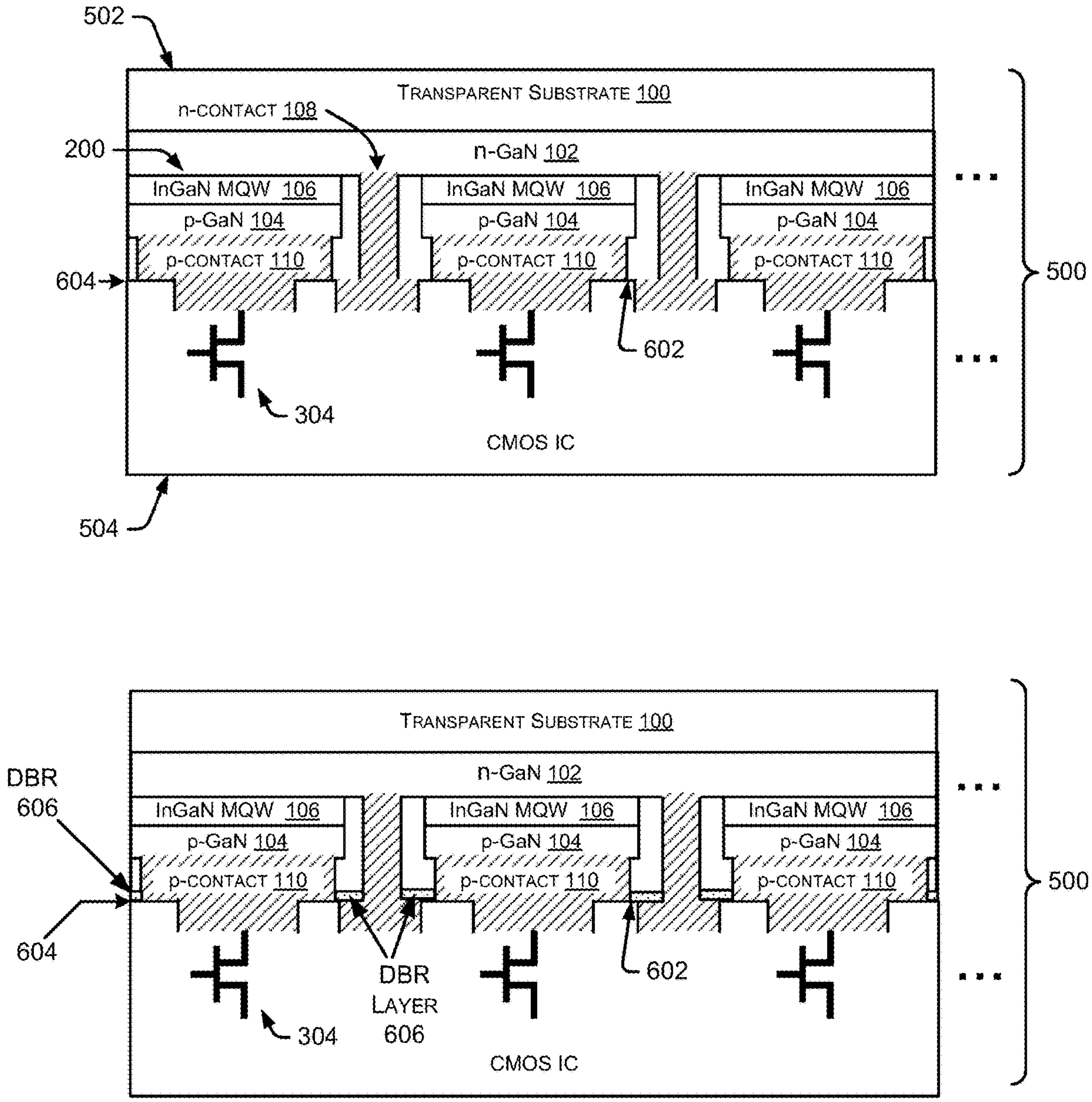

502
Transparent Substrate 100
n-contact 108
n-GaN 102
200
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-contact 110
p-contact 110
p-contact 110
604
602
304
CMOS IC
504
500
Transparent Substrate 100
n-GaN 102
DBR 606
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-contact 110
p-contact 110
p-contact 110
604
DBR Layer 606
602
304
CMOS IC
500

*Fig. 6*

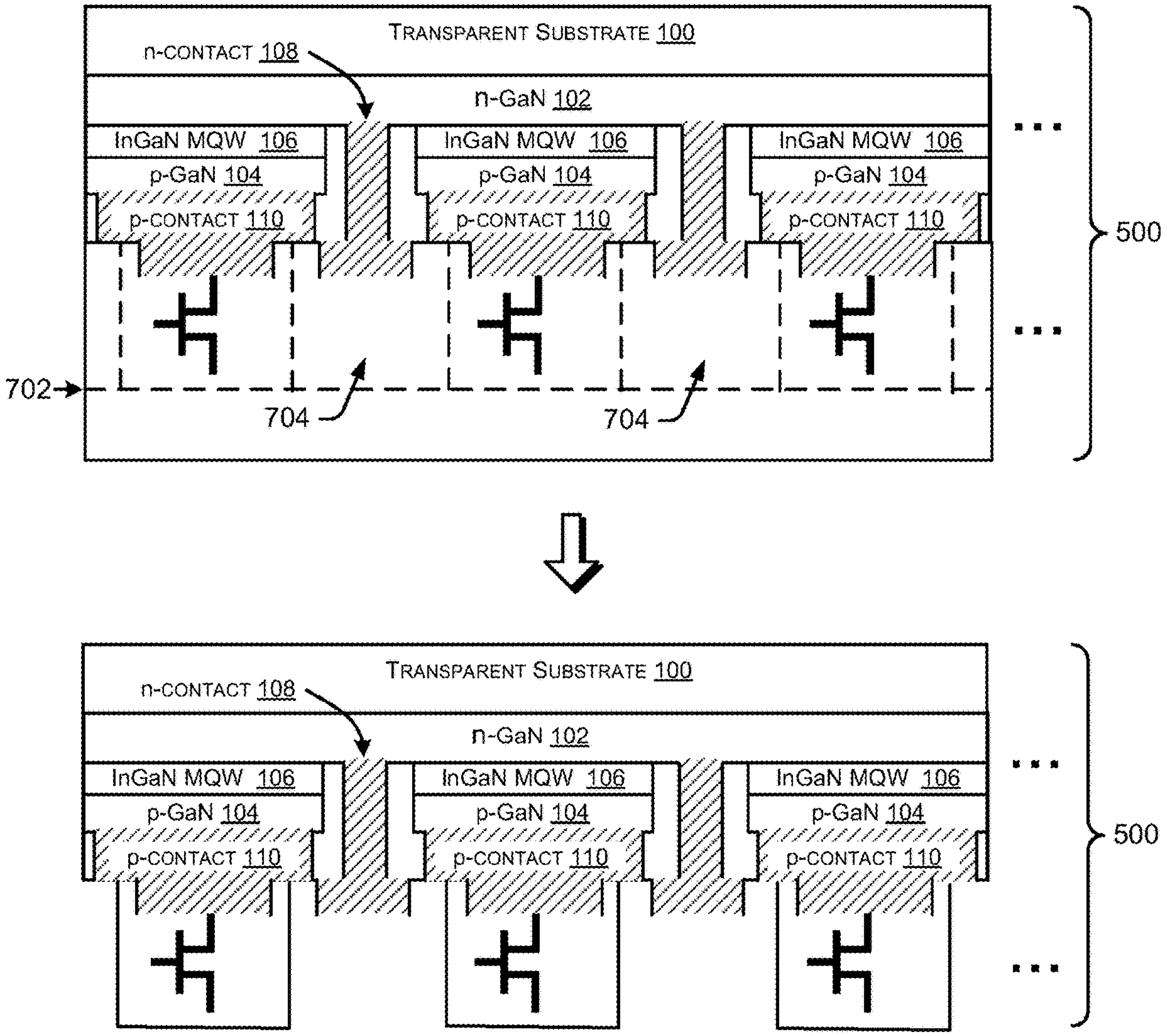

TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
500
702
704
704
TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
500

*FIG. 7*

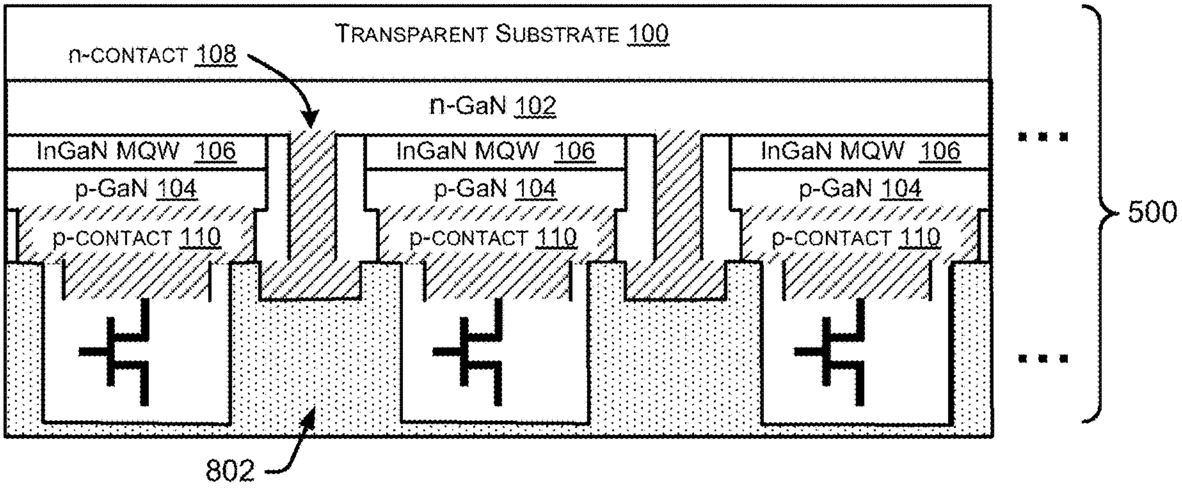

TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
500
802
...
...

FIG. 8

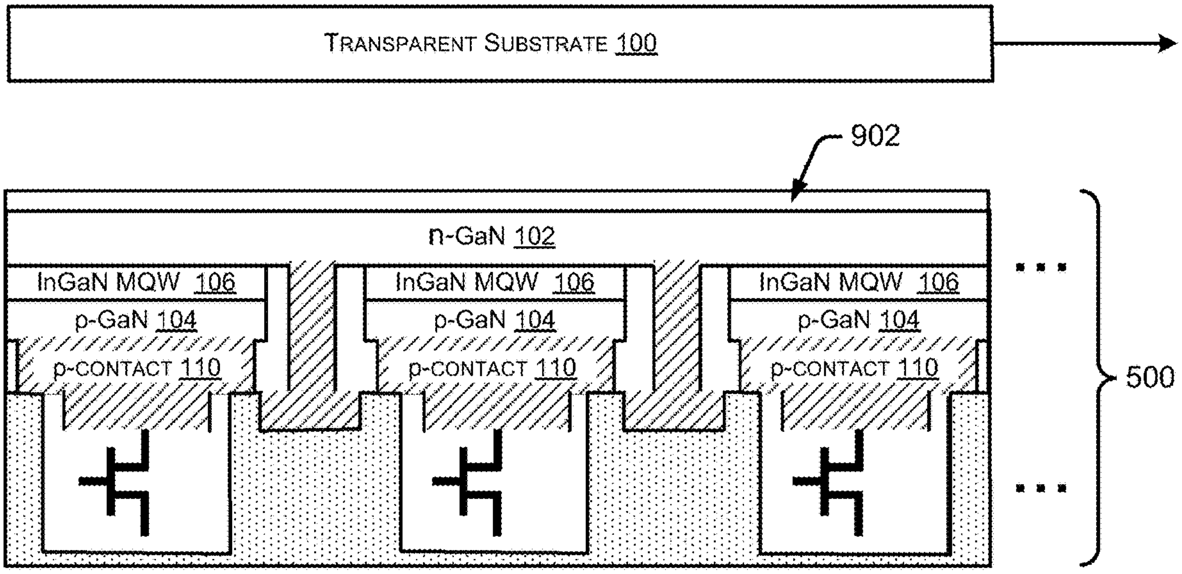

TRANSPARENT SUBSTRATE 100
902
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
500

FIG. 9

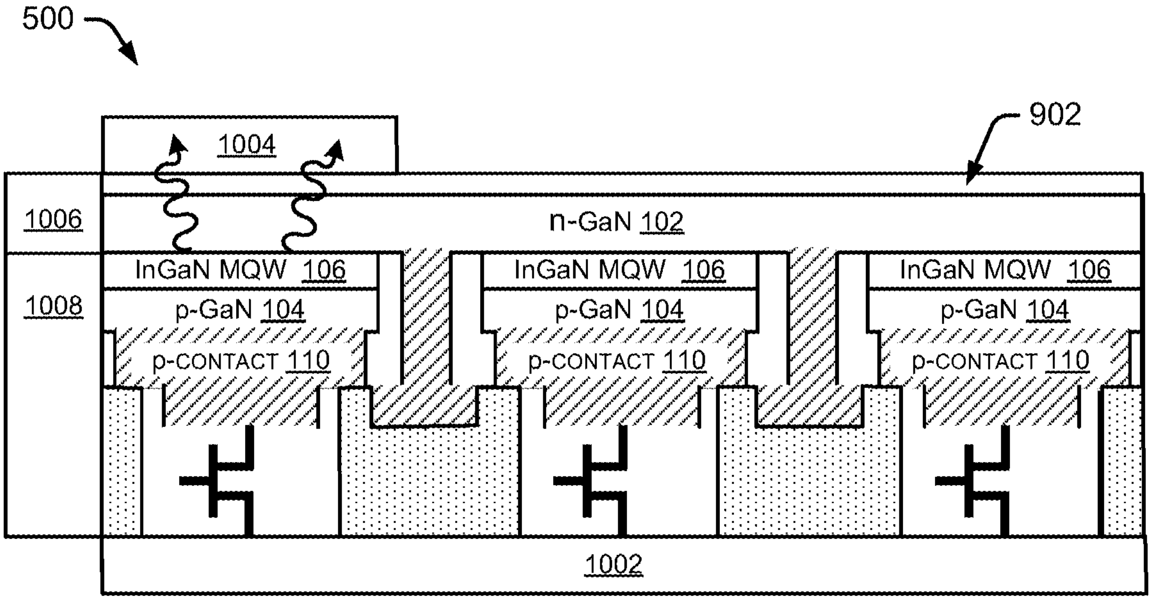

500
902
1004
1006
n-GaN 102
1008
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
1002

FIG. 10

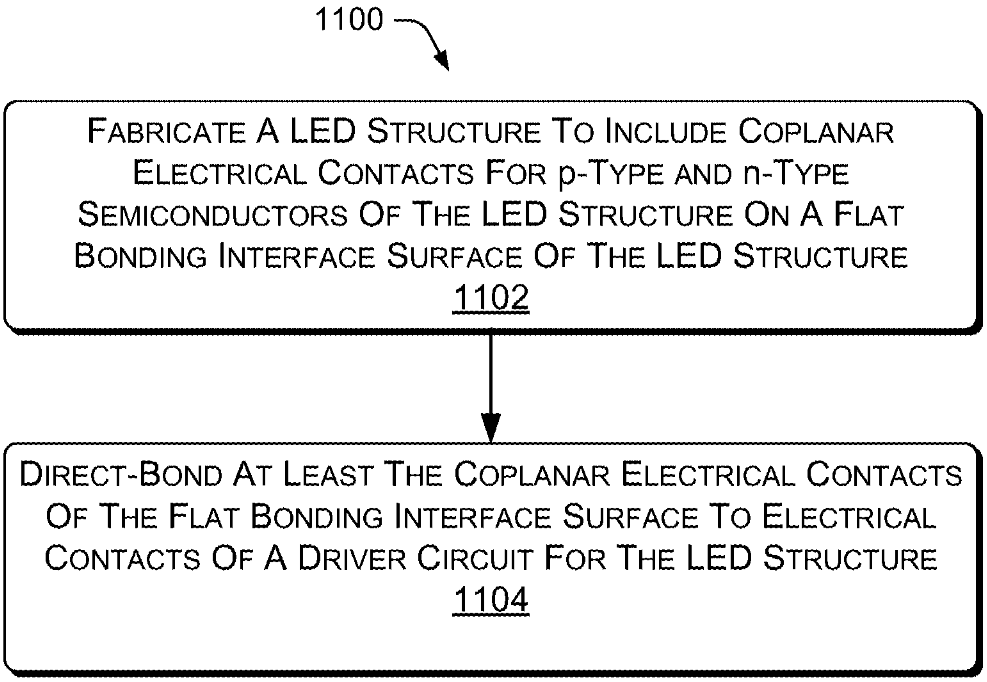

1100
Fabricate A LED Structure To Include Coplanar Electrical Contacts For p-Type and n-Type Semiconductors Of The LED Structure On A Flat Bonding Interface Surface Of The LED Structure
1102
Direct-Bond At Least The Coplanar Electrical Contacts Of The Flat Bonding Interface Surface To Electrical Contacts Of A Driver Circuit For The LED Structure
1104

*FIG. 11*

# DIRECT-BONDED OPTOELECTRONIC DEVICES

## REFERENCE TO PRIORITY APPLICATIONS

**[0001]** This application is a continuation of U.S. application Ser. No. 18/206,512, filed Jun. 6, 2023, which is a continuation of U.S. application Ser. No. 17/327,169, filed May 21, 2021 (now U.S. Pat. No. 11,715,730), which is a continuation of U.S. application Ser. No. 16/840,245, filed Apr. 3, 2020 (now U.S. Pat. No. 11,329,034), which is a continuation of U.S. application Ser. No. 15/919,570, filed Mar. 13, 2018 (now U.S. Pat. No. 10,629,577), which claims priority to U.S. Provisional Patent Application No. 62/472,363, filed Mar. 16, 2017, the disclosures of which are hereby incorporated by reference herein in their entireties for all purposes.

## BACKGROUND

**[0002]** MicroLEDs, also known as micro-LEDs, μLEDs, and “mLEDs” as used herein, are gaining significant attraction as an emerging flat panel display technology. But as of yet, mLED displays have not been mass-produced or commercialized widely. The mLED displays are arrays of microscopic LEDs forming individual pixel elements. Compared to the widespread LCD technology, mLED displays provide greater contrast and faster response times, while using less energy.

**[0003]** Along with organic light-emitting diodes (OLEDs), in which a film of organic compound is stimulated to emit electroluminescence, mLEDs can be used in small low-energy devices such as smart phones and smart watches, where battery power is at a premium.

**[0004]** Both mLEDs and OLEDs require less energy than conventional LCD systems. Unlike OLEDs, however, the mLED technology utilizes conventional III-V inorganic semiconductor materials (GaN, InGaN, etc.) for use as self-emissive LEDs for lighting and display, which can offer higher overall brightness (e.g., 30× over OLEDs) and higher contrast than OLED products, with higher efficiency in lux per watt (lux/W) light output. The mLED technology can also provide a longer working life for the product that is hosting the mLED technology. Versions of this mLED array technology may be ideal for automotive, virtual reality, and augmented reality displays.

## SUMMARY

**[0005]** Direct-bonded LED arrays and applications are provided. An example process fabricates a LED structure that includes coplanar electrical contacts for p-type and n-type semiconductors of the LED structure on a flat bonding interface surface of the LED structure. The coplanar electrical contacts of the flat bonding interface surface are direct-bonded to electrical contacts of a driver circuit for the LED structure. In a wafer-level process, micro-LED structures are fabricated on a first wafer, including coplanar electrical contacts for p-type and n-type semiconductors of the LED structures on the flat bonding interface surfaces of the wafer. At least the coplanar electrical contacts of the flat bonding interface are direct-bonded to electrical contacts of CMOS driver circuits on a second wafer. The process provides a transparent and flexible micro-LED array display, with each micro-LED structure having an illumination area approximately the size of a pixel or a smallest controllable element of an image represented on a high-resolution video display.

**[0006]** This summary is not intended to identify key or essential features of the claimed subject matter, nor is it intended to be used as an aid in limiting the scope of the claimed subject matter.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0007]** Certain embodiments of the disclosure will hereafter be described with reference to the accompanying drawings, wherein like reference numerals denote like elements. It should be understood, however, that the accompanying figures illustrate the various implementations described herein and are not meant to limit the scope of various technologies described herein.

**[0008]** FIG. **1** is a diagram of an example conventional nitride light emitting diode (LED).

**[0009]** FIG. **2** is a diagram of an example LED structure suitable for direct-bonding of electrical contacts enabling wafer level, chip array-level, and individual chip-level construction of direct-bonded micro-LED structures.

**[0010]** FIG. **3** is a diagram of the example LED structure of FIG. **2**, in a direct-bonding operation with driver circuitry.

**[0011]** FIG. **4** is a diagram of an example process of fabricating the LED structure of FIG. **2**.

**[0012]** FIG. **5** is a diagram of a first stage of fabricating an example LED array display.

**[0013]** FIG. **6** is a diagram of a second stage of fabricating the example LED array display.

**[0014]** FIG. **7** is a diagram of a third stage of fabricating the example LED array display.

**[0015]** FIG. **8** is a diagram of a fourth stage of fabricating the example LED array display.

**[0016]** FIG. **9** is a diagram of a fifth stage of fabricating the example LED array display.

**[0017]** FIG. **10** is a diagram of a completed LED array display and optional components.

**[0018]** FIG. **11** is a block diagram of an example process of making a direct-bonded LED structure.

## DESCRIPTION

**[0019]** This disclosure describes example direct-bonded light emitting diode (LED) arrays and applications. New processes for forming actively driven mLED (microLED) structures and display cells are described, including example processes of array-bonding III-V compound semiconductor mLEDs to silicon driver chips to form actively driven mLED display cells. Some of these processes may be used to mass-produce mLED array displays.

### Example Processes and Structures

**[0020]** FIG. **1** shows an example of a conventional epilayer structure **50** of a light emitting diode (LED) over a sapphire substrate **100**, illustrating and comparing some LED components used in example structures and processes described herein. The example conventional LED structure **50** may produce green or blue light, for example. Semiconductor materials are layered on a carrier, such as a sapphire substrate **100**. The large mismatches in lattice constants and thermal expansion coefficients between GaN and sapphire **100** would cause high crystalline defect densities in the GaN films, which leads to degradation of device performance;

hence a lattice and CTE matched buffer material **101** is deposited on sapphire **100** to grow GaN. Optoelectronic devices like the conventional LED structure **50** utilize semiconductor doping, for example, a small amount of silicon or germanium is added to gallium nitride (GaN) to make the GaN a conductor for electrons (n-type) n-GaN **102**, and a small amount of magnesium is added to the gallium nitride (GaN) to make the GaN into a conductor for holes (electron holes) (p-type) p-GaN **104**. Between the layer of n-GaN **102** and the layer of p-GaN **104** is sandwiched an ultrathin layer of a light-producing quantum well or multiple quantum well (MQW) material, that has a smaller band gap (and slightly less conductivity) than either the n-GaN **102** and the p-GaN **104**, such as indium gallium nitride InGaN, a semiconductor material made of a mix of gallium nitride (GaN) and indium nitride (InN). InGaN is a ternary group III/group V direct band gap semiconductor. The example InGaN/GaN or InGaN MQW layer **106** provides quantum confinement, or discrete energy subbands, in which the carriers can have only discrete energy values, providing better performance in optical devices. Conventional LED structures **50** may have many variations in the number or layers used, and the materials used for each layer. In FIG. **1**, the layers, and especially the MQW layer **106**, are not shown to relative scale.

**[0021]** The example conventional LED structure **50** is characterized by an n contact **108** and a p contact **110** at different vertical levels on different surfaces of the conventional LED structure **50**. The difference in vertical heights between p contact **110** and n contact **108** is conventionally compensated for by wire bond or solder connections. Or, an example conventional structure **50** may have an n contact **108** that is not exposed (not shown).

**[0022]** FIGS. **2**-**3** show an example LED structure **200** and process overview, for direct-bonding LED components containing III-V semiconductor elements to driver circuitry, for making mLED array displays. The example LED structure **200** provides an ultra-flat bonding interface **202**, made flat by chemical-mechanical polishing (CMP) for example, with both n contact **108** and p contact **110** surrounded by an insulator **204**, such as a silicon oxide, and exposed on the ultra-flat bonding interface **202** with respective coplanar conductive footprints **206** & **208** on the ultra-flat bonding interface **202**.

**[0023]** The n contact **108** and p contact **110** may be made of a metal, or combination of alloyed metals, or laminated metals that enhance direct bonding. Besides metal composition, the ultra-flat bonding interface **202** itself also facilitates direct bonding between the n and p contacts **108** & **110** and respective conductive surfaces being bonded to. The ultra-flat bonding interface **202** fabricated by damascene methods, for example, is also ultra-clean, and flat within a few tens of nanometers, such as less than ¼ the wavelength of an illumination source of monochromatic green light at the 546.1 nm or helium-neon red laser light at 632.8 nm. In some embodiments the roughness of the flat polished surface **202** is less than 5% of the wavelength of an illumination source and preferably less than 10 nm.

**[0024]** FIG. **3** shows an example direct-bonding process **300** between the example LED structure **200** of FIG. **2**, and a driver circuit **302** on a chip **304**, to form LED circuitry, such as thin-film transistor (TFT) drivers. The example direct-bonding process **300** can be performed at the level of individual chips, or at a chip array level, or at wafer level. For subsequent lift-off and thinning, wafer level direct-bonding may be the best approach.

**[0025]** In an implementation, the mLED ultra-flat bonding interface **202** can be bonded to the respective ultra-flat bonding interface **306** of a silicon-based driver integrated circuit (IC) **304**, for example. The ultra-flat bonding interface **306** may have a contacting surface that is topped with a flat silicon oxide layer and copper (Cu) pads to facilitate direct-bonding, for example direct-bonding via a ZiBond® brand process or a DBI® brand process, to form LED circuitry (Xperi Corporation, San Jose, CA). In an implementation, the sapphire substrate **100** may then be laser-lifted off. If desirable, both top and bottom sides can be thinned further to make the entire stack flexible.

**[0026]** FIG. **4** shows stages of example structure fabrication, illustrating an example process flow for making an LED structure **200** suitable for direct-bonding with a silicon driver ICs **304**, for example.

**[0027]** In a first stage **400** of the example process flow, an example wafer, such as a sapphire substrate **100**, is built up with beginning epitaxial layers of n-GaN **102**, InGaN MQW **106**, and p-GaN **104**.

**[0028]** In a second stage **402** of the example process flow, the top epitaxial layers are patterned and etched to expose the n-GaN layer **102** at specific locations **404**. Although the single exposed location **404** is shown at the edge at the die, there may be more than one location. For example, one or more through-vias may expose the n-GaN layer **102**. The patterning resist can be left on.

**[0029]** In a third stage **406** of the example process flow, an insulator or dielectric, such as a silicon oxide layer **204** is deposited to cover both the exposed p-GaN **104** and the exposed n-GaN **102**, at least at the location of the contacting pads.

**[0030]** In a fourth stage **408** of the example process flow, the silicon oxide layer **204** is patterned and etched over the p-GaN **104** and n-GaN **102** layers to make cavities **410** through the silicon oxide **204** for conductive metals to become the electrodes of the LED structure **200**. In an implementation, the total thickness of the p-GaN **104** layer and the MQW **106** layer is approximately 2 μm, making the structure at this stage suitable for one-step etching and metallization (MQW layer **106** not shown to scale). One or more of such cavities **410** can be formed to form one or more electrodes contacting the n-GaN **102** layer and the p-GaN **104** layer.

**[0031]** In an alternative implementation, the example process deposits a flat silicon oxide layer **204** as in the third stage **406** above, then bonds this oxide surface directly with the driving chip(s) **304** using a ZiBond® brand direct-bonding process, or other direct bonding technique. Then, through-silicon-vias (TSVs) are drilled to create the electrical connectivity from the n contact **108** and the p contact **110** to the driver chip **304**.

**[0032]** In a fifth stage **412** of the example process flow, the cavities **410** can be metalized with a conductive material **414**. In an implementation, barrier and seed layer coatings **416** may be applied and formed, then cavities filled with the conductor **414**, followed by annealing, and chemical-mechanical planarization (CMP). In an implementation, a low melting temperature metal, such as indium, may be coated in the cavities.

**[0033]** In a sixth stage **418** of the example process, a top surface of the example LED structure **200** is plasma-activated **420** for the direct-bonding operation. Plasma-activation **420** may be optional for some types of direct-bonding techniques, while in others, the plasma-activation step **420** enhances the bond strength between two metal surfaces, for example, during contact bonding. Plasma-activation **420** may also be applied to the opposing surfaces to be bonded on the driver chip(s) **304**.

**[0034]** In various implementations, the example process flow depicted in FIG. **4** may include picking and transferring many small LED chips with high throughput, and direct-bonding at very fine pitch, for example at a pitch of less than 1 mm (even smaller pitch for making micro-projectors), and at a 0.05 mm spacing, and in various implementations all the way down to a 12 um pitch with 6 um bump. The pixel array optics achieve high parallelity of the LED dies **200** to the Si dies **304**. Post-processing, such as thinning and laser lift-offs, can be accomplished because the direct-bonding applied results in the flat topography and strong bonding interfaces achieved.

**[0035]** FIGS. **5-9** show an example process for creating a thin, transparent, and flexible mLED array display **500**, in which a wafer **502** with the LED structures **200** made by the process of FIG. **4** are now bonded to (for example) a CMOS driver chip wafer **504** to make the transparent and flexible array display **500**.

**[0036]** In FIG. **5**, in an implementation, after the flat and activated surface on the LED device wafer **502** is formed, the CMOS wafer **504** is planarized with CMP or other means of obtaining an ultra-flat surface, and plasma-activated **420**.

**[0037]** In FIG. **6**, the two wafers **502** & **504** are bonded. For example, the first wafer **502** with the LED structures **200** and with coplanar bonding surfaces of the n contacts **108** and p contacts **110**, and the second wafer **504** with CMOS driver chips **304**, are brought together for direct-bonding between metallic conductors and in an implementation, between nonmetallic dielectric surfaces **602** also. Exposed silicon oxide of the first wafer **502** in contact with exposed silicon oxide of the second wafer **504** bonds first through oxide bonding, as with a ZiBond® brand direct-bonding process. The metal contact pads of the respective wafers **502** & **504** form a metal-to-metal bond during higher-than-room-temperature annealing, as with a DBI® brand direct-bonding process. The bonding interface **604** may be annealed at approximately 100-200° C. to form a strong direct bond interface, such as the ZiBond® or DBI® brand direct-bond interface.

**[0038]** An optical reflective coating, such as distributed Bragg reflector (DBR) **606** (not shown to relative scale), can be deposited to increase light output of the package by choosing different types and thickness of the dielectric layers on top of wafer **502** at the interface (**606**) between the first wafer **502** and the second wafer **504**. Alternatively, the DBR **606** could also be formed on top of the second wafer **504** prior to bonding. In this orientation of a DBR **606**, light can escape from the sapphire side of the device. If DBRs **606** are formed on the first wafer **502**, then the thin dielectrics need to be deposited at the end of the second stage **402** or the third stage **406** of the process shown in FIG. **4**. The DBR **606** is a structure formed from multiple layers of alternating materials with varying refractive index, or by periodic variation of some characteristic, for example, thickness of the dielectrics, resulting in periodic variation in the effective refractive index. These thin layers of dielectric coatings may be the combination of silicon oxide, magnesium fluoride, tantalum pentoxide, zinc sulfide, and titanium dioxide, for example. A silicon oxide SiOx layer on a top surface of the compound wafer **502** can also serve as the last of the coatings which is then bonded directly with direct bonding techniques, such as a ZiBond® or a DBI® process, to wafer **504**.

**[0039]** In another embodiment, DBR may be formed at between sapphire and n-GaN. In this orientation, the light will be reflected towards CMOS wafer **504**. However, less amount of light will escape as CMOS chip would be obstructing the escape route.

**[0040]** In FIG. **7**, the thin-film transistor (TFT) backplane can be thinned **702**, which can be facilitated by a ZiBond® brand direct-bonding process. Then the non-transistor parts **704** of the thinned backplane can also be etched away. In this embodiment, the location of one or more n-contacts **108** and p-contacts **110** can be designed such that they may be exposed from the backside after etching of the backplane; and hence can be contacted for power delivery from the back side.

**[0041]** In FIG. **8**, the thinned and etched transistor surface may be coated with a polyimide (PI) layer **802** or any other dielectric material for protection.

**[0042]** In FIG. **9**, a laser-lift-off of the sapphire substrate layer **100** may be performed, and this exposed side of the wafer **502** then coated with a flexible organic substrate **902**.

**[0043]** In another embodiment, the process to etch and backfill by the transistor backplane by PI may be skipped before a laser-lift-off of the sapphire substrate layer **100**. In this embodiment, one or more through-electrodes may be needed in the backplane for power delivery to the electrodes.

**[0044]** FIG. **10** shows operational access available on all sides of example transparent and flexible mLED array displays **500** created with direct-bonding. This versatility is due at least in part to the strong bonds possible with direct bonding, such as DBI® and ZiBond® brand bonding processes, which result in a final structure able to tolerate further processing on multiple sides of the structure **500**. For example, besides lifting off the transparent (e.g., sapphire) substrate **100** to make a flexible display **500** bonded to a flexible organic substrate **902**, post grinding may be applied and further lift-off performed to make the display thinner, more transparent, and more flexible.

**[0045]** The backside of the mLED array display **500** may be added onto with backside build-up layers **1002** for further 3D integration to attach to memory, printed circuit boards (PCBs), tactile and other sensors, and so forth.

**[0046]** One or more optical waveguides **1004** may be integrated on top of the transparent substrate **902** to transmit optical signals from the LED elements, and also lines for electrical signals may be added. In an implementation, the one or more optical waveguides **1004** are attached to the example LED array display **500** by a direct-bonding technique.

**[0047]** On the sides of the example mLED array display **500**, an edge emitting configuration **1006** may be added, and/or optical waveguides on the sides, similar to the one or more optical waveguides **1004** on top. In this embodiment, reflectors may be needed on both sides of the LED devices **200**, at layer **902**, as well as at the direct-bond (e.g., ZiBond®) interface **604**/**606**.

**[0048]** The structure of the example mLED array display **500** enables multi-junction stacking of compound semiconductors, for solar cells and solar panels, for example.

**[0049]** The sides of the example mLED array display **500** can also accommodate cooling structures **1008**.

**[0050]** After removing sapphire layer **100**, as in FIG. **8**, the surface may be roughened and indium tin oxide (ITO) added to improve the electrical conductivity of the LEDs.

**[0051]** The example steps just described and illustrated above provide direct-bonded light emitting diode (LED) arrays **500**, for example arrays of mLEDs, wherein group III-V semiconductor elements are direct-bonded to LED driver circuitry, in wafer-level processes, for example. The arrays **500**, made through a direct-bonding process, may be flexible, and possess an optically transparent surface.

**[0052]** In general, the example compound semiconductor-based LED array devices **500** are made with a flat surface composed of coplanar metal regions and dielectric regions. The coplanar metal regions are electrically connected to the active regions of the compound semiconductors of each LED element.

**[0053]** The above compound semiconductor-based LED array structures **500** may include bonds to a CMOS based device connected in a direct-bonding manner. The metal regions and the dielectric regions of the compound semiconductor-based LED array device **500** may be bonded directly to the respective metal regions and dielectric regions of the CMOS based device. Although described with respect to a wafer level process, the example process of FIGS. **5-9** can be used not only for wafer-to-wafer (W2 W) processes, but also die-to-die (D2D), or one or multiple dies-to-wafer (D2 W) processes.

**[0054]** The resulting example LED array structures **500** may also have other characteristics and features:

**[0055]** The resulting LED array structures **500** may have an absence of substrate where the group III-V-based semiconductor light-emitting devices are grown. Further, a surface of the microstructure of the group III-V semiconductor-based light-emitting devices can be advantageously roughened for improved light extraction.

**[0056]** The electrode shape for electrically connecting to the n-GaN **102** and p-GaN **104** active regions via a direct-bonding process, such as a DBI® brand direct-bonding process, can be specially designed, such as frame-traced dot arrays for the electrode or contact **108** of the n-GaN **102** region, and a dot array in a circular or square area for the electrode or contact **110** of the p-GaN **104** region.

## Example Processes

**[0057]** FIG. **11** shows an example method **1100** of making a direct-bonded LED structure. In the flow diagram, operations of the example method **1100** are shown in individual blocks.

**[0058]** At block **1102**, a LED structure is fabricated with electrical contacts to p-type and n-type semiconductor elements coplanar on a first surface comprising a flat bonding interface of the LED structure.

**[0059]** At block **1104**, the first surface is direct-bonded to a second surface comprising a flat bonding interface of a driver circuit for the LED structure.

**[0060]** The direct-bonding operation used in the example method **1100**, such as a ZiBond® or a DBI® brand direct-bonding process, may be applied in a wafer level, single chip-level, or a chip array-level process.

**[0061]** In the specification and appended claims: the terms "connect," "connection," "connected," "in connection with," and "connecting," are used to mean "in direct connection with" or "in connection with via one or more elements." The terms "couple," "coupling," "coupled," "coupled together," and "coupled with," are used to mean "directly coupled together" or "coupled together via one or more elements."

**[0062]** While the present disclosure has been disclosed with respect to a limited number of embodiments, those skilled in the art, having the benefit of this disclosure, will appreciate numerous modifications and variations possible given the description. It is intended that the appended claims cover such modifications and variations as fall within the true spirit and scope of the disclosure.

**1**. A method of forming an optoelectronic device, comprising:
- directly bonding a lower surface of a first substrate to an upper surface of a second substrate at a bonding interface, the first substrate comprising a plurality of optoelectronic devices;
- after directly bonding, thinning the second substrate from a lower side opposite the upper surface of the second substrate;
- after directly bonding, etching non-device portions of the second substrate from the lower side between device portions of the second substrate; and
- refilling spaces between the device portions with a dielectric material.

**2**. The method of claim **1**, wherein directly bonding comprises
- directly bonding a first dielectric surface of the first substrate to a second dielectric surface of the second substrate at the bonding interface; and
- directly bonding first electrical contacts of the first substrate to second electrical contacts of the second substrate at the bonding interface.

**3**. (canceled)

**4**. (canceled)

**5**. The method of claim **1**, wherein directly bonding comprises hybrid bonding.

**6**. The method of claim **1**, further comprising forming electrical connections though the dielectric material to the optoelectronic devices of the first substrate.

**7**. The method of claim **1**, wherein directly bonding comprises annealing the first and second substrate.

**8**. (canceled)

**9**. The method of claim **1**, further comprising plasma activating at least one of the lower surface of the first substrate and the upper surface of the second substrate prior to directly bonding.

**10**. The method of claim **9**, further comprising planarizing each of the lower surface of the first substrate and the upper surface of the second substrate prior to directly bonding.

**11**. The method of claim **1**, wherein the first substrate comprises a compound semiconductor substrate and the second substrate comprises a silicon substrate.

**12**. (canceled)

**13**. The method of claim **11**, wherein the optoelectronic devices comprise an array of light emitting diodes, and the device portions comprise transistors forming part of light emitting diode driver circuitry.

**14**. The method of claim **1**, further comprising integrating a plurality of optical elements over an upper surface of the first substrate opposite the lower surface of the first substrate.

**15**. The method of claim **14**, wherein optical elements comprise at least one of a beam steering element or a beam shaping element.

**16**. (canceled)

**17**. (canceled)

**18**. (canceled)

**19**. The method of claim **1**, wherein etching the non-device portions comprises exposing a portion of the first substrate.

**20**. A bonded optoelectronic device, comprising:

a first element comprising a plurality of optoelectronic devices, the first element having an upper surface and a lower surface opposite the upper surface; and

a second element comprising a plurality of transistors, the second element having an upper surface and a lower surface opposite the upper surface, the second element comprising dielectric-refilled non-transistor portions between semiconductor transistor portions;

the lower surface of the first element being directly bonded to the upper surface of the second element at a bond interface; and

a plurality of electrical connections connecting the optoelectronic devices of the first element to the plurality of transistors of the second element through the bond interface.

**21**. The device of claim **20**, wherein the plurality of electrical connections include electrodes extending from the lower surface of the second element through the dielectric-refilled non-transistor portions to the optoelectronic devices.

**22**. The device of claim **20**, wherein the lower surface of the first element and the upper surface of the second element comprise directly bonded dielectric surfaces.

**23**. The device of claim **20**, wherein the electrical connections include electrodes through the dielectric-filled non-transistor portions.

**24**. The device of claim **20**, wherein the dielectric-refilled non-transistor portions separate the semiconductor transistor portions.

**25**. A bonded optoelectronic device, comprising:

a first element comprising at least one optoelectronic device, the first element having an upper surface and a lower surface opposite the upper surface; and

a second element comprising a semiconductor active device portion, the second element having an upper surface and a lower surface opposite the upper surface, the second element comprising dielectric-refilled non-active portions adjacent the semiconductor active portion;

the lower surface of the first element being directly bonded to the upper surface of the second element at a bond interface; and

a plurality of electrical connections connecting the optoelectronic devices of the first element to the active device portions of the second element through the bond interface.

**26**. The device of claim **25**, wherein the plurality of electrical connections include electrodes extending from the lower surface of the second element through the dielectric-refilled non-active portions to the optoelectronic devices.

**27**. The device of claim **25**, wherein the at least one optoelectronic device comprises a light emitting diode.

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