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(54) **SEMICONDUCTOR DEVICE AND A DATA STORAGE SYSTEM INCLUDING THE SAME**


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| ***H01L 27/11573*** | (2006.01) |

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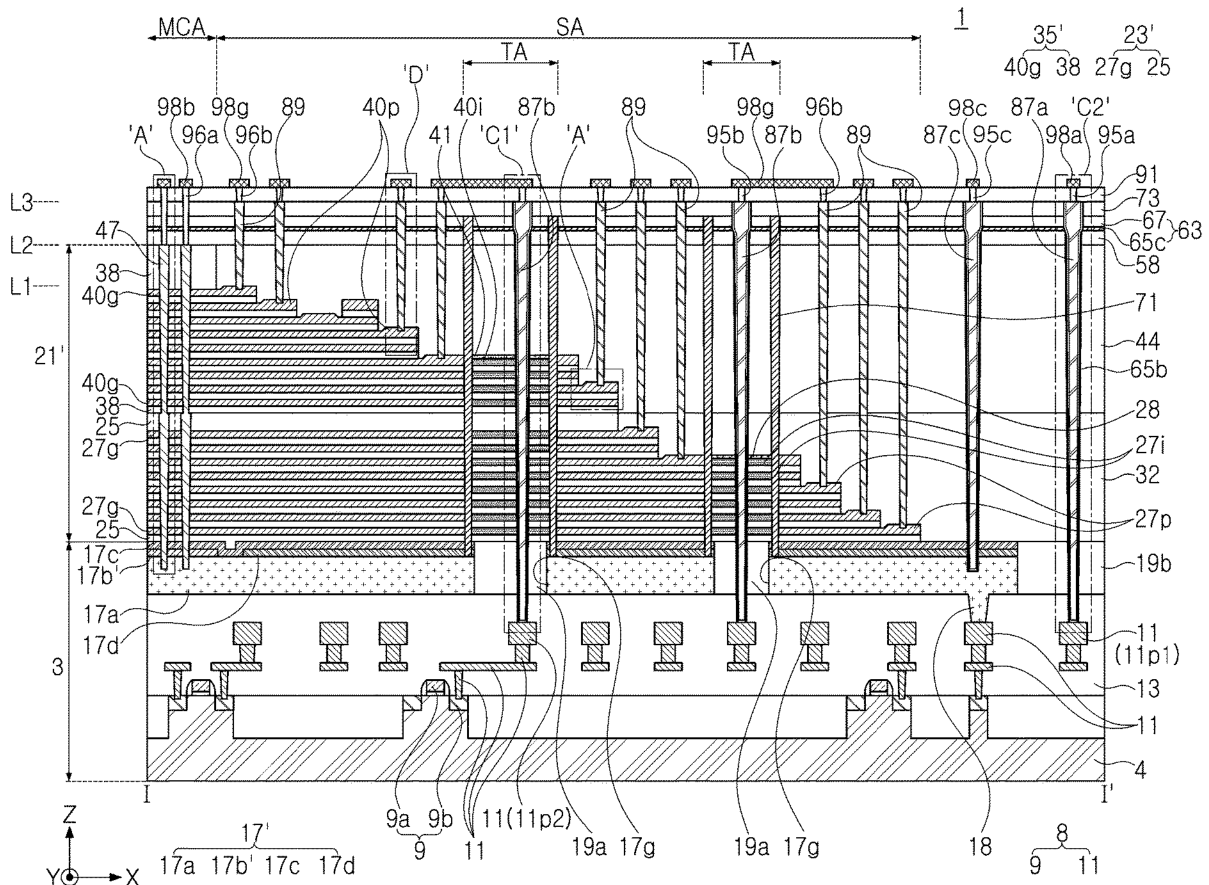
(57) **ABSTRACT**


A semiconductor device includes a structure including a stack structure including a first stack structure and a second stack structure on the first stack structure; a memory vertical structure penetrating the structure; a support vertical structure including a portion penetrating the structure and including an air gap; and a peripheral contact plug, wherein the first and second stack structures includes interlayer insulating layers and gate layers alternately stacked, a side of the memory vertical structure includes a slope changing portion, the peripheral contact plug includes an upper region disposed on a level higher than an upper surface of an uppermost gate layer, the upper region of the peripheral contact plug includes a first region, a second region and a connection region between the first and second regions, and the connection region has a slope different from a slope of at least one of the first and second regions.

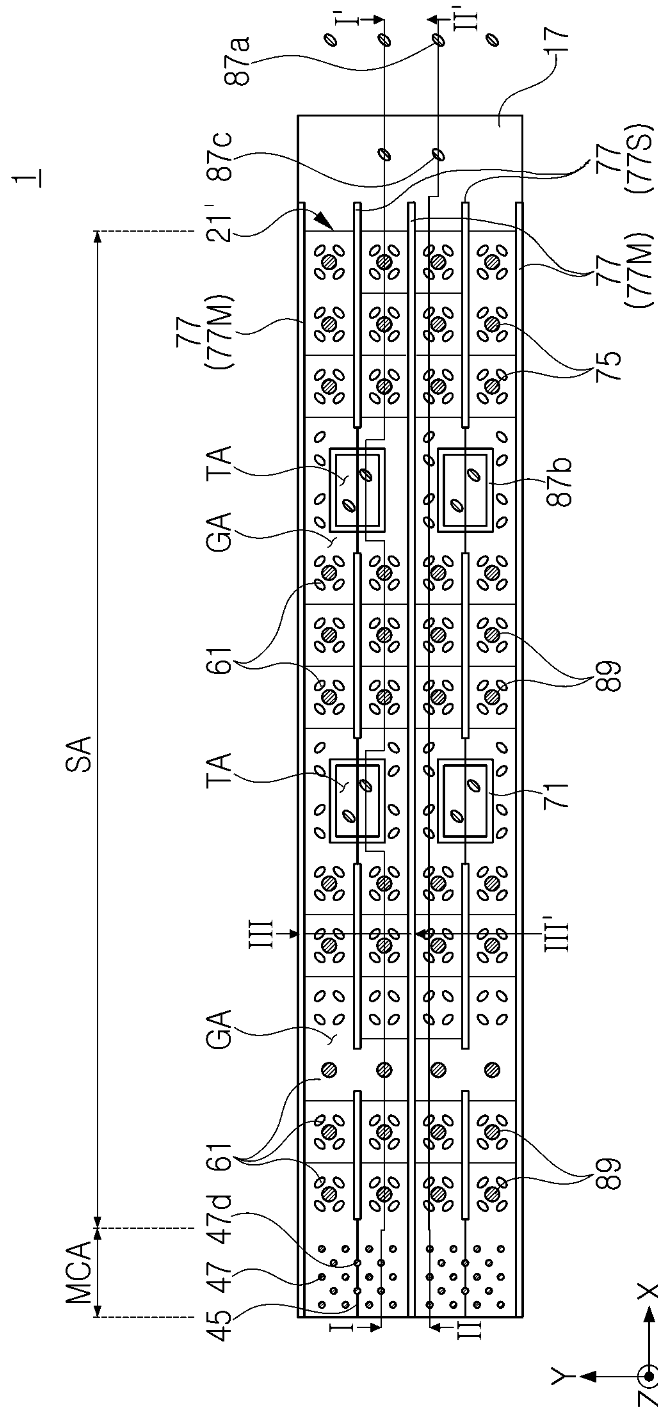



FIG. 1

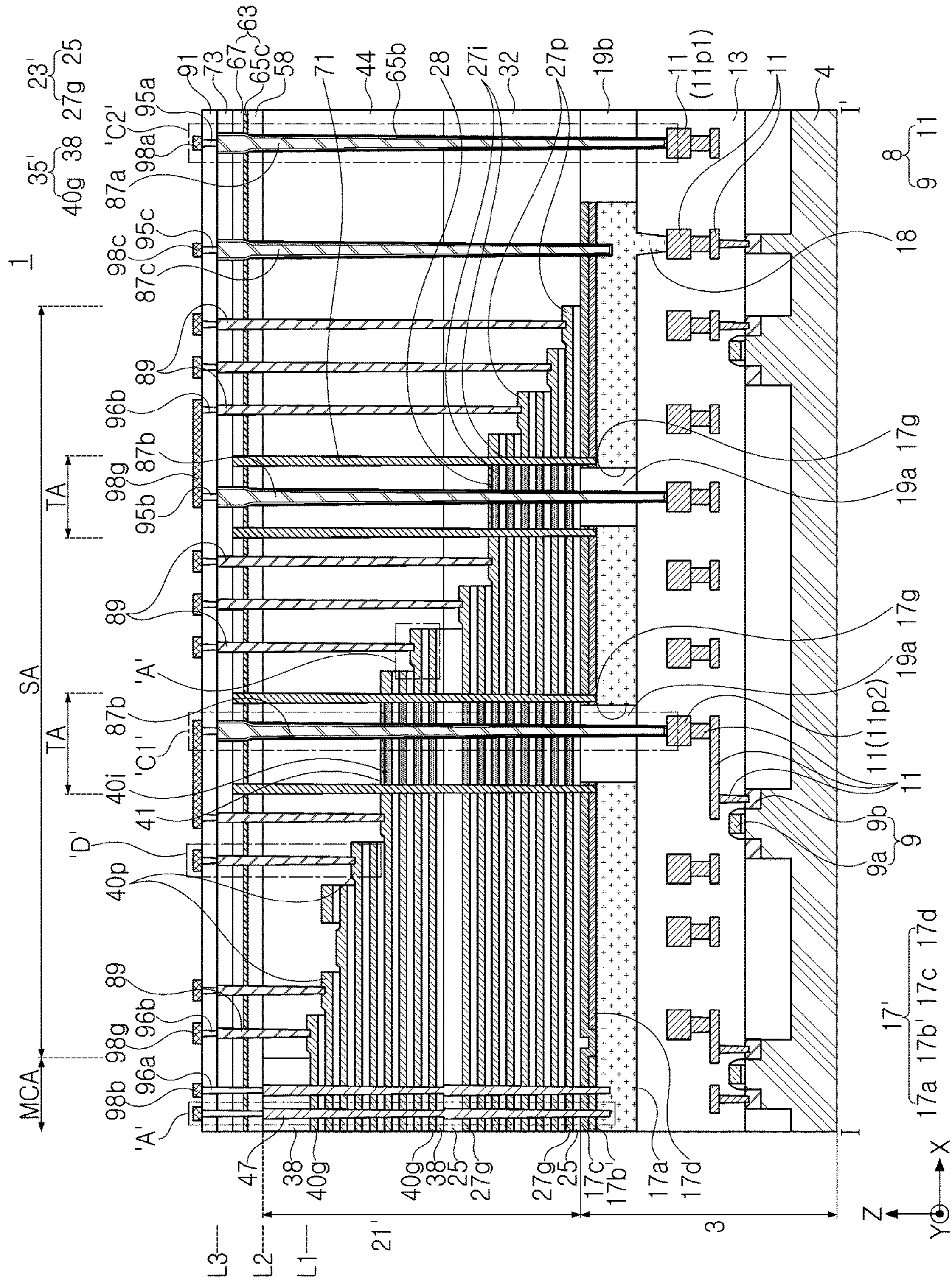


FIG. 2A

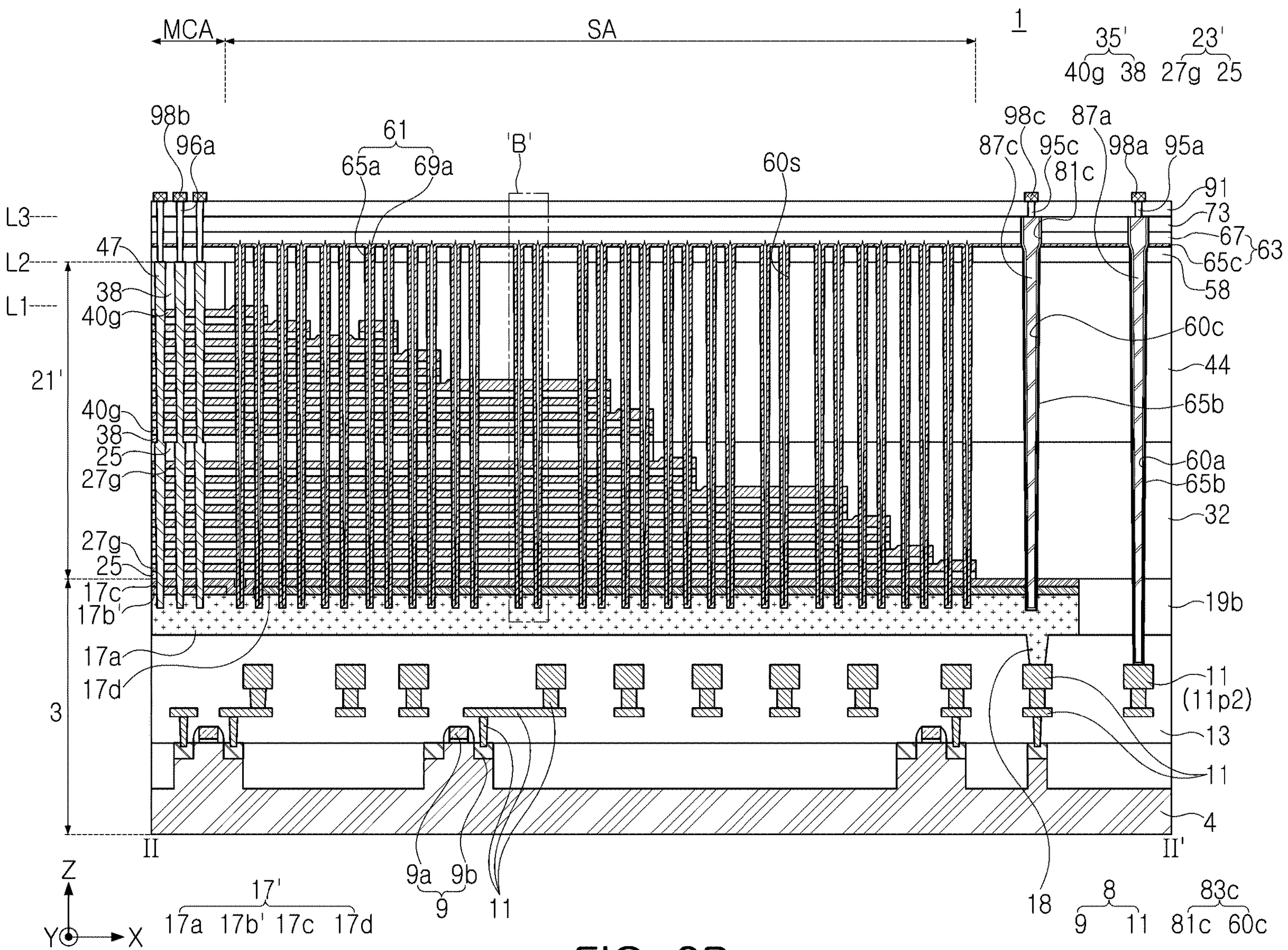



FIG. 2B

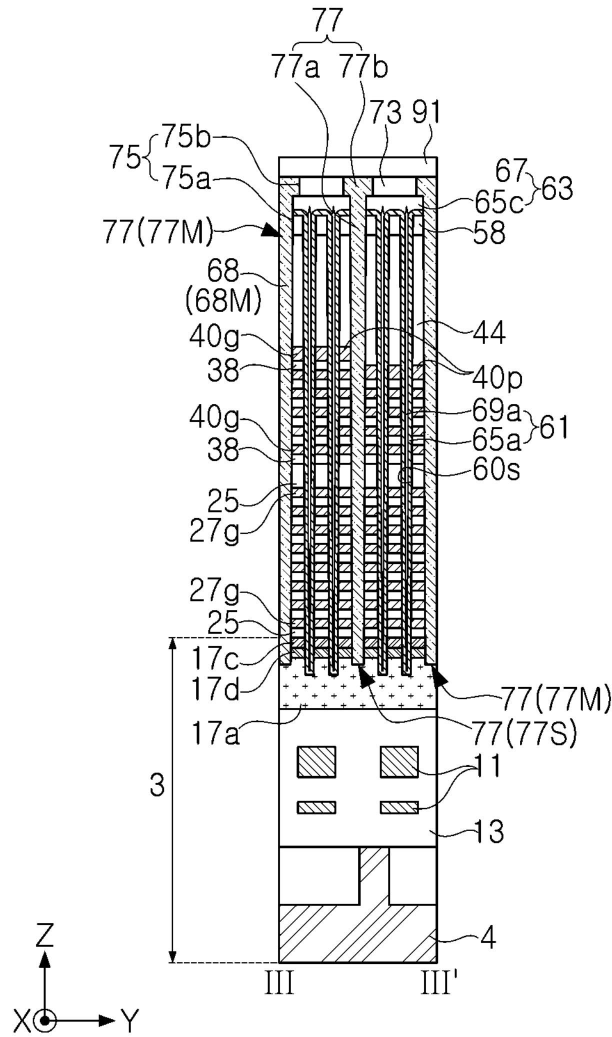



FIG. 2C

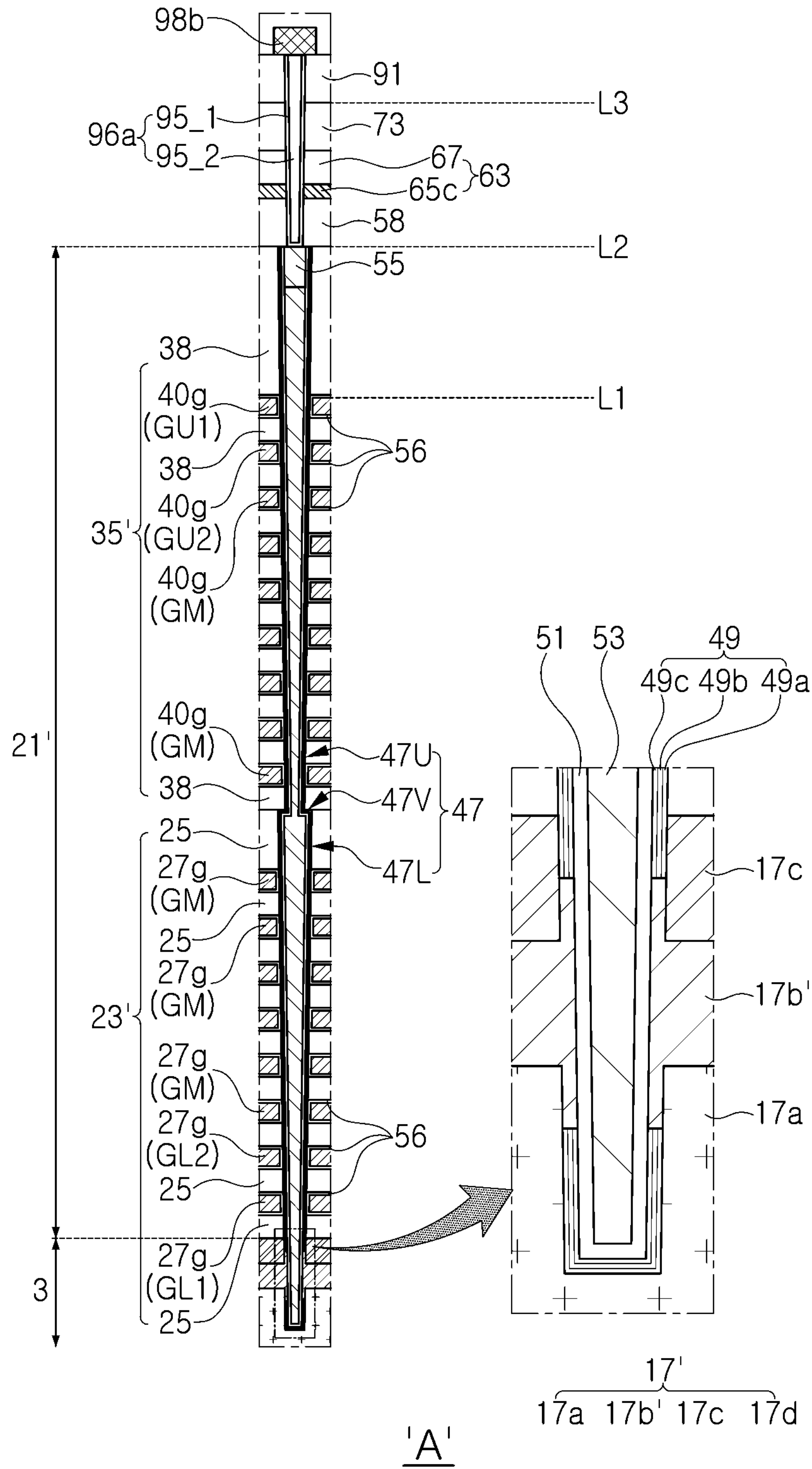



FIG. 3A

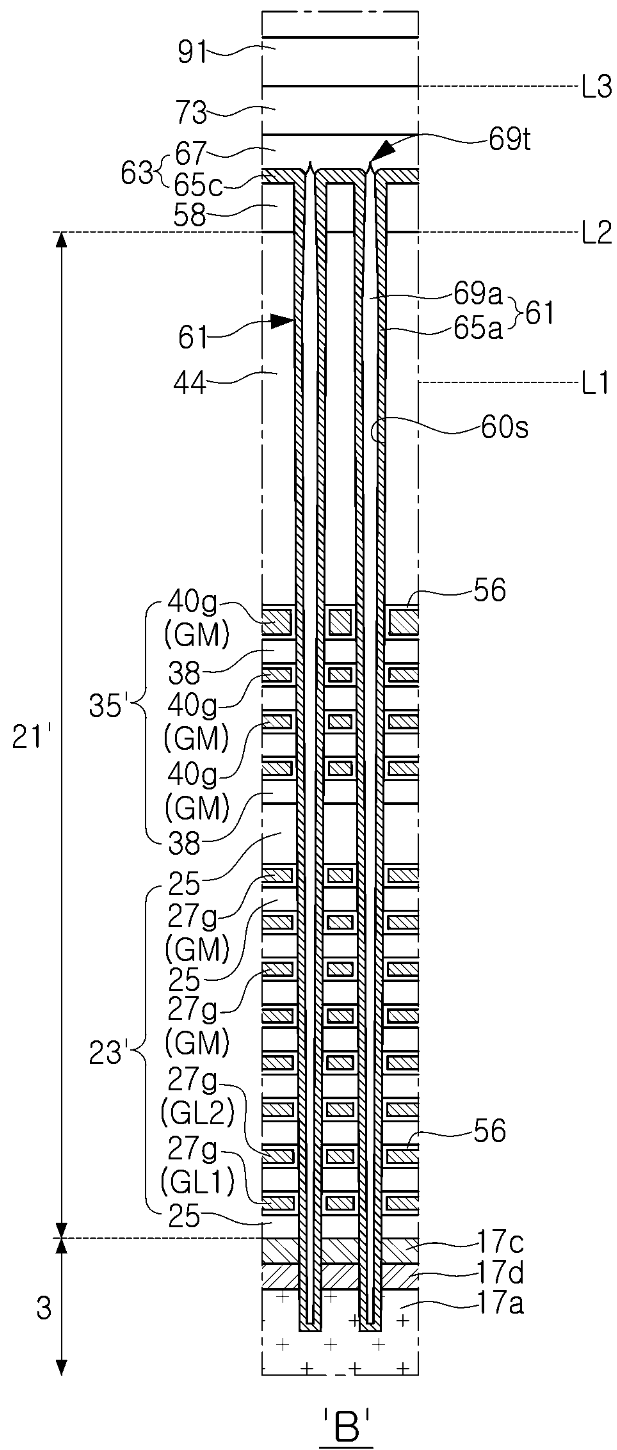



FIG. 3B

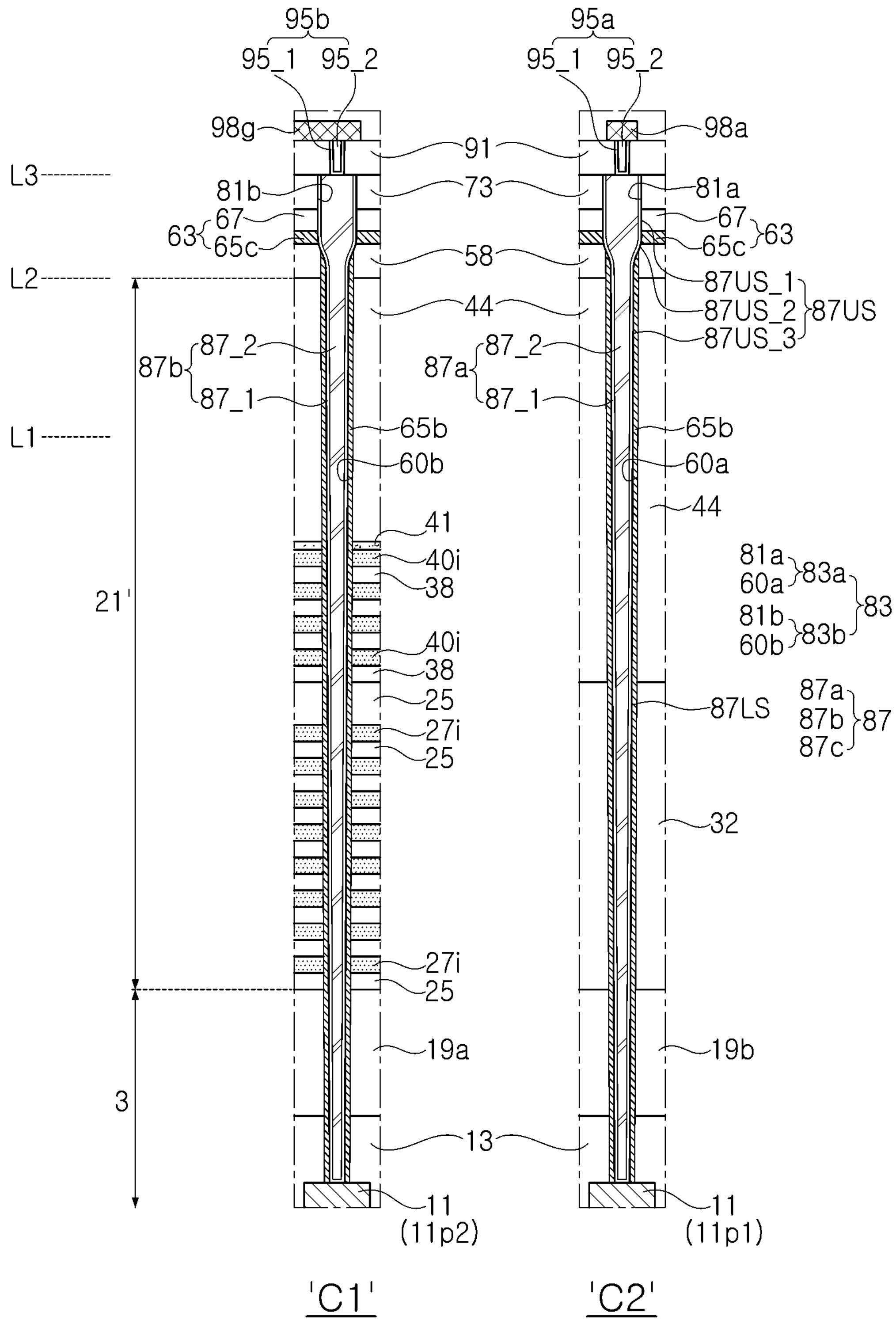



FIG. 3C

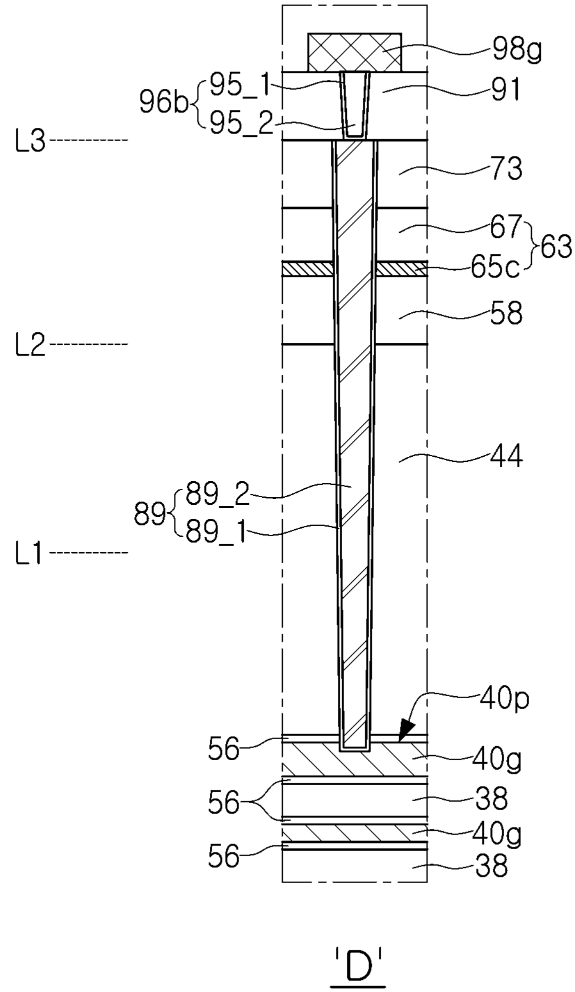



FIG. 3D

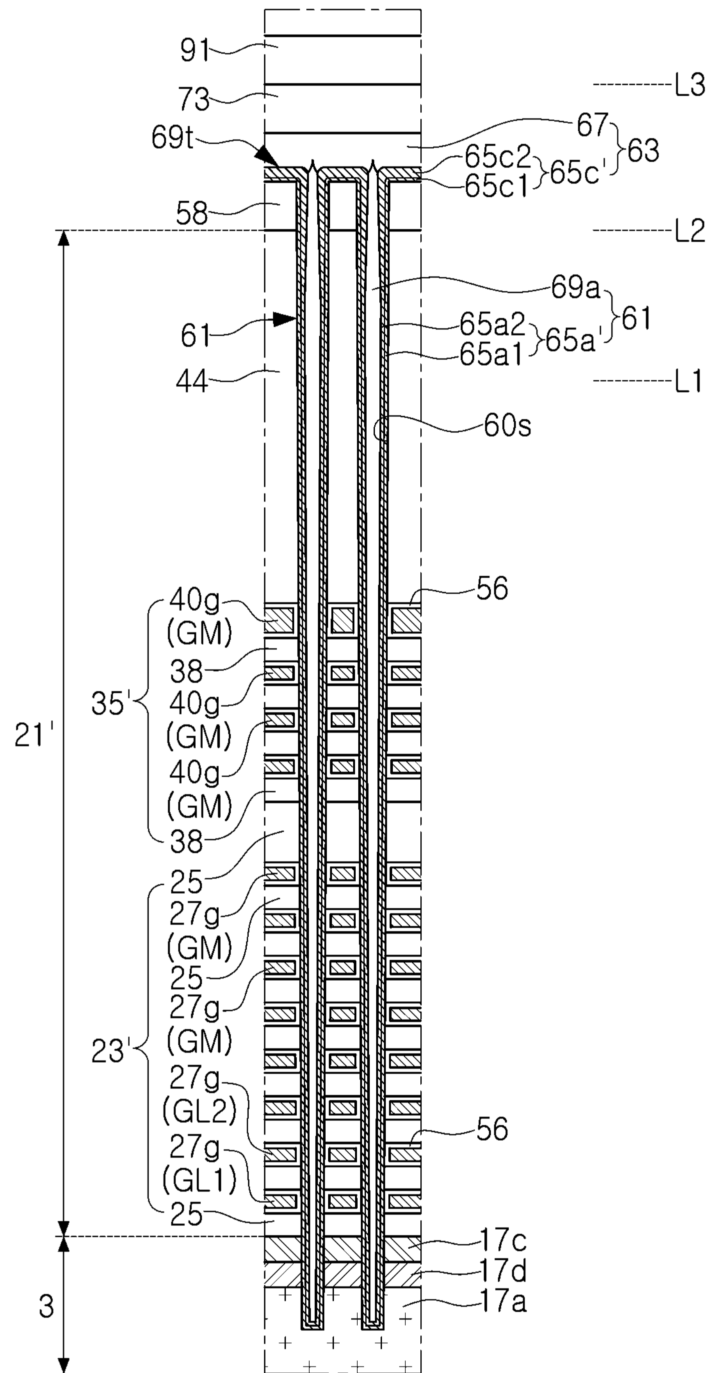



FIG. 4A

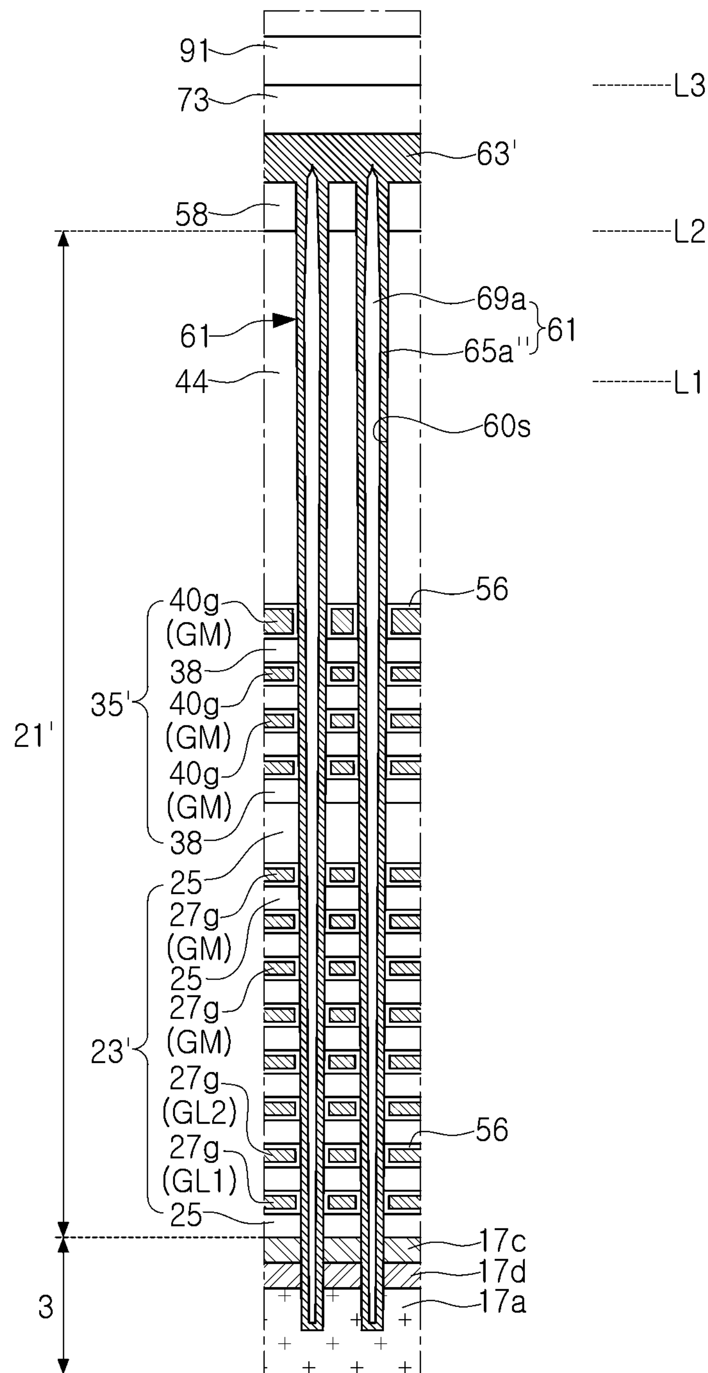



FIG. 4B

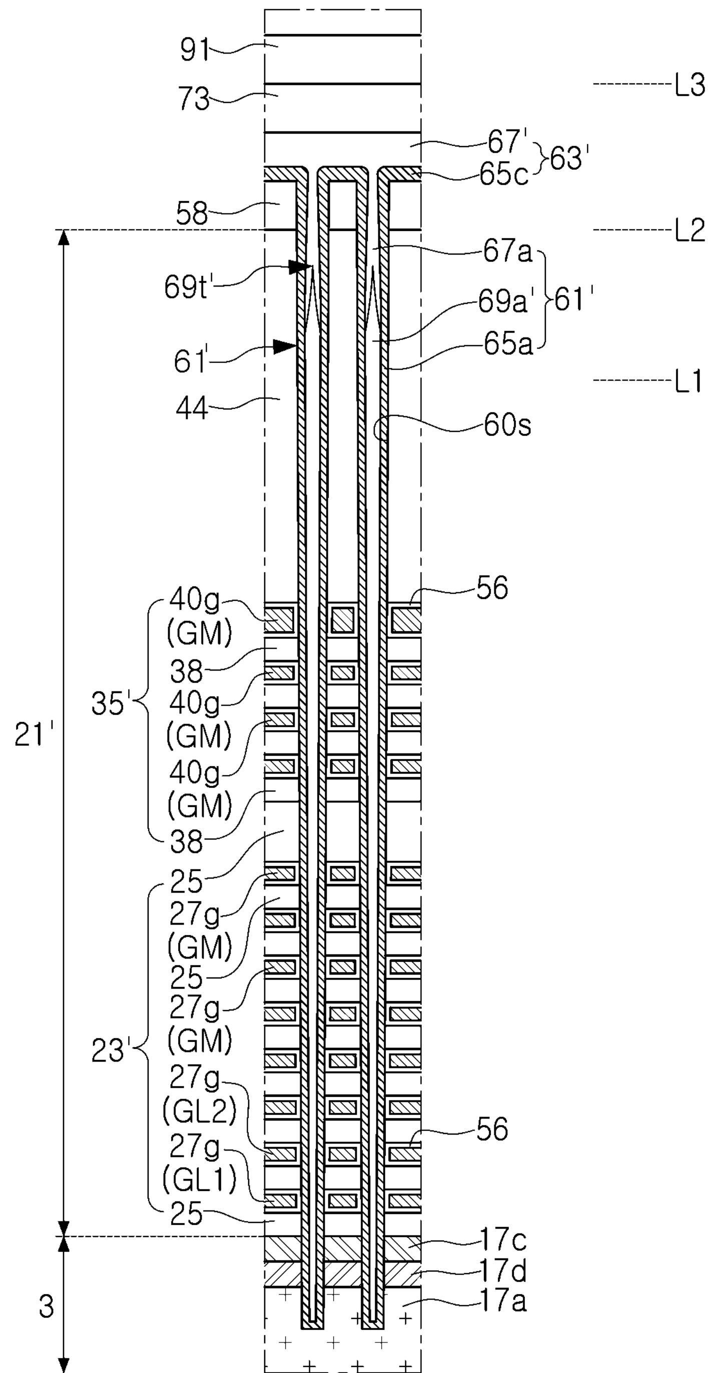



FIG. 5A

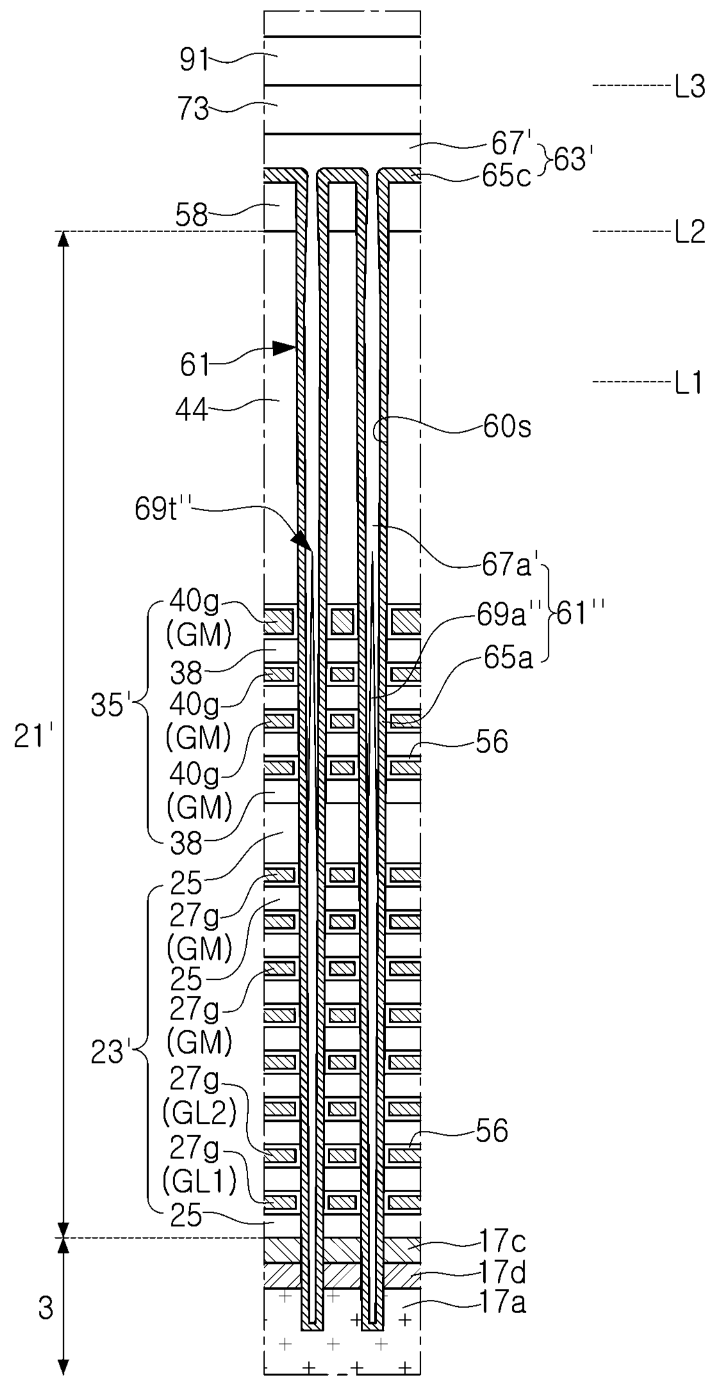



FIG. 5B

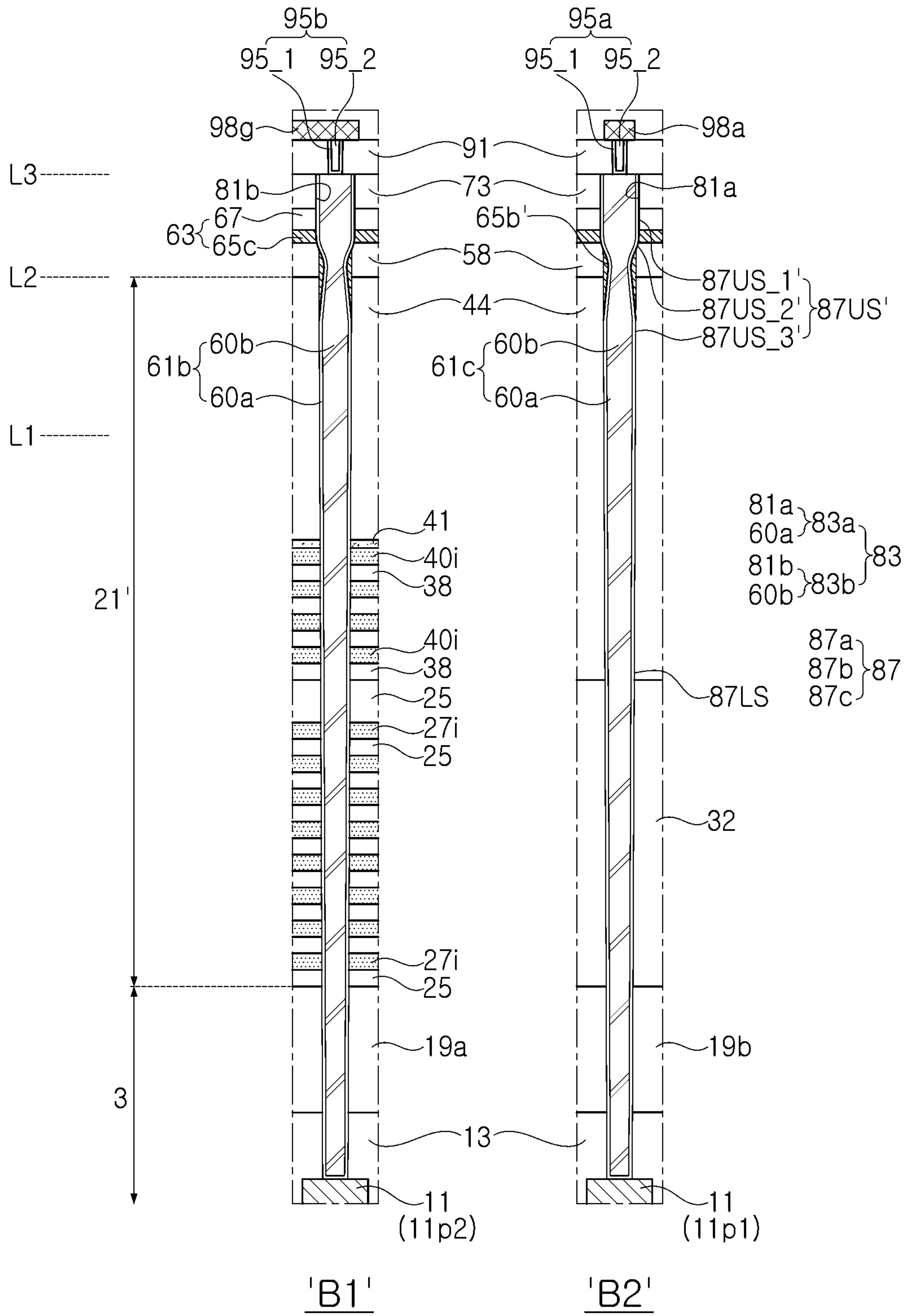



FIG. 6A

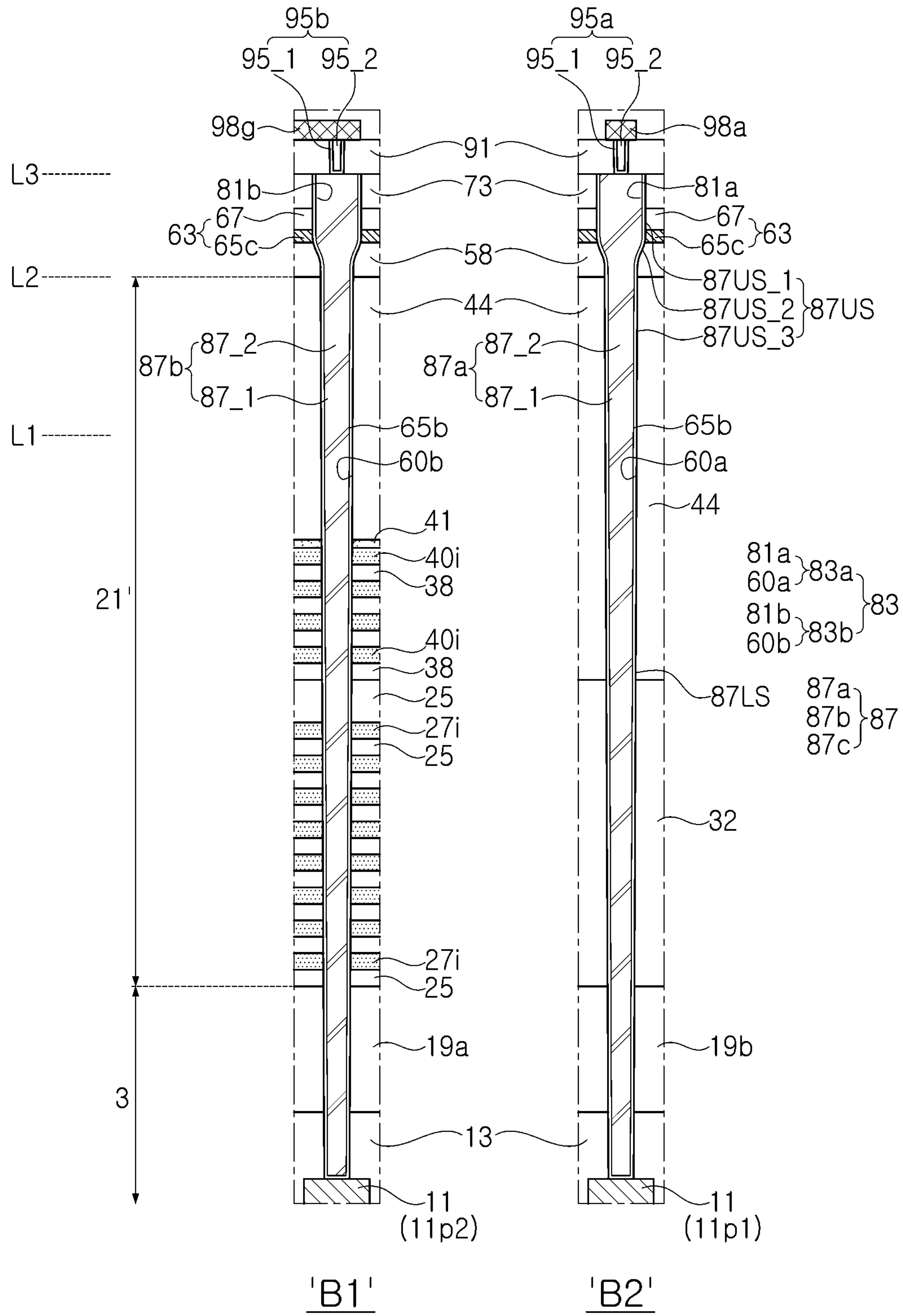



FIG. 6B

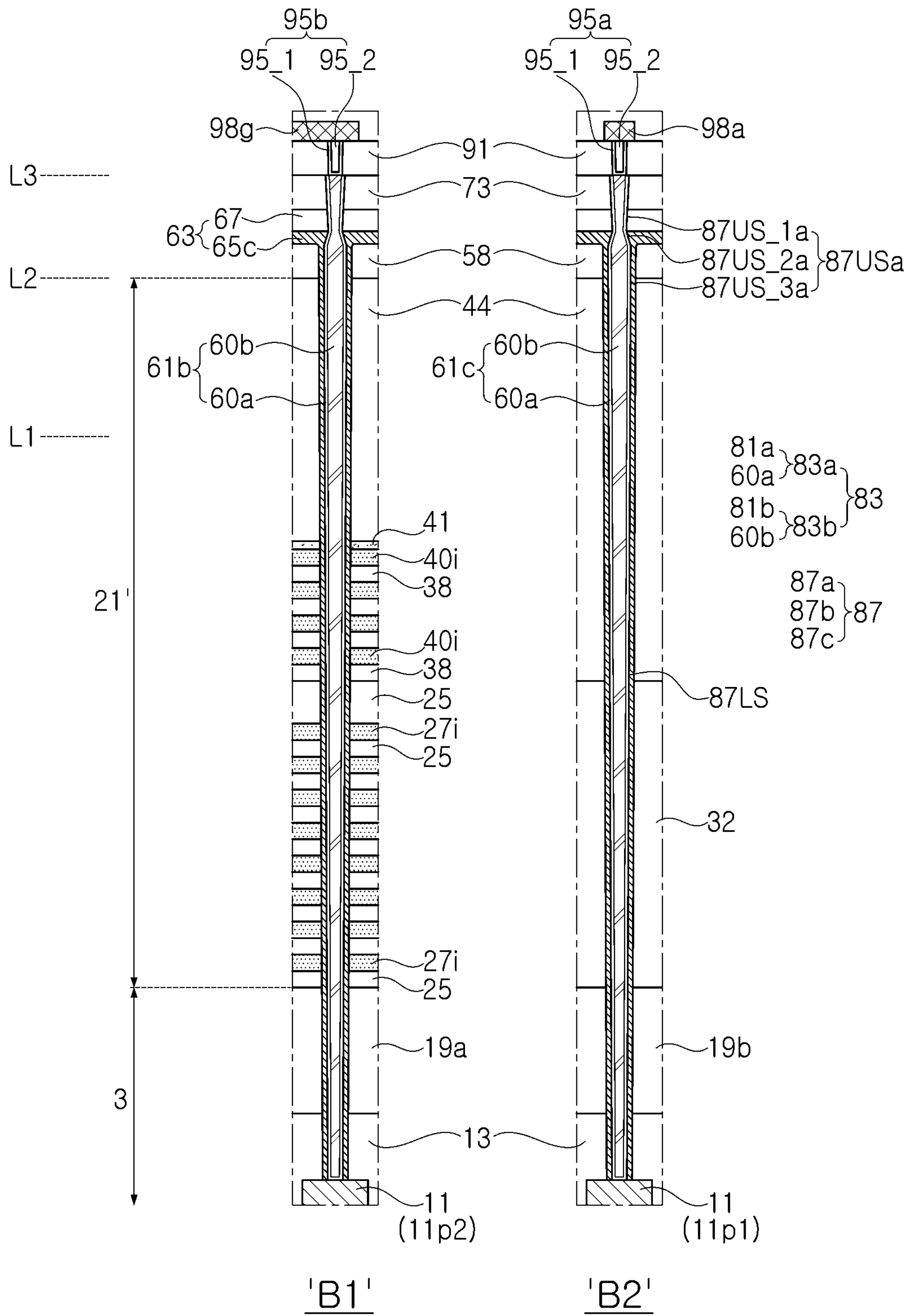



FIG. 7A

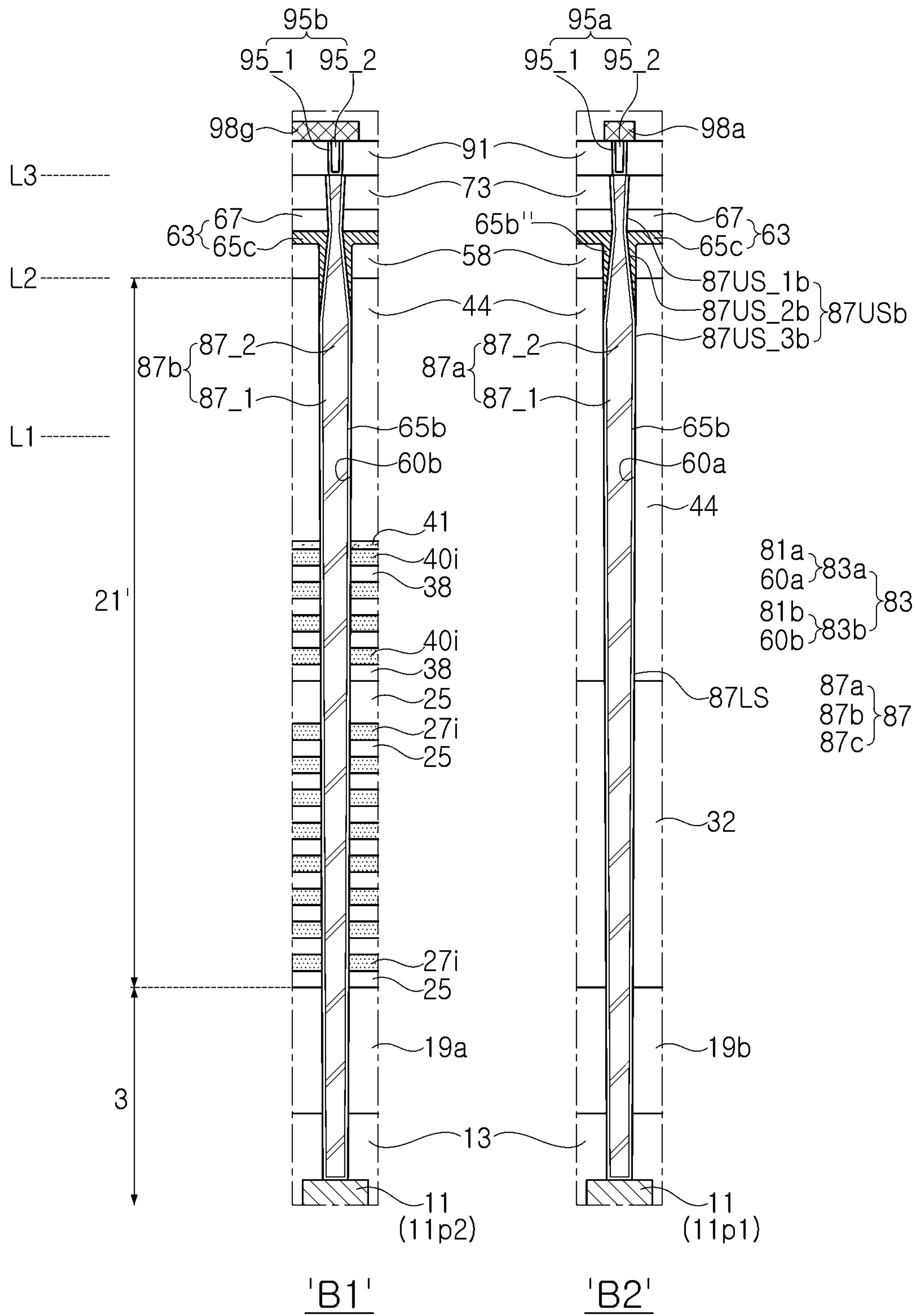



FIG. 7B

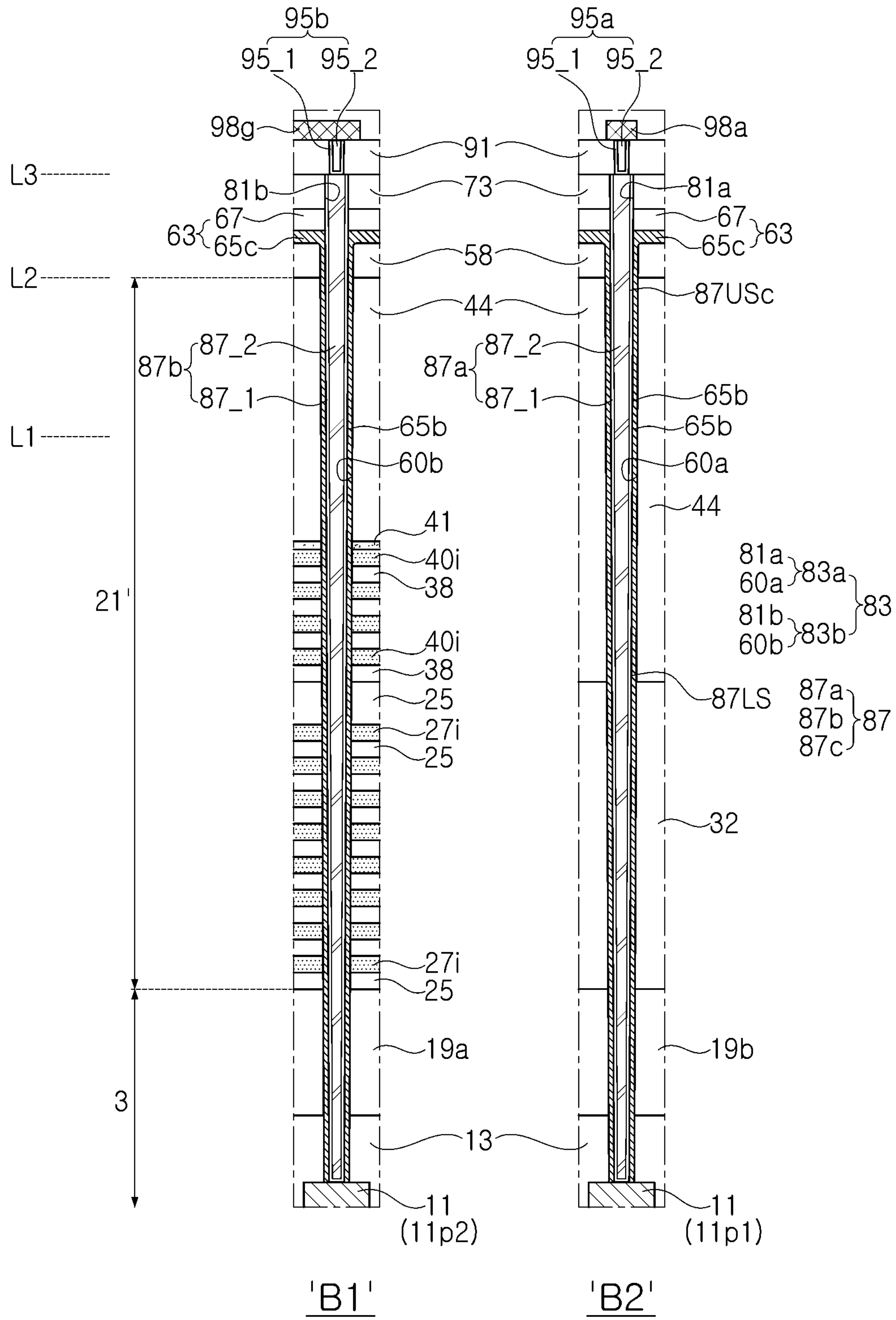



FIG. 7C

FIG. 8A

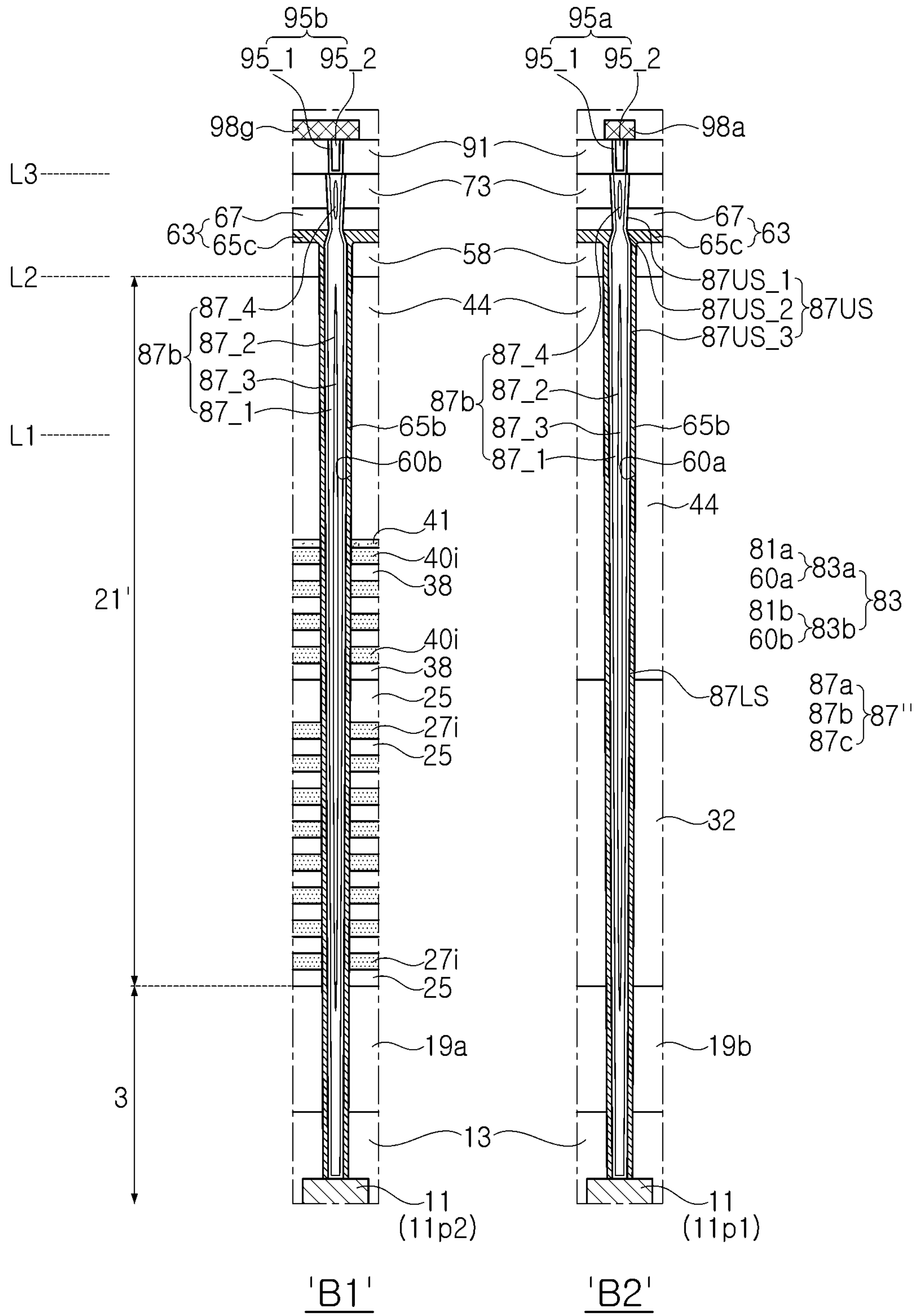



FIG. 8B

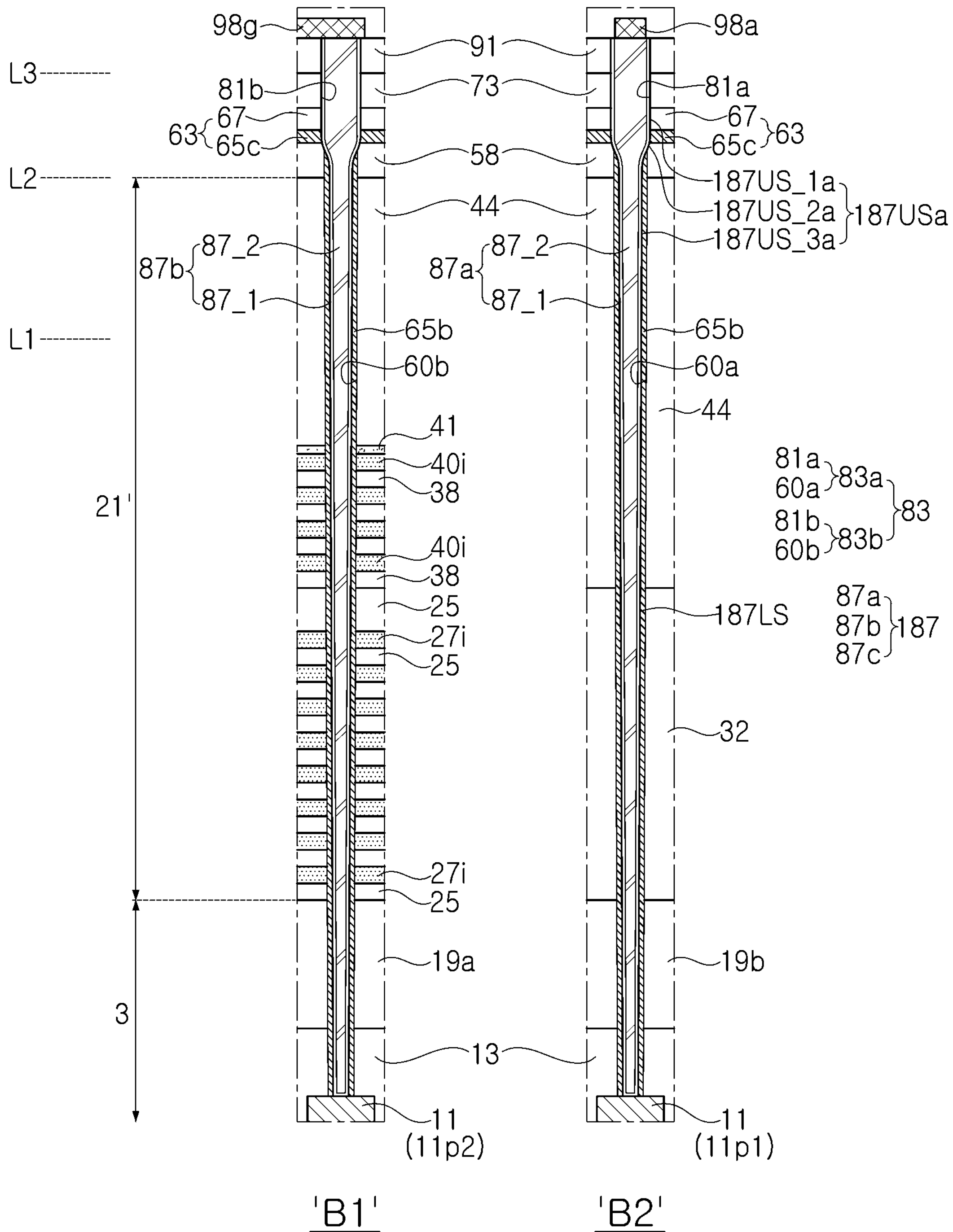



FIG. 9A

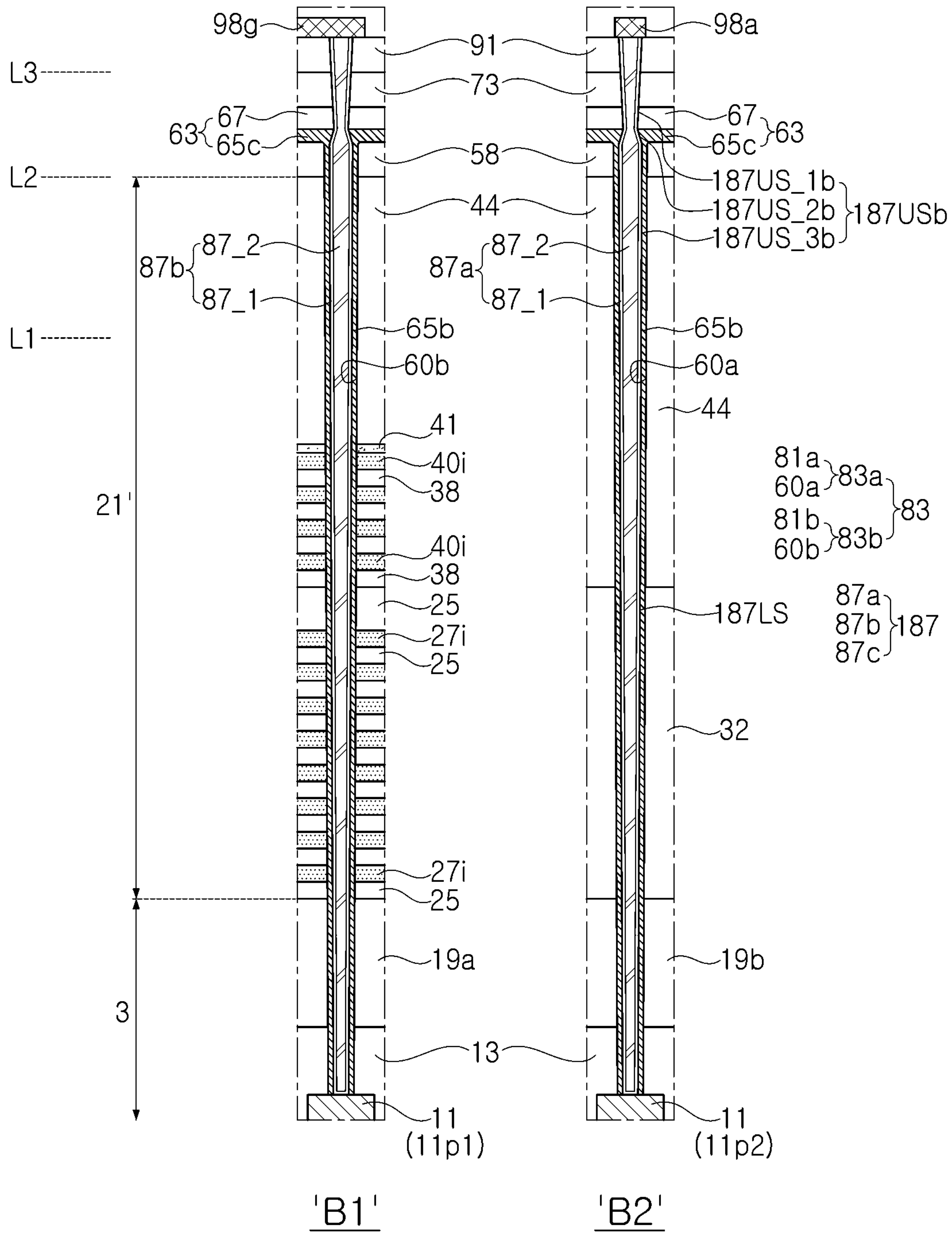



FIG. 9B

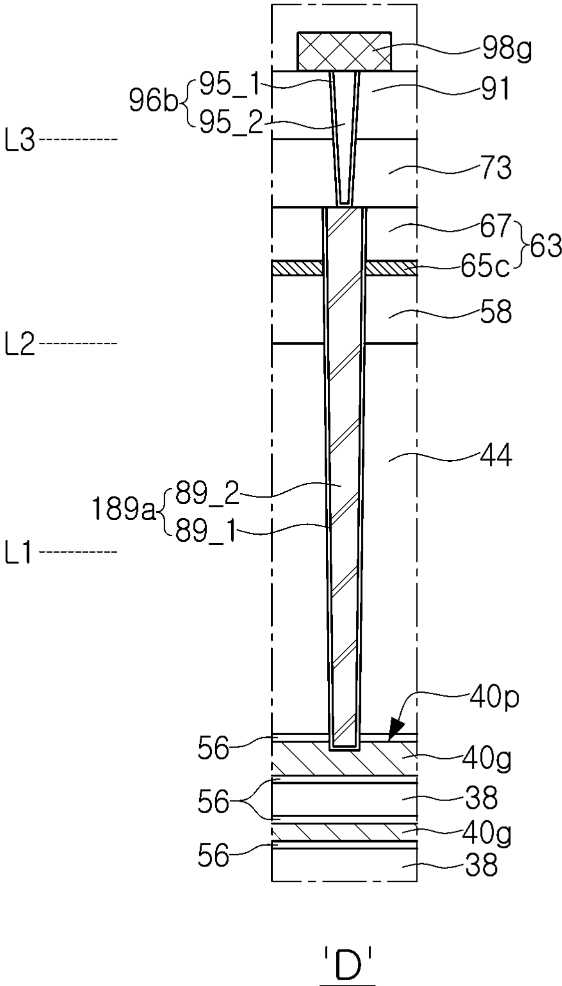



FIG. 10A

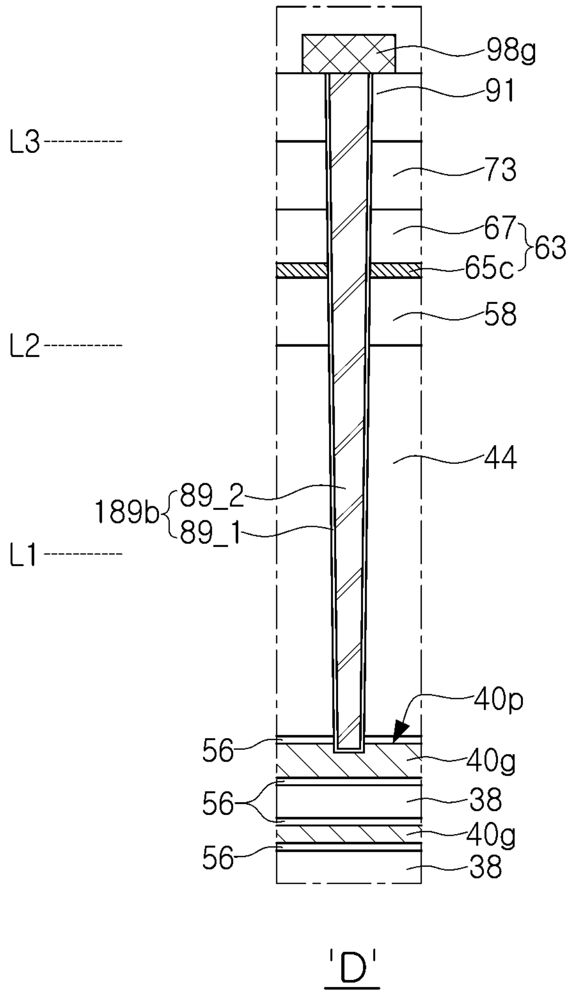



FIG. 10B

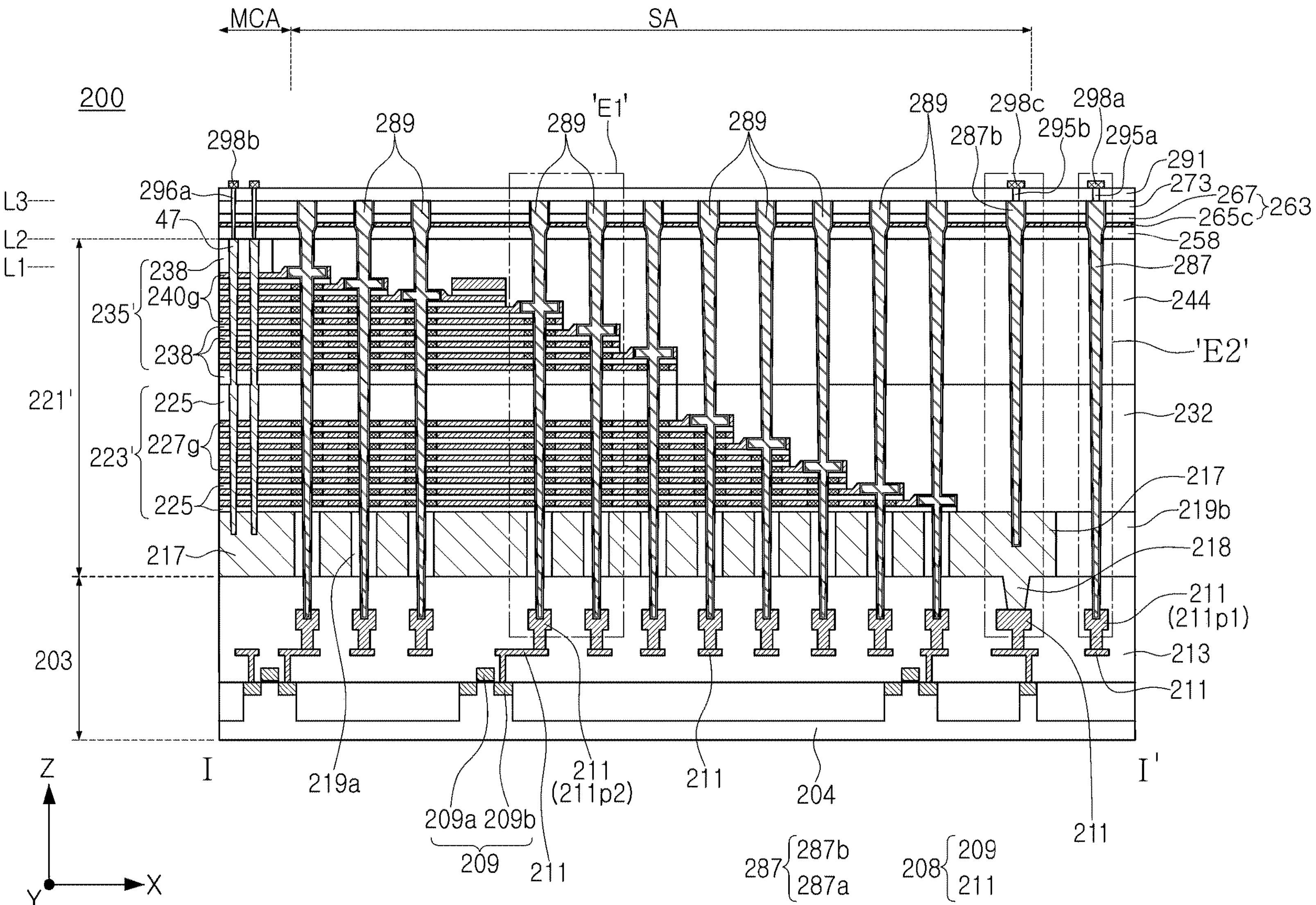



FIG. 11A

FIG. 11B

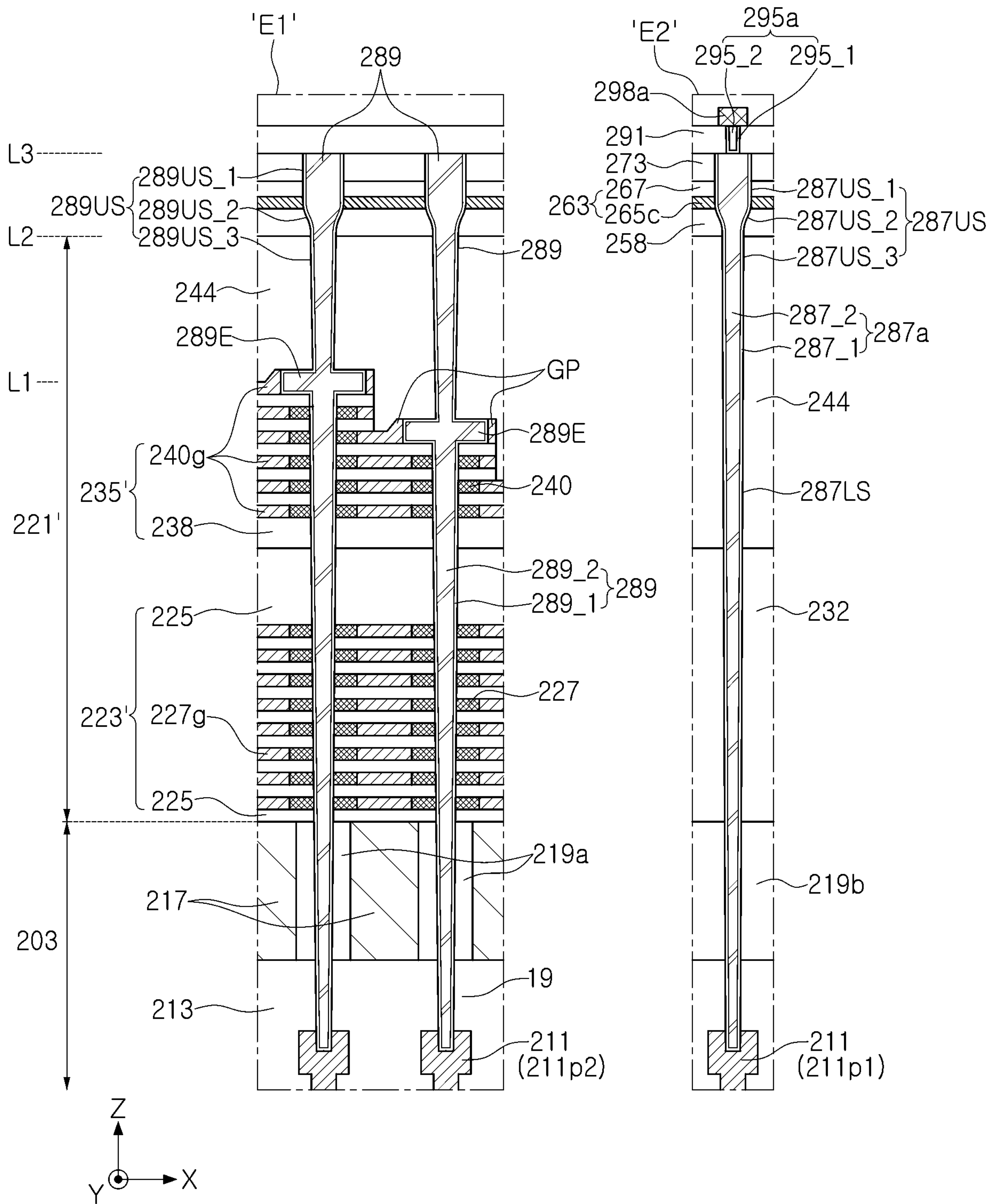



FIG. 12

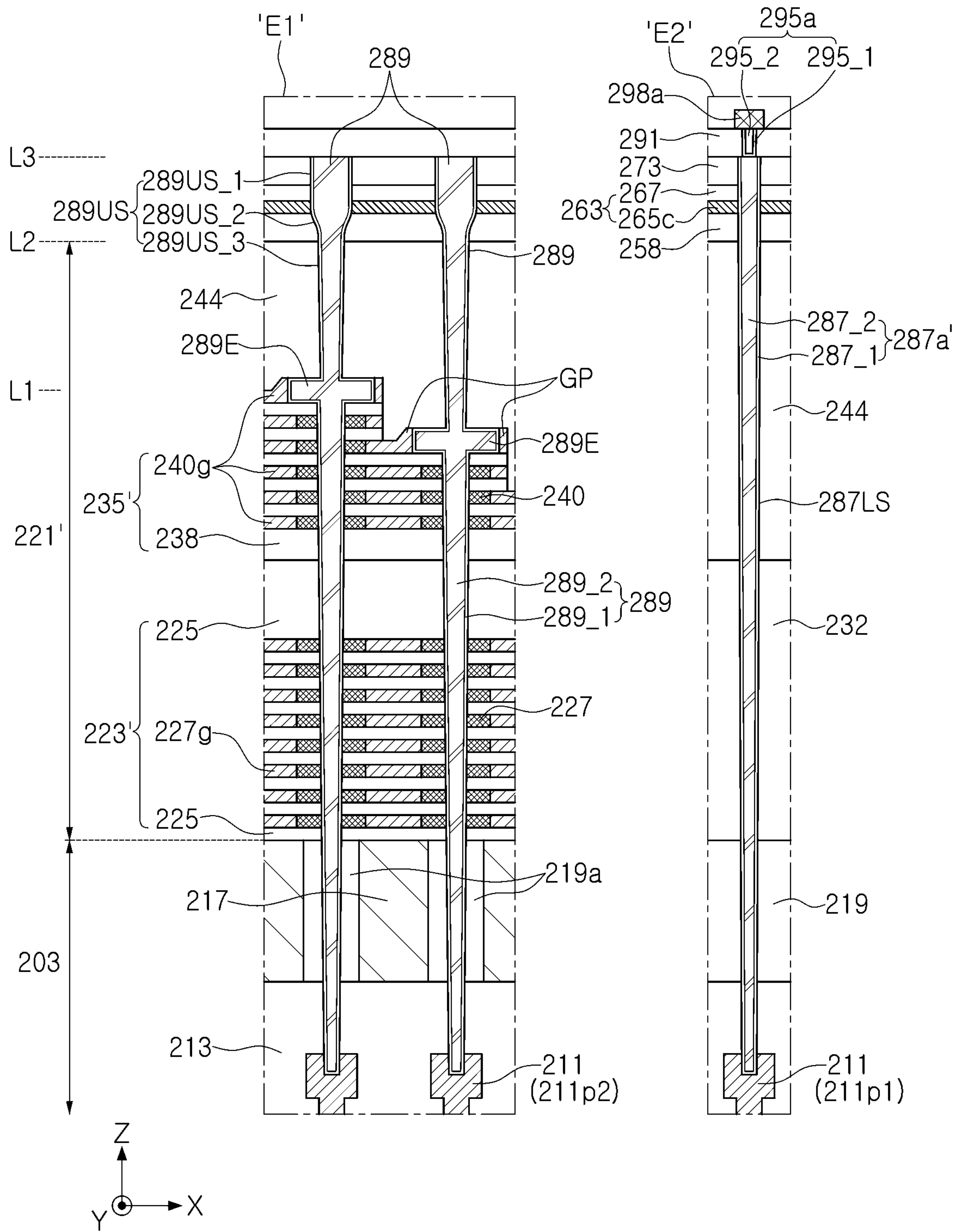



FIG. 13

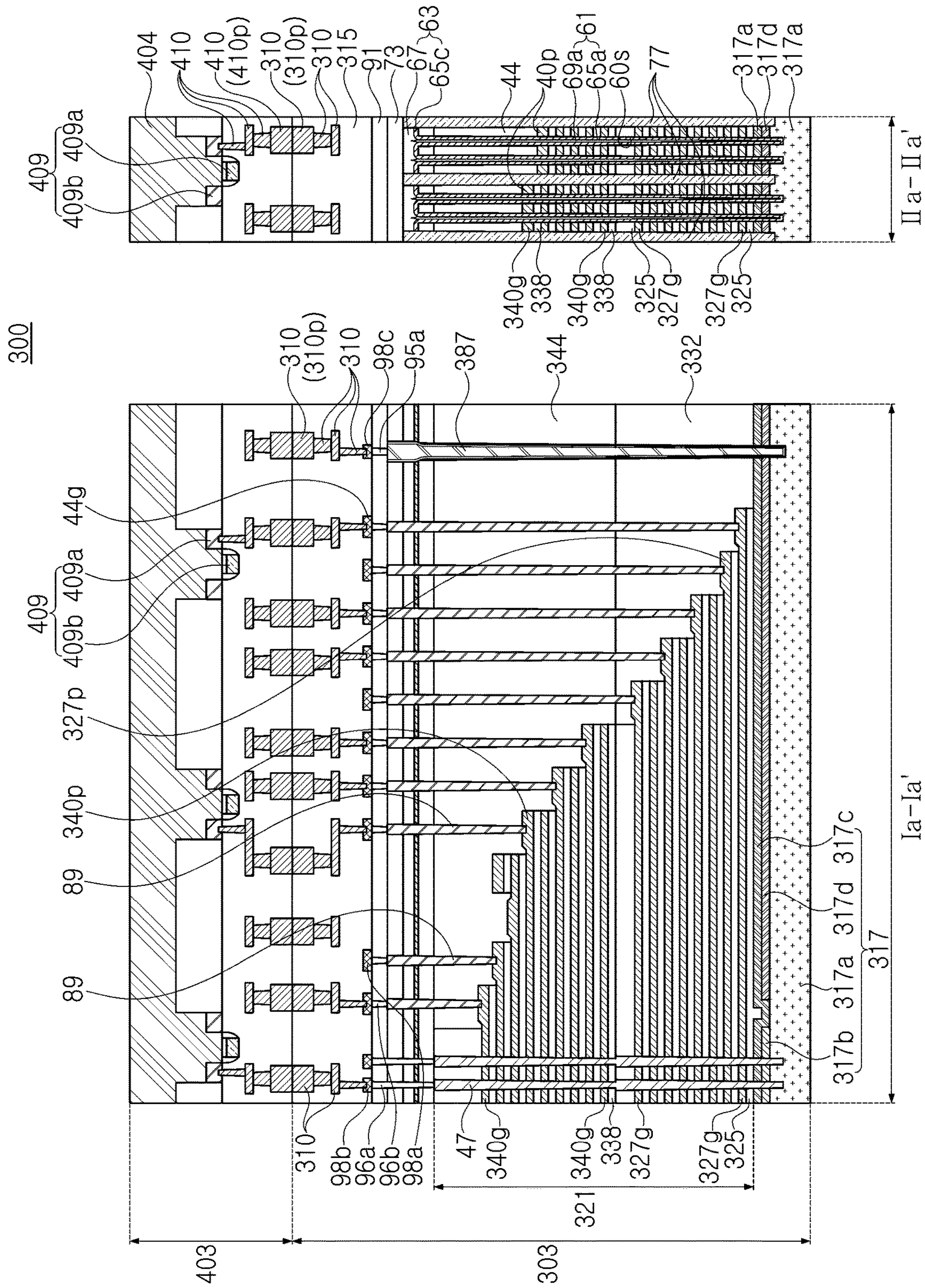



FIG. 14

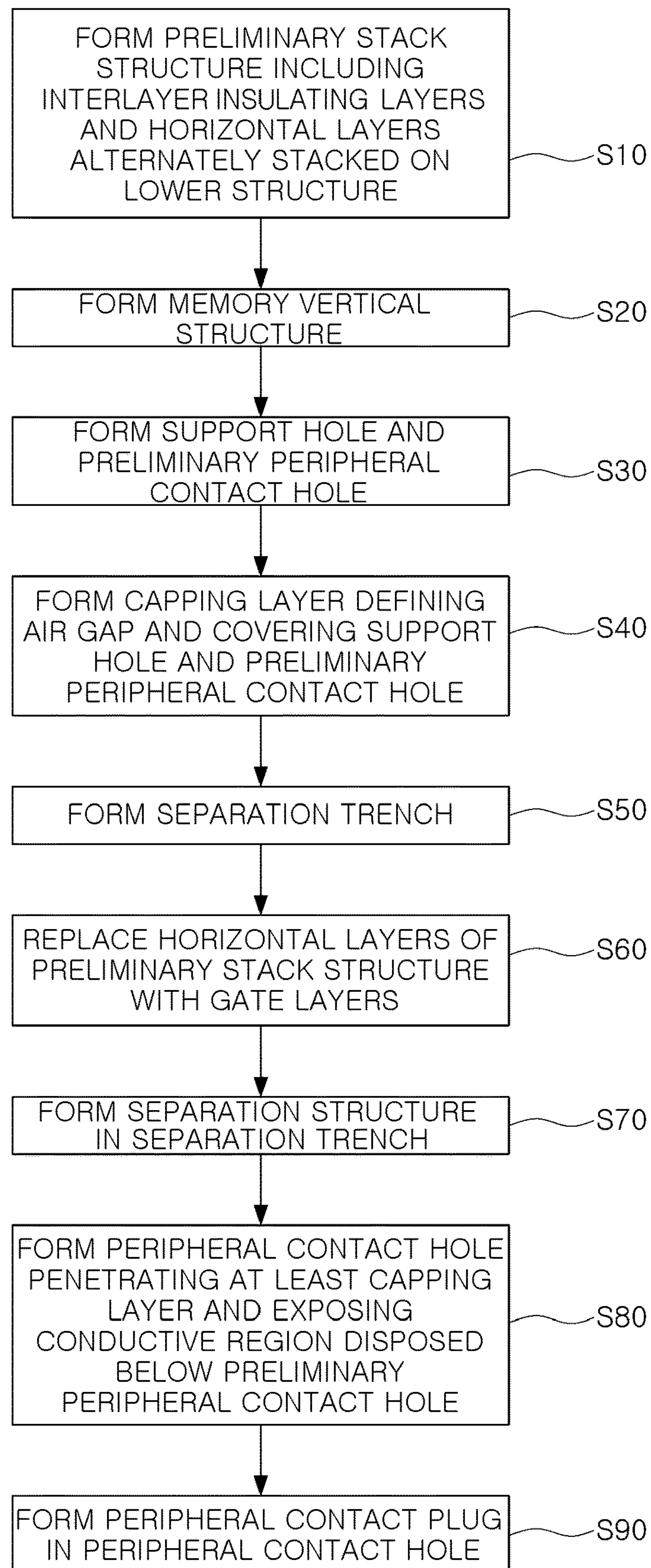



FIG. 15

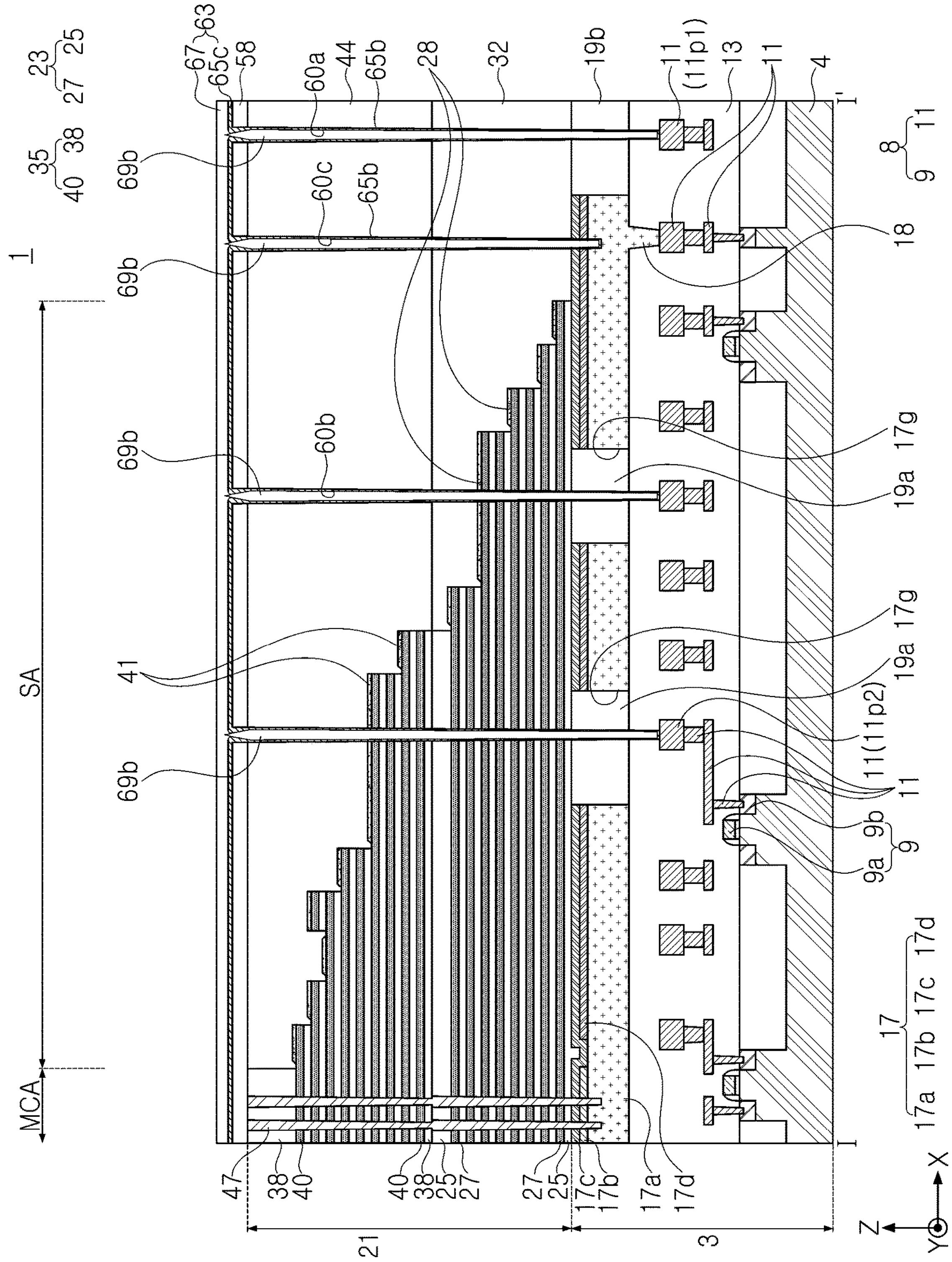



FIG. 16A

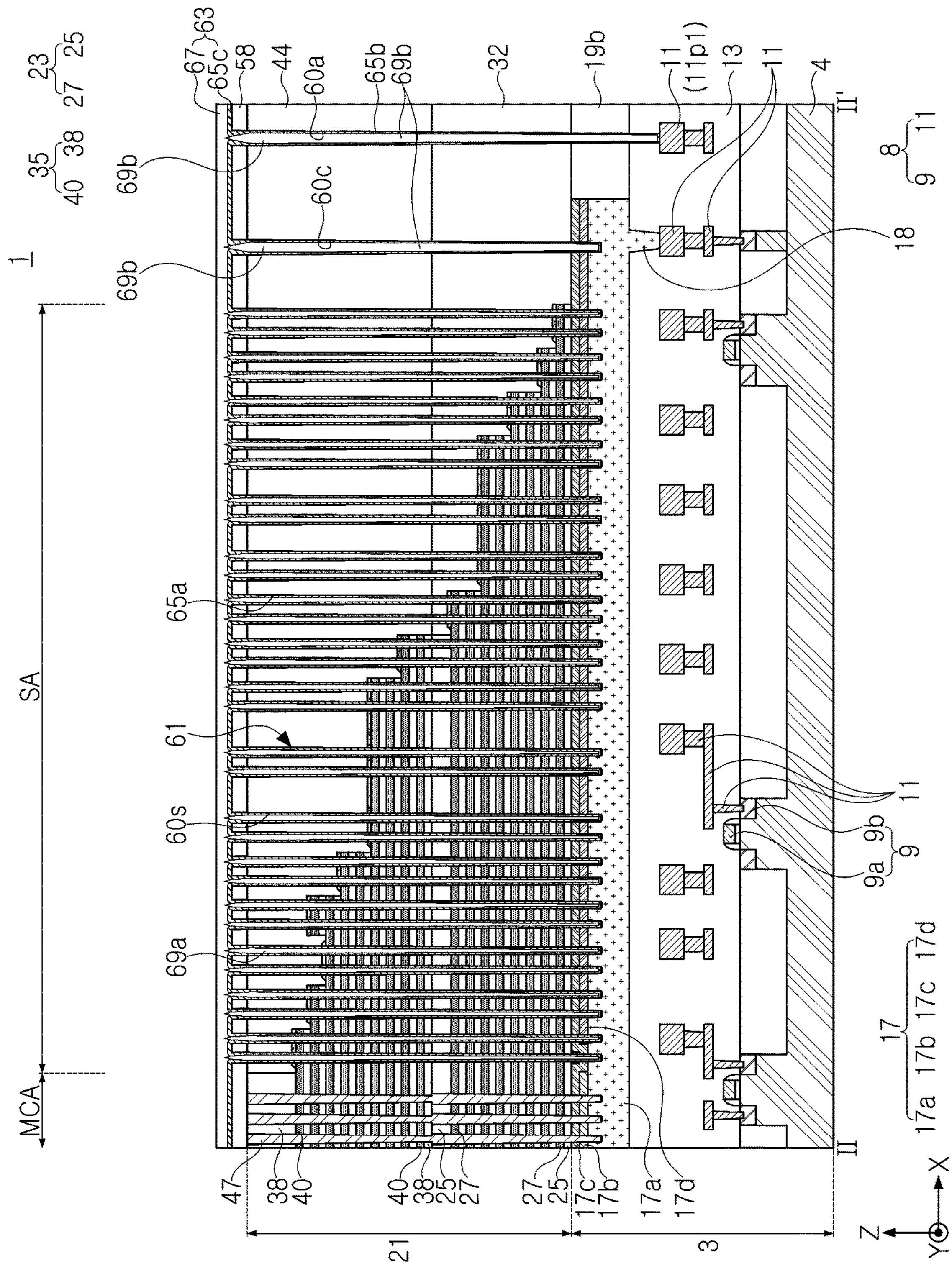



FIG. 16B

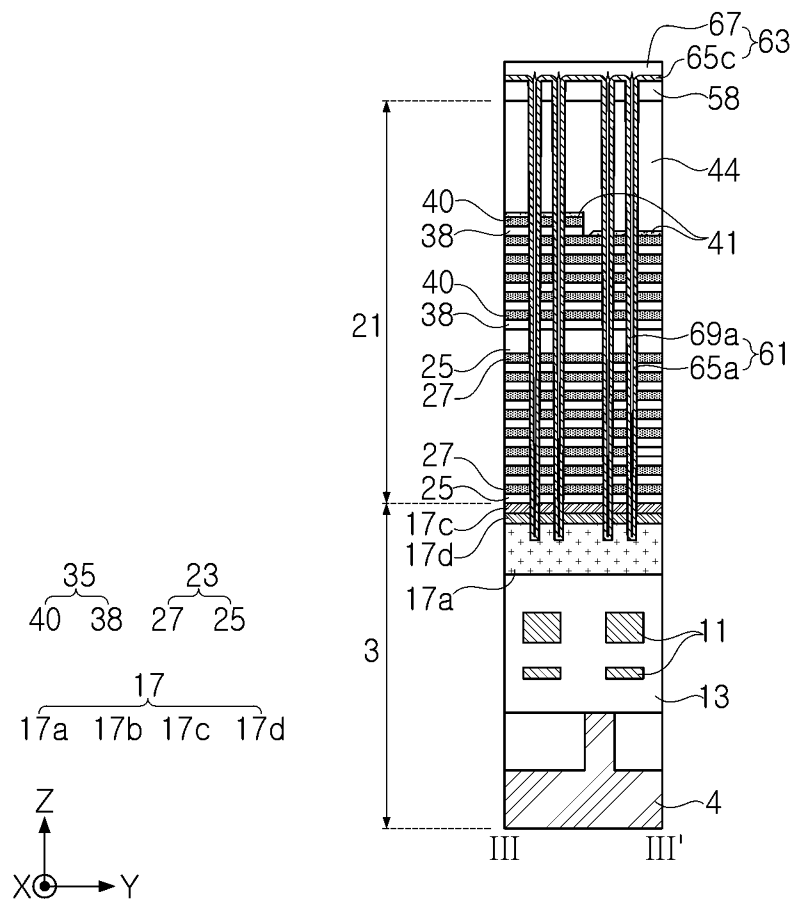



FIG. 16C

FIG. 17

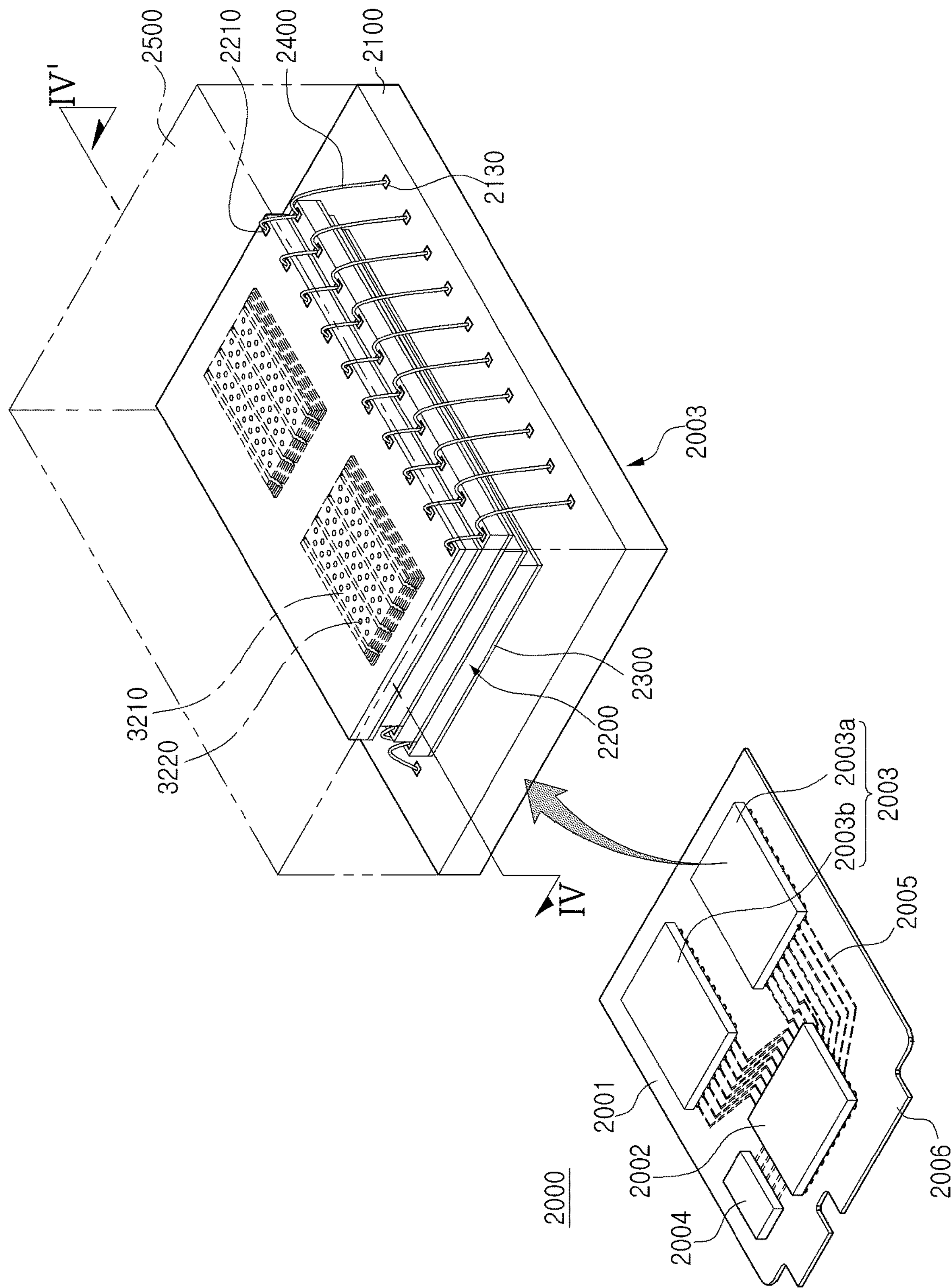



FIG. 18

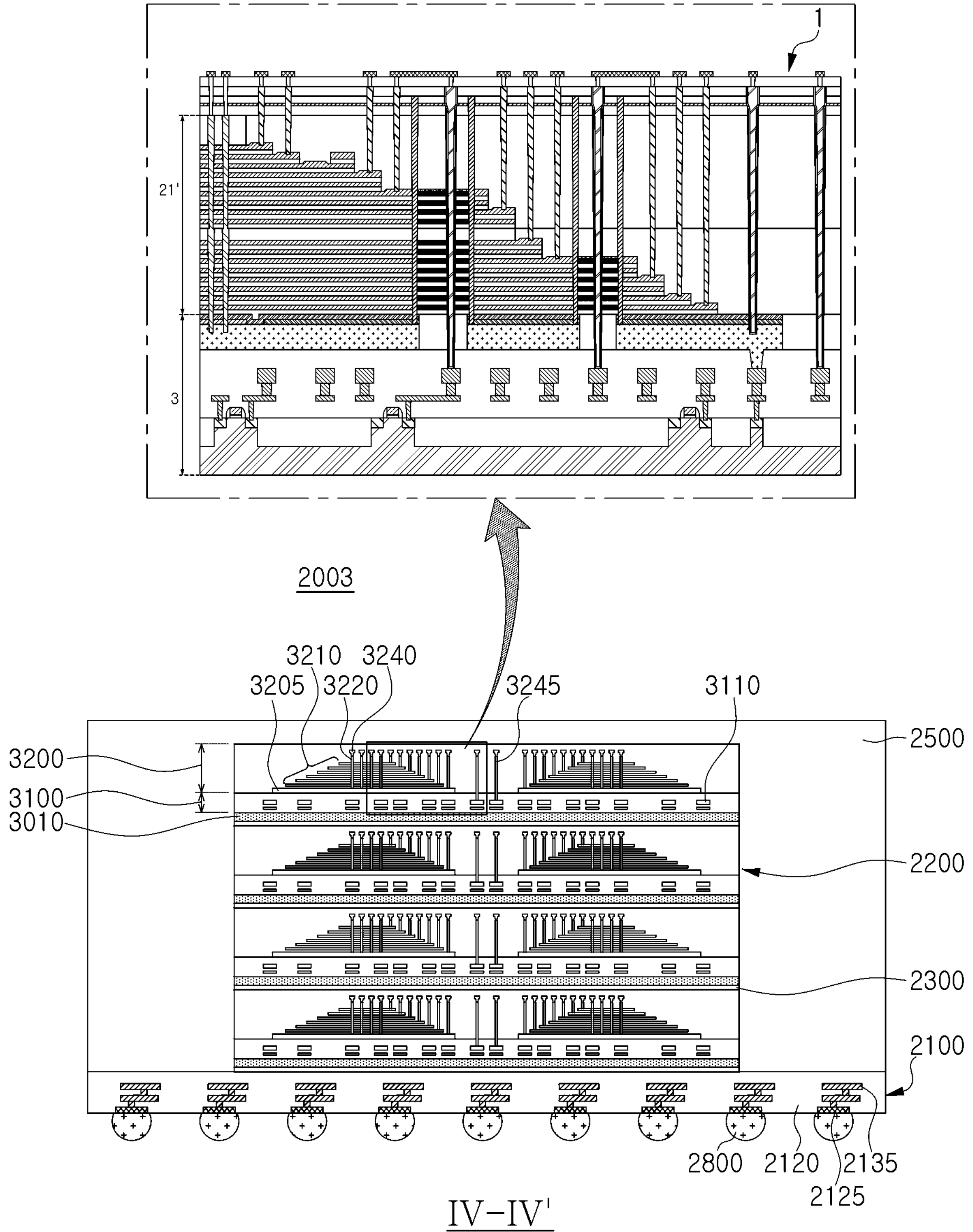



FIG. 19

# SEMICONDUCTOR DEVICE AND A DATA STORAGE SYSTEM INCLUDING THE SAME

## CROSS TO REFERENCE TO RELATED APPLICATION(S)

**[0001]** This application claims priority under 35 U.S.C. 119 to Korean Patent Application No. 10-2021-0038071 filed on Mar. 24, 2021 in the Korean intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

## TECHNICAL FIELD

**[0002]** Example embodiments of the present disclosure relate to a semiconductor device and a data storage system including the same.

## DISCUSSION OF RELATED ART

**[0003]** There is increasing demand for a semiconductor device that offers higher-capacity storage potential than a semiconductor device including cells arranged two-dimensionally. Accordingly, a semiconductor device including memory cells arranged three-dimensionally, has been developed.

## SUMMARY

**[0004]** An example embodiment of the present disclosure is to provide a semiconductor device which may increase integration density and reliability.

**[0005]** An example embodiment of the present disclosure is to provide a data storage system including a semiconductor device.

**[0006]** According to an example embodiment of the present disclosure, a semiconductor device includes: a first structure; a second structure including a stack structure including a first stack structure on the first structure and a second stack structure on the first stack structure, and an intermediate insulating layer covering at least a portion of the stack structure; an insulating structure on the second structure; a memory vertical structure penetrating the second structure; a support vertical structure penetrating the second structure and including an air gap and a support layer defining at least a lower portion and a sidewall of the air gap; a peripheral contact plug penetrating the second structure; and gate contact plugs, wherein each of the first and second stack structures includes interlayer insulating layers and gate layers alternately stacked, wherein the gate layers are spaced apart from each other in a vertical direction in a first region and include gate pads arranged in a second region adjacent to the first region, wherein the gate contact plugs are electrically connected to the gate pads, wherein the memory vertical structure penetrates the stack structure in the first region, wherein the memory vertical structure includes a slope changing portion between an uppermost gate layer among the gate layers of the first stack structure and a lowermost gate layer among the gate layers of the second stack structure, wherein the support vertical structure penetrates at least a portion of the gate layers in the second region, wherein the air gap of the support vertical structure includes a portion disposed on the same level as the slope changing portion of the memory vertical structure, wherein the peripheral contact plug is spaced apart from the gate layers, wherein the peripheral contact plug includes an upper region disposed on a level higher than an upper surface of an uppermost gate layer among the gate layers of the stack structure and a lower region disposed on a level lower than the upper surface of the uppermost gate layer among the gate layers of the stack structure, wherein the upper region of the peripheral contact plug includes a first portion, a second portion and a connection portion disposed between the first portion and the second portion, and wherein the connection portion has a slope different from a slope of at least one of the first portion and the second portion.

**[0007]** According to an example embodiment of the present disclosure, a semiconductor device includes: a pattern structure including a silicon layer; a stack structure including a first stack structure and a second stack structure on the first stack structure on the pattern structure, wherein each of the first and second stack structures includes interlayer insulating layers and gate layers alternately stacked, and in the first and second stack structures, the gate layers are vertically stacked and spaced apart from each other in a first region, and include gate pads arranged in a staircase shape in a second region adjacent to the first region; an insulating structure on the stack structure; separation structures penetrating the stack structure and extending in the insulating structure in the first region and the second region; a memory vertical structure penetrating the stack structure between the separation structures in the first region; a support vertical structure penetrating the stack structure and including an air gap between the separation structures in the second region; gate contact plugs in contact with the gate pads; a peripheral contact plug spaced apart from the gate layers; and bit line contact plugs on the memory vertical structure, wherein the peripheral contact plug includes an upper region disposed on a level higher than an upper surface of an uppermost gate layer among the gate layers of the stack structure and a lower region disposed on a level lower than the upper surface of the uppermost gate layer among the gate layers of the stack structure, wherein the upper region of the peripheral contact plug includes a first portion, a connection portion disposed below the first portion, and a second portion disposed below the connection portion, wherein a side of the connection portion has a slope different from a slope of at least one of a side of the first portion and the second portion, wherein a side of the memory vertical structure includes a slope changing portion in which a slope of the side of the memory vertical structure changes on a level between an uppermost gate layer among the gate layers of the first stack structure and a lowermost gate layer among the gate layers of the second stack structure, and wherein a side of the lower region of the peripheral contact plug is substantially vertical on the level between the uppermost gate layer among the gate layers of the first stack structure and the lowermost gate layer among the gate layers of the second stack structure.

**[0008]** According to an example embodiment of the present disclosure, a data storage system includes: a main board; a semiconductor device on the main board; and a controller electrically connected to the semiconductor device on the main board, wherein the semiconductor device includes: a pattern structure including a silicon layer; a stack structure including a first stack structure and a second stack structure on the first stack structure on the pattern structure, wherein each of the first and second stack structures includes interlayer insulating layers and gate layers alternately stacked, and in the first and second stack structures, the gate layers are vertically stacked and spaced apart from each other in a first region, and include gate pads arranged in a staircase

shape in a second region adjacent to the first region an insulating structure on the stack structure; separation structures penetrating the stack structure and extending into the insulating structure in the first region and the second region; a memory vertical structure penetrating the stack structure between the separation structures in the first region; a support vertical structure penetrating the stack structure and including an air gap between the separation structures in the second region; gate contact plugs in contact with the gate pads; a peripheral contact plug spaced apart from the gate layers; and bit line contact plugs on the memory vertical structure, wherein the peripheral contact plug includes an upper region disposed on a level higher than an upper surface of an uppermost gate layer among the gate layers of the stack structure and a lower region disposed on a level lower than the upper surface of the uppermost gate layer the gate layer among of the stack structure, wherein the upper region of the peripheral contact plug includes a first portion, a connection portion disposed below the first portion, and a second portion disposed below the connection portion, wherein a side of the connection portion has a slope different from a slope of at least one of a side of the first portion and a side of the second portion, wherein a side of the memory vertical structure includes a slope changing portion on a level between an uppermost gate layer among the gate layers of the first stack structure and a lowermost gate layer among the gate layers of the second stack structure, and wherein a side of the lower region of the peripheral contact plug is substantially vertical on the level between the uppermost gate layer among the gate layers of the first stack structure and the lowermost gate layer among the gate layers of the second stack structure.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]** The above and other features of the present disclosure will be more clearly understood from the following detailed description, taken in conjunction with the accompanying drawings, in which:

**[0010]** FIGS. **1**, **2**A, **2**B, **2**C, **3**A, **3**B, **3**C and **3**D are diagrams illustrating a semiconductor device according to an example embodiment of the present disclosure;

**[0011]** FIG. **4**A is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0012]** FIG. **4**B is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0013]** FIG. **5**A is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0014]** FIG. **5**B is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0015]** FIG. **6**A is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0016]** FIG. **6**B is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0017]** FIG. **7**A is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0018]** FIG. **7**B is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0019]** FIG. **7**C is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0020]** FIG. **8**A is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0021]** FIG. **8**B is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0022]** FIG. **9**A is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0023]** FIG. **9**B is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0024]** FIG. **10**A is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0025]** FIG. **10**B is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0026]** FIGS. **11**A, **11**B, and **12** are diagrams illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;

**[0027]** FIG. **13** is an enlarged diagram illustrating a modified example of a semiconductor device, illustrating a portion of the semiconductor device according to an example embodiment of the present disclosure;

**[0028]** FIG. **14** is a diagram illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;

**[0029]** FIG. **15** is a flowchart illustrating a method of manufacturing a semiconductor device according to an example embodiment of the present disclosure;

**[0030]** FIGS. **16**A, **16**B and **16**C are cross-sectional diagrams illustrating a method of manufacturing a semiconductor device according to an example embodiment of the present disclosure;

**[0031]** FIG. **17** is a diagram illustrating a data storage system including a semiconductor device according to an example embodiment of the present disclosure;

**[0032]** FIG. **18** is a perspective diagram illustrating a data storage system including a semiconductor device according to an example embodiment of the present disclosure; and

**[0033]** FIG. **19** is a cross-sectional diagram illustrating a data storage system including a semiconductor device according to an example embodiment of the present disclosure.

## DETAILED DESCRIPTION OF THE EMBODIMENTS

**[0034]** Hereinafter, example embodiments of the present disclosure will be described with reference to the accompanying drawings. In the drawings, like reference numerals may refer to like elements.

**[0035]** An example of a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIGS. **1** to **2**C. FIG. **1** is a plan diagram illustrating a semiconductor device according to an example embodiment of the present disclosure, FIG. **2**A is a cross-sectional diagram illustrating the region taken along line I-I' in FIG. **1**. FIG. **2**B is a cross-sectional diagram illustrating the region taken along line II-II' in FIG. **1**, and FIG. **2**C is a cross-sectional diagram illustrating the region taken along line III-III' in FIG. **1**.

**[0036]** Referring to FIGS. **1** to **2**C, a semiconductor device **1** according to an example embodiment of the present disclosure may include a first structure **3** and a second structure **21'** overlapping the first structure **3** in the vertical direction Z.

**[0037]** The first structure **3** may include a pattern structure **17'**. The pattern structure **17'** may include at least one silicon layer.

**[0038]** The pattern structure **17'** may include a first pattern layer **17**_a_, a second pattern layer **17**_b_', a third pattern layer **17**_c_, and a fourth pattern layer **17**_d_. The second pattern layer **17**_b_' and the fourth pattern layer **17**_d_ may be spaced apart from each other on the first pattern layer **17**_a_. In other words, the second pattern layer **17**_b_' and the fourth pattern layer **17**_d_ may be disposed on the first pattern layer **17**_a_. The third pattern layer **17**_c_ may cover the second pattern layer **17**_b_' and the fourth pattern layer **17**_d_ on the first pattern layer **17**_a_. The third pattern layer **17**_c_ may contact the first pattern layer **17**_a_ between the second and fourth pattern layers **17**_b_' and **17**_d_. The first pattern layer **17**_a_ may have a thickness greater than a thickness of each of the second pattern layer **17**_b_', the third pattern layer **17**_c_, and the fourth pattern layer **17**_d_. At least one of the first pattern layer **17**_a_, the second pattern layer **17**_b_', the third pattern layer **17**_c_, and the fourth pattern layer **17**_d_ may include a silicon layer. For example, the first pattern layer **17**_a_, the second pattern layer **17**_b_', and the third pattern layer **17**_c_ may include a silicon layer, such as, for example, a silicon layer having N-type conductivity, and the fourth pattern layer **17**_d_ may include a material different from that of the silicon layer. For example, the fourth pattern layer **17**_d_ may include a plurality of layers stacked in order, a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer, for example.

**[0039]** The first structure **3** may include a semiconductor substrate **4**, a peripheral circuit **8** on the semiconductor substrate **4**, and a lower insulating layer covering the peripheral circuit **8** on the semiconductor substrate **4**. The peripheral circuit **8** may include a circuit device **9** such as a transistor including a peripheral gate **9**_a_ and a peripheral source/drain **9**_b_, and a circuit interconnection **11** electrically connected to the circuit device **9**. A portion of the circuit interconnection **11** may be first and second peripheral circuit pads **11**_p_**1** and **11**_p_**2**.

**[0040]** The pattern structure **17'** may be disposed on a lower insulating layer **13**.

**[0041]** The pattern structure **17'** may further include a ground pattern **18**. For example, the ground pattern **18** may be disposed below the first pattern layer **17**_a_ and may be grounded to the semiconductor substrate **4** through a portion of the circuit interconnection **11**. The ground pattern **18** may extend from the first pattern layer **17**_a_. For example, when the first pattern layer **17**_a_ is formed of a silicon layer, the ground pattern **18** may be formed of a silicon layer extending from the silicon layer.

**[0042]** The pattern structure **17'** may have gaps **17**_g_. Each of the gaps **17**_g_ may be implemented as a slit or an opening penetrating the pattern structure **17'**.

**[0043]** The first structure **3** may further include an internal insulating layer **19**_a_ filling the gaps **17**_g_ and an external insulating layer **19**_b_ disposed on an external side of the pattern structure **17'**.

**[0044]** The second structure **21'** may include a first region MCA and a second region SA. The second structure **21'** may include stack structures **23'** and **35'** disposed in the first region MCA and extending from the first region MCA into the second region SA.

**[0045]** In example embodiments of the present disclosure, the first region MCA may be a memory cell region, and the second region SA may be a staircase region, an extension region, or a contact region. Hereinafter, for ease of description, the first region MCA will be referred to as a memory cell region and the second region SA will be referred to as a staircase region.

**[0046]** The stack structures **23'** and **35'** may include a first stack structure **23'** and a second stack structure **35'** on the first stack structure **23'**. The first stack structure **23'** may include first interlayer insulating layers **25** and first gate layers **27**_g_ alternately stacked in the vertical direction Z. The vertical direction Z may be disposed in a direction perpendicular to an upper surface of the pattern structure **17'**. The first gate layers **27**_g_ may have first gate pads **27**_p_ arranged in a staircase shape in the staircase region SA.

**[0047]** The second stack structure **35'** may include second interlayer insulating layers **38** and second gate layers **40**_g_ alternately stacked in the vertical direction Z. The second gate layers **40**_g_ may have second gate pads **40**_p_ arranged in a staircase shape in the staircase region SA.

**[0048]** The first interlayer insulating layers **25** and the second interlayer insulating layers **38** may form interlayer insulating layers **25** and **38**, and the first gate layers **27**_g_ and the second gate layer **40**_g_ may form gate layers **27**_g_ and **40**_g_. Accordingly, the first and second stack structures **23'** and **35'** may include the interlayer insulating layers **25** and **38** and the gate layers **27**_g_ and **40**_g_ alternately stacked in the vertical direction Z. The gate layers **27**_g_ and **40**_g_ may have the first and second gate pads **27**_p_ and **40**_p_ arranged in a staircase shape in the staircase region SA.

**[0049]** In example embodiments of the present disclosure, the "gate pad" may be a region of the gate layer of which an upper portion is not covered by another gate layer disposed thereon in the staircase region SA.

**[0050]** In example embodiments of the present disclosure, the first and second gate pads **27**_p_ and **40**_p_ may be arranged in the staircase shape illustrated in the drawings, and also in various staircase shapes.

**[0051]** Each of the first and second gate pads **27**_p_ and **40**_p_ may have a thickness greater than a thickness of each of the

first and second gate layers **27***g* and **40***g* disposed in the memory cell array region MCA.

**[0052]** The first and second gate layers **27***g* and **40***g* may include a conductive material. For example, each of the first and second gate layers **27***g* and **40***g* may be formed of two or more materials among a doped polysilicon, a metal-semiconductor compound (e.g., TiSi, TaSi, CoSi, NiSi, WSi, or the like), a metal nitride (e.g., TiN, TaN or WN, or the like) or a metal (e.g., Ti or W, or the like). The interlayer insulating layers **25** and **38** may be formed of an insulating material such as silicon oxide.

**[0053]** The first and second stack structure or multi layer structures **23'** and **35'** may further include one or a plurality of through regions TA. Each of the through regions TA may further include insulating horizontal layers **27***i* and **40***i* disposed on the same level as a level of first and second gate layers **27***g* and **40***g* adjacent to the through regions TA among the first and second gate layers **27***g* and **40***g*. For example, among the through regions TA, a portion of the through region TA adjacent to the first gate layers **27***g* may include first insulating horizontal layers **27***i* disposed on the same level as a level of the first gate layers **27***g*, and a portion of the through region TA adjacent to the second gate layers **40***g* may include second insulating horizontal layers **40***i* disposed on the same level as a level of the second gate layers **40***g*.

**[0054]** In an example embodiment of the present disclosure, each of the through regions TA may further include reinforcing horizontal layers **28** and **41** in contact with an uppermost insulating horizontal layer on an uppermost insulating horizontal layer among the insulating horizontal layers **27***i* and **40***i*. For example, the through region TA in a position spaced apart from the second stack structure **35'** may include a first reinforcing horizontal layer **28** in contact with the uppermost first insulating horizontal layer among the first insulating horizontal layers **27***i*. For example, the first reinforcing horizontal layer **28** may cover the uppermost first insulating horizontal layer among the first insulating horizontal layers **27***i*. The through region TA disposed in the first and second stack structures **23'** and **35'** may include a second reinforcing horizontal layer **41** in contact with an uppermost second insulating horizontal layer among the second insulating horizontal layers **40***i*. For example, the second reinforcing horizontal layer **41** may cover the uppermost second insulating horizontal layer among the second insulating horizontal layers **40***i*.

**[0055]** The first and second insulating horizontal layers **27***i* and **40***i* may be formed of an insulating material different from that of the first and second interlayer insulating layers **25** and **38**. For example, the first and second insulating horizontal layers **27***i* and **40***i* may be formed of first silicon nitride, and the first and second interlayer insulating layers **25** and **38** may be formed of silicon oxide.

**[0056]** The first and second reinforcing horizontal layers **28** and **41** may be formed of a second silicon nitride having an etch rate different from that of the first silicon nitride of the first and second insulating horizontal layers **27***i* and **40***i*. The second silicon nitride may be a material having an etch rate higher than that of the first silicon nitride.

**[0057]** When viewed in on the same plane as in FIG. **1**, in the stack structures **23'** and **35'**, each of the through regions TA may be surrounded by a gate region GA (in FIG. **1**). In the gate region GA, the first and second gate layers **27***g* and **40***g* may be disposed. Accordingly, each of the through regions TA may be surrounded by adjacent first and second gate layers **27***g* and **40***g*. The second structure **21'** may further include intermediate insulating layers **32** and **44**. The intermediate insulating layers **32** and **44** may include a first intermediate insulating layer **32** and a second intermediate insulating layer **44**. The first intermediate insulating layer **32** may include the first gate pads **27***p*, a portion of the pattern structure **17'** not covered by the first stack structure **23'**, and the external insulating layer **19***b*. The second intermediate insulating layer **44** may cover the second gate pads **40***p* and the first intermediate insulating layer **32**. The first and second intermediate insulating layers **32** and **44** may be formed of an insulating material such as silicon oxide.

**[0058]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a memory vertical structure **47** including a portion penetrating the second structure **21'**. The memory vertical structure **47** may include a portion penetrating the first and second stack structures **23'** and **35'** in the memory cell array region MCA. The memory vertical structure **47** may extend into the pattern structure **17'** from a portion penetrating the second structure **21'** and may be in contact the pattern structure **17'**. For example, the memory vertical structure **47** may penetrate the third pattern layer **17***c* and the second pattern layer **17***b'* in order and may extend into the first pattern layer **17***a*. The memory vertical structure **47** may be in contact with at least one of the first to third pattern layers **17***a*, **17***b'*, and **17***c* formed as a silicon layer.

**[0059]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a string separation pattern **45** penetrating one or a plurality of upper gate layers disposed thereon among the second gate layers **40***g*. The string separation pattern **45** may be formed of silicon oxide. The string separation pattern **45** may be disposed on a level higher than a second gate layer, which may be a word line, among the second gate layers **40***g*.

**[0060]** The semiconductor device **1** according to all example embodiment of the present disclosure may include a dummy vertical structure **47***d* penetrating the string separation pattern **45** and also penetrating the second structure **21'**, and in contact with the pattern structure **17'**. The dummy vertical structure **47***d* may have the same cross-sectional structure as that of the memory vertical structure **47** and may be formed of the same material as that of the memory vertical structure **47**.

**[0061]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a first upper insulating layer **58** on the second structure **21'**. The first upper insulating layer **58** may include silicon oxide.

**[0062]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include support holes **60***s* penetrating the first upper insulating layer **58** and the second structure **21'** and exposing a portion of the pattern structure **17'**, and support vertical structures **61** disposed in the support holes **60***s*. Each of the support vertical structures **61** may include a portion penetrating at least a portion of the first and second gate layers **27***g* and **40***g* of the second structure **21'** in the staircase region SA. When viewed on the plane, each of the support vertical structures **61** may have a circular shape or an elliptical shape.

**[0063]** At least a portion of the support vertical structures **61** may penetrate the third pattern layer **17***c* and the fourth pattern layer **17***d* of the pattern structure **17'** in order, and may extend into the first pattern layer **17***a*. One of the support vertical structures **61** may be spaced apart from the fourth pattern layer **17***d*, may penetrate the third pattern layer **17***c*, and may extend into the first pattern layer **17***a*.

**[0064]** Hereinafter, a single support hole **60***s* and a single support vertical structure **61** will be mainly described for ease of description.

**[0065]** An upper surface of the support vertical structure **61** may be disposed on a level higher than the upper surface of the memory vertical structure **47**.

**[0066]** In example embodiments, "level" may refer to a level when viewed with respect to the upper surface of the pattern structure **17'** or a level when viewed with respect to the upper surface of the semiconductor substrate **4**.

**[0067]** The support vertical structure **61** may include an air gap **69***a* and a support layer **65***a* defining at least a portion of the air gap **69***a*.

**[0068]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a capping layer **63** disposed on the first upper insulating layer **58** and covering the support vertical structure **61**.

**[0069]** The capping layer **63** may include a lower capping layer **65***c* and an upper capping layer **67** on the lower capping layer **65***c*.

**[0070]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include dam structures **71**. Each of the dam structures **71** may penetrate the capping layer **63**, the first upper insulating layer **58**, and the second structure **21'**, and may surround each of the through regions TA. Accordingly, when viewed on the plane, each of the darn structures **71** may be disposed between the gate region GA (in FIG. **1**) and each of the through regions TA (in FIG. **1**).

**[0071]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a second upper insulating layer **73** on the capping layer **63**. The second upper insulating layer **73** may be in direct contact with the upper capping layer **67**.

**[0072]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include separation structures **77** penetrating the second upper insulating layer **73**, the capping layer **63**, the first upper insulating layer **58**, and the second structure **21'**. Each of the separation structures **77** may be formed of silicon oxide or silicon oxide having a void therein. In another example, each of the separation structures **77** may include a conductive pattern in contact with the pattern structure **17'** and an insulating layer covering a side surface of the conductive pattern.

**[0073]** Each of the separation structures **77** may include a lower separation portion **77***a* penetrating the capping layer **63**, the first upper insulating layer **58** and the second structure **21'** and an upper separation portion **77***b* penetrating the second upper insulating layer **73**. The lower separation portion **77***a* and the upper separation portion **77***b* may be integrated with each other.

**[0074]** In at least one of the separation structures **77**, the upper separation portion **77***b* may have a width different from a width of the lower separation portion **77***a*. For example, in at least one of the separation structures **77**, the upper separation portion **77***b* may have a width greater than a width of the lower separation portion **77***a*.

**[0075]** In at least one of the separation structures **77**, at least a portion of a side surface of the upper separation portion **77***b* may not be vertically aligned with at least a portion of a side surface of the lower separation portion **77***a*.

**[0076]** The separation structures **77** may include a plurality of main separation structures **77**M parallel to each other, and auxiliary separation structures **77**S disposed between the main separation structures **77**M. Each of the separation structures **77** may include a line portion extending in the first horizontal direction X. The first horizontal direction X may be parallel to an upper surface of the pattern structure **17'**. The first horizontal direction X may be a direction from the memory cell array region MCA toward the staircase region SA. Each of the auxiliary separation structures **77**S may have a length shorter than that of each of the main separation structures **77**M. For example, a plurality of the auxiliary separation structures **77**S may be arranged in the first direction X next to a single main separation structure **77**M arranged in the first direction X. The main separation structures **77**M may penetrate the second structure **21'** and may separate the first and second stack structures **23'** and **35'** in the second horizontal direction Y. The second horizontal direction Y may be parallel to the upper surface of the pattern structure **17'** and may be perpendicular to the first horizontal direction X. Each of the separation structures **77** may be in contact with the first and second gate layers **27***g* and **40***g* adjacent to the separation structure **77**.

**[0077]** The separation structures **77** may extend downwardly from a portion penetrating the second structure **21'** and may be in contact the pattern structure **17'**. At least one of the separation structures **77** may be in contact with the first pattern layer **17***a*.

**[0078]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include peripheral contact plugs **87**. The peripheral contact plugs **87** may include a first peripheral contact plug **87***a*, a second peripheral contact plug **87***b*, and a third peripheral contact plug **87***c*. The peripheral contact plugs **87** may penetrate the second upper insulating layer **73**, the capping layer **63**, the first upper insulating layer **58**, and the second structure **21'**, and may extend into the lower structure **3**.

**[0079]** The first peripheral contact plug **87***a* may be spaced apart from the first and second gate layers **27***g* and **40***g*, may penetrate the first and second intermediate insulating layers **32** and **44**, may be in contact with the first peripheral circuit pad **11***p***1**, and may be electrically connected to the first peripheral circuit pad **11***p***1**.

**[0080]** The second peripheral contact plug **87***b* may be spaced apart from the first and second gate layers **27***g* and **40***g*, may penetrate the first and second insulating horizontal layers **27***i* and **40***i* of the through regions TA, may be in contact with the second peripheral circuit pad **11***p***2**, and may be electrically connected to the second peripheral circuit pad **11***p***2**.

**[0081]** The third peripheral contact plug **87***c* may be spaced apart from the first and second gate layers **27***g* and **40***g*, may penetrate the first and second intermediate insulating layers **32** and **44**, and may be in contact with the first pattern layer **17***a*, and may be electrically connected to the first pattern layer **17***a*. In the pattern structure **17'**, the first pattern layer **17***a*, which may be formed as a polysilicon layer having N-type conductivity, may be a common source,

and the third peripheral contact plug **87***c* may be a common source contact plug electrically connected to the common source.

**[0082]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a spacer layer **65***b* covering a side surface of each of the first to third peripheral contact plugs **87***a*, **87***b*, and **87***c*.

**[0083]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include gate contact plugs in contact with the first and second gate pads **27***p* and **40***p* and electrically connected to the first and second gate pads **27***p* and **40***p*. Gate contact plugs **89** may penetrate the second upper insulating layer **73**, the capping layer **63** and the first upper insulating layer **58**, may extend into the second structure **21**', and may be in contact with the first and second gate pads **27***p* and **40***p*.

**[0084]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a third upper insulating layer **91** disposed on the second upper insulating layer **73**. The first, second, and third upper insulating layers **58**, **73**, and **91** may include silicon oxide.

**[0085]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include peripheral upper plugs **95***a*, **95***b*, and **95***c* penetrating the third upper insulating layer **91**. The peripheral upper plugs **95***a*, **95***b*, and **95***c* may further include a first peripheral upper plug **95***a* electrically connected to the first peripheral contact plug **87***a*, a second peripheral upper plug **95***b* electrically connected to the second peripheral contact plug **87***b*, and a third peripheral upper plug **95***c* electrically connected to the third peripheral contact plug **87***c*.

**[0086]** The first peripheral upper plug **95***a* may include a side surface not vertically aligned with the side surface of the first peripheral contact plug **87***a*. The second peripheral upper plug **95***b* may include a side surface not vertically aligned with a side surface of the second peripheral contact plug **87***b*. The third peripheral upper plug **95***c* may include a side surface not vertically aligned with a side surface of the third peripheral contact plug **87***c*.

**[0087]** A width of each of the first to third peripheral upper plugs **95***a*, **95***b*, and **95***c* may be different from a width of each of the first to third peripheral contact plugs **87***a*, **87***b*, and **87***c*. In one example, a width of each of the first to third peripheral upper plugs **95***a*, **95***b*, and **95***c* may be smaller than a width of each of the first to third peripheral contact plugs **87***a*, **87***b*, and **87***c*. In another example, a width of each of the first to third peripheral upper plugs **95***a*, **95***b* and **95***c* may be greater than a width of each of the first to third peripheral contact plugs **87***a*, **87***b* and **87***c*. The semiconductor device **1** according to an example embodiment of the present disclosure may further include a bit line contact plug **96***a* penetrating the first to third upper insulating layers **58**, **73**, and **71** and the capping layer **63**, and electrically connected to the memory vertical structure **47**.

**[0088]** The semiconductor device **1** according to an example embodiment of the present disclosure further may include gate upper plugs **96***b* penetrating the third upper insulating layer **91** and electrically connected to the gate contact plugs **89**.

**[0089]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include wirings **98***b*, **98***g*, **98***a*, and **98***c* disposed on the third upper insulating layer **91**. The wirings **98***b*, **98***g*, **98***a*, and **98***c* may include bit lines **98***b* electrically connected to the bit line contact plugs **96***a*, gate connection wirings **98***g* electrically connecting each of the gate upper plugs **96***b* to the plurality of second peripheral upper plugs **95***b*, a first peripheral wiring **98***a* electrically connected to the first peripheral upper plug **95***a*, and a second peripheral wiring **98***c* electrically connected to the third peripheral upper plug **95***c*.

**[0090]** Hereinafter, a level on which the upper surface of the uppermost gate layer among the first and second gate layers **27***g* and **40***g* is disposed may be referred to as a first level L**1**, a level on which the upper surface of the memory vertical structure **47** is disposed may be referred to as a second level L**2**, and a level on which the upper surface of the second upper insulating layer **73** is disposed may be referred to as a third level L**3**.

**[0091]** In the description below, examples of the first and second gate layers **27***g* and **40***g* and the memory vertical structure **47** described in the aforementioned example embodiment will be described with reference to FIG. **3**A. FIG. **3**A is an enlarged diagram illustrating region "A" in FIG. **2**A.

**[0092]** Referring to FIGS. **2**A and **3**A, the first and second gate layers **27***g* and **40***g* also just referred to as the gate layers may include one or a plurality of lower gate layers GL**1** and GL**2**, one or the plurality of upper gate layers GU**1** and GU**2**, and plurality of intermediate gate layers GM disposed between the one or the plurality of lower gate layers GL**1** and GL**2** and the one or the plurality of upper gate layers GU**1** and GU**2**. The one or the plurality of upper gate layers GU**1** and GU**2** may be spaced apart from each other in the vertical direction Z. For example, the plurality of upper gate layers GU**1** and GU**2** may include a first upper gate layer GU**1** and a second upper gate layer GU**2** disposed below the first upper gate layer GU**1**.

**[0093]** The one or the plurality of lower gate layers GL**1** and GL**2** may be spaced apart from each other in the vertical direction Z. For example, the plurality of lower gate layers GL**1** and GL**2** may include a first lower gate layer GL**1** and a second lower gate layer GL**2** disposed on the first lower gate layer GL**1**.

**[0094]** A portion of the plurality of intermediate gate layers GM may be word lines.

**[0095]** In one example, the first lower gate layer GL**1** may be a ground select gate line of a ground select transistor, and the second lower gate layer GL**2** may be a dummy gate line.

**[0096]** In another example, the first lower gate layer GL**1** may be an erase control gate line of an erase control transistor which may be used for an erase operation for removing data stored in memory cells using a gate induce drain leakage (GIDL) phenomenon, and the second lower gate layer GL**2** may be a ground select gate line of a ground select transistor.

**[0097]** In an example, the plurality of upper gate layers GU**1** and GU**2** may be string select gate lines of string select transistors.

**[0098]** In another example, the first upper gate layer GU**1** of the plurality of upper gate layers GU and GU**2** may be an erase control gate line of an erase control transistor, and the second upper gate layer can of the plurality of upper gate layers GU**1** and GU**2** may be a string select gate line of the string select transistor.

**[0099]** The memory vertical structure **47** may include a lower vertical portion **47**L penetrating the first stack structure **23'** and an upper vertical portion **47**U penetrating the second stack structure **35'**.

**[0100]** A width of an upper region of the lower vertical portion **47**L may be different from a width of a lower region of the upper vertical portion **47**U. For example, a width of an upper region of the lower vertical portion **47**L may be greater than a width of a lower region of the upper vertical portion **47**U. In other words, the width of the lower vertical portion **47**L where the lower vertical portion **47**L and the upper vertical portion **47**U meet may be greater than that of the upper vertical portion **47**U.

**[0101]** A side surface of the lower vertical portion **47**L and a side surface of the upper vertical portion **47**U, adjacent to each other, may not be aligned in the vertical direction Z.

**[0102]** A middle side surface of the memory vertical structure **47** disposed on a level between an uppermost first gate layer among the first gate layers **27***g* of the first stack structure **23'** and a lowermost second gate layer of the second gate layers **40***g* of the second stack structure **35'** may include a slope changing portion **47**V in which a slope may change.

**[0103]** In example embodiments of the present disclosure, the "slope changing portion" may be a side-surface portion of the memory vertical structure **47** having a third slope different from a first slope and a second slope between an upper side-surface portion having the first slope and a lower side-surface portion having the second slope. The third slope may be gentler (e.g., not as steep) than the first slope and the second slope, and the first slope and the second slope may be a vertical slope or an almost vertical slope. Therefore, the "slope changing portion" may be a portion having a gentle slope between the upper portion and the lower portion. For example, in the memory vertical structure **47**, the lower vertical portion **47**L may have a side surface having the first slope which may be vertical or almost vertical, the upper vertical portion **47**U may have a side surface having the second slope which may be vertical or almost vertical, and the slope changing portion **47**V may have a slope gentler than the first slope and the second slope.

**[0104]** On the same level as a level of the slope changing portion **47**V of the middle side surface of the memory vertical structure **47**, a side surface of each of the support vertical structure **61**, the first to third peripheral contact plugs **87***a*, **87***b*, and **87***c*, the separation structures **77**, and the dam structure **71**, described above, may have a substantially linear shape or a monotonically changing shape with regularity.

**[0105]** The memory vertical structure **47** may include an insulating gap-fill layer **53**, a channel layer **51** covering an external side surface and a bottom surface of the insulating gap-fill layer **53**, a data storage structure **49** covering an external side surface and a bottom surface of the channel layer **51**, and a pad material layer **55** on the insulating gap-fill layer **53**.

**[0106]** The data storage structure **49** may include a first dielectric layer **49***c* covering the external side surface and the bottom surface of the channel layer **51**, a data storage material layer **49***b* covering the external side surface and the bottom surface of the first dielectric layer **49***c*, and a second dielectric layer **49***a* covering the external side surface and the bottom surface of the storage material layer **49***b*. The first dielectric layer **49***c* may be in contact with the channel layer **51**, and the data storage material layer **49***b* may be spaced apart from the channel layer **51**. The insulating gap-fill layer **53** may include silicon oxide, such as for example, silicon oxide formed by an atomic layer deposition process, or silicon oxide having voids formed therein. The first dielectric layer **49***a* may include silicon oxide or silicon oxide doped with impurities. The second dielectric layer **49***c* may include at least one of silicon oxide and a high-k dielectric. The data storage material layer **49***b* may include a material for trapping charges and storing data, such as, for example, silicon nitride.

**[0107]** The data storage material layer **49***b* of the data storage structure **49** of the memory vertical structure **47** may include regions for storing data in a semiconductor device such as a flash memory device. The channel layer **51** may include polysilicon. The pad material layer **55** may include at least one of doped polysilicon, metal nitride (e.g., TiN, or the like), a metal (e.g., W, or the like), and a metal-semiconductor compound (e.g., TiSi, or the like). The pad material layer **55** may be electrically connected to and in contact with the bit line contact plug **96***a*.

**[0108]** The memory vertical structure **47** may penetrate the third pattern layer **17***c* and the second pattern layer **17***b'* of the pattern structure **17'** in order, and may extend into the first pattern layer **17***a*. In the pattern structure **17'**, the second pattern layer **17***b'* may penetrate the data storage structure **49** and may be in contact with the channel layer **51**.

**[0109]** The semiconductor device **1** according to an example embodiment of the present disclosure may further include a dielectric layer **56** covering an upper surface and a lower surface of each of the first and second gate layers **27***g* and **40***g* and disposed between a side surface of the memory vertical structure **47** and a side surface of each of the first and second gate layers **27***g* and **40***g*. The dielectric layer **56** may include a high-k dielectric having a dielectric constant higher than that of silicon oxide. For example, the dielectric layer **56** may be formed of a high-k dielectric such as aluminum oxide, lanthanum oxide, or hafnium oxide.

**[0110]** In the description below, with reference to FIG. **3**B, an example of the support vertical structure **61** and the capping layer **63** described above will be described. FIG. **3**B is an enlarged diagram illustrating region "B" in FIG. **2**B.

**[0111]** Referring to FIGS. **2**B and **3**B, as described above, the support vertical structure **61** may include the air gap **69***a* and the support layer **65***a* defining at least a portion of the air gap **69***a*, and the capping layer **63** may include the lower capping layer **65***c* and the upper capping layer **67**. For example, the support layer **65***a* may limit at least a lower portion and a sidewall of the air gap **69***a*.

**[0112]** The support layer **65***a* may extend continuously from the lower capping layer **65***c*. The upper capping layer **67** may limit an upper portion of the air gap **69***a*.

**[0113]** The lower capping layer **65***c* and the support layer **65***a* may be formed of the same material. The lower capping layer **65***c* and the support layer **65***a* may be integrated with each other. For example, the lower capping layer **65***c* and the support layer **65***a* may be formed of a material layer continuously extending without a boundary surface. For example, the lower capping layer **65***c* and the support layer **65***a* may include an insulating material layer.

**[0114]** In an example, the lower capping layer **65***c* and the support layer **65***a* may be formed of a silicon oxide layer.

**[0115]** In another example, the lower capping layer **65***c* and the support layer **65***a* may be formed of a silicon nitride layer.

**[0116]** In another example, the lower capping layer **65***c* and the support layer **65***a* may be formed in a multilayer structure, such as, for example, a multilayer structure of a silicon oxide layer and a silicon nitride layer.

**[0117]** A maximum thickness of the lower capping layer **65***c* may be greater than a minimum thickness of the support layer **65***a*. The support layer **65***a* may have a maximum thickness in a portion adjacent to the lower capping layer **65***c*. be support layer **65***a* may have a minimum thickness in a portion far from the lower capping layer **65***c*.

**[0118]** The upper capping layer **67** may include a material layer formed by a method different from a method of forming the lower capping layer **65***c*. For example, the lower capping layer **65***c* may include a silicon oxide layer formed by an atomic layer deposition process (ALD), and the upper capping layer **67** may include a silicon oxide layer formed by a chemical vapor deposition process (CVD).

**[0119]** In one example, an upper end of the air gap **69***a* may be disposed on a level higher than a level of the upper surface of the memory vertical structure **47**. In one example, the air gap **69***a* may extend upwardly from a portion disposed in the support hole **60***s*, and an upper end **69***t* of the air gap **69***a* may be disposed on a level higher than a level of the upper surface of the first upper insulating layer **58**. The upper end **69***t* of the air gap **69***a* may come to point and be narrower than other portions of the air gap **69***a* therebelow.

**[0120]** In an example, the upper end **69***t* of the air gap **69***a* may be disposed on a level higher than a level of the upper surface of the lower capping layer **65***c*.

**[0121]** In the description below, examples of the peripheral contact plugs **87**, the first to third peripheral upper plugs **95***a*, **95***b*, and **95***c*, and the spacer layer **65***b*, and the gate contact plugs **89**, described above, will be described with reference to FIGS. **3**C and **3**D. FIG. **3**C is an enlarged diagram illustrating regions "C**1**" and "C**2**" in FIG. **2**A, and FIG. **3**D is an enlarged diagram illustrating region "D" in FIG. **2**A.

**[0122]** Referring to FIGS. **2**A, **3**C and **3**D, each of the peripheral contact plugs **87** may include a lower region **87**LS disposed below a first level L**1** and an upper region **87**US disposed above the first level L**1**. For example, in each of the peripheral contact plugs **87**, the upper region **87**US may be disposed on a level higher than a level of the upper surface of the uppermost gate layer **40***g* among the first and second gate layers **27***g* and **40***g*, the lower region **87**LS may be disposed on a level lower than a level of the upper surface of the uppermost gate layer **40***g*.

**[0123]** In the description below, the lower region **87**LS and the upper region **87**US of one of the peripheral contact plugs **87** will be mainly described.

**[0124]** A side-surface profile of the lower region **87**LS may be different from a side-surface profile of the upper region **87**US. For example, the lower region **87**LS may have a substantially vertical side surface, and the upper region **87**US may have at least one curved side surface. For example, the upper region **87**US may include a first region **87**US_**1**, a connection region **87**US_**2** disposed below the first region **87**US_**1**, and a second region **87**US_**3** disposed below the connection region **87**US_**2**. A side surface of the connection region **87**US_**2** may have a slope different from at least one of a side surface of the first region **87**US_**1** and a side surface of the second region **87**US_**2**. For example, a side surface of the connection region **87**US_**2** may have a slope different from a side surface of the first region **87**US_**1** having a first slope and a side surface of the second region **87**US_**2** having a second slope. For example, the side surface of the first region **87**US_**1** and the side surface of the second region **87**US_**2** may have a vertical slope or an almost vertical slope which may be steep, and the side surface of the connection region **87**US_**2** may have a gentle slope. In example embodiments of the present disclosure, the expression "substantially perpendicular" may indicate the configuration of being substantially perpendicular to the upper surface of the lower structure **3** or the upper surface of the semiconductor substrate **4**. For example, forming the plug may include forming a hole by an anisotropic etching process and forming a plug in the hole, and the side surface profile of the plug may be a side-surface profile of the hole formed by the anisotropic etching process. The side surface of the hole formed by the anisotropic etching process may be perpendicular to or may be almost perpendicular to the upper surface of the semiconductor substrate **4**. Accordingly, the expression "substantially perpendicular" may indicate the configuration of being perpendicular to the upper surface of the semiconductor substrate **4**, but the present disclosure is not limited thereto, and the expression may refer to a shape of a side surface of the hole formed within a range of a process margin of an anisotropic etching process, which may be, for example, a shape almost perpendicular to the upper surface of the semiconductor substrate **4**, such as a shape almost perpendicular to the upper surface of the semiconductor substrate **4** and having a constant slope or a shape almost perpendicular to the upper surface of the semiconductor substrate **4** and having a slope that changes.

**[0125]** At least a portion of the first region **87**US_**1** may be in contact with the second upper insulating layer **73** and the upper capping layer **67**.

**[0126]** The first region **87**US_**1** may be in contact with the second upper insulating layer **73**, the upper capping layer **67**, and the lower capping layer **65***c*. The first region **87**US_**1** may extend from the connection region **87**US_**2** and contact the lower capping layer **65***c*, the upper capping **67** and the second upper insulating layer **73** in sequence.

**[0127]** The side surface of the first region **87**US_**1** and the side surface of the second region **87**US_**3** may not be aligned in the vertical direction Z.

**[0128]** At least a portion of the connection region **87**US_**2** may be disposed on a level lower than that of the lower capping layer **65***c*.

**[0129]** At least a portion of the connection region **87**US_**2** may be disposed on a level higher than that of the second level L**2**.

**[0130]** A maximum width of the upper region **87**US may be greater than a maximum width of the lower region **87**LS.

**[0131]** In the upper region S7US, the first region **87**US_**1** may have a minimum width greater than a minimum width of the connection region **87**US_**2**, and the second region **87**US_**3** may have a maximum width less than a maximum width of the connection region **87**US_**2**.

**[0132]** The gate contact plugs **89** disposed on the same level as a level of the upper region **87**US may have a side-surface profile different from that of the upper region **87**US. For example, each region of the gate contact plugs **89** disposed on the same level as a level of the upper region

**87**US of the peripheral contact plug **87** may have a side surface having a substantially vertical slope.

**[0133]** The spacer layer **65***b* may surround a side surface of the lower region **87**LS, may extend upwardly, and may cover a portion of a side surface of the upper region **87**US. For example, the spacer layer **65***b* may cover a side surface of the second region **87**US_**3** of the upper region **87**US, and may be disposed on a level lower than the first region **87**US_**1** of the upper region **87**US and may be spaced apart from the first region **87**US_**1**.

**[0134]** The spacer layer **65***b* may cover at least a portion of the connection region **87**US_**2** of the upper region **87**US. For example, the spacer layer **65***b* may cover a side surface of a lower portion of the connection region **87**US_**2** and may not cover a side surface of an upper portion of the connection region **87**US_**2**.

**[0135]** Each of the first to third peripheral upper plugs **95***a*, **95***b*, and **95***c* may have a width different from each of the peripheral contact plugs **87**. For example, a width of each of the first to third peripheral upper plugs **95***a*, **95***b* and **95***c* may be smaller than a width of each of the peripheral contact plugs **87**.

**[0136]** Each of the peripheral contact plugs **87** may include a plug pattern **87_2** and a conductive liner **87_1** covering a side surface and a bottom surface of the plug pattern **87_2**. Each of the gate contact plugs **89** may include a plug pattern **89_2** and a conductive liner **89_1** covering a side surface and a bottom surface of the plug pattern **89_2**.

**[0137]** In an example, the peripheral contact plugs **87** and the gate contact plugs **89** may be simultaneously formed. Accordingly, the peripheral contact plugs **87** and the gate contact plugs **89** may be formed of the same material.

**[0138]** In an example, upper surfaces of the peripheral contact plugs **87** may be coplanar with upper surfaces of the gate contact plugs **89**. For example, the upper surfaces of the peripheral contact plugs **87** and the gate contact plugs **89** may be disposed on the third level L**3**.

**[0139]** In example embodiments of the present disclosure, the bit line contact plug **96***a*, the gate upper plugs **96***b*, and the first to third peripheral upper plugs **95***a*, **95***b*, and **95***c* may be formed simultaneously and may include the same material. For example, each of the bit line contact plug **96***a*, the gate upper plugs **96***b*, and the first to third peripheral upper plugs **95***a*, **95***b* and **95***c* may include a plug pattern **95_2** and a conductive liner **95_1** covering a bottom surface and a side surface of the plug pattern **95_2**. The conductive line **95_1** may be in direct contact with the peripheral contact plug **87** or the gate contact plug **89** therebelow. The bit line contact plug **96***a*, the gate upper plugs **96***b*, and the first to third peripheral upper plugs **95***a*, **95***b*, and **95***c* may have upper surfaces coplanar with each other.

**[0140]** In the description below, various modifications of the support vertical structure **61** and the capping layer **63** described above will be described with reference to FIGS. **4**A, **4**B, **5**A and **5**B. FIGS. **4**A, **4**B, **5**A and **5**B are enlarged diagrams illustrating a modified portion of the example in the enlarged diagram in FIG. **3**B. Various modified structures described below with reference to FIGS. **4**A, **4**B, **5**A, and **5**B may replace the structure in FIG. **3**B.

**[0141]** In a modified example, referring to FIG. **4**A, the lower capping layer **65***c* described with reference to FIG. **3**B may be replaced with a lower capping layer **65***c*' including a first layer **65***c***1** and a second layer **65***c***2** on the first layer **65***c***1**. The support layer **65***a* described with reference to FIG. **3**B may be replaced with a support layer **65***a*' including a first layer **65***a***1** and a second layer **65***a***2** on the first layer **65***a***1**. The first layer **65***a***1** of the support layer **65***a*' and the first layer **65***c***1** of the lower capping layer **65***c*' may be integrated with each other, and the second layer **65***a***2** of the support layer **65***a*' and the second layer **65***c***2** of the lower capping layer **65***c*' may be integrated with each other.

**[0142]** In an example, the first layers **65***a***1** and **65***c***1** and the second layers **65***a***2** and **65***c***2** may be formed as material layers having different step coverages. For example, one of the first layers **65***a***1** and **65***c***1** and the second layers **65***a***2** and **65***c***2** may have a step coverage higher than the other. For example, one of the first layers **65***a***1** and **65***c***1** and the second layers **65***a***2** and **65***c***2** may be formed to have a uniform thickness as compared to a thickness of the other layer.

**[0143]** In an example, the first layers **65***a***1** and **65***c***1** and the second layers **65***a***2** and **65***c***2** may be formed of the same type of material. For example, the first layers **65***a***1** and **65***c***1** may be formed of a silicon oxide layer having a uniform thickness as compared to that of the second layers **65***a***2** and **65***c***2**, and the second layers **65***a***2** and **65***c***2** may be formed of silicon oxide layer having a non-uniform thickness as compared to that of the first layers **65***a***1** and **65***c***1**. In another example, the first layers **65***a***1** and **65***c***1** and the second layers **65***a***2** and **65***c***2** may be formed of different materials. For example, the first layers **65***a***1** and **65***c***1** may be formed of a silicon oxide layer, and the second layers **65***a***2** and **65***c***2** may be formed of a different material from the silicon oxide layer, such as, for example, a silicon nitride layer, a silicon oxynitride layer, or a silicon nitride layer including carbon. The spacer layer **65***b* (in FIG. **3**C) described above may be formed of the same material as that of the support layer **65***a*'. Accordingly, the spacer layer **65***b* (in FIG. **3**C) may be modified to include the same first layer and the second layer as those of the support layer **65***a'*.

**[0144]** In another modified example, referring to FIG. **4**B, the capping layer **63** including the lower capping layer **65***c* and the upper capping layer **67** described with reference to FIG. **3**B, and the support layer **65***a* may be replaced by a capping layer **63'** and a support layer **65***a*'', which may limit the air gap **69***a* by a single material layer. For example, the support layer **65***a*'' may be integrated with the capping layer **63'**. For example, in FIG. **3**B, the upper capping layer **67** formed by a process different from the process of forming the support layer **65***a* may limit an upper portion of the air gap **69***a*, but in FIG. **4**B, the capping layer **63'** formed by the same process as the process of forming the support layer **65***a*'' may limit an upper portion of the air gap **69***a*.

**[0145]** In another modified example, referring to FIG. **5**A, the support vertical structure **61** described with reference to FIG. **3**B may be replaced with a support vertical structure **61'** including an air gap **69***a*', a support layer **65***a* defining a portion of the air gap **69***a*', and an upper gap-fill layer **67***a* defining an upper portion of the air gap **69***a*'. The capping layer **63** including the lower capping layer **65***c* and the upper capping layer **67** described with reference to FIG. **3**B may be replaced with a capping layer **63'** including an upper capping layer **67'** extending from the upper gap-fill layer **67***a*.

**[0146]** In an example, the upper end **69***t*' of the air gap **69'** may be lower than the second level L**2**, and may be higher than the first level L**1**. In this case, the upper gap-fill layer

**67***a* may be provided on the upper end **69***t*' of the air gap **69**' between the first level L**1** and the second level L**2**.

**[0147]** In another modified example, referring to FIG. **5**B, the support vertical structure **61**' described with reference to FIG. **3**A may be replaced with a support vertical structure **61**" including an air gap **69***a*" having an upper end **69***t*" lower than the first level L**1**, a support layer **65***a* defining a portion of the air gap **69***a*", and an upper gap-fill layer **67***a*' defining an upper portion of the air gap **69***a*".

**[0148]** In the description below, various modified examples of the peripheral contact plug **87** and/or the spacer layer **65***b* described above will be described with reference to FIGS. **6**A, **6**B, **7**A and **7**B. FIGS. **6**A, **6**B, **7**A and **7**B are enlarged diagrams illustrating a modified portion of the example in the enlarged diagram in FIG. **3**C. Various modified structures described below with reference to FIGS. **6**A, **6**B, **7**A and **7**B may replace the structure in FIG. **3**C.

**[0149]** In a modified example, referring to FIG. **6**A, in the peripheral contact plug **87** including the lower region **87**LS and the upper region **87**US described with reference to FIG. **3**C, the upper region **87**US may be replaced with the same shape as that of the upper region **87**US' in FIG. **6**A.

**[0150]** The upper region **87**US' may include a second region **87**US_**3**', a connection region **87**US_**2**' on the second region **87**US_**3**', and a first region **87**US_**1**' on the connection region **87**US_**2**'. The connection region **87**US_**2**' may have a concave side surface. For example, in the upper region **87**U', the connection region **87**US_**2**' may have a concave side surface in a direction toward a center of the upper region **87**U' as compared to the first and second regions **87**US_**1**' and **87**US_**3**'. In the upper region **87**U', a minimum width of the connection region **87**US_**2**' may be smaller than a width of the second region **87**US_**3**' adjacent to the connection region **87**US_**2**'.

**[0151]** In the upper region **87**US', a minimum width of the connection region **87**US_**2**' may be smaller than a minimum width of the first region **87**US_**1**'.

**[0152]** In the upper region **87**US', a width of the first region **87**US_**1**' may be greater than a width of the second region **87**US_**3**'.

**[0153]** The spacer layer **65***b* described with reference to FIG. **3**C may be replaced with a spacer layer **65***b*' which may not cover the lower region **87**LS and may cover the side surface of the connection region **87**US_**2**'. For example, the spacer layer **65***b*' may fill the concave side surface of the connection region **87**US_**2**'.

**[0154]** In a modified example, referring to FIG. **6**B, the spacer layer **65***b* describes with reference to FIG. **3**C may not be provided. For example, the peripheral contact plugs **87** may include a portion in direct contact with the second structure **21**'.

**[0155]** In a modified example, referring to FIG. **7**A, in the peripheral contact plug **87** including the lower region **87**LS and the upper region **87**US described with reference to FIG. **3**C, the upper region **87**US may be replaced with the same shape as that of the upper region **87**USa in FIG. **7**A.

**[0156]** The upper region **87**USa may include a second region **87**US_**3***a*, a connection region **87**US_**2***a* on the second region **87**US_**3***a*, and a first region **87**US_**1***a* on the connection region **87**US_**2***a*.

**[0157]** In the upper region **87**USa, a minimum width of the first region **87**US_**1***a* may be smaller than a maximum width of the connection region **87**US_**2***a*, a maximum width of the second region **87**US_**3***a* may be greater than a minimum width of the connection region **87**US_**2***a*, and the maximum width of the second region **87**US_**3***a* may be greater than the maximum width of the first region **87**US_**1***a*. The spacer layer **65***b* described with reference to FIG. **3**C may be continuously connected to and integrated with the capping layer **65***c*.

**[0158]** In a modified example, referring to FIG. **7**B, in the peripheral contact plug **87** including the lower region **87**LS and the upper region **87**US described with reference to FIG. **3**C, the upper region **87**US may be replaced with the same shape as that of the upper region **87**USb in FIG. **7**B, and the spacer layer **65***b* described with reference to FIG. **3**C may be replaced by a spacer layer **65***b*" as in FIG. **7**B.

**[0159]** The upper region **87**USb may include a second region **87**US_**3***b*, a connection region **87**US_**2***b* on the second region **87**US_**3***b*, and a first region **87**US_**1***b* on the connection region **87**US_**2***b*, and a width of the first region **87**US_**1***b* may be smaller than a width of the second region **87**US_**3***b*. The connection region **87**US_**2***b* may have a tapered shape that narrows as it approaches the first region **87**US_**1***b*.

**[0160]** The spacer layer **65***b*" may cover at least a portion of the side surface of the connection region **87**US_**2***b*. The spacer layer **65***b*" may not cover an entire side surface of the second region **87**US_**3***b* or may not cover a portion of the side surface of the second region **87**US_**3***b*. The peripheral contact plug **87** disposed below the spacer layer **65***b*" may include a portion in contact with the second structure **21**'. The spacer layer **65***b*" may be continuously connected to and integrated with the lower capping layer **65***c*.

**[0161]** In a modified example, referring to FIG. **7**C, in the peripheral contact plug **87** including the lower region **87**LS and the upper region **87**US described with reference to FIG. **3**C, the upper region **87**US may be replaced with the upper region **87**USc extending from the lower region **87**LS to have a constant width or to have a monotonically changing width. For example, the side surface of the peripheral contact plug **87** including the lower region **87**LS and the upper region **87**USc may have a substantially linear shape or a monotonically changing shape with regularity.

**[0162]** In the description below, a modified example of the peripheral contact plug **87** described above will be described with reference to FIG. **8**A. FIG. **8**A is an enlarged diagram illustrating a modified portion of the example in the enlarged diagram in FIG. **3**C. The modified structure of the peripheral contact plug **87** described below with reference to FIG. **8**A may replace the structure of the peripheral contact plug **87** in FIG. **3**C and also the structure of the peripheral contact plug **87** described with reference to FIGS. **6**A to **7**C.

**[0163]** In the modified example, referring to FIG. **8**A, the peripheral contact plug **87** described with reference to FIG. **3**C or the peripheral contact plug **87** described with reference to FIGS. **6**A to **7**C may be replaced with a peripheral contact plug **87**' further including an air gap **87**_**3**. For example, the peripheral contact plug **87**' may include a plug pattern **87**_**2**, a conductive liner **87**_**1** covering a side surface and a bottom surface of the plug pattern **87**_**2**, and an air gap **87**_**3** in the plug pattern **87**_**2**.

**[0164]** In the peripheral contact plug **87**', an upper end of the air gap **87**_**3** may be lower than the second level L**2**.

**[0165]** In the peripheral contact plug **87**', an upper end of the air gap **87**_**3** may be higher than the first level L**1**.

**[0166]** In the description below, a modified example of the peripheral contact plug **87** described above will be described

with reference to FIG. **8**B. FIG. **8**B is an enlarged diagram illustrating a modified portion of the example in the enlarged diagram in FIG. **7**A. The modified structure of the peripheral contact plug **87** described below with reference to FIG. **8**B may replace the structure of the peripheral contact plug **87** in FIG. **7**A, and also the structure of the peripheral contact plug **87** described with reference to FIGS. **3**C, **6**A, **6**B, **7**B, and **7**C.

**[0167]** In a modified example, referring to FIG. **8**B, the peripheral contact plug **87** described with reference to FIG. **7**A or the peripheral contact plug **87** described with reference to FIGS. **3**A, **6**A, **6**B, **7**B and **7**C may be replaced with a peripheral contact plug **87"** further including a lower air gap **87_3** and an upper air gap **87_4**. For example, the peripheral contact plug **87"** may include a plug pattern **87_2**, a conductive liner **87_1** covering a side surface and a bottom surface of the plug pattern **87_2**, and the lower air gap **87_3** and the upper air gap **87_4** disposed in the plug pattern **87_2** and spaced apart from each other. In other words, the lower air gap **87_3** and the upper air gap **87_4** constitute two separate air gaps.

**[0168]** In the peripheral contact plug **87"**, an upper end of the lower air gap **87_3** may be lower than the second level L**2**.

**[0169]** In the peripheral contact plug **87"**, the upper end of the lower air gap **87_3** may be higher than the first level L**1**.

**[0170]** In the peripheral contact plug **87"**, the upper air gap **87_4** may be higher than the second level L**2**. An upper end of the upper air gap **87_4** may be lower than the third level L**3**. In the alternative, the upper end of the upper air gap **87_4** may be higher than the third level L**3**.

**[0171]** In the description below, a modified example of the above-described peripheral contact plug **87** will be described with reference to FIGS. **9**A and **9**B. FIG. **9**A is an enlarged diagram illustrating a modified portion of the example in the enlarged diagram in FIG. **3**C, and FIG. **9**B is an enlarged diagram illustrating a modified portion of the example in the enlarged diagram in FIG. **7**A. The modified structure of the peripheral contact plug **87** described below with reference to FIGS. **9**A and **9**B, a structure in which the level of the upper surface is increased, for example, may be reflected in the structure of the peripheral contact plug **87** in FIGS. **3**C and **7**A and also in the peripheral contact plugs **87**, **87'** and **87"** described with reference to FIGS. **6**A, **6**B, **7**B, **7**C, **8**A, and **8**B. For example, the level of the upper surfaces of the peripheral contact plugs **87**, **87'**, and **87"** described with reference to FIGS. **6**A, **6**B, **7**B, **7**C, **8**A, and **8**B may be modified to increase.

**[0172]** In a modified example, referring to FIG. **9**A, the peripheral contact plug **87** including the upper region **87**US described with reference to FIG. **3**C may be replaced with a peripheral contact plug **187** including an upper region **187**USa including an upper surface disposed on a higher level than previously described peripheral contact plugs. The peripheral contact plug **187** may include a lower region **187**LS substantially the same as the lower region **87**LS described with reference to FIG. **3**C.

**[0173]** The upper region **187**USa may include a second region **187**US_**3***a* and a connection region **187**US_**2***a* substantially the same as the second region **87**US_**3** and the connection region **87**US_**2** described with reference to FIG. **3**C, and may include a first region **187**US_**1***a* disposed on a level higher than a level of the first region **87**US_**1** described with reference to FIG. **3**C.

**[0174]** The upper region **187**USa may have an upper surface coplanar with the upper surface of the third upper insulating layer **91**. The upper surface of the upper region **187**USa of the peripheral contact plug **187** may be higher than the third level L**3**.

**[0175]** The peripheral contact plug **187** may have upper surfaces disposed on a level higher than upper surfaces of the gate contact plugs **89** (in FIG. **2**A).

**[0176]** In a modified example, referring to FIG. **9**B, the peripheral contact plug **87** including the upper region **87**USa described with reference to FIG. **7**A may be replaced with a peripheral contact plug **187** including an pp region **187**USb having an upper surface disposed on a higher level than some of the previously described peripheral contact plugs.

**[0177]** Similarly to the upper region **187**USa described with reference to FIG. **9**A, the upper region **187**USb may include a second region **187**US_**3***b* and a connection region **187**US_**2***b*, which may be substantially the same as the second region **87**US_**3***a* and the connection region **87**US_**2***a* described with reference to FIG. **7**A, and may include a first region **187**US_**1***b* disposed on a level higher than a level of the first region **87**US_**1***a* described with reference to FIG. **7**A. The first region **187**US_**1***b* of FIG. **9**B may be narrower than the first region **187**US_**1***a* of FIG. **9**A.

**[0178]** In the description below, a modified example of the gate contact plug **89** described above will be described with reference to FIGS. **10**A and **10**B. FIGS. **10**A and **10**B are enlarged diagrams illustrating a modified portion of the example in the enlarged diagram in FIG. **3**D.

**[0179]** In a modified example, referring to FIG. **10**A, the gate contact plug **89** described with reference to FIG. **3**D may be replaced with a gate contact plug **189***a* having an upper surface disposed on a lower level than the gate contact plug **89**. The gate contact plug **189***a* may have an upper surface coplanar with the upper surface of the capping layer **63**. In other words, the upper surface of the gate contact plug **189***a* may not extend beyond the second upper insulating layer **73**. Accordingly, the upper surface of the gate contact plug **189***a* may be disposed on a level lower than a level of the upper surfaces of the peripheral contact plugs **87**, **87'**, **87"**, and **187** of the various examples described in FIGS. **3**C, **6**A, **6**B, **7**A, **7**B, **7**C, **8**A, **8**B, **9**A, and **9**B.

**[0180]** In a modified example, referring to FIG. **10**B, the gate contact plug **89** described with reference to FIG. **3**D may be replaced with a gate contact plug **189***b* having an upper surface disposed on a higher level than the gate contact plug **89**. The gate contact plug **189***b* may have an upper surface coplanar with an upper surface of the third upper insulating layer **91**. In this case, the upper surface of the gate contact plug **189***a* may extend beyond the second upper insulating layer **73**. For example, the gate contact plug **189***b* may have an upper surface coplanar with the upper surface of the peripheral contact plug **187** of the various examples described with reference to FIGS. **9**A and **9**B.

**[0181]** A modified example of a semiconductor device according to an example embodiment will be described with reference to FIGS. **11**A, **11**B and **12**. FIG. **11**A is a cross-sectional diagram illustrating a cross-sectional structure taken in a first direction X, FIG. **11**B is a cross-sectional diagram illustrating a cross-sectional structure taken in a second direction Y perpendicular to the first direction X, and FIG. **12** is an enlarged diagram illustrating regions "E**1**" and "E**2**" in FIG. **11**A.

**[0182]** Referring to FIGS. **11**A, **11**B, and **12**, a semiconductor device **200** according to an example embodiment of the present disclosure may include a first structure **203** and a second structure **221'** overlapping the first structure **203** in the vertical direction Z.

**[0183]** The first structure **203** may include a pattern structure **217**. The pattern structure **217** may include at least one silicon layer. The pattern structure **217** may be substantially the same as the pattern structure **17'** in FIGS. **2**A and **2**B.

**[0184]** The first structure **203** may include a semiconductor substrate **204**, a peripheral circuit **208** on the semiconductor substrate **204**, and a lower insulating layer **213** covering the peripheral circuit **208** on the semiconductor substrate **204**. The peripheral circuit **208** may include a circuit device **209** such as a transistor including a peripheral gate **209***a* and a peripheral source/drain **209***b*, and a circuit interconnection **211** electrically connected to the circuit device **209**. A portion of the circuit interconnection **211** may be first and second peripheral circuit pads **211***p***1** and **211***p***2**. The pattern structure **217** may be disposed on the lower insulating layer **213**. The pattern structure **217** may further include a ground pattern **218**. For example, the ground pattern **218** may be disposed below the pattern structure **217** and may be grounded to the semiconductor substrate **204** through a portion of the circuit interconnection **211**.

**[0185]** The first structure **203** may further include internal insulating layers **219***a* penetrating the pattern structure **217** and an external insulating layer **219***b* disposed on an external side of the pattern structure **217**.

**[0186]** The second structure **221'** may include a memory cell region MCA and a staircase region SA. The second structure **221'** may include stack structures **223'** and **235'** disposed in the memory cell region MCA and extending from the memory cell region MCA into the staircase region SA.

**[0187]** The stack structures **223'** and **235'** may include a first stack structure **223'** and a second stack structure **235'** on the first stack structure **223'**. The first stack structure **223'** may include first interlayer insulating layers **225** and first gate layers **227***g* alternately stacked in the vertical direction Z. The first gate layers **227***g* may have gate pads GP arranged in a staircase shape in the staircase region SA. The second stack structure **225'** may include second interlayer insulating layers **238** and second gate layers **240***g* alternately stacked in the vertical direction Z. The second gate layers **240***g* may have gate pads GP arranged in a staircase shape in the staircase region SA.

**[0188]** The first interlayer insulating layers **225** and the second interlayer insulating layers **238** may form interlayer insulating layers **225** and **238**, and the first gate layers **227***g* and the second gate layers **240***g* may form gate layers **227***g* and **240***g*. The gate pads GP of the gate layers **227***g* and **240***g* may have a thickness greater than a thickness of each of the gate layers **227***g* and **240***g* disposed in the memory cell array region MCA. The gate layers **227***g* and **240***g* may be formed of substantially the same material as that of the gate layers **27***g* and **40***g* in FIGS. **2**A and **2**B.

**[0189]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include a memory vertical structure **47** penetrating the second structure **221'**. The memory vertical structure **47** may be substantially the same as the memory vertical structure **47** in FIGS. **2**A **2**B, and **3**A, and the pattern structure **217** in contact with the memory vertical structure **47** may be substantially the same as the pattern structure **17** in FIGS. **2**A, **2**B and **3**A.

**[0190]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include a first upper insulating layer **258** on the second structure **221'**. The first upper insulating layer **258** may include silicon oxide.

**[0191]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include support holes **60***s* penetrating the first upper insulating layer **258** and the second structure **221'** and exposing a portion of the pattern structure **217**, and support vertical structures **61** disposed in the support holes **60***s*. The support vertical structures **61** may be substantially the same as one of the support vertical structures **61** and **61'** described in reference to FIGS. **2**B, **2**C, **3**B, **4**A, **4**B, **5**A and **5**B, the support vertical structure **61** described with reference to FIG. **3**B, for example. For example, as described with reference to FIG. **3**B, the support vertical structure **61** may include an air gap **69***a* and a support layer **65***a* defining at least a portion of the air gap **69***a*.

**[0192]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include a capping layer **263** disposed on the first upper insulating layer **258** and covering the support vertical structure **61**. Similarly to the capping layer **63** described with reference to FIGS. **1** to **3**D, the capping layer **263** may include a lower capping layer **265***c* and an upper capping layer **267** on the lower capping layer **265***c*.

**[0193]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include a second upper insulating layer **273** on the capping layer **263**.

**[0194]** A level on which an upper surface of an uppermost gate layer among the gate layers **227***g* and **240***g* is disposed may be a first level L**1**, a level on which an upper surface of the memory vertical structure **47** is disposed may be a second level L**2**, and a level on which an upper surface of the second upper insulating layer **273** is disposed may be a third level L**3**.

**[0195]** The semiconductor device **200** according to an example embodiment may include separation structures **77** penetrating the second upper insulating layer **273**, the capping layer **263**, the first upper insulating layer **258**, and the second structure **221'**. The separation structures **277** may be substantially the same as the separation structures **77** in FIGS. **1** and **2**C.

**[0196]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include peripheral contact plugs **287**. The peripheral contact plugs **287** may include a first peripheral contact plug **287***a* and a second peripheral contact plug **287***b*. The peripheral contact plugs **287** may penetrate the second upper insulating layer **273**, the capping layer **263**, the first upper insulating layer **258**, and the second structure **221'**, and may extend into the lower structure **203**.

**[0197]** The first peripheral contact plug **287***a* may be spaced apart from the first and second gate layers **227***g* and **240***g*, may penetrate intermediate insulating layers **232** and **244**, may be in contact with the first peripheral circuit pad **211***p***1**, and may be electrically connected to the first peripheral circuit pad **211***p***1**.

**[0198]** The second peripheral contact plug **287***b* may be spaced apart from the first and second gate layers **227***g* and **240***g*, may penetrate the intermediate insulating layers **232** and **244**, and may be in contact with and electrically connected to the pattern structure **217**.

**[0199]** The peripheral contact plugs **287** may have the same structure as that of one of the structures of the peripheral contact plugs **87**, **87'**, **87''**, and **187** of the various examples described in reference to FIGS. **3**C, **6**A, **6**B, **7**A, **7**B, **7**C, **8**A, **8**B, **9**A, and **9**B. For example, the peripheral contact plugs **287** may have substantially the same structure as that of the peripheral contact plug **87** described with reference to FIG. **6**B. For example, the peripheral contact plug **287** may include a lower region **287**US and an upper region **287**US, and the upper region **287**US may include a first region **287**US_**1**, a second region **287**US_**3**, and a connection region **287**US_**2** corresponding to the first region **87**US_**1** (in FIG. **6**B), the second region **87**US_**3** (in FIG. **6**B), and the connection region **87**US_**2** (in FIG. **6**B), respectively.

**[0200]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include gate contact plugs **289**. The gate contact plugs **289** may penetrate the second upper insulating layer **273**, the capping layer **263**, the first upper insulating layer **258**, and the second structure **221'**, and may extend into the lower structure **203**. The gate contact plugs **289** may penetrate the gate pads GP of the gate layers **227***g* and may also penetrate the gate layers **227***g* and **240***g*, and may be in contact with the gate pads GP and may be electrically connected to the gate pads GP. The gate contact plugs **289** may be electrically connected to the second peripheral circuit pads **211***p***2** in the lower structure **203**.

**[0201]** The gate contact plugs **289** may be in contact with the gate pads GP and may be spaced apart from the other gate layers **227***g* and **240***g*. For example, one of the gate contact plugs **289** may be in contact with the gate pad GP of one of the gate layers **227***g* and **240***g*, and may be spaced apart from the gate layers **227***g* and **240***g* disposed on a level lower than a level of one of the gate layers by buffer insulating layers **227** and **240**.

**[0202]** The gate contact plugs **289** may include protrusions **289**E protruding in a horizontal direction from portions of the gate contact plugs **289** in contact with the gate pads GP. Accordingly, the protrusions **289**E of the gate contact plugs **289** may be in contact with the gate pads GP.

**[0203]** Each of the gate contact plugs **289** may include an upper region **289**US disposed on the same level as a level of the upper region **287**US of the peripheral contact plug **287**, and the structure of the upper region **289**US of the contact plugs **289** may be substantially the same as the structure of the upper region **287**US of the peripheral contact plug **287**. For example, the upper region **289**US of each of the gate contact plugs **289** may include a first region **289**US_**1**, a second region **289**US_**3**, and a connection region **289**US_**2** corresponding to the first region **287**US_**1**, the second region **287**US_**3**, and the connection region **287**US_**2** of the upper region **287**US of the peripheral contact plug **287**, respectively.

**[0204]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include a third upper insulating layer **291** disposed on the second upper insulating layer **273**.

**[0205]** The semiconductor device **2** according to an example embodiment of the present disclosure may further include peripheral upper plugs **295***a* and **295***b* penetrating the third upper insulating layer **291**. The peripheral upper plugs **295***a* and **295***b* may include a first peripheral upper plug **295***a* electrically connected to the first peripheral contact plug **287***a*, and a second peripheral upper plug **295***b* electrically connected to the second peripheral contact plug **287***b*.

**[0206]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include a bit line contact plug **296***a* penetrating the first to third upper insulating layers **258**, **273**, **271** and the capping layer **263**, and electrically connected to the memory vertical structure **47**.

**[0207]** Each of the peripheral upper plugs **295***a* and **295***b* and the bit line contact plug **296***a* may include a plug pattern **295**_**2** and a conductive liner **295**_**1** covering a side surface and a bottom surface of the plug pattern **295**_**2**.

**[0208]** The semiconductor device **200** according to an example embodiment of the present disclosure may further include wirings **298***b*, **298***a*, and **298***c* disposed on the third upper insulating layer **291**. The wirings **298***b*, **298***a*, and **298***c* may include bit lines **298***b* electrically connected to the bit line contact plugs **296***a*, a first peripheral wiring **298***a* electrically connected to the first peripheral upper plug **295***a*, and a second peripheral wiring **298***c* electrically connected to the second peripheral upper plug **295***b*.

**[0209]** In the description below, a modified example of the peripheral contact plug **287** described with reference to FIGS. **11**A and **12** will be described with reference to FIG. **13**. FIG. **13** may illustrate a modified structure of the peripheral contact plug **287** in the example in the enlarged diagram in FIG. **12**.

**[0210]** In a modified example, referring to FIG. **13**, the peripheral contact plug **287** in FIG. **12** may be modified to a peripheral contact plug **287***a'* having the same width or having a monotonically changing width. Accordingly, on the same level as a level of the upper region **289**US of each of the gate contact plugs **289**, a side-surface profile of the peripheral contact plug **287***a'* may be different from a side-surface profile of the upper region **289**US of each of the gate contact plugs **289**.

**[0211]** In the description below, a modified example of a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIG. **14**. In FIG. **14**, region Ia-Ia' may be a cross-sectional region illustrating a region taken in a first horizontal direction, and region IIa-IIa' may be a cross-sectional region illustrating a region taken in a second horizontal direction perpendicular to the first horizontal direction.

**[0212]** Referring to FIG. **14**, the semiconductor device **300** according to an example embodiment of the present disclosure may include a lower structure **303** and an upper structure **403** overlapping in a vertical direction. The lower structure **303** may be a memory semiconductor chip, and the upper structure **403** may be a logic semiconductor chip.

**[0213]** The lower structure **303** may include a pattern structure **317** and a structure **321** on the pattern structure **317**. The pattern structure **317** may include first, second, third and fourth pattern layers **317***a*, **317***b*, **317***c* and **317***d* corresponding to the first to fourth pattern layers **17***a* to **17***d* described with reference to FIGS. **1** to **2**C, respectively.

**[0214]** The structure **321** may have substantially the same structure as that of a portion of the second structure **21'** other than the through regions TA, described with reference to FIGS. **1** to **2**C. For example, the structure **321** may include a stack structure including gate layers **327***g* and **340***g* and interlayer insulating layers **325** and **338** alternately stacked. The gate layers **327***g* and **340***g* may include gate pads **327***p* and **340***p* substantially the same as the examples described with reference to FIGS. **1** to **2**C. The structure **221** may include first and second intermediate insulating layers **332** and **344** corresponding to those described with reference to FIGS. **1** to **2**C.

**[0215]** The lower structure **303** may further include the first upper insulating layer **58**, the capping layer **63**, the second upper insulating layer **73**, and the third upper insulating layer **91**, which may be the same as the examples described with reference to FIGS. **1** to **2**C.

**[0216]** The lower structure **303** may include the separation structures **77**, the memory vertical structure **47**, the support vertical structure **61**, the gate contact plugs **89**, the bit line contact plug **96***a*, and the gate upper plug **96***b*, which may be the same as the examples described with reference to FIGS. **1** to **2**C. The lower structure **303** may further include a peripheral contact plug **387** substantially the same as the third peripheral contact plug **87***c* described with reference to FIGS. **1** to **2**C. The lower structure **303** may further include a peripheral upper plug **95***a* substantially the same as the third peripheral upper plug **95***c* described with reference to FIGS. **1** to **2**C.

**[0217]** The lower structure **303** may include wirings **98***b*, **98***a*, and **98***c* in contact with and electrically connected to the bit line contact plug **96***a*, the gate upper plug **96***b*, and the peripheral upper plug **95***a*, respectively.

**[0218]** The lower structure **303** may include a capping insulating structure **315** on the third upper insulating layer **91** and a lower bonding wiring structure **310** electrically connected to the wirings **98***b*, **98***a*, and **98***c* in the capping insulating structure **315**. The lower bonding wiring structure **310** may further include lower bonding pads **310***p*.

**[0219]** The upper structure **403** may include a semiconductor substrate **404**, a peripheral circuit **409** disposed between the semiconductor substrate **404** and the lower structure **303**, and an upper bonding wiring structure **410** disposed between the peripheral circuit **409** and the lower structure **303**. The upper bonding wiring structure **410** may include upper bonding pads **410***p*. The peripheral circuit **409** may include peripheral devices such as a transistor including a peripheral gate **409***a* and a peripheral source/drain **409***b*. The lower bonding pads **310***p* of the lower bonding wiring structure **310** may be in contact with the upper bonding pads **410***p* of the upper bonding wiring structure **410**. The lower bonding pads **310***p* and the upper bonding pads **410***p* may include a copper material.

**[0220]** An example of a method of forming a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIG. **15**. FIG. **15** is a flowchart illustrating a method of forming a semiconductor device according to an example embodiment of the present disclosure.

**[0221]** Referring to FIG. **15**, a preliminary stack structure including interlayer insulating layers and mold layers alternately stacked on a lower structure may be formed (S**10**). A memory vertical structure may be formed (S**20**). The memory vertical structure may penetrate the preliminary stack structure and may be in contact with the lower structure. A support hole and a lower peripheral contact hole may be formed (S**30**). The support hole and the lower peripheral contact hole may penetrate the preliminary stack structure and may expose the lower structure. A capping layer defining the air gap and covering the support hole and the lower peripheral contact hole may be formed (S**40**). A separation trench may be formed (S**50**). The separation trench may expose side surfaces of the mold layers of the preliminary stack structure. The mold layers of the preliminary stack structure may be replaced with gate layers (S**60**). A separation structure may be formed in the separation trench (S**70**). A peripheral contact hole penetrating at least the capping layer and exposing a conductive region disposed below the lower peripheral contact hole may be formed (S**80**). A peripheral contact plug may be formed in the peripheral contact hole (S**90**).

**[0222]** In the description below, an example of the method of forming the semiconductor device **1** described above with reference to FIGS. **1** to **2**C will be described with reference to FIGS. **16**A to **16**C together with FIG. **15**. In FIGS. **16**A to **16**C, FIG. **16**A is a cross-sectional diagram illustrating region taken along line I-I' in FIG. **1**, FIG. **16**B is a cross-sectional diagram illustrating a region taken along line II-II' in FIG. **1**, and FIG. **16**C is a cross-sectional diagram illustrating a region taken along line III-III' in FIG. **1**.

**[0223]** Referring to FIGS. **1**, **15** and **16**A to **16**C, a lower structure **3** may be formed. The forming the lower structure **3** may include forming a peripheral circuit **8** on a semiconductor substrate **4** and a lower insulating layer **13** covering the peripheral circuit **8**, forming a preliminary pattern structure **17** having gaps **17***g* on the lower insulating layer **13**, and internal and external insulating layers **19***a* and **19***b* filling the gaps **17***g* and disposed on an external side surface of the preliminary pattern structure **17**. The peripheral circuit **8** may include a circuit device **9** such as a transistor including a peripheral gate **9***a* and a peripheral source/drain **9***b*, and a circuit interconnection **11** electrically connected to the circuit device **9**. A portion of the circuit interconnection **11** may be first and second peripheral circuit pads **11***p***1** and **11***p***2**.

**[0224]** The forming the preliminary pattern structure **17** may include forming a first pattern layer **17***a*, forming a first preliminary intermediate pattern layer **17***b* and a second preliminary intermediate pattern layer **17***d* spaced apart from each other on the first pattern layer **17***a*, and forming a third pattern layer **17***c* covering the first preliminary intermediate pattern layer **17***b* and the second preliminary intermediate pattern layer **17***d* on the first pattern layer **17***a*. The first and third pattern layers **17***a* and **17***c* may be formed of a silicon layer. Each of the first preliminary intermediate pattern layer **17***b* and the second intermediate pattern layer **17***d* may include a plurality of layers stacked in order, such as, for example, a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer stacked in order.

**[0225]** The internal and external insulating layers **19***a* and **19***b* may include an internal insulating layer **19***a* filling the gaps **17***g* and an external insulating layer **19***b* formed on the external side surface of the preliminary pattern structure **17**.

**[0226]** Preliminary stack structures **23** and **35** including interlayer insulating layers **25** and **38** and horizontal layers **27** and **40** alternately stacked on the lower structure **3** may be formed (S**10**). An insulating structure covering at least a portion of the preliminary stack structures **23** and **35** may be formed. The preliminary stack structures **23** and **35** and the

insulating structure may form the preliminary upper structure **21**. The insulating structure may include first and second insulating layers **32** and **44**.

**[0227]** The forming of the preliminary upper structure **21** may include forming a first preliminary stack structure **23** on the preliminary pattern structure **17**, forming a first insulating layer **32** covering a portion of the first preliminary stack structure **23** and the external insulating layer **19***b*, forming a second preliminary stack structure **35** on the first preliminary stack structure **23**, and forming a second insulating layer **44** covering a portion of the second preliminary stack structure **35** and the first insulating layer **32**.

**[0228]** The first preliminary stack structure **23** may include first interlayer insulating layers **25** and first horizontal layers **27** alternately stacked. The second preliminary stack structure **35** may include second interlayer insulating layers **38** and second horizontal layers **40** alternately stacked. The first and second interlayer insulating layers **25** and **38** may be formed of silicon oxide, and the first and second horizontal layers **27** and **40** may be formed of silicon nitride.

**[0229]** In an example embodiment of the present disclosure, on at least one side of the first preliminary stack structure **23**, the first horizontal layers **27** may include pad regions arranged in a staircase shape. On at least one side of the second preliminary stack structure **35**, the second horizontal layers **40** may include pad regions arranged in a staircase shape. In the preliminary upper structure **21**, a region in which pad regions of the first and second horizontal layers **27** and **40** arranged in a staircase shape are disposed may be referred to as a staircase region SA, and a region in which the first and second horizontal layers **27** and **40** are disposed in a region adjacent to the staircase region SA may be referred to as a memory cell array region MCA.

**[0230]** In the example embodiment of the present disclosure, before forming the first insulating layer **32**, first reinforcing horizontal layers **28** may be formed on regions of the first horizontal layers **27** arranged in a staircase shape. Before forming the second insulating layer **44**, second reinforcing horizontal layers **41** may be formed on pad regions of the second horizontal layers **40** arranged in a staircase shape. The first and second reinforcing horizontal layers **41** may be formed of silicon nitride.

**[0231]** A memory vertical structure **47** may be formed (S**20**). The forming the memory vertical structure **47** may include forming a sacrificial vertical portion penetrating the first preliminary stack structure **23**, forming the second preliminary stack structure **35**, forming an upper channel hole penetrating the second preliminary stack structure **35** and exposing the sacrificial vertical portion, forming a lower channel hole by removing the sacrificial vertical portion exposed by the upper channel hole, and forming the memory vertical structure **47** in the lower and upper channel holes, before forming the second preliminary stack structure **35**.

**[0232]** A first upper insulating layer **58** may be formed on the preliminary upper structure **21**.

**[0233]** A support hole **60***s* and lower peripheral contact holes **60***a*, **60***b*, and **60***c* may be formed (S30). The support hole **60***s* and the lower peripheral contact holes **60***a*, **60***b*, and **60***c* may be simultaneously formed. The lower peripheral contact holes **60***a*, **60***b*, and **60***c* may include a first lower peripheral contact hole **60***a*, a second lower peripheral contact hole **60***b*, and a third preliminary peripheral contact hole **60***c*.

**[0234]** The support hole **60***s* may penetrate the first upper insulating layer **58** and the preliminary upper structure **21**, and may expose the first pattern layer **17***a* of the preliminary pattern structure **17**. The support hole **60***s* may penetrate at least a portion of the preliminary stack structures **23** and **35**.

**[0235]** The first lower peripheral contact hole **60***a* may penetrate the first upper insulating layer **58**, the insulating structure, and the external insulating layer **19***b*, may extend downwardly, may expose the first peripheral circuit pad **11***p***1**.

**[0236]** The second lower peripheral contact hole **60***b* my penetrate the first upper insulating layer **58**, the preliminary upper structure **21**, and the internal insulating layer **19***a*, may extend downwardly, and may expose the second peripheral circuit pad **11***p***2**.

**[0237]** The third lower peripheral contact hole **60***c* may penetrate the first upper insulating layer **58** and the preliminary upper structure **21**, and may expose the first pattern layer **17***a* of the preliminary pattern structure **17**.

**[0238]** A capping material layer defining the air gaps **69***a* and **69***b* and covering the support holes **60***s* and the lower peripheral contact holes **60***a*, **60***b*, and **60***c* may be formed (S**40**). In an example embodiment of the present disclosure, the forming of the capping material layer may include forming the first capping layer and the upper capping layer **67** in order. The first capping layer may cover internal walls of the support hole **60***s* and the lower peripheral contact holes **60***a*, **60***b*, and **60***c*, defining at least a portion of the air gaps **69***a* and **69***b* in the lower peripheral contact holes **60***a*, **60***b*, and **60***c*, and may cover an upper portion of the first upper insulating layer **58**. The upper capping layer **67** may cover the support holes **60***s* and the lower peripheral contact holes **60***a*, **60***b*, and **60***c* on the first capping layer and may limit upper portions of the air caps **69***a* and **69***b*. The air gaps **69***a* and **69***b* may include a first air gap **69***a* and a second air gap **69***b*. The first air gap **69***a* may be limited by the first capping layer and the upper capping layer **67**, and at least a portion of the first air gap **69***a* may be formed in the support hole **60***s*. The second air gap **69***b* may be limited by the first capping layer and the upper capping layer **67**, and at least a portion of the second air gap **69***b* may be formed in each of the lower peripheral contact holes **60***a*, **60***b*, and **60***c*.

**[0239]** In the first capping layer, a portion of the first capping layer covering the internal wall of the support hole **60***s* may be a support layer **65***a*, a portion covering the lower peripheral contact holes **60***a*, **60***b*, and **60***c* may be a spacer layer **65***b*, and a portion covering an upper portion of the first upper insulating layer **58** may be a lower capping layer **65***c*. Accordingly, the support layer **65***a*, the spacer layer **65***b*, and the lower capping layer **65***c* may be integrated with each other. In an example embodiment of the present disclosure, the lower capping layer **65***c* and the upper capping layer **67** may form the capping layer **63**.

**[0240]** In an example embodiment of the present disclosure, the first capping layer may be formed of a single layer or two or more layers. For example, the first capping layer may include silicon oxide covering the internal wall of the support hole **60***s* with a minimum thickness and may be formed to have a thick thickness on the support hole **60***s*. The first capping layer may include silicon oxide formed by an atomic layer deposition process. In another example, the forming the first capping layer may include forming a silicon oxide layer and forming a silicon nitride layer on the silicon oxide layer.

**[0241]** Referring back to FIGS. **1**, **15**, and **2**A to **2**C, a preliminary separation trench and a dam trench penetrating the capping layer **63**, the first upper insulating layer **58** and the preliminary upper structure **21** (in FIGS. **16**A to **16**C), form a preliminary separation structure and a dam structure **71** filling the preliminary separation trench and the dam trench, respectively, and form a second upper insulating layer **73** on the capping layer **63**.

**[0242]** The preliminary separation structure and the dam structure **71** may include an insulating material layer. For example, the forming of the preliminary separation structure and the dam structure **71** may include forming an insulating material layer (e.g., a silicon oxide layer and/or a silicon nitride layer, or the like) covering internal walls of the preliminary separation trench and the dam trench, and forming a polysilicon layer on the insulating material layer.

**[0243]** The first and second horizontal layers **27** and **40** limited by the dam structure **71** may be referred to as the first and second insulating horizontal layers **27***i* and **40***i* as described with reference to FIGS. **1** to **2**C. Regions of the upper structure **21'** in which the first and second insulating horizontal layers **27***i* and **40***i* are formed may be referred to as through regions TA.

**[0244]** Separation trenches **75** may be formed (S**50**). The forming of the separation trenches **75** may include forming an upper separation trench **75***b* penetrating the second upper insulating layer **73** and exposing the preliminary separation structure, and forming a lower separation trench **75***a* by removing the preliminary separation structure. Accordingly, each of the separation trenches **75** may include the lower separation trench **75***a* and the upper separation trench **75***b*. A width of the upper separation trench **75***b* may be greater than a width of the lower separation trench **75***a*. The upper separation trench **75***b* may be disposed on an upper surface of the capping layer **63**.

**[0245]** In an example embodiment of the present disclosure, the second intermediate pattern layer **17***d* in the staircase region SA may be disposed between the separation trenches **75** and may not be exposed by the separation trenches **75**.

**[0246]** In an example embodiment of the present disclosure, in the memory cell array region MCA, the separation trenches **75** may penetrate the first preliminary intermediate pattern layer **17***b*, and may expose the first intermediate pattern layer **17***b*. An empty space may be formed by etching a portion of the memory vertical structure **47** while etching the first intermediate pattern layer **17***b*, and a first intermediate pattern layer **17***b*' may be formed in the empty space. The intermediate pattern layer **17***b*' may be formed of a silicon layer, such as, for example, a polysilicon layer having N-type conductivity. Before exposing the first preliminary intermediate pattern layer **17***b*, sacrificial spacers may be formed on side surfaces of the preliminary stack structures **23** and **35** exposed by the separation trenches **75**, and thereafter, the intermediate pattern layer **17***b*' may be formed, and the sacrificial spacer may be removed to expose side surfaces of the preliminary stack structures **23** and **35** (in FIGS. **16**A to **16**C).

**[0247]** Empty spaces may be formed by etching the first and second horizontal layers **27** and **40** (in FIGS. **16**A-**16**C) of the preliminary stack structure **23** and **35** (in FIGS. **16**A to **16**C) exposed by the separation trenches **75**, and first and second gate layers **27***g* and **40***g* may be formed in the empty spaces. The first preliminary stack structure **23** (in FIGS. **16**A to **16**C) may be formed as a first stack structure **23'** including the first interlayer insulating layers **25** and the first gate layers **27***g*, and the second preliminary stack structure **35** (in FIGS. **16**A to **16**C) may be formed as a second stack structure **35'** including the second interlayer insulating layers **38** and the second gate layers **40***g*. Accordingly, the preliminary upper structure **21** (in FIGS. **16**A to **16**C) may be formed as the upper structure **21'** including the first and second stack structures **23'** and **35'**.

**[0248]** In an example embodiment of the present disclosure, before forming the first and second gate layers **27***g* and **40***g* in the empty spaces, the dielectric layer **57** described with reference to FIG. **2**C may be conformally formed.

**[0249]** The forming of the first and second gate layers **27***g* and **40***g* in the empty spaces may include forming conductive material layers in the empty spaces and etching the conductive material layers.

**[0250]** Separation structures **77** may be formed in the separation trenches **75**. In one example, the separation structures **77** may be formed of silicon oxide. In another example, the separation structures **77** may be formed to include a conductive pattern and an insulating layer covering a side surface of the conductive pattern.

**[0251]** In an example embodiment of the present disclosure, gate contact holes penetrating the second upper insulating layer **73**, the capping layer **63**, and the insulating structure, and exposing gate pads **27***p* and **40***p* of the first and second gate layers **27***g* and **40***g* in the staircase region SA may be formed.

**[0252]** Peripheral contact holes penetrating at least the capping layer **63** and exposing conductive regions disposed below the lower peripheral contact holes **60***a*, **60***b*, and **60***c* may be formed (S**80**). The forming the peripheral contact holes may include forming upper peripheral contact holes penetrating the second upper insulating layer **73** and the capping layer **63** and overlapping the lower peripheral contact holes **60***a*, **60***b*, and **60***c*, and exposing the first peripheral circuit pad **11***p***1**, the second peripheral circuit pad **11***p***2**, and the first pattern layer **17***a* of the preliminary pattern structure **17** by etching at least a portion of the spacer layer **65***b* in the lower peripheral contact holes **60***a*, **60***b*, and **60***c* disposed below the upper peripheral contact holes.

**[0253]** The upper peripheral contact holes may include a first upper peripheral contact hole, a second upper peripheral contact hole, and a third upper peripheral contact hole. The peripheral contact holes may include a first peripheral contact hole, a second peripheral contact hole, and a third peripheral contact hole. The first peripheral contact hole may include the first lower peripheral contact hole **60***a* and the first upper peripheral contact hole, the second peripheral contact hole may include the second peripheral contact hole **60***a* and the second upper peripheral contact hole, and the third peripheral contact hole may include the third lower peripheral contact hole **60***c* and the third upper peripheral contact hole.

**[0254]** Peripheral contact plugs **87***a*, **87***b* and **87***c* may be formed in the peripheral contact holes (S**90**). The peripheral contact plugs **87***a*, **87***b*, and **87***c* may include a first peripheral contact plug **87***a* in the first peripheral contact hole, a second peripheral contact plug **87***b* in the second peripheral contact hole, and a third peripheral contact plug **87***c* in the third peripheral contact hole.

**[0255]** Gate contact plugs **89** filling the gate contact holes may be formed. The gate contact plugs **89** may be formed

simultaneously with the peripheral contact plugs **87**a, **87**b, and **87**c. For example, the peripheral contact plugs **87**a, **87**b, and **87**c and the gate contact plugs **89** may include plug patterns **87_2** and **89_2** and conductive liners **87_1** and **97_1** covering a side surface and a bottom surface of the plug patterns **87_2** and **89_2**, respectively.

**[0256]** A third upper insulating layer **91** may be formed on the second upper insulating layer **73**.

**[0257]** A bit line contact plug **96**a electrically connected to the memory vertical structure **47**, gate upper plugs **96**b electrically connected to the gate contact plugs **89**, and the first to third peripheral upper plugs **95**a, **95**b, and **95**c electrically connected to the first to third peripheral contact plugs **87**a, **87**b, and **87**c may be formed simultaneously. Each of the bit line contact plug **96**a, the gate upper plugs **96**b, and the first to third peripheral upper plugs **95**a, **95**b and **95**c may include a plug pattern **95_2** and conductive liner **95_1** covering a bottom surface and a side surface of the plug pattern **95_2**.

**[0258]** A bit line **98**b electrically connected to the bit line contact plug **96**a, gate connection wirings **98**g electrically connected to the gate upper plugs **96**b and the second peripheral upper contact plug **95**b, a first peripheral wiring **98**a electrically connected to the first peripheral upper plug **95**a, and a second peripheral wiring **98**c electrically connected to the third peripheral upper plug **95**c may be formed simultaneously on the third upper insulating layer **91**.

**[0259]** In the description below, a data storage system including the semiconductor device described in an example embodiment of the present disclosure will be described with reference to FIGS. **17**, **18**, and **19**.

**[0260]** FIG. **17** is a diagram illustrating a data storage system including a semiconductor device according to an example embodiment of the present disclosure.

**[0261]** Referring to FIG. **11**, a data storage system **1000** according to an example embodiment of the present disclosure may include a semiconductor device **1100** and a controller **1200** electrically connected to the semiconductor device **1100**. The data storage system **1000** may be implemented as a storage device including the semiconductor device **1100** or an electronic device including a storage device. For example, the data storage system **1000** may be implemented as a solid state drive device (SSD) device including the semiconductor device **1100**, a universal serial bus (USB), a computing system, a medical device, or a communication device.

**[0262]** In an example embodiment of the present disclosure, the data storage system **1000** may be implemented as an electronic system for storing data.

**[0263]** The semiconductor device **1100** may be the semiconductor device described in one of the aforementioned example embodiments described with reference to FIGS. **1** to **16**C. The semiconductor device **1100** may include a first structure **1100**F and a second structure **1100**S on the first structure **1100**F.

**[0264]** The first structure **1100**F may be configured as a peripheral circuit structure including a decoder circuit **1110**, a page buffer **1120**, and a logic circuit **1130**. For example, the first structure **1100**F may include the peripheral circuit **8** (in FIG. **2**A).

**[0265]** The second structure **1100**S may be configured as a memory cell structure including a bit line BL, a common source line CSL, word lines WL, first and second gate upper lines UL**1** and UL**2**, first and second gate lower lines LL**1** and LL**2**, and memory cell strings CSTR between the bit line BL and the common source line CSL.

**[0266]** The pattern structure **17**' (in FIGS. **2**A to **2**C) described above may include a silicon layer having N-type conductivity, and the silicon layer having N-type conductivity may be the common source line CSL.

**[0267]** In the second structure **1100**S, each of the memory cell strings CSTR may include lower transistors LT**1** and LT**2** adjacent to the common source line CSL, upper transistors UT**1** and UT**2** adjacent to the bit line BL, and a plurality of memory cell transistors MCT disposed between the lower transistors LT**1** and LT**2** and the upper transistors UT**1** and UT**2**. The number of the lower transistors LT**1** and LT**2** and the number of the upper transistors UT**1** and UT**2** may be varied in example embodiments. For example, only one lower transistor and only one upper transistor may be employed in an example embodiment of the present disclosure.

**[0268]** In example embodiments of the present disclosure, the upper transistors UT**1** and UT**2** may include string select transistors, and the lower transistors LT**1** and LT**2** may include ground select transistors. The gate lower lines LL**1** and LL**2** may be gate electrodes of the lower transistors LT**1** and LT**2**, respectively. The word lines WL may be gate electrodes of the memory cell transistors MCT, and the gate upper lines UL**1** and UL**2** may be gate electrodes of the upper transistors UT**1** and UT**2**, respectively.

**[0269]** Among the first and second gate layers **27**g and **40**g described with reference to FIG. **5**, the lower gate layers GL**1** and GL**2** may be the gate lower lines LL**1** and LL**2**, at least a plurality of the intermediate gate layers GM may be the word lines WL, and the upper gate layers GU**1** and GU**2** may be the gate upper lines UL**1** and UL**2**.

**[0270]** In example embodiments of the present disclosure, the lower transistors LT**1** and LT**2** may include a lower erase control transistor LT**1** and a ground select transistor LT**2** connected to each other in series. The upper transistors UT**1** and UT**2** may include a string select transistor UT**1** and an upper erase control transistor UT**2** connected to each other in series. At least one of the lower erase control transistor LT**1** and the upper erase control transistor UT**1** may be used in an erase operation for erasing data stored in the memory cells using a gate induce drain leakage (GIDL) phenomenon.

**[0271]** The common source line CSL, the first and second gate lower lines LL**1** and LL**2**, the word lines WL, and the first and second gate upper lines UL**1** and UL**2** may be electrically connected to the decoder circuit **1110** through first connection wirings **1115** extending from the first structure **1100**F to the second structure **1100**S.

**[0272]** In example embodiments of the present disclosure, the lower gate layers GL**1** and GL**2** (in FIG. **2**A) described above may be the gate lower lines LL**1** and LL**2**, and the upper gate layers GU**1** and GU**2** (in FIG. **2**A) may be the gate upper lines UL**1** and UL**2**. A plurality of the intermediate gate layers GM (in FIG. **2**A) may be the word lines WL.

**[0273]** The bit lines BL may be electrically connected to the page buffer **1120** through second connection wirings **1125** extending from the first structure **1100**F to the second structure **1100**S. The bit lines BL may be the bit lines **96**b in FIGS. **2**A and **2**B described above.

**[0274]** In the first structure **1100**F, the decoder circuit **1110** and the page buffer **1120** may perform a control operation on at least one select memory cell transistor among the plurality

of memory cell transistors MCT. The decoder circuit **1110** and the page buffer **1120** may be controlled by the logic circuit **1130**. The semiconductor device **1000** may communicate with the controller **1200** through an input/output pad **1101** electrically connected to the logic circuit **1130**. The input/output pad **1101** may be electrically connected to the logic circuit **1130** through an input/output connection wiring **1135** extending from the first structure **1100**F to the second structure **1100**S.

**[0275]** The controller **1200** may include a processor **1210**, a NAND controller **1220**, and a host interface **1230**. In example embodiments of the present disclosure, the data storage system **1000** may include a plurality of semiconductor devices **1100**, and in this case, the controller **1200** may control the plurality of semiconductor devices **1100**.

**[0276]** The processor **1210** may control overall operation of the data storage system **1000** including the controller **1200**. The processor **1210** may operate according to a predetermined firmware, and may access the semiconductor device **1100** by controlling the NAND controller **1220**. The NAND controller **1220** may include a NAND interface **1221** for processing communications with the semiconductor device **1100**. Through the NAND interface **1221**, a control command for controlling the semiconductor device **1100**, data to be written in the memory cell transistors MCT of the semiconductor device **1100**, and data to be read from the memory cell transistors MCT may be transmitted. The host interface **1230** may provide a communication function between the data storage system **1000** and an external host. When a control command is received from an external host through the host interface **1230**, the processor **1210** may control the semiconductor device **1100** in response to the control command.

**[0277]** FIG. **18** is a perspective diagram illustrating a data storage system including a semiconductor device according to an example embodiment of the present disclosure.

**[0278]** Referring to FIG. **18**, a data storage system **2000** according to an example embodiment of the present disclosure may include a main substrate **2001**, a controller **2002** mounted on the main substrate **2001**, one or more semiconductor packages **2003**, and a DRAM **2004**. The semiconductor package **2003** and the DRAM **2004** may be connected to the controller **2002** by wiring patterns **2005** formed on the main substrate **2001**.

**[0279]** The main board **2001** may include a connector **2006** including a plurality of pins coupled to an external host. The number and the arrangement of the plurality of pins in the connector **2006** may be varied depending on a communication interface between the data storage system **2000** and the external host. In example embodiments of the present disclosure, the data storage system **2000** may communicate with the external host through one of interfaces such as a universal serial bus (USB), a peripheral component interconnect express (PCI-Express), a serial advanced technology attachment (SATA), and an M-phy for universal flash storage (UFS). In example embodiments of the present disclosure, the data storage system **2000** may operate by power supplied from the external host through the connector **2006**. The data storage system **2000** may further include a power management integrated circuit (PMIC) for distributing power supplied from the external host to the controller **2002** and the semiconductor package **2003**.

**[0280]** The controller **2002** may write data in the semiconductor package **2003** or may read data from the semiconductor package **2003**, and may increase an operation speed of the data storage system **2000**.

**[0281]** The DRAM **2004** may be configured as a buffer memory for mitigating a difference in speeds between the semiconductor package **2003**, which may be a data storage space, and an external host. The DRAM **2004** included in the data storage system **2000** may also operate as a cache memory, and may provide a space for temporarily storing data in a control operation for the semiconductor package **2003**. When the DRAM **2004** is included in the data storage system **2000**, the controller **2002** may further include a DRAM controller for controlling the DRAM **2004** in addition to the NAND controller for controlling the semiconductor package **2003**

**[0282]** The semiconductor package **2003** may include first and second semiconductor packages **2003*a*** and **2003*b*** spaced apart from each other. Each of the first and second semiconductor packages **2003*a*** and **2003*b*** may be configured as a semiconductor package including a plurality of semiconductor chips **2200**. Each of the semiconductor chips **2200** may include a semiconductor device described in one of the aforementioned example embodiments described with reference to FIGS. **1** to **16**C. More than two individual semiconductor packages may be included in the semiconductor package **2003**.

**[0283]** Each of the first and second semiconductor packages **2003*a*** and **2003*b*** may include a package substrate **2100**, semiconductor chips **2200** on the package substrate **2100**, adhesive layers **2300** disposed on lower surfaces of the semiconductor chips **2200**, respectively, a connection structure **2400** electrically connecting the semiconductor chips **2200** to the package substrate **2100**, and a molding layer **2500** covering the semiconductor chips **2200** and the connection structure **2400** on the package substrate **2100**.

**[0284]** The package substrate **2100** may be configured as a printed circuit board including package upper pads **2130**. Each of the semiconductor chips **2200** may include an input/output pad **2210**.

**[0285]** In example embodiments of the present disclosure, the connection structure **2400** may be a bonding wiring electrically connecting the input/output pad **2210** to the package upper pads **2130**. Accordingly, in each of the first and second semiconductor packages **2003*a*** and **2003*b***, the semiconductor chips **2200** may be electrically connected to each other through a bonding wire method, and may be electrically connected to the package upper pads **2130** of the package substrate **2100**. In example embodiments of the present disclosure, in each of the first and second semiconductor packages **2003*a*** and **2003*b***, the semiconductor chips **2200** may be electrically connected to each other by a connection structure including a through silicon via (TSV), instead of the connection structure **2400** of a bonding wire method.

**[0286]** In example embodiments of the present disclosure, the controller **2002** and the semiconductor chips **2200** may be included in a single package. For example, the controller **2002** and the semiconductor chips **2200** may be mounted on a separate interposer substrate different from the main substrate **2001**, and the controller **2002** may be connected to the semiconductor chips **2200** by wirings formed on the interposer substrate.

**[0287]** FIG. **19** is a cross-sectional diagram illustrating a data storage system including a semiconductor device according to an example embodiment of the present disclo-

sure. FIG. **19** illustrates an example embodiment of the semiconductor package **2003** in FIG. **18**, illustrating a cross-sectional region of the semiconductor package **2003** in FIG. **18** taken along line VI-VI'.

**[0288]** Referring to FIG. **19**, in the semiconductor package **2003**, the package substrate **2100** may be configured as a printed circuit board. The package substrate **2100** may include a package substrate body portion **2120**, package upper pads **2130** disposed on an upper surface of the package substrate body portion **2120**, lower pads **2125** disposed on a lower surface of the package substrate body portion **2120** or exposed through the lower surface, and internal wirings **2135** electrically connecting the upper pads **2130** to the lower pads **2125** in the package substrate body portion **2120**. The upper pads **2130** may be electrically connected to the connection structures **2400**. The lower pads **2125** may be connected to the wiring patterns **2005** of the main substrate **2001** of the data storage system **2000** through conductive connection portions **2800**.

**[0289]** Each of the semiconductor chips **2200** may include a semiconductor substrate **3010** and a first structure **3100** and a second structure **3200** stacked in order on the semiconductor substrate **3010**. The first structure **3100** may include a peripheral circuit region including peripheral wirings **3110**. The second structure **3200** may include a common source line **3205**, a gate stack structure **3210** on the common source line **3205**, memory channel structures **3220** and separation structures penetrating the gate stack structure **3210**, bit lines **3240** electrically connected to the memory channel structures **3220**, and gate connection wirings **98***g* (in FIG. **2**A) electrically connected to the word lines WL of the gate stack structure **3210**. The first structure **3100** may include the first structure **1100**F in FIG. **17**, and the second structure **3200** may include the second structure **1100**S in FIG. **17**.

**[0290]** Each of the semiconductor chips **2200** may include a through wiring **3245** electrically connected to the peripheral wirings **3110** of the first structure **3100** and extending into the second structure **3200**. The through wiring **3245** may penetrate the gate stack structure **3210** and may be further disposed on an external side of the gate stack structure **3210**.

**[0291]** Each of the semiconductor chips **2200** may further include an input/output connection wiring electrically connected to peripheral wirings **3110** of the first structure **3100** and extending into the second structure **3200**, and an input/output pad **2210** electrically connected to the input/output connection wiring **3265**.

**[0292]** In FIG. **19**, the enlarged portion indicated by reference numeral "**1**" is provided to describe the example in which the semiconductor chips **2200** in FIG. **19** may be modified to have a cross-sectional structure as in FIG. **2**A. Accordingly, each of the semiconductor chips **2200** may include the semiconductor device **1**, **100**, and **300** in one of the aforementioned example embodiments described with reference to FIGS. **1** to **16**C.

**[0293]** According to the aforementioned example embodiments, a stable and reliable support vertical structure and a peripheral contact plug may be provided.

**[0294]** While the example embodiments of the present disclosure have been illustrated and described above, it will be apparent to those skilled in the art that modifications and variations could be made thereto without departing from the scope of the present disclosure as set forth by the appended claims.

What is claimed is:

**1**. A semiconductor device, including:

a first structure;

a second structure including a stack structure including a first stack structure on the first structure and a second stack structure on the first stack structure, and an intermediate insulating layer covering at least a portion of the stack structure;

an insulating structure on the second structure;

a memory vertical structure penetrating the second structure;

a support vertical structure penetrating the second structure and including an air gap and a support layer defining at least a lower portion and a sidewall of the air gap;

a peripheral contact plug penetrating the second structure; and

gate contact plugs,

wherein each of the first and second stack structures includes interlayer insulating layers and gate layers alternately stacked,

wherein the gate layers are spaced apart from each other in a vertical direction in a first region and include gate pads arranged in a second region adjacent to the first region,

wherein the gate contact plugs are electrically connected to the gate pads,

wherein the memory vertical structure penetrates the stack structure in the first region,

wherein the memory vertical structure includes a slope changing portion between an uppermost gate layer among the gate layers of the first stack structure and a lowermost gate layer among the gate layers of the second stack structure,

wherein the support vertical structure penetrates at least a portion of the gate layers in the second region,

wherein the air gap of the support vertical structure includes a portion disposed on the same level as the slope changing portion of the memory vertical structure,

wherein the peripheral contact plug is spaced apart from the gate layers,

wherein the peripheral contact plug includes an upper region disposed on a level higher than an upper surface of an uppermost gate layer among the gate layers of the stack structure and a lower region disposed on a level lower than the upper surface of the uppermost gate layer among the gate layers of the stack structure,

wherein the upper region of the peripheral contact plug includes a first portion, a second portion and a connection portion disposed between the first portion and the second portion, and

wherein a side of the connection portion has a slope different from a slope of at least one of a side of the first portion and a side of the second portion.

**2**. The semiconductor device of claim **1**, wherein, among the gate contact plugs, a portion of the gate contact plug disposed on a level higher than the upper surface of the uppermost gate layer among the gate layers of the stack

structure has a side-surface profile different from a side-surface profile of the upper region of the peripheral contact plug.

**3**. The semiconductor device of claim **2**, wherein, among the gate contact plugs, a side of a portion of the gate contact plug disposed on a level higher than the upper surface of the uppermost gate layer among the gate layers of the stack structure is substantially vertical.

**4**. The semiconductor device of claim **1**, wherein the gate contact plugs and the peripheral contact plug have upper surfaces coplanar with each other.

**5**. The semiconductor device of claim **1**, wherein upper surfaces of the gate contact plugs are disposed on a level different from an upper surface of the peripheral contact plug.

**6**. The semiconductor device of claim **1**,

wherein the insulating structure includes a lower capping layer extending from the support layer and an upper capping layer on the lower capping layer, and

wherein the support layer and the lower capping layer include an insulating material.

**7**. The semiconductor device of claim **1**, wherein an upper end of the air gap is disposed on a level than higher than an upper surface of the memory vertical structure.

**8**. The semiconductor device of claim **1**, wherein an upper end of the air gap is disposed on a level lower than an upper surface of the uppermost gate layer among the gate layers of the stack structure.

**9**. The semiconductor device of claim **1**, wherein, in the upper region of the peripheral contact plug, the first portion has a minimum width greater than a minimum width of the connection portion, and the second portion has a maximum width smaller than a maximum width of the connection portion.

**10**. The semiconductor device of claim **1**, wherein, in the upper region of the peripheral contact plug, the first portion has a minimum width less than a maximum width of the connection portion, the second portion has a maximum width greater than a minimum width of the connection portion, and the maximum width of the second portion is greater than a maximum width of the first portion.

**11**. The semiconductor device of claim **1**,

wherein the first structure further includes a semiconductor substrate, first and second peripheral circuit pads on the semiconductor substrate, and a pattern structure disposed on a level higher than the first and second peripheral circuit pads on the semiconductor substrate, and

wherein the memory vertical structure and the support vertical structure are in contact with the pattern structure.

**12**. The semiconductor device of claim **11**,

wherein the pattern structure includes a first pattern layer, a second pattern layer on the first pattern layer, and a third pattern layer on the second pattern layer,

wherein the memory vertical structure penetrates the second and third pattern layers and extends into the first pattern layer;

wherein the memory vertical structure includes an insulating gap-fill layer, a channel layer covering a side and a bottom of the insulating gap-fill layer, a pad material layer in contact with the channel layer on the insulating gap-fill layer, and a data storage structure covering at least an external side of the channel layer,

wherein the data storage structure includes a first dielectric layer, a second dielectric layer, and a data storage layer between the first and second dielectric layers; and

wherein the second pattern layer penetrates the data storage structure and is in contact with the channel layer.

**13**. The semiconductor device of claim **12**, wherein a lower surface of the peripheral contact plug is in contact with the first peripheral circuit pad.

**14**. The semiconductor device of claim **11**,

wherein the gate contact plugs penetrate the gate pads and are in contact with the gate pads,

wherein lower surfaces of the gate contact plugs are in contact with the second peripheral circuit pads, and

wherein, among the gate contact plugs, a portion of the gate contact plug disposed on a level higher than the upper surface of the uppermost gate layer among the gate layers of the stack structure has a side profile substantially the same as a side profile of the upper region of the peripheral contact plug.

**15**. The semiconductor device of claim **1**, further including:

a chip structure including a peripheral circuit, wherein the chip structure is disposed on the insulating structure.

**16**. The semiconductor device of claim **1**, further including:

a bit line contact plug in contact with the memory vertical structure on the memory vertical structure,

wherein an upper surface of the bit line contact plug and an upper surface of the peripheral contact plug are coplanar with each other, and

wherein each of the bit line contact plug and the peripheral contact plug includes a plug pattern and a conductive liner covering a lower surface and a side surface of the plug pattern.

**17**. The semiconductor device of claim **1**, wherein the peripheral contact plug includes a plug pattern, a conductive liner covering a lower surface and a side surface of the plug pattern, and a first air gap disposed in the plug pattern.

**18**. The semiconductor device of claim **17**, further including:

a second air gap disposed on the first air gap in the plug pattern and spaced apart from the first air gap.

**19**. A semiconductor device, including:

a pattern structure including a silicon layer;

a stack structure including a first stack structure and a second stack structure on the first stack structure on the pattern structure, wherein each of the first and second stack structures includes interlayer insulating layers and gate layers alternately stacked, and in the first and second stack structures, the gate layers are vertically stacked and spaced apart from each other in a first region, and include gate pads arranged in a staircase shape in a second region adjacent to the first region;

an insulating structure on the stack structure;

separation structures penetrating the stack structure and extending in the insulating structure in the first region and the second region;

a memory vertical structure penetrating the stack structure between the separation structures in the first region;

a support vertical structure penetrating the stack structure and including an air gap between the separation structures in the second region;

gate contact plugs in contact with the gate pads;

a peripheral contact plug spaced apart from the gate layers; and
bit line contact plugs on the memory vertical structure,
wherein the peripheral contact plug includes an upper region disposed on a level higher than an upper surface of an uppermost gate layer among the gate layers of the stack structure and a lower region disposed on a level lower than the upper surface of the uppermost gate layer among the gate layers of the stack structure,
wherein the upper region of the peripheral contact plug includes a first portion, a connection portion disposed below the first portion, and a second portion disposed below the connection portion,
wherein a side of the connection portion has a slope different from a slope of at least one of a side of the first portion and the second portion,
wherein a side of the memory vertical structure includes a slope changing portion in which a slope of the side of the memory vertical structure changes on a level between an uppermost gate layer among the gate layers of the first stack structure and a lowermost gate layer among the gate layers of the second stack structure, and
wherein a side of the lower region of the peripheral contact plug is substantially vertical on the level between the uppermost gate layer among the gate layers of the first stack structure and the lowermost gate layer among the gate layers of the second stack structure.

**20**. A data storage system, including:
a main board;
a semiconductor device on the main board; and
a controller electrically connected to the semiconductor device on the main board,
wherein the semiconductor device includes:
a pattern structure including a silicon layer;
a stack structure including a first stack structure and a second stack structure on the first stack structure on the pattern structure, wherein each of the first and second stack structures includes interlayer insulating layers and gate layers alternately stacked, and in the first and second stack structures, the gate layers are vertically stacked and spaced apart from each other in a first region, and include gate pads arranged in a staircase shape in a second region adjacent to the first region;
an insulating structure on the stack structure;
separation structures penetrating the stack structure and extending into the insulating structure in the first region and the second region;
a memory vertical structure penetrating the stack structure between the separation structures in the first region;
a support vertical structure penetrating the stack structure and including an air gap between the separation structures in the second region;
gate contact plugs in contact with the gate pads;
a peripheral contact plug spaced apart from the gate layers; and
bit line contact plugs on the memory vertical structure,
wherein the peripheral contact plug includes an upper region disposed on a level higher than an upper surface of an uppermost gate layer among the gate layers of the stack structure and a lower region disposed on a level lower than the upper surface of the uppermost gate layer the gate layer among of the stack structure,
wherein the upper region of the peripheral contact plug includes a first portion, a connection portion disposed below the first portion, and a second portion disposed below the connection portion,
wherein a side of the connection portion has a slope different from a slope of at least one of a side of the first portion and a side of the second portion,
wherein a side of the memory vertical structure includes a slope changing portion on a level between an uppermost gate layer among the gate layers of the first stack structure and a lowermost gate layer among the gate layers of the second stack structure, and
wherein a side of the lower region of the peripheral contact plug is substantially vertical on the level between the uppermost gate layer among the gate layers of the first stack structure and the lowermost gate layer among the gate layers of the second stack structure.

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