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(54) **OPERATIONAL AMPLIFIER**

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(57) **ABSTRACT**

There is provided an operational amplifier capable of detecting that an input terminal has been open circuited without restricting the voltage range of an input signal. The operational amplifier includes a first comparator which detects that an inverting input terminal of an operational amplifier has been open circuited, a second comparator which detects that a non-inverting input terminal of the operational amplifier has been open circuited, a first resistor and a first switch which are controlled by output signals of the first comparator and the second comparator and which are connected in series between the non-inverting input terminal and a ground terminal of the operational amplifier, and a second resistor and a second switch which are connected in series between the inverting input terminal and a supply terminal of the operational amplifier.

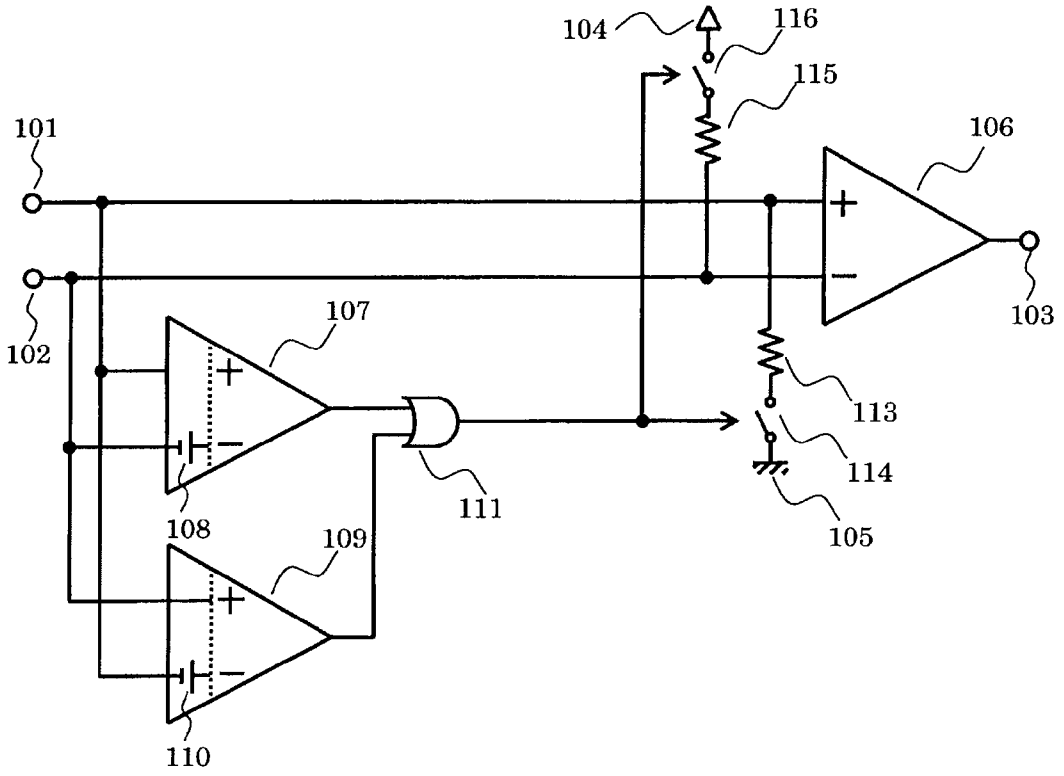


FIG. 1

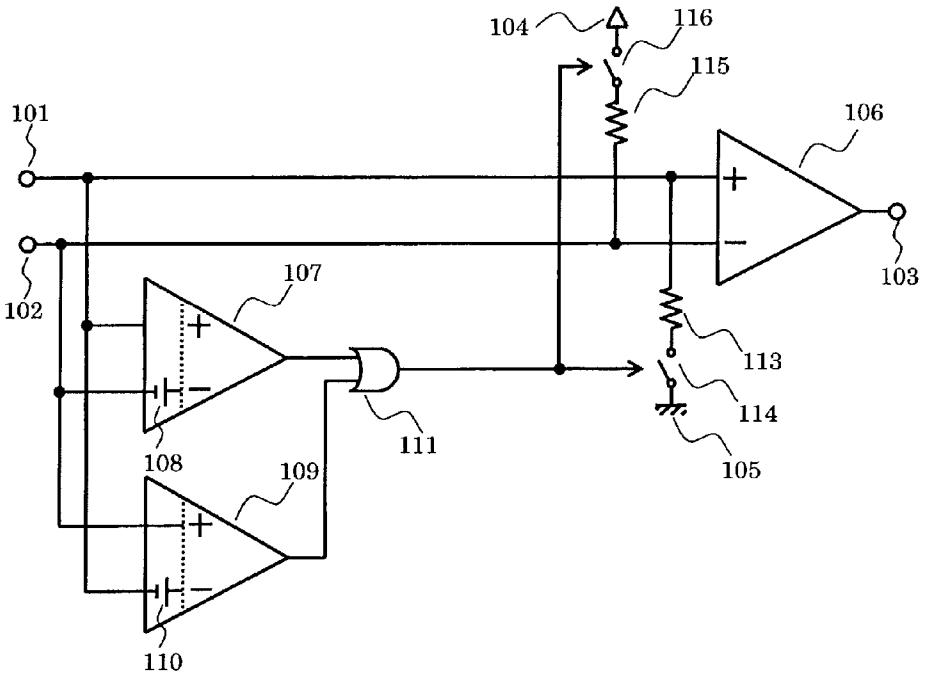


FIG. 2

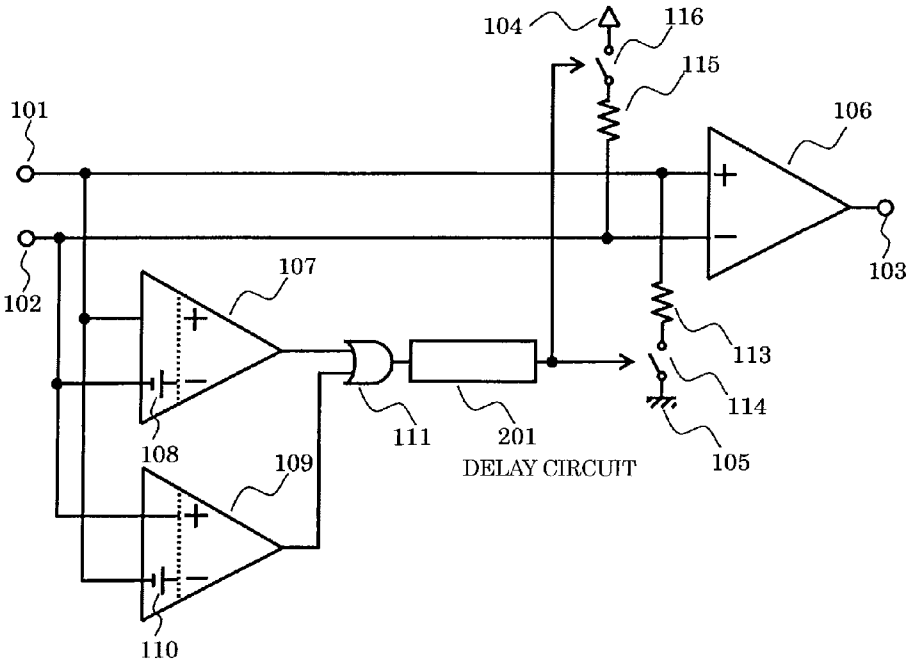
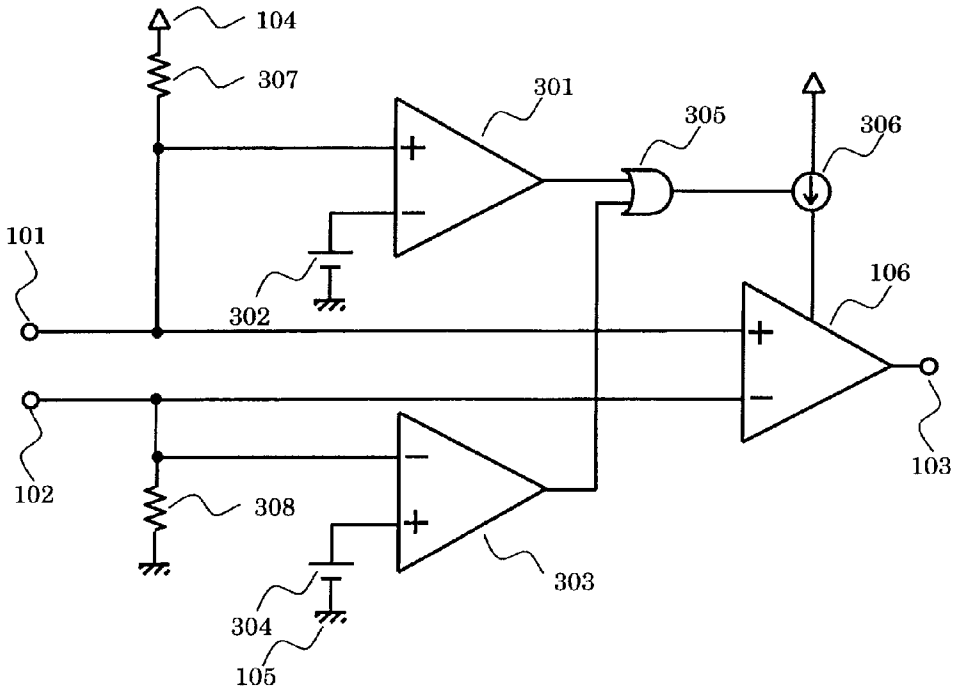

104
116
115
101
106
102
107
103
113
114
108
111
201
DELAY CIRCUIT
105
109
110

FIG. 3

PRIOR ART



OPERATIONAL AMPLIFIER

RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. §119 to Japanese Patent Application No. 2013-039652 filed on Feb. 28, 2013, the entire content of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an operational amplifier and more particularly to an operational amplifier capable of preventing, without restricting an input signal voltage range, an output terminal from becoming inconstant when an input terminal is open circuited.

[0004] 2. Background Art

[0005] FIG. **3** is a circuit diagram of a conventional operational amplifier. The conventional operational amplifier is comprised of comparators **301** and **303**, reference voltage circuits **302** and **304**, an OR circuit **305**, a constant current circuit **306**, an operational amplifier **106**, resistors **307** and **308**, input terminals **101** and **102**, an output terminal **103**, a supply terminal **104**, and a ground terminal **105**.

[0006] The operation of the conventional operational amplifier will be described.

[0007] The comparator **301** outputs a high signal when the voltage of a non-inverting input terminal exceeds the voltage of the reference voltage circuit **302**. The voltage of the reference voltage circuit **302** is set to a voltage that is lower than a voltage VDD of the supply terminal **104**. When the input terminal **101** is placed in an open state, the non-inverting input terminal of the comparator **301** is pulled up to the voltage VDD by the resistor **307**. This enables the comparator **301** to detect that the input terminal **101** has been open circuited.

[0008] The comparator **303** outputs the High signal when the voltage of the inverting input terminal reduces to be lower than the voltage of the reference voltage circuit **304**. The voltage of the reference voltage circuit **304** is set to a voltage that is higher than a voltage VSS of the ground terminal **105**. If the input terminal **102** is open circuited, then the inverting input terminal of the comparator **303** is pulled down to the voltage VSS by the resistor **308**. This enables the comparator **303** to detect that the input terminal **102** has been open circuited.

[0009] If an output signal of either one of the comparator **301** and the comparator **303** becomes a high signal, then the OR circuit **305** outputs a high signal. The constant current circuit **306** stops, so that the output terminal **103** of the operational amplifier **106** exhibits high impedance, making it possible to externally notify that the input terminal of the operational amplifier has been open circuited (refer to, for example, Patent Document 1).

[0010] [Patent Document 1] Japanese Patent Application Laid-Open No. 2003-143239

[0011] However, according to the conventional operational amplifier, there has been a problem in that an input terminal resistance cannot be increased in a normal operation mode, thus inconveniently restricting the voltage range of input signals that can be handled by the operational amplifier.

[0012] There has been another problem in that the output of the output terminal becomes inconstant when the input terminal is open circuited, resulting in an unstable operation of a circuit connected to the output terminal of the operational amplifier.

SUMMARY OF THE INVENTION

[0013] The present invention has been made to solve the problems described above and an object of the invention is to provide an operational amplifier that is capable of increasing an input terminal resistance in a normal operation mode and capable of detecting that an input terminal has been open circuited without restricting the voltage range of an input signal that can be handled by the operational amplifier.

[0014] To this end, an operational amplifier in accordance with the present invention has the following configuration.

[0015] The operational amplifier includes: a first comparator which has a non-inverting input terminal of the operational amplifier connected to a non-inverting input terminal thereof and which has an inverting input terminal of the operational amplifier connected to an inverting input terminal thereof having an input offset voltage; a second comparator which has an inverting input terminal of the operational amplifier connected to the non-inverting input terminal thereof and which has the non-inverting input terminal of the operational amplifier connected to an inverting input terminal thereof having an input offset voltage; an amplifier which has the non-inverting input terminal of the operational amplifier connected to a non-inverting input terminal thereof and which has the inverting input terminal of the operational amplifier connected to an inverting input terminal thereof; a logic circuit connected to an output terminal of the first comparator and an output terminal of the second comparator; a first resistor and a first switch which are provided between the non-inverting input terminal and a ground terminal of the operational amplifier and which are connected in series; and a second resistor and a second switch which are provided between the inverting input terminal and a supply terminal of the operational amplifier and which are connected in series.

[0016] According to the present invention, the comparators detect that the input terminal is open circuited, and the input terminal resistance can be increased in the normal operation mode by pulling down or pulling up the input terminal only when the input terminal is open circuited. This makes it possible to detect that the input terminal has been open circuited without restricting the voltage range of an input signal that can be handled by the operational amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. **1** is a circuit diagram of an operational amplifier according to a first embodiment of the present invention;

[0018] FIG. **2** is a circuit diagram of an operational amplifier according to a second embodiment of the present invention; and

[0019] FIG. **3** is a circuit diagram of a conventional operational amplifier.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0020] FIG. **1** is a circuit diagram of an operational amplifier according to a first embodiment. The operational amplifier according to the first embodiment is comprised of comparators **107**, **109**, an OR circuit **111**, switches **114**, **116**, an

operational amplifier **106**, resistors **113**, **115**, input terminals **101**, **102**, an output terminal **103**, a supply terminal **104**, and a ground terminal **105**.

[0021] The comparator **107** has a non-inverting input terminal thereof connected to the input terminal **101**, a inverting input terminal thereof connected to the input terminal **102**, and an output terminal thereof connected to a first input terminal of the OR circuit **111**. The comparator **109** has an inverting input terminal thereof connected to the input terminal **101**, the non-inverting input terminal thereof connected to the input terminal **102**, and the output terminal thereof connected to the second input terminal of the OR circuit **111**. An output of the OR circuit **111** is connected to the switch **116** and the switch **114** to control the ON/OFF thereof. The operational amplifier **106** has the non-inverting input terminal thereof connected to the input terminal **101**, the inverting input terminal thereof connected to the input terminal **102**, and the output thereof connected to the output terminal **103**. The resistor **115** has one terminal thereof connected to the switch **116** and the other terminal thereof connected to the input terminal **102**. The other terminal of the switch **116** is connected to the supply terminal **104**. The resistor **113** has one terminal thereof connected to the switch **114** and the other terminal thereof connected to the input terminal **101**. The other terminal of the switch **114** is connected to the ground terminal **105**.

[0022] The operation of the operational amplifier according to the first embodiment will be described.

[0023] The comparator **107** has an offset **108** set at the inverting input terminal thereof Further, the comparator **109** has an offset **110** set at the inverting input terminal thereof. The voltage of the input terminal **101** will be denoted by V+, the voltage of the input terminal **102** will be denoted by V−, the voltage of the offset **108** will be denoted by VA, and the voltage of the offset **110** will be denoted by VB.

[0024] If (V+)>(V−)+(VA), then the comparator **107** outputs a high signal, while the comparator **109** outputs a low signal. This is expressed as follows.

$$(V+)-(V-)>(VA) \tag{1}$$

[0025] If the potential difference between the input terminal **101** and the input terminal **102** exceeds the voltage of the offset **108**, then the comparator **107** outputs the high signal.

[0026] If (V−)>(V+)+(VB), then the comparator **109** outputs the high signal, while the comparator **107** outputs the low signal. This is expressed as follows.

$$(V+)-(V-)<-(VB) \tag{2}$$

[0027] If the potential difference between the input terminal **101** and the input terminal **102** becomes smaller than the voltage obtained by multiplying the voltage of the offset **110** by −, then the comparator **109** outputs the high signal.

[0028] Thus, the offset voltages VA and VB are set such that they are sufficiently large so as not to limit the voltage range of an input signal that can be handled by the operational amplifier and that the open circuiting of the input terminal can be detected.

[0029] The outputs of the comparator **107** and the comparator **109** are input to the OR circuit **111**, and if either one of the comparator **107** and the comparator **109** outputs the high signal, then the OR circuit **111** outputs the high signal, thus turning the switches **116** and **114** on. Then, the input terminal **102** is pulled up to the voltage VDD of the supply terminal **104**, while the input terminal **101** is pulled down to the voltage VSS of the ground terminal. Then, the output of the operational amplifier **106** is fixed to a low level.

[0030] The resistance values of the resistors **113** and **115** are set to be sufficiently large. Therefore, unless the input terminal **101** is open circuited, the input terminal **101** will not be pulled down to the voltage VSS even if the switch **114** is turned on. Similarly, even if the switch **116** is turned on, the input terminal **102** will not be pulled up to the voltage VDD.

[0031] When the input terminal **101** is open circuited, expression (2) is satisfied, so that the comparator **109** outputs the high signal. Upon receipt of the high signal output from the comparator **109**, the OR circuit **111** outputs the high signal. Upon receipt of the high signal output from the OR circuit, the switch **114** is turned on, connecting the non-inverting input terminal of the operational amplifier **106** to the voltage VSS through the resistor **113**. Upon receipt of the high signal output from the OR circuit **111**, the switch **116** is turned on, connecting the inverting input terminal of the operational amplifier **106** to the voltage VDD through the resistor **115**.

[0032] In this case, the input terminal **101** is open circuited, so that the non-inverting input terminal of the operational amplifier is pulled down to the voltage VSS. Hence, the operational amplifier **106** outputs the low signal to the output terminal **103**. Thus, the operational amplifier according to the first embodiment detects that the input terminal **101** has been open circuited and externally notifies to that effect by fixing the output of the operational amplifier **106** to the low level.

[0033] When the input terminal **102** is open circuited, expression (1) is satisfied, so that the comparator **107** outputs the high signal. The OR circuit **111** outputs the high signal upon receipt of the high signal output from the comparator **107**. The switches **116** and **114** turn on upon the receipt of the high signal.

[0034] In this case, the input terminal **102** is open circuited, so that the non-inverting input terminal of the operational amplifier **106** is pulled up to the voltage VDD. Hence, the operational amplifier **106** outputs the low signal to the output terminal **103**. Thus, the operational amplifier according to the first embodiment detects that the input terminal **102** has been open circuited and externally notifies to that effect by fixing the output of the operational amplifier **106** to the low level.

[0035] In a normal operation state wherein a voltage signal is applied to the input terminal **101** and the input terminal **102**, neither expression (1) nor (2) is satisfied, so that the comparators **107** and **109** output the low signal. The OR circuit **111** outputs the low signal, causing the switches **116** and **114** to turn off. Thus, the lowering of the input terminal resistance due to the resistors **115** and **113** can be prevented, making it possible to prevent the input signal voltage range from being restricted.

[0036] As described above, the operational amplifier according to the first embodiment allows the input terminal resistance to be increased during the normal operation state. This makes it possible to detect that an input terminal has been open circuited without restricting the voltage range of the input signals that can be handled by the operational amplifier.

Second Embodiment

[0037] FIG. **2** is a circuit diagram of an operational amplifier according to a second embodiment. The difference from operational amplifier according to the first embodiment is the addition of a delay circuit **201**. The delay circuit **201** is con-

nected between an OR circuit **111** and switches **116** and **114**. The rest of the circuit configuration is the same as that of the operational amplifier according to the first embodiment, so that the like reference numerals will be assigned and the description of the connections will be omitted.

[0038] The operation of the operational amplifier according to the second embodiment will be described.

[0039] A comparator **107** has an offset **108** set at an inverting input terminal. Further, a comparator **109** has an offset **110** set at an inverting input terminal. The voltage of an input terminal **101** will be denoted by V+, the voltage of an input terminal **102** will be denoted by V−, the voltage of the offset **108** will be denoted by VA, and the voltage of the offset **110** will be denoted by VB.

[0040] If (V+)>(V−)+(VA), then the comparator **107** outputs a high signal, while the comparator **109** outputs a low signal.

[0041] If (V−)>(V+)+(VB), then the comparator **109** outputs the high signal, while the comparator **107** outputs the low signal.

[0042] The outputs of the comparator **107** and the comparator **109** are input to an OR circuit **111**, and if either of the comparators **107** and **109** outputs the high signal, then the OR circuit **111** outputs the high signal, causing the switches **116** and **114** to turn on through the delay circuit **201**. Then, the input terminal **102** is pulled up to the voltage VDD of a supply terminal **104** and the input terminal **101** is pulled down to the ground terminal **105**, fixing the output of the operational amplifier **106** to a low level.

[0043] In this case, the delay circuit **112** operates not to output the high signal from the OR circuit **111** to a circuit in a following stage for a certain period of time or less thereby to prevent a malfunction from taking place due to a transient voltage fluctuation of the input terminal **101** or **102**.

[0044] As described above, the operational amplifier according to the second embodiment allows an input terminal resistance to be increased in a normal operation state, making it possible to detect that the input terminal has been open circuited without restricting the voltage range of input signals that can be handled by the operational amplifier. In addition, even if a transient voltage fluctuation takes place at an input terminal in the normal operation state, a malfunction of the circuit can be prevented.

What is claimed is:

1. An operational amplifier having an inverting input terminal, a non-inverting input terminal, and an output terminal, the operational amplifier comprising:

a first comparator having a non-inverting input terminal of the operational amplifier connected to a non-inverting input terminal thereof and an inverting input terminal of the operational amplifier connected to an inverting input terminal thereof that has an input offset voltage;

a second comparator having an inverting input terminal of the operational amplifier connected to a non-inverting input terminal thereof and a non-inverting input terminal of the operational amplifier connected to an inverting input terminal thereof that has an input offset voltage;

an amplifier having the non-inverting input terminal of the operational amplifier connected to a non-inverting input terminal thereof and the inverting input terminal of the operational amplifier connected to an inverting input terminal thereof;

a logic circuit connected to an output terminal of the first comparator and an output terminal of the second comparator;

a first resistor and a first switch which are provided between the non-inverting input terminal and a ground terminal of the operational amplifier and which are connected in series; and

a second resistor and a second switch which are provided between the inverting input terminal and a supply terminal of the operational amplifier and which are connected in series,

wherein the first switch and the second switch are controlled by an output signal of the logic circuit.

2. The operational amplifier according to claim **1**, wherein the output terminal of the logic circuit is provided with a delay circuit.

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