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(54) **AIR GAP FORMING TECHNIQUES BASED ON ANODIC ALUMINA FOR INTERCONNECT STRUCTURES**

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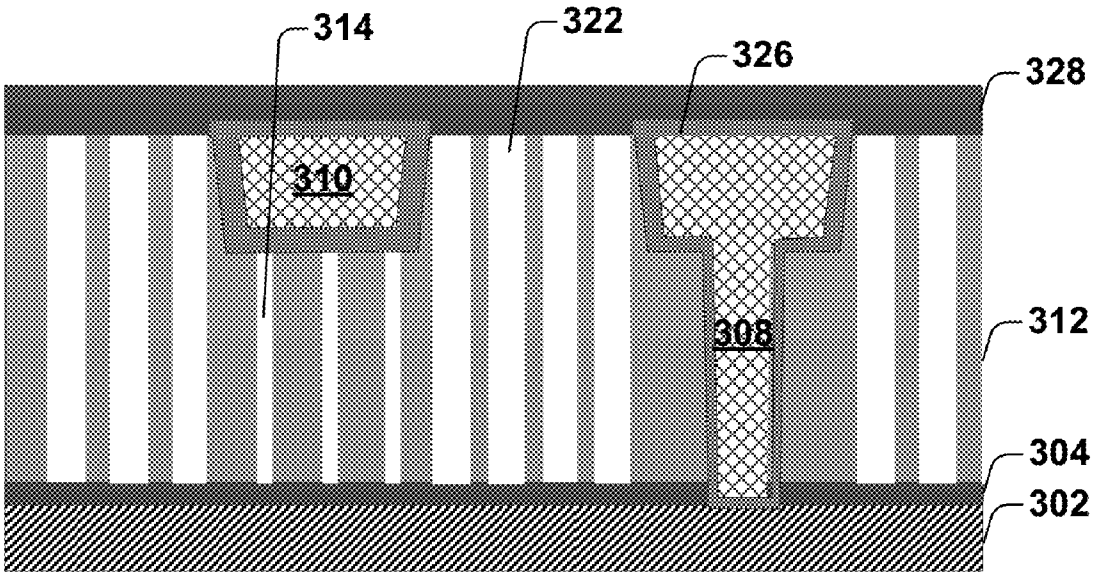
(57) **ABSTRACT**

An aluminum (Al) layer is formed over a semiconductor substrate. A selective portion of the Al layer is removed to form openings. The Al layer is anodized to obtain an alumina dielectric layer with a plurality of pores substantially perpendicular to a surface of the semiconductor substrate. The openings are filled with a conductive interconnect material. The pores are widened to form air gaps and a top etch stop layer is formed over the alumina dielectric layer.



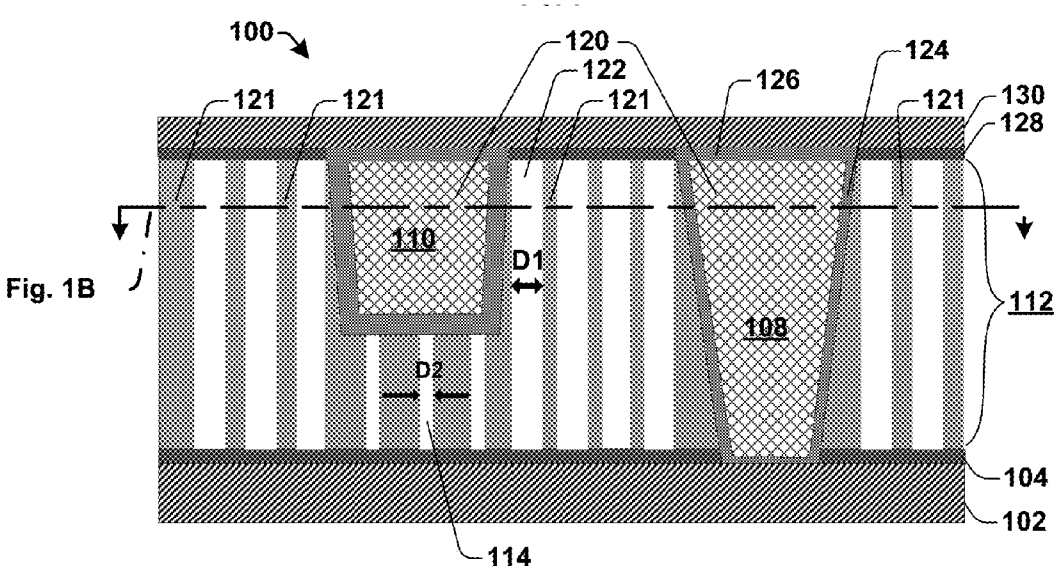


Fig. 1B

Fig. 1A

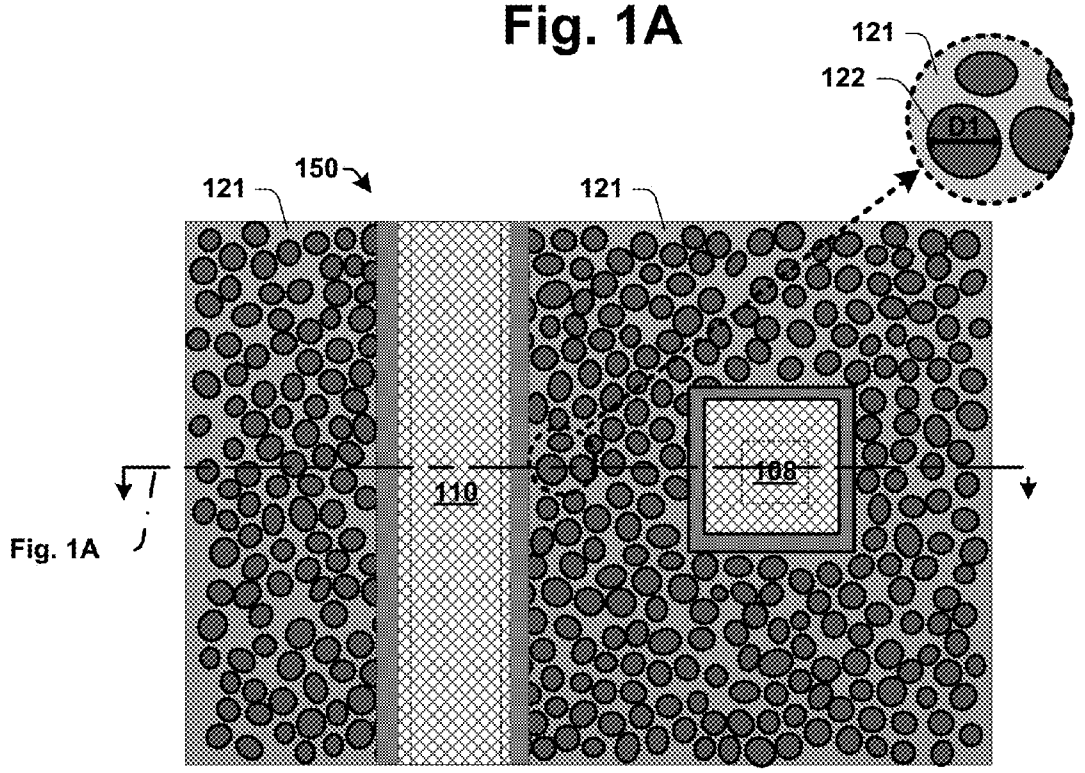


Fig. 1A

Fig. 1B

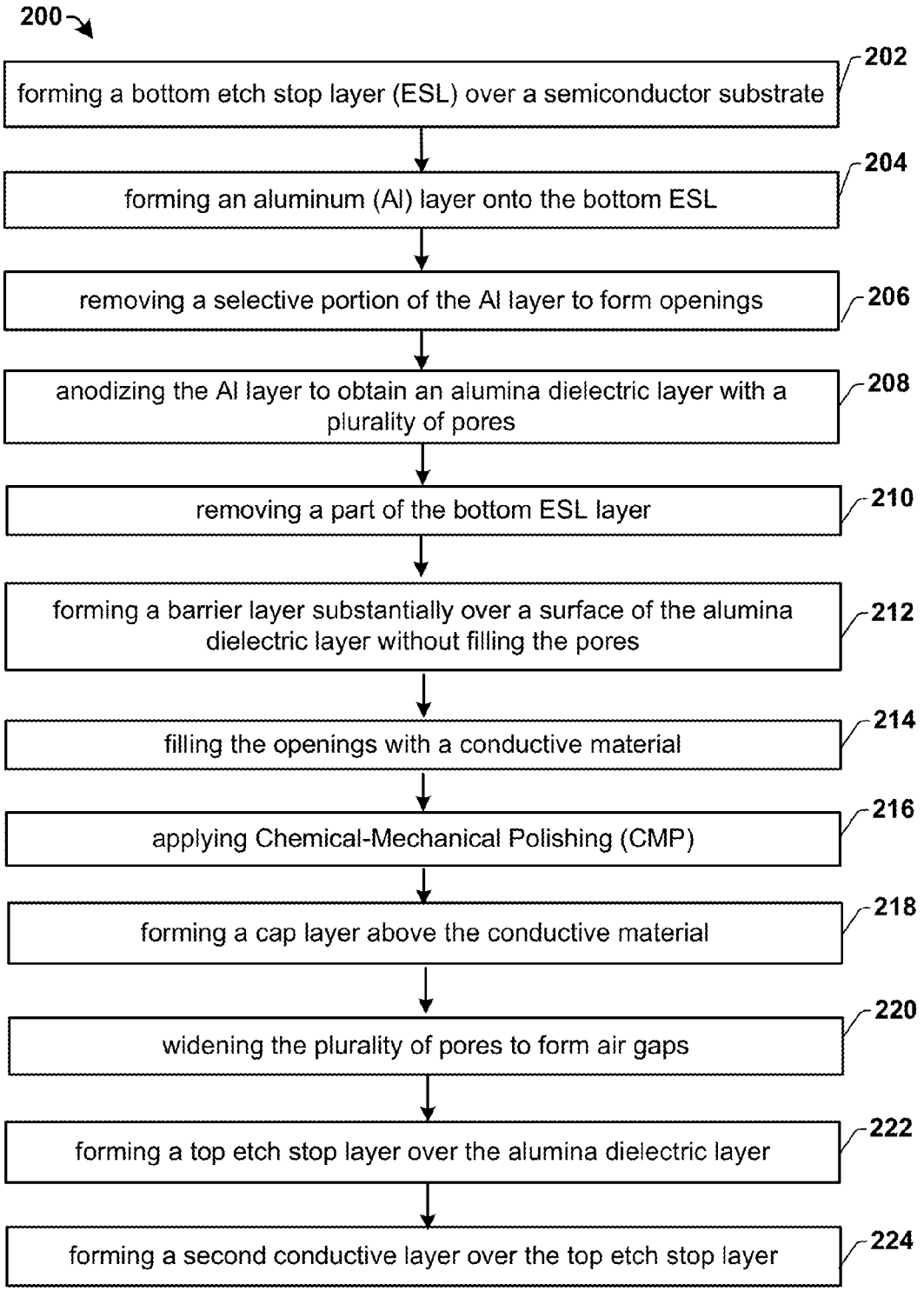

200
forming a bottom etch stop layer (ESL) over a semiconductor substrate
202
forming an aluminum (Al) layer onto the bottom ESL
204
removing a selective portion of the Al layer to form openings
206
anodizing the Al layer to obtain an alumina dielectric layer with a plurality of pores
208
removing a part of the bottom ESL layer
210
forming a barrier layer substantially over a surface of the alumina dielectric layer without filling the pores
212
filling the openings with a conductive material
214
applying Chemical-Mechanical Polishing (CMP)
216
forming a cap layer above the conductive material
218
widening the plurality of pores to form air gaps
220
forming a top etch stop layer over the alumina dielectric layer
222
forming a second conductive layer over the top etch stop layer
224

Fig. 2

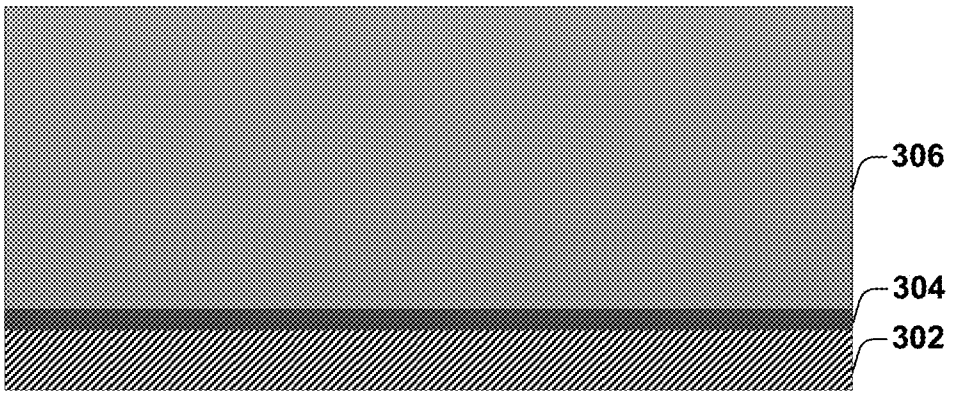


Fig. 3a

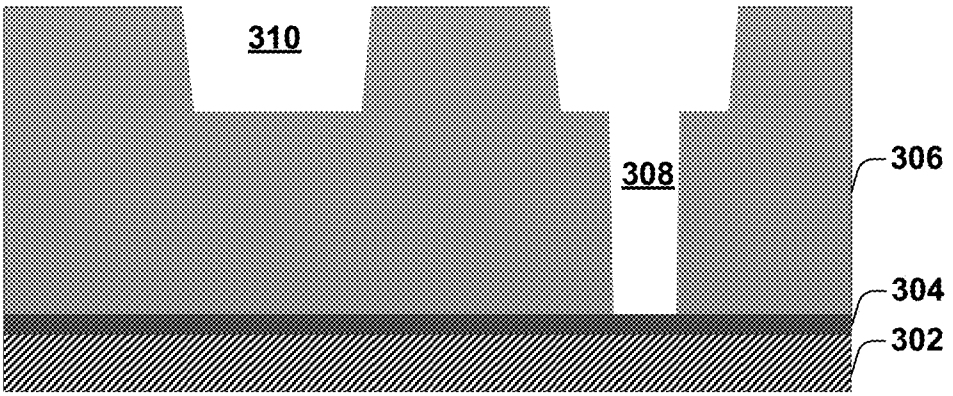


FIG. 3b

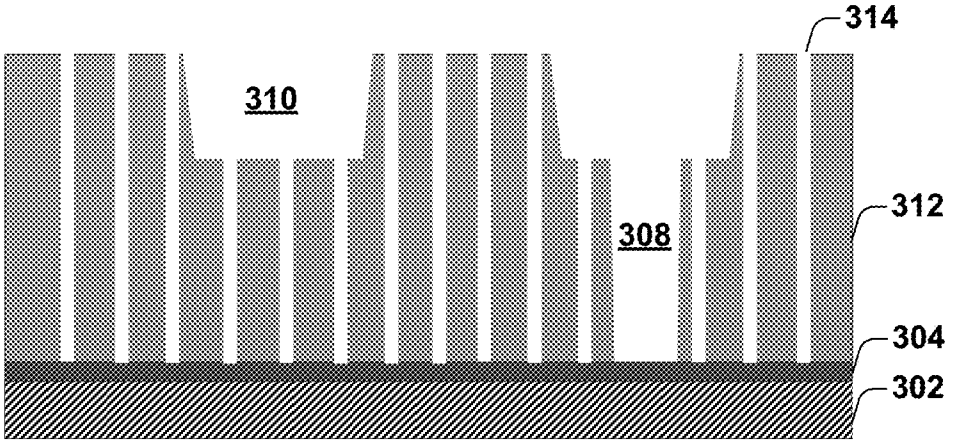


Fig. 3c

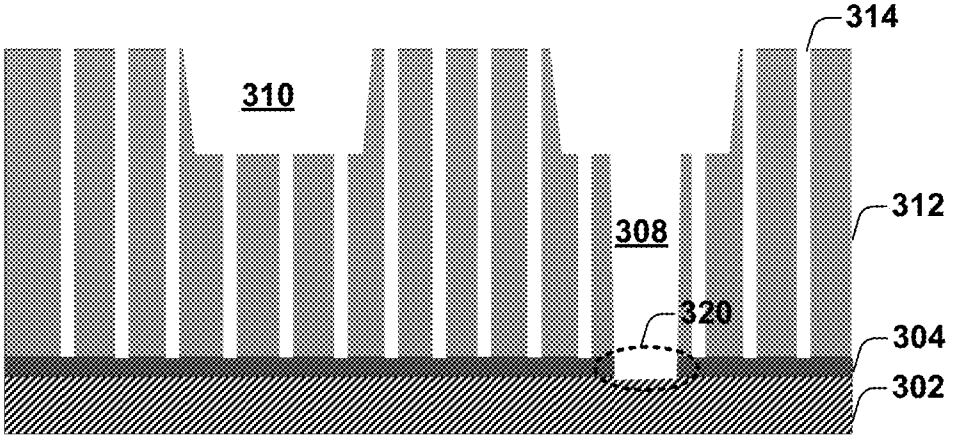


Fig. 3d

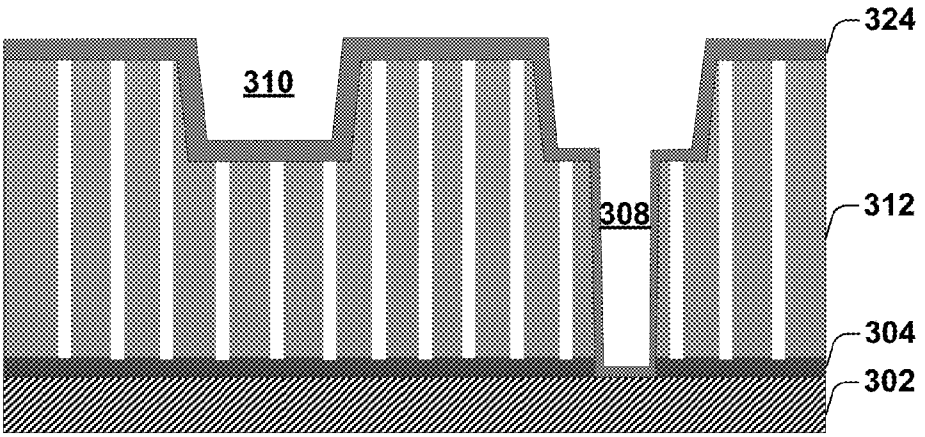


Fig. 3e

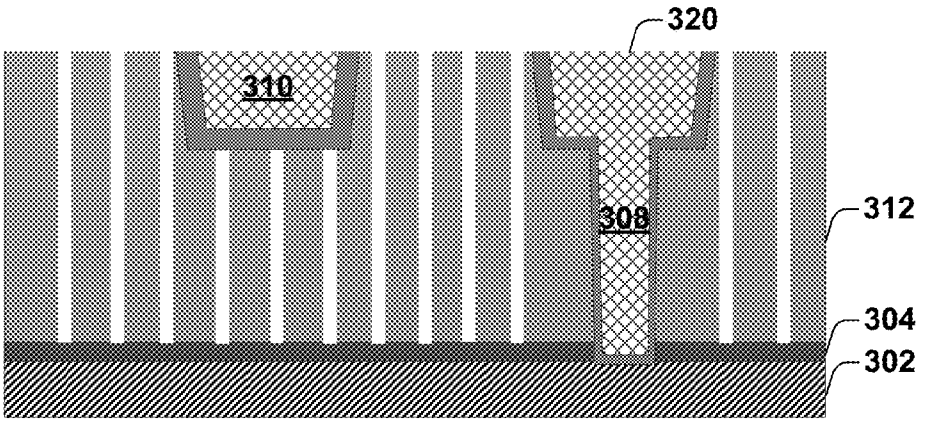


Fig. 3f

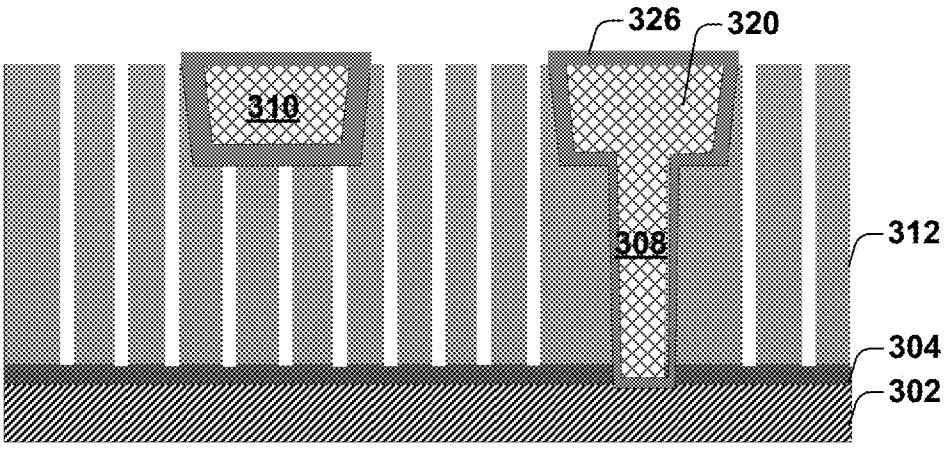


Fig. 3g

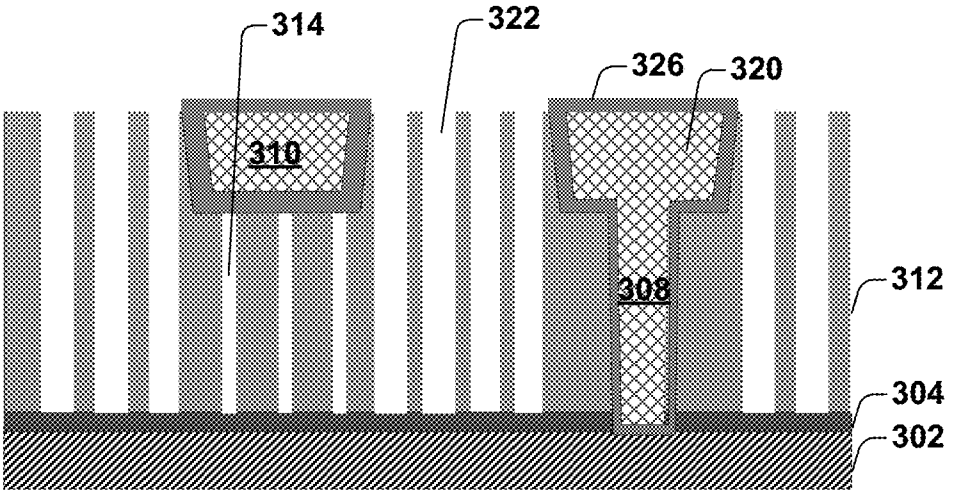


Fig. 3h

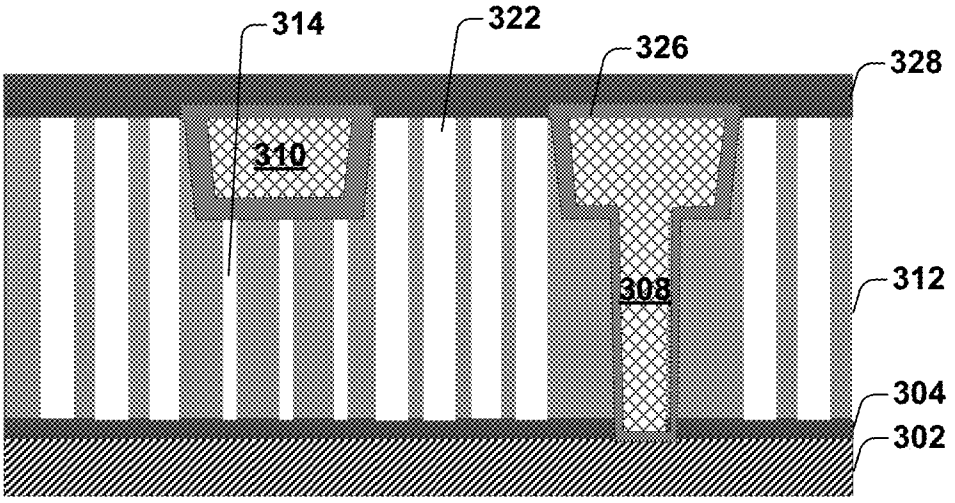


Fig. 3i

AIR GAP FORMING TECHNIQUES BASED ON ANODIC ALUMINA FOR INTERCONNECT STRUCTURES

[0001] As dimensions and feature sizes of semiconductor integrated circuits (ICs) are scaled down, the density of the elements forming the ICs is increased and the spacing between elements is reduced. Such spacing reductions are limited by light diffraction of photo-lithography, mask alignment, isolation and device performance among other factors. As the distance between any two adjacent conductive features decreases, the resulting capacitance increases, which will increase power consumption and time delay.

[0002] To reduce parasitic capacitance and correspondingly improve device performance, IC designers utilize low-k dielectrics. One kind of low-k material is produced by creating large voids or pores in a dielectric. Voids can have a dielectric constant of nearly 1, thereby reducing the overall dielectric constant of the porous material by increasing the porosity of the material. Large pores, also referred to as air gaps, can provide an extremely low-k dielectric between the two conductive features.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. **1**A illustrates a cross-sectional view of an interconnect structure in accordance with some embodiments.

[0004] FIG. **1**B illustrates a top view of the interconnect structure of FIG. **1**A in accordance with some embodiments.

[0005] FIG. **2** illustrates a flow diagram of a method of forming an air gap for interconnect structures in accordance with some embodiments.

[0006] FIGS. **3***a*-**3***i* illustrate cross-sectional views of a semiconductor substrate showing a method of forming an air gap for interconnect structures in accordance with some embodiments.

DETAILED DESCRIPTION

[0007] The description herein is made with reference to the drawings, wherein like reference numerals are generally utilized to refer to like elements throughout, and wherein the various structures are not necessarily drawn to scale. In the following description, for purposes of explanation, numerous specific details are set forth in order to facilitate understanding. It may be evident, however, to one skilled in the art, that one or more aspects described herein may be practiced with a lesser degree of these specific details. In other instances, known structures and devices are shown in block diagram form to facilitate understanding.

[0008] The existence of air gaps in low-k dielectrics can help to reduce an overall k value of the dielectrics. However, it is challenging further reducing the k value by increasing the volume of a single air gap or the density of air gaps considering requirements for the mechanical strength and the photolithography accuracy. The present disclosure relates to interconnect structures where a porous anodic alumina dielectric layer (for example, Al_2O_3) is applied as a low-k material. The alumina dielectric layer is initially formed with air-filled pores therein, and at least some of these air-filled pores are widened to form air gaps in the alumina dielectric layer. Because this alumina dielectric layer has a significant number of air gaps therein, it can provide a low-k value. For example, in some embodiments, the alumina dielectric layer can have an effective dielectric constant value is smaller than approximately 1.8. At the same time, the strong mechanical strength of the alumina structure provides a relative strong dielectric layer on which interconnect layers and/or device features can be built. Further, in some embodiments, self-aligned alumina anodizing processes can be beneficial in that they limit the amount of alignment required at some stages in manufacturing.

[0009] FIG. **1**A illustrates a cross-sectional view **100** of some embodiments of an interconnect structure of a semiconductor device, and FIG. **1**B shows a corresponding top view **150**. A first conductive layer **102** is over a semiconductor substrate (not shown). An alumina dielectric layer **112** is disposed over the first conductive layer **102**. The alumina dielectric layer **112** includes an alumina matrix **121** and a plurality of air gaps, for example, **122**. The air gaps are substantially perpendicular to a surface of the semiconductor substrate. A conductive body **108** is disposed in the alumina dielectric layer and electrically connects the first conductive layer **102** to a second conductive layer **130** over the alumina dielectric layer **112**. In some embodiments, a bottom etch stop layer **104** is disposed between the first conductive layer **102** and the alumina dielectric layer **112**. Another top etch stop layer **128** can be disposed between the alumina dielectric layer **112** and the second conductive layer **130**.

[0010] In some embodiments, the first conductive layer **102** is an interconnecting metal layer that can be one of multiple metal layers of the interconnect structures. In some other embodiments, the first conductive layer **102** can be active regions of devices disposed over or in the semiconductor substrate. For example, the first conductive layer can be source/drain regions of a FET device. The second conductive layer can also be an interconnecting metal layer, or can be a bond pad, solder bump or some other conductive layer.

[0011] In some embodiments, average diameters of the plurality of air gaps, for example, D**1** of the air gap **122** is approximately 9 nm. A volume density of the plurality of air gaps to the alumina dielectric layer can be larger than around 70%. Notably, in some embodiments, there is a region in the alumina dielectric layer **112** where a plurality of pores (e.g., **114**) is disposed. The pores (e.g., **114**) and air gaps (e.g., **122**) can be columnar in that sidewalls of a given pore/air gap can extend substantially vertically between top and bottom surfaces of alumina dielectric layer **112**, where a given pore/air gap can have a substantially constant diameter between top and bottom surfaces of alumina dielectric layer **112**. Respective diameters of the plurality of pores are smaller than the respective diameters of the plurality of air gaps. For example, a pore **114** that is substantially perpendicular to the surface of the semiconductor substrate is disposed in a lower portion of the alumina dielectric layer that is under a trench **110** disposed in an upper portion of the alumina dielectric layer with a diameter D**2** approximately 3 nm. The conductive body **108** can be a via as shown in FIG. **1** or a dual damascene structure similar to **308** shown in FIG. **3***i*. The conductive body **108** couples a first metal line in the first conductive layer **102** and a second metal line in the second conductive layer **130**. It will be appreciated that the relative sizes of the air gaps (e.g., **122**), pores (e.g., **114**), and conductive bodies **108**, **110**, illustrated in FIG. **1**A-**1**B are merely illustrative and that the relative sizes of these features can vary widely from what is shown.

[0012] FIG. **2** illustrates a flow diagram of some embodiments of a method of forming an air gap for interconnect structures.

[0013] While disclosed methods (e.g., methods **200**) are illustrated and described below as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

[0014] At **202**, a bottom etch stop layer (ESL) is formed over a semiconductor substrate. The semiconductor substrate may comprise any type of semiconductor material including a bulk silicon wafer, a binary compound substrate (e.g., GaAs wafer), or higher order compound substrates, with or without additional insulating or conducting layers formed thereover, among others.

[0015] At **204**, an aluminum (Al) layer is formed onto the bottom ESL. In some embodiments, for example, the Al layer has a thickness of from about 1000 Å to about 10000 Å. The Al layer can be deposited by physical vapor deposition (PVD).

[0016] At **206**, a selective portion of the Al layer is removed to form openings. In some embodiments, the openings comprise some trenches which extend along a horizontal surface of the semiconductor and some vias which extend vertically through the Al layer. In some embodiments, dual damascene structure is patterned during this step by via first, trench first or self-aligned process.

[0017] At **208**, the Al layer is anodized to obtain an alumina dielectric layer with a plurality of pores. In some embodiments, preparation conditions, for example, annealing to enhance grain size and to obtain homogeneous conditions for pore growth over large areas, or electropolishing to improve surface roughness are applied. In some embodiments for example, an anodizing voltage of about 5 V is applied and a copper plate is applied over the Al layer as a cathode. An electrolyte solution may comprise Hydrogen peroxide (H_2O_2), Phosphoric acid (H_3PO_4) or Sulfuric Acid (H_2SO_4) is applied. The anodizing process can be applied by more than one step of anodizing in different conditions with different electrolyte. For example, a 1.8 M Sulfuric Acid (H_2SO_4) aqua-solution is applied as an electrolyte. A temperature of around 5° C. is applied during anodizing. A substantially ordered plurality of pores with a diameter of about 3 nm is achieved.

[0018] At **210**, a part of the bottom ESL that is under a bottom surface of the openings is removed.

[0019] At **212**, a barrier layer is formed substantially over a surface of the alumina dielectric layer without filling the pores.

[0020] At **214**, a conductive interconnect material, for example, copper, is filled to the openings.

[0021] At **216**, a Chemical-Mechanical Polishing (CMP) process is applied to smooth surfaces and remove a top part of the conductive interconnect material that is not needed.

[0022] At **218**, a cap layer is formed above the filled conductive interconnect material. The cap layer can help to protect the filled conductive interconnect material from subsequent chemical reaction processes.

[0023] At **220**, the plurality of pores are widened to form air gaps. In some embodiments, a wet etching process comprising a wet etchant may be applied within a processing chamber held at a temperature of from approximately 0° C. to approximately 50° C. For example, the wet etchant may comprise Phosphoric acid (H_3PO_4) or Sulfuric Acid (H_2SO_4). Diameters of the widened pores are related to but not limited to temperature, time of reaction and chemical concentration. For example, in some embodiments, the workpiece can be subjected to a 5% (by weight) H_3PO_4 solution at 25° C. for approximately 5 minutes, which can widen pores to about 9 nm in diameter, on average.

[0024] At **222**, a top etch stop layer is formed over the alumina dielectric layer.

[0025] At **224**, a second conductive layer is formed over the top etch stop layer.

[0026] FIGS. **3***a*-**3***i* illustrate some embodiments of cross-sectional views and corresponding top-sectional views of a semiconductor substrate showing a method of forming an air gap for interconnect structures. Although FIGS. **5-13** are described in relation to method **200**, it will be appreciated that the structures disclosed in FIGS. **3***a*-**3***i* are not limited to such a method.

[0027] As shown in FIG. **3***a*, a bottom etch stop layer (ESL) **304** is formed over a semiconductor substrate and an aluminum (Al) layer **306** is formed onto the bottom ESL **304**. A previous layer **302** can be either a conductive layer or a dielectric layer formed previously.

[0028] As shown in FIG. **3***b*, a selective portion of the Al layer **306** is removed to form openings. In some embodiments, the openings comprise a trench **310** that does not extend through a bottom surface of the Al layer **306** and a via **308** that extends through the bottom surface of the Al layer **306**. In some embodiments, a trench first, via first, or self-aligned dual damascene process is applied to form the openings that extend through the bottom surface of the Al layer **306**.

[0029] As shown in FIG. **3***c*, the Al layer **306** is anodized to obtain an alumina dielectric layer **312** with a plurality of pores **314**. Notably, the plurality of pores **314** are substantially perpendicular to a surface of the semiconductor substrate. The Al layer **306** is anodized by applying an electric field substantially perpendicular to a surface of the semiconductor substrate.

[0030] As shown in FIG. **3***d*, a part of the bottom ESL **320** that is under a bottom surface of the opening **308** is removed. The part **320** is kept during forming the openings to protect layers underneath from chemical reactions and is removed after anodizing.

[0031] As shown in FIG. **3***e*, a barrier layer **324**, for example, comprising Titanium (Ta), Titanium Nitride (TaN), Cobalt (Co) or their alloy is formed and/or a seed layer, for example, comprising copper, is formed substantially over a surface **330** of the alumina dielectric layer **312** without filling the pores. The barrier layer **324** remains substantially over the surface **330** of the alumina dielectric layer **312**.

[0032] As shown in FIG. **3***f*, a conductive interconnect material **320**, for example, copper, is used to fill the openings **308** and **310**. For example, electro-plating can be used to fill the openings **308**, **310** with the conductive interconnect material **320**. A Chemical-Mechanical Polishing (CMP) process is applied to smooth surfaces and remove a top part that is not needed.

[0033] As shown in FIG. **3***g*, a cap layer **326**, for example, comprising Co cap and a silicide material, is formed above the filled conductive interconnect material **320**.

[0034] As shown in FIG. **3***h*, the plurality of pores are widened to form air gaps **322**. Notably, in some embodiments, a plurality of pores **314** are disposed underneath the trench **310** and are not widened. Thus, pores **314** under the trench **310** can have a first average diameter, while air gaps between trenches can have a second average diameter that is larger than the first average diameter.

[0035] As shown in FIG. **3***i*, a top etch stop layer **328** is formed over the alumina dielectric layer **312**.

[0036] It will be appreciated that while reference is made throughout this document to exemplary structures in discussing aspects of methodologies described herein, that those methodologies are not to be limited by the corresponding structures presented. Rather, the methodologies (and structures) are to be considered independent of one another and able to stand alone and be practiced without regard to any of the particular aspects depicted in the Figs. Additionally, layers described herein, can be formed in any suitable manner, such as with spin on, sputtering, growth and/or deposition techniques, etc.

[0037] Also, equivalent alterations and/or modifications may occur to those skilled in the art based upon a reading and/or understanding of the specification and annexed drawings. The disclosure herein includes all such modifications and alterations and is generally not intended to be limited thereby. For example, although the figures provided herein, are illustrated and described to have a particular doping type, it will be appreciated that alternative doping types may be utilized as will be appreciated by one of ordinary skill in the art.

[0038] In addition, while a particular feature or aspect may have been disclosed with respect to only one of several implementations, such feature or aspect may be combined with one or more other features and/or aspects of other implementations as may be desired. Furthermore, to the extent that the terms "includes", "having", "has", "with", and/or variants thereof are used herein, such terms are intended to be inclusive in meaning—like "comprising." Also, "exemplary" is merely meant to mean an example, rather than the best. It is also to be appreciated that features, layers and/or elements depicted herein are illustrated with particular dimensions and/or orientations relative to one another for purposes of simplicity and ease of understanding, and that the actual dimensions and/or orientations may differ substantially from that illustrated herein.

[0039] In some embodiments, a semiconductor device comprises a first conductive layer disposed over a semiconductor substrate and a second conductive layer disposed over the first conductive layer. An alumina dielectric layer is arranged between the first and second conductive layers to provide electrical isolation between the first and second conductive layers. The alumina dielectric layer includes an alumina matrix with a plurality of air gaps extending there through. The air gaps extend substantially perpendicular to a surface of the semiconductor substrate as they extend through the alumina matrix.

[0040] In other embodiments, the present disclosure relates to a method of forming an air gap for interconnect structures. The method comprises forming an aluminum (Al) layer over a semiconductor substrate, removing a selective portion of the Al layer to form openings, anodizing the Al layer to obtain an alumina dielectric layer with a plurality of pores substantially perpendicular to a surface of the semiconductor substrate, filling the openings with a conductive interconnect material, widening the pores to form air gaps and forming a top etch stop layer over the alumina dielectric layer.

[0041] In yet other embodiments, the present disclosure relates to a method of forming an air gap for interconnect structures. The method comprises forming an etch stop layer (ESL) over a semiconductor substrate, forming an aluminum (Al) layer onto the ESL, removing a selective portion of the Al layer to form openings, anodizing the Al layer to obtain an alumina dielectric layer with a plurality of pores substantially perpendicular to a surface of the semiconductor substrate, removing a part of the ESL layer that is under a bottom surface of the openings, filling the openings with a conductive interconnect material and widening the plurality of pores to form air gaps.

1. A semiconductor device comprising:

a first conductive layer disposed over a semiconductor substrate;

a second conductive layer disposed over the first conductive layer; and

an alumina dielectric layer arranged between the first and second conductive layers to provide electrical isolation between the first and second conductive layers, the alumina dielectric layer including an alumina matrix with a plurality of air gaps extending there through, wherein the air gaps extend substantially perpendicular to a surface of the semiconductor substrate as they extend through the alumina matrix.

2. The semiconductor device of claim **1**, wherein an effective dielectric constant of the alumina dielectric layer is less than approximately 1.8.

3. The semiconductor device of claim **1**, wherein the plurality of air gaps in the alumina dielectric layer have diameters which are, on average, approximately 9 nm.

4. The semiconductor device of claim **1**, further comprising:

a trench in an upper portion of the alumina dielectric layer;

wherein the alumina dielectric layer further comprises a plurality of pores disposed underneath the trench and wherein the air gaps are arranged in the alumina dielectric layer on either side of the trench, wherein the plurality of pores have respective diameters which are, on average, smaller than respective diameters of the plurality of air gaps.

5. The semiconductor device of claim **4**, wherein the plurality of pores have average diameters of approximately 3 nm.

6. The semiconductor device of claim **1**, further comprising a conductive body disposed in the alumina dielectric layer to electrically connect the first conductive layer to the second conductive layer.

7. The semiconductor device of claim **6**, wherein the conductive body is a via or a dual damascene structure to couple a first metal line in the first conductive layer to a second metal line in the second conductive layer.

8. The semiconductor device of claim **1**, further comprising:

an etch stop layer disposed between the first conductive layer and the alumina dielectric layer.

9-20. (canceled)

21. A semiconductor device comprising:

a first conductive layer disposed over a semiconductor substrate;

a second conductive layer disposed over the first conductive layer;

an alumina dielectric layer arranged between the first and second conductive layers to provide electrical isolation between the first and second conductive layers; and

a conductive body extending through the alumina dielectric layer to electrically connect the first conductive layer to the second conductive layer;

wherein the alumina dielectric layer includes an alumina matrix with a plurality of air gaps therein, wherein the air gaps in aggregate consume more than 70% of a total volume of the alumina dielectric layer and the alumina matrix consumes less than 30% of the total volume of the alumina dielectric layer.

22. The semiconductor device of claim **21**, further comprising:

an upper etch stop layer disposed between the second conductive layer and the alumina dielectric layer; and

a lower etch stop layer disposed between the first conductive layer and the alumina dielectric layer;

wherein the plurality of air gaps extends through the alumina dielectric layer and reaches onto the upper and lower etch stop layers.

23. The semiconductor device of claim **21**, wherein an effective dielectric constant of the alumina dielectric layer is less than approximately 1.8.

24. The semiconductor device of claim **21**, wherein the plurality of air gaps in the alumina dielectric layer have diameters which are, on average, approximately 9 nm.

25. The semiconductor device of claim **21**, the conductive body further comprising:

a trench line disposed in an upper portion of the alumina dielectric layer; and

a via with a smaller width than that of the trench line, disposed in an lower portion of the alumina dielectric layer under the trench line.

26. The semiconductor device of claim **25**, wherein the alumina dielectric layer further comprises a plurality of pores disposed underneath the trench line, wherein the plurality of pores have respective diameters which are, on average, smaller than respective diameters of the plurality of air gaps.

27. The semiconductor device of claim **26**, wherein the plurality of pores have average diameters of approximately 3 nm.

28. The semiconductor device of claim **21**, further comprising:

an etch stop layer disposed between the first conductive layer and the alumina dielectric layer.

29. A semiconductor device comprising:

a first conductive layer disposed over a semiconductor substrate;

a second conductive layer disposed over the first conductive layer; and

an alumina dielectric layer arranged between the first and second conductive layers to provide electrical isolation between the first and second conductive layers, the alumina dielectric layer including an alumina matrix with a plurality of air gaps extending there through, wherein the air gaps extend substantially perpendicular to a surface of the semiconductor substrate as they extend through the alumina matrix;

wherein an effective dielectric constant of the alumina dielectric layer is less than approximately 1.8.

30. The semiconductor device of claim **29**, wherein the plurality of air gaps in aggregate consume more than 70% of a total volume of the alumina dielectric layer.

31. The semiconductor device of claim **29**, further comprising:

a dual damascene structure comprising a trench line and an underlying via disposed in the alumina dielectric layer to electrically connect the first conductive layer to the second conductive layer.

32. The semiconductor device of claim **31**, the alumina dielectric layer further comprising:

a plurality of pores disposed under the trench line, extending substantially perpendicular to a surface of the semiconductor substrate; wherein the plurality of pores have respective diameters which are, on average, smaller than respective diameters of the plurality of air gaps.

* * * * *