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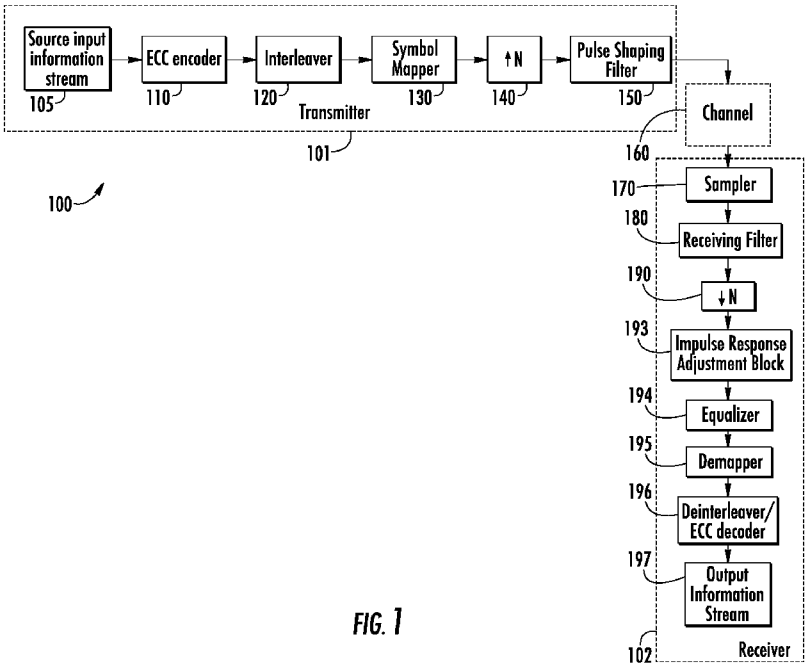

FIG. 1

(57) Abstract: In some embodiments, a bandwidth constrained equalized transport (BCET) communication system comprises a transmitter that transmits a signal, a communication channel that transports the signal, and a receiver that receives the signal. The transmitter can comprise a pulse-shaping filter that intentionally introduces memory into the signal, and an error control code encoder that is a low- density parity-check (LDPC) error control code encoder. The error control encoder comprises code that is optimized based on the intentionally introduced memory into the signal, a code rate, a signal -to-noise ratio, and an equalizer structure in the receiver. In some embodiments, the communication system is bandwidth constrained, and the transmitted signal comprises an information rate that is higher than for an equivalent system without intentional introduction of the memory at the transmitter.

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BANDWIDTH CONSTRAINED COMMUNICATION SYSTEMS WITH OPTIMIZED LOW-DENSITY PARITY-CHECK CODES

RELATED APPLICATIONS

[001] The application claims the benefit of: 1) U.S. Provisional Patent Application No. 62/676,942 filed on May 26, 2018, and entitled "Reduced-Complexity Receiver Architecture Design in Bandwidth Constrained Communication Systems"; and 2) U.S. Provisional Patent Application No. 62/795,993 filed on January 23, 2019, and entitled "Optimized Low-Density Parity-Check Codes for Bandwidth Constrained Communication Systems"; and 3) U.S. Non-Provisional Patent Application No. 16/418,798 filed on May 21, 2019, and entitled "Bandwidth Constrained Communication Systems With Optimized Low-Density Parity-Check Codes"; all of which are hereby incorporated by reference for all purposes.

BACKGROUND

[002] Communication systems strive to reliably transmit a high quantity of information over a channel of a given bandwidth. In traditional design of communication systems, predominantly modulation formats without memory are used. These systems cannot approach the theoretical bounds of spectral efficiency, also known as the Shannon limit or Shannon capacity without the aid of error control coding (ECC). Coupled with sophisticated encoding schemes that jointly optimize the modulation and error control coding, communication systems without memory can perform close to the theoretical bounds. Error-control codes typically append redundant information bits, or symbols, so as to achieve resilience and/or improved performance in the presence of obstacles in the process of the information transfer, such as noise and distortions.

[003] Improved performance can be achieved with so-called iterative decoding at the receiver, in which the reliability estimates on the received information symbols are exchanged between the constituent codes' decoders multiple times, with an improved estimate on the information symbols being obtained with each additional iteration.

[004] The process of iterative decoding encompasses interleaving and de-interleaving processes. In these processes, the passing of the codewords between

multiple constituent decoders can include the permutation of the relevant information symbols corresponding to the pertinent constituent codes.

SUMMARY

[005] In some embodiments, a bandwidth constrained equalized transport (BCET) communication system comprises a transmitter that transmits a signal, a communication channel that transports the signal, and a receiver that receives the signal. The transmitter can comprise an error control code encoder, a pulse-shaping filter, and a first interleaver. The receiver can comprise a receiving filter, an information-retrieving equalizer, a deinterleaver with an error control code decoder, and a second interleaver. In some embodiments, the error control code encoder appends redundant information onto the signal, and the pulse-shaping filter in the transmitter intentionally introduces memory into the signal in the form of inter-symbol interference. The receiving filter can be matched to the pulse-shaping filter and the information-retrieving equalizer can be a trellis-based equalizer. In some embodiments, the information-retrieving equalizer, the second interleaver, and the deinterleaver with the error control code decoder are joined in an iterative turbo equalization loop. In some embodiments, the error control code encoder is a low-density parity-check (LDPC) error control code encoder, and the error control encoder comprises code that is optimized based on the intentionally introduced memory into the signal, a code rate, a signal-to-noise ratio, and an equalizer structure in the receiver. In some embodiments, the communication system is bandwidth constrained, and the transmitted signal comprises an information rate that is higher than for an equivalent system without intentional introduction of the memory at the transmitter.

[006] In some embodiments, a method comprises providing a signal comprising symbols, encoding the symbols using an error control code encoder in a transmitter of a communication system to produce encoded symbols, interleaving the encoded symbols using a first interleaver in the transmitter to produce interleaved symbols, intentionally introducing memory into the interleaved symbols in the form of inter-symbol interference using a pulse-shaping filter in the transmitter to produce pulse-shaped symbols, transmitting the pulse-shaped symbols to a receiver of the communication system over a physical memoryless channel with additive white Gaussian noise, receiving the transmitted pulse-shaped symbols using a receiving filter in the receiver to produce a receiving filtered signal, equalizing the receiving

filtered signal using an information-retrieving equalizer in the receiver to produce equalized symbols, deinterleaving the equalized symbols using a deinterleaver in the receiver to produce deinterleaved symbols, processing the deinterleaved symbols using a non-linear function block in the receiver to produce a non-linear signal, decoding the non-linear signal using an error control code decoder in the receiver to produce decoded symbols, and iteratively updating the decoded symbols using a turbo equalization loop in the receiver to produce updated decoded symbols after each iteration.

[007] In some embodiments of the above method, the turbo equalization loop in the receiver comprises iteratively repeating: equalizing iterated interleaved symbols using the information-retrieving equalizer to produce iterated equalized symbol likelihoods, deinterleaving the iterated equalized symbol likelihoods using a deinterleaver in the turbo equalization loop to produce iterated deinterleaved symbol likelihoods, transforming the iterated deinterleaved symbol likelihoods using a non-linear function to produce iterated non-linearly transformed symbol likelihoods, decoding the iterated non-linearly transformed symbol likelihoods to produce the updated decoded symbol likelihoods, and interleaving the updated decoded symbol likelihoods using a second interleaver in the turbo equalization loop to produce an iterated interleaved signal comprising the updated decoded symbols. In some embodiments of the above method, the error control code encoder appends redundant information onto the symbol stream, the error control code encoder is a low-density parity-check (LDPC) error control code encoder, and the error control encoder comprises code that is optimized based on the intentionally introduced memory into the signal, a code rate, a signal-to-noise ratio, and the receiver equalizer structure. In some embodiments of the above method, the receiving filter is matched to the pulse-shaping filter. In some embodiments, the information-retrieving equalizer is a trellis-based equalizer. In some embodiments of the above method, the non-linear function block transforms the deinterleaved symbols according to a non-linear function. In some embodiments of the above method, the communication system is bandwidth constrained, and the transmitted signal comprises an information rate that is higher than for an equivalent system without intentional introduction of the memory at the transmitter.

[008] In some embodiments, a method comprises: a. providing a bandwidth constrained equalized transport (BCET) communication system comprising a

transmitter, a receiver, a partial channel response, a channel equalization structure, a low-density parity-check (LDPC) error control code encoder in the transmitter, and a non-linear function block in the receiver; and providing input parameters comprising a codeword length, a code rate, a level of parallelism, and a maximum variable degree; b. initializing a variable node degree distribution; c. calculating a check node degree distribution for the provided input parameters; d. optimizing a variable node degree distribution for the LDPC codes in the LDPC error control encoder, and non-linear parameters of a non-linear function using a density evolution algorithm for partial response channels; e. calculating a corresponding threshold; f. repeating steps b. – e. for different input parameters to generate a database of possible solutions; and g. recalculating the variable node degree distribution and the check node degree distribution for a part of a parity check matrix (H_1) excluding a double diagonal matrix.

BRIEF DESCRIPTION OF THE DRAWINGS

[009] FIG. 1 shows a block diagram of an example of a bandwidth constrained equalized transport (BCET) communication system, in accordance with some embodiments.

[0010] FIG. 2 shows an example of a frequency response of a pulse shaping filter, with 300% bandwidth reduction compared to Nyquist signaling, in accordance with some embodiments.

[0011] FIG. 3 shows examples of achievable information rates for signals in a BCET communication system using three different optimized pulse shaping filters, in accordance with some embodiments.

[0012] FIG. 4 shows a block diagram of a turbo equalization loop in a BCET system, in accordance with some embodiments.

[0013] FIG. 5 shows frame error rate (FER) performance with different number of turbo iterations, in accordance with some embodiments.

[0014] FIG. 6 is a simplified flowchart for a process for optimizing low-density parity-check (LDPC) codes in BCET systems, in accordance with some embodiments.

[0015] FIG. 7 is a simplified flowchart for a process for generating a quasi-cyclic (QC) irregular repeat accumulator (IRA) code design in BCET systems, in accordance with some embodiments.

[0016] FIG. 8 is an example of a parity check matrix, in accordance with some embodiments.

[0017] FIG. 9 shows acheived FER and bit error rates (BER) for BCET systems with optimized LDPC codes, in accordance with some embodiments.

[0018] FIG. 10 shows achieved information rates for four code rates, in accordance with some embodiments.

[0019] FIG. 11 shows achieved information rates for various codeword lengths and various number of turbo iterations, in accordance with some embodiments.

[0020] FIG. 12 is a simplified flowchart for a process for BCET, in accordance with some embodiments.

[0021] FIG. 13 is a simplified flowchart for a process for BCET, in accordance with some embodiments.

DETAILED DESCRIPTION

[0022] The present invention includes systems and methods directed at improving the performance of bandwidth constrained systems and/or the capacity of communication systems and in particular with the aim of reducing the associated processing, or circuit implementation complexity. In some embodiments, the described systems and methods also simplify the receiver structure in bandwidth constrained systems. In some embodiments, the described communication systems and methods are referred to as bandwidth constrained equalized transport (BCET) systems and methods. The term "BCET communication system" (or "BCET system") as used herein is defined as a communication system that uses narrowband filtering in the transmitter to intentionally introduce memory into a signal, and equalization techniques in the receiver to account for the intentionally introduced memory. If properly designed, the achievable information rate in BCET systems can be improved over conventional communication systems that do not intentionally introduce memory in the signal.

[0023] BCET systems typically rely on equalization to mitigate the effect of bandwidth limitation. In particular, the systems with high spectral efficiency, or equivalently a considerable amount of bandwidth limitation, can be affected by distortions that induce a significant extension of the channel response duration, thus requiring long, and/or complex equalization structures to appropriately handle the effects of the induced intersymbol interference. Complex equalizers required to implement the sophisticated encoding schemes not only significantly increase the complexity and the practical realization of their systems, but also increase the overall system power consumption.

[0024] The overall performance and the underlying complexity of the equalizer used in communication systems represent critical concerns in their practical realizations, and are of particular importance for wideband systems with high throughput. These properties result in both higher reliability and/or capacity in communication systems, as well as a lower receiver and system overall power dissipation and an easier practical implementation.

[0025] In some embodiments, a BCET system includes a receiver comprising an equalizer, an optional pre-processing approach applied to the incoming waveforms (i.e., samples) availing the utilization of a lower complexity information retrieving equalizer, and an error control decoder matched to the encoder in the transmitter and

to the bandwidth constrained channel. Advantageously, BCET systems can obtain superior system performance, with lower system complexity, latency and power dissipation. In some cases, BCET systems employ digital reshaping at the receiver in a specific way, so as to avail utilization of lower complexity information retrieving equalizers in the receiver processing chain.

[0026] In some embodiments, a method for receiving data in a BCET communications system includes the following steps: (1) shortening the channel response by means of a specific signal processing step; (2) equalization, or information retrieval by an appropriate equalizer, and (3) error control decoding. The equalizers in the receiver can be implemented in the time domain or the frequency domain.

[0027] In some embodiments, a method for complexity reduction of equalizers in communication systems, consists of the following steps: (1) acquiring a full length channel response, i.e., for symbol patterns equal in length (or longer) to the length of the channel spread, (2) reducing the set of channel responses by averaging (e.g., weighted averaging) the subsets of responses chosen in a particular way (e.g., the channel responses are divided into subgroups, based on the underlying symbol patterns they correspond to), and (3) using the thus obtained reduced set of responses as a model channel response for lower complexity equalization. In some cases, steps (1) and (2) in the method above can be repeated periodically (e.g., in the case of time varying channels).

[0028] Systems and methods relating to BCET systems are described more completely in U.S. Patent Application Pub. No. 2014/0269894 and U.S. Pat. No. 9,154,346, the entirety of which are incorporated herein by reference.

[0029] The present invention employs optimized error control coding in conjunction with bandwidth constriction (i.e., intentionally introducing memory into the communication system) to attain a novel quality (e.g., in performance and capacity) in communication systems. In some embodiments, a system architecture is applied at the receiver of a bandwidth constrained communication system (or in a BCET communication system with intentionally introduced memory) to attain a novel quality (e.g., in performance and capacity). In some embodiments, the systems and methods described herein can operate even closer to the theoretical bounds than conventional systems (e.g., those mentioned above). For example, the systems and

methods described herein can operate close to or above the Shannon limit for memoryless channels with additive white Gaussian noise.

[0030] The present communication systems provide superior system performance, latency and power dissipation compared to conventional systems, with complexity levels suitable for practical implementations. In different embodiments, the described systems include non-orthogonal pulse shape transmission, receivers comprising equalizers, optionally a pre-processing method applied to the incoming waveforms with the goal of using a lower complexity information retrieving equalizer, and/or error control coders and decoders matched to the bandwidth constrained channels of the systems.

[0031] A method is described for use with bandwidth restricted communication systems, which includes an appropriate combination of partial response channel design, equalization, and error control coding, and qualitatively improves the overall system performance and capacity. A "partial response channel" usually denotes a channel where the channel output at some time instant is a weighted sum (or other function) of a finite number of previous channel inputs, rather than just the amplified channel input value at the same time instant (plus some noise value). In contrast, a "full response channel" is a channel with no inter-symbol interefence (ISI). For example, in BCET systems partial response channels are intentionally created by using specially designed pulse-shape filters that are non-orthogonal to the sample rate. However, partial response channels are traditionally considered as unwanted phenomenon in communication transmission, which appear as a consequence of some implementation imprecision or multipath propagation effects. In some embodiments, a partial response channel in a bandwidth restricted communication system transmits a bandwidth limited signal (e.g., signals that have been shaped using particular types of pulse shaping filters, such as root-cosine and root-raised-cosine filters). In some embodiments, in addition to the intentional pulse shaping performed on the bandwidth constrained signal, partial response channels can also unintentionally distort signals during transmission through the channel. In some embodiments, the described systems and methods include digital reshaping at the receiver in a specific way (e.g., to whiten colored noise samples after matched filtering, and to shorten the channel response), which enables the use of lower complexity information retrieving equalizers in the receiver processing chain. In some embodiments, the described systems and methods include the following steps: (1) implementation of a non-

orthogonal partial response channel design; (2) shortening of the channel response by means of a specific signal processing step; (3) equalization (or information retrieval by an appropriate equalizer); and (4) error control decoding.

[0032] The present invention is different from conventional systems and methods. Some examples of differences, in some embodiments, include that the described systems and methods: (1) encompass a particular combination of processing steps (e.g., specific pulse shape design, optimized error control coding in bandwidth constricted systems, and intersymbol interference shortening and trellis-based equalization) that provide qualitatively novel and improved system performance; (2) enable a significant complexity reduction of the information retrieving equalizer by introducing a pre-processing step of signal reshaping; (3) enable additional gains by employing nonlinear processing elements on internal receiver signal paths: (4) provide additional gains closer to theoretical capacities (e.g., close to or exceeding the Shannon limit for memoryless channels with additive white Gaussian noise) by optimizing error control code structures according to introduced narrowband response parameters. The present systems employ bandwidth constriction to improve the information rate by advantageously intentionally introducing memory (or ISI) through unconventional pulse shaping in the transmitter. This is in contrast to conventional systems, which may be affected by unintentional memory (or ISI), which is minimized, and viewed as a problem or disadvantage.

[0033] The present invention is applicable to a wide range of transmission technologies and/or communication protocols. For example, it can be used for binary and/or M-ary information streams, a variety of error-correction schemes, as well as in M-ary single carrier or Orthogonal-Frequency Division Multiplex (OFDM) modulation modes.

[0034] Furthermore, the present invention is not restricted to a certain equalization techniques. For example, pulse shaping filters can be employed with the optimal full complexity BCJR equalizer (i.e., a Bahl-Cocke-Jelinek-Raviv equalizer, named after the inventors), BCJR equalizers with reduced complexity (e.g., M-BCJR, T-BCJR), or Viterbi-based equalizers. The described systems and methods are also applicable to a BCET system with an arbitrary bandwidth narrowing factor and/or equalizer complexity level.

[0035] In some embodiments, the receivers of the systems described herein contain a detector, a filter, an equalizer and a decoder with an interleaver (and

optionally, a de-mapper). Similar components can be found in conventional receivers. However, the systems described herein are bandwidth constrained systems with intentionally introduced memory, and therefore conventional components and methods are insufficient. For example, the equalizers in the current systems (e.g., BCJR equalizers) are much more complex than conventional equalizers employed to deal with unintentional partial response channels. Such complex equalizers are not used in conventional receivers, due to the inherent exponential complexity with memory. For another example, the current data extraction systems and methods can contain turbo-equalization-loops (i.e., multiple circular exchanges of information between the equalizer and the decoder, which are described more completely below), which, in addition to adding complexity, also adds significant latency. The advantage of the current systems and methods over conventional systems and methods is that exceptional performance can be achieved with lower complexity than has been previously described.

[0036] Additionally, in some embodiments, methods for designing optimized structured irregular low-density parity-check (LDPC) codes are described. These codes can be applied as error correction methods within trellis-based equalization in turbo loops in BCET systems.

[0037] In some embodiments, the method enables construction of optimized LDPC codes that fulfil one or more of the following requirements: 1) the code belongs to the irregular repeat accumulator (IRA) class of codes, that enables linear complexity of the encoding; 2) the parity check matrix can be rearranged in quasi-cyclic (QC) form, that enables layered decoding without hardware memory (i.e., information storage within electronic hardware such as field programmable gate array / application-specific integrated circuit (FPGA/ASIC), and not memory effects applied to a signal such as intersymbol interference) conflicts; 3) the degree distributions and the parameters of the turbo loop are optimized for the known (i.e., designed) partial response channel and required level of parallelism; and 4) the designed code compensates for the imprecision caused by reducing the complexity of the equalization part of a turbo loop.

[0038] In some embodiments, the present invention combines different optimization techniques in a unique fashion, to produce optimized LDPC codes that are adjusted to BCET pulse shaping and receiving filters in BCET systems. These

optimized LDPC codes can enable reliable communication rates in BCET systems that operate close to or even potentially exceed the Shannon limit.

[0039] FIG. 1 illustrates an example of a bandwidth constrained equalized transport (BCET) system 100 comprised of a transmitter 101, a receiver 102 and a communication channel 160. The transmitter 101 incorporates the following blocks: source information input stream 105 error-correction code (ECC) encoder 110, interleaver 120, symbol mapper 130, up-sampler 140 and pulse-shaping filter 150. The pulse-shaping filter 150 narrows the signal waveform bandwidth. The receiving side of the transmission chain (i.e., the receiver 102) contains the following elements: sampler 170, receiving filter 180, down-sampler 190, impulse response adjustment block 193, information-retrieving equalizer (i.e., equalizer or equalization block) 194, de-mapper 195, and deinterleaver/ECC decoder 196, and produces the output information stream 197.

[0040] In some embodiments, the information is encoded with error-control redundant symbols using an ECC encoder (e.g., in element 110) with a Low-Density Parity-Check (LDPC) code, a turbo code, a polar code, or other type of error control code. Although different types of error-control codes can have different strengths and weaknesses, the systems and methods described herein are not limited to a particular type of code. For instance, LDPC codes can enable superior system capacity while using attractive implementation architectures (e.g., with layered LDPC decoders), compared to turbo codes. LDPC code optimization is discussed in more detail below. Polar codes also can enable high system capacity, but can have higher complexity for practical implementations (e.g., using a successive cancellation decoder), compared to systems based on LDPC codes. In another example, polar codes can be used in ECC encoders in BCET systems by replacing the block polarization kernel that is used in the polar code construction for channels without memory by a kernel appropriate for channels with memory and possibly a convoluted kernel. In adoption of polar codes for BCET systems, the successive cancellation list decoding algorithm can be used, that is a sub-optimal version of the successive cancellation decoding algorithm, which in turn enables higher information throughputs of the overall system as well as a lower receiver complexity. In some embodiments, the ECC encoder includes a cascade of two component encoders (e.g., an outer and an inner encoder). Throughout this disclosure, the present systems and methods are often described within the context of LDPC codes, however, the examples above illustrate that the

systems and methods described herein are applicable to applications using many different types of codes (e.g., turbo codes or polar codes).

[0041] In some embodiments, the pulse-shaping filter 150 narrows the bandwidth required for the transmission by spreading the value of a single modulated symbol to L neighboring symbols, i.e., producing ISI and thus intentionally introducing memory into the transmitted signals. In other words, L is the symbol memory length in the BCET system. The systems and methods described herein intentionally distort the signal (i.e., by narrowband filtering) and contain an ECC optimized for the distorted signal, which unexpectedly improve system performance (e.g., increases the spectral efficiency of the system, improves the dispersion of the system, and/or increases the system capacity). The systems described herein are therefore different than traditional communication systems, which have unintentional distortions that degrade system performance. System capacity, as used herein, refers to the information rate per bandwidth of frequency that is achieved at a given signal-to-noise ratio (SNR). Systems and methods wherein memory is intentionally introduced into transmitted signals in communications systems with increased spectral efficiency and/or dispersion are described more completely in U.S. Pat. No. 8,155,530, the entirety of which is incorporated herein by reference.

[0042] In some embodiments, the pulse-shaping is the result of a specific design optimization procedure. In some embodiments, the pulse-shaping filter 150 is compatible with one or more of the following design requirements: 1) a high achievable information rate; 2) overall narrowband response (NBR) energy clustering; 3) spectral power concetration (or power in/out of band (PIB/POB) criterion); 4) compliance with the existing spectral masks for wireless transmission; 5) appropriate peak-to-average-power-ratio (PAPR); and 6) appropriate complexity of the information-retrieving equalizer on the receiver side of the system.

[0043] In some embodiments, a parameter to consider in pulse shape optimization is the complexity of the information retrieving equalizer. More symbol memory intentionally induced in the system 100 (i.e., increasing L), corresponds to an exponential increase in hardware complexity of the equalizer. In some embodiments, the present pulse shaping filters (e.g., 150) have the required PIB (Power in Band) performance criterion, for example 99% or 99.9% of the power inside a specified constrained bandwith, and also induce low memory that is acceptable for practical implementations of the system. An example of an optimal pulse shape that fulfills

these criteria are Prolate Spheroidal Wave Functions (PSWF). In some cases, those pulse shapes have optimal time-bandwidth properties. FIG. 2 is an illustrative example of a PSWF filter response in the spectral domain. The graph in FIG. 2 represents the power spectrum of the filter 210, where the x-axis is the normalized frequency and the y-axis is the magnitude of the response of the filter. In this example, the filter introduces a factor of 3 of spectral compression compared to the square-root raised cosine (SRRC) power spectrum 220, which is denoted as NBR3 in Table 1 and discussed further below. In other embodiments, the pulse-shaping filter introduces a factor of 2 or more, 3 or more, 4 or more, 5 or more, or a factor from 3 to 10, of spectral compression compared to the square-root raised cosine (SRRC) power spectrum. Additionally, considering time-bandwidth optimality, another example of possible pulse shapes are Gaussian pulse shapes, which have slightly larger time-bandwidth product for the specified PIB criterion. In other embodiments, the pulse-shaping filter utilizes a prolate spheroid wave function, a Gaussian wave function, or digital or discrete representations of thereof. The pulse-shaping filter can utilize any wave function shape that introduces a factor of 2 or more, 3 or more, 4 or more, 5 or more, or a factor from 3 to 10, of spectral compression compared to the square-root raised cosine (SRRC) power spectrum.

[0044] In some embodiments, a pulse-shaping filter narrows the bandwith to a specified value, and maximizes the spectral efficiency and achievable information rates, and has PAPR that is not significantly larger than the PAPR of an orthogonal Nyquist linear modulated signal with higher order modulations with the same spectral efficiency (for a specified PIB criterion, a required hardware complexity, and a maximal memory (i.e., maximum L) induced in the system 100).

[0045] FIG. 3 illustrates an example of achievable information rates for three NBRs, designed with PSWF pulse shapes, combined with Quadrature Phase Shift Keying (QPSK) modulation, denoted by NBR1 (302), NBR2 (304) and NBR3 (306). In these examples, the LDPC codes are optimized to the different NBRs (i.e., NBR1, NBR2 and NBR3). The plot in FIG. 3 shows the achievable information rate versus SNR for NBR1 (302), NBR2 (304) and NBR3 (306), and for the Shannon limit 308. The PIB criterion is 99% for the NBRs in this example. The NBRs in this example also satisfy the following constraints: 1) bandwidth reduction compared to spectrum required for the SRRC pulse shaping is 220%, 260% and 300%, for NBR1, NBR2 and NBR3, respectively; and 2) PAPRs for all of the NBRs are comparable to the PAPR

of the system with an SRRC filter, Nyquist signalling, and high order modulation achieving the similar information rate as BCET systems. The parameters of the NBRs in this example are summarized in TABLE 1.

[0046] Table 1: Narrowband Response Parameters

Narrow band response	NBR length after shortening	Modulation scheme	Maximal spectral efficiency	Peak-to-average-power ratio of T1
NBR1	3	QPSK	3.55 b/s/Hz	5.2 dB
NBR2	4	QPSK	4.27 b/s/Hz	6.1 dB
NBR3	5	QPSK	5.33 b/s/Hz	6.9 dB

[0047] Returning to FIG. 1, after re-shaping the received signal by the matched filter 180, and down-sampling it by the down-sampler 190, symbols can be optionally additionally processed by the impulse response adjustment block 193, which is an additional processing step prior to the information retrieving equalizer. In some embodiments, the matched filter at the receiver side is a narrow-band filter that is complementary to the pulse-shaping filter 150 in the transmitter. For example, the function used in filter in block 180 can be a conjugated time-reversed version of the function used in filter in block 150, implemented in the frequency domain.

[0048] In some embodiments, the equalization block 194 works directly on symbols obtained by matched filtering, wherein the filter transfer characteristic is matched to the characteristic of the pulse-shaping filter 150. In some cases, the symbol observations contain samples of the noise that are correlated (e.g., those generated using the so-called Ungerboeck observation model). In such cases, an equalizer algorithm is used that can accommodate the colored noise.

[0049] In some embodiments, optional impulse response adjustment block 193 is used to whiten the colored noise samples after matched filtering, and shorten the channel response, enabling the utilization of a less complex information-retrieving equalizer. In some embodiments, impulse response adjustment block 193 contains a noise whitening filter which is designed to partially or fully decorrelate the noise samples and/or cluster the majority of the energy of the equivalent partial response to only a small number of samples $L' < L$.

[0050] In some embodiments, the impulse response adjustment block 193 can be realized as a finite impulse response filter, which additionally shortens the impulse response (i.e., effectively reduces L), however other similar approaches achieving the

same effect can be applied. Channel shortening is advantageous because it can shorten the effective impulse response, which enables lower complexity equalizer design. In some cases, it is not necessary to adapt the equalizer algorithm to work with the colored noise samples (e.g., using the so-called Forney observation model).

[0051] Continuing with FIG. 1, intentionally added ISI, by the pulse shaping filter 150, as well as interference potentially produced by the channel 160, can be treated (e.g., removed or mitigated) in the equalization block 194.

[0052] In some embodiments, the BCET equalization is a two-step process: in the first step interference introduced by the communication channel is removed or mitigated, for which any conventional equalizer can be used (e.g., Feed-Forward and/or Decision-Feedback Equalizers), while in the second step a sophisticated equalization technique (e.g., utilizing a BCJR equalizer) is employed to extract transmitted symbols from the intentionally introduced ISI. The equalization process can be optionally joined with the de-mapper 195, interleaver and deinterleaver/ECC decoder 196 blocks in an iterative loop, i.e., a turbo equalization loop, as described further herein.

[0053] In some embodiments, the equalizer in a BCET system contains the BCJR algorithm. Equalizers using the BCJR algorithm are optimal for BCET systems (considering MAP (maximum a posteriori probability) criteria). BCJR is a sequential algorithm with a trellis structure where the number of states in each stage of the trellis is M^L, where M is the size of the modulation alphabet (e.g., M=2 for BPSK, M=4 for QPSK, M=8 for 8PSK, etc.), and L is the span of ISI memory. The algorithm processes a received (input) data sequence (e.g., an LDPC codeword) on a symbol-by-symbol basis starting from the beginning of the sequence. In some embodiments, the equalizer contains a sub-optimal BCJR variant of the algorithm, such as M-BCJR, T-BCJR, or similar families of algorithms (e.g., Viterbi algorithm, or soft output Viterbi algorithm (SOVA)).

[0054] Both the optimal BCJR and sub-optimal algorithms described above typically process data serially. The sequential nature of the algorithms used in BCET system can pose a significant constraint on the achievable throughput of the system using such equalizers.

[0055] In order to improve this imposed throughput constraint, in some embodiments, the equalizer in a BCET system contains a plurality of modules in a parallel arrangement, where each module contains a BCJR algorithm utilizing

windows or partitions. In some cases, the trellis length N (i.e., the length of the received sequence) of the algorithm can be partitioned into K smaller trellises that are processed in parallel (e.g., one in each module), thereby increasing the system throughput K-fold. In such cases, the length of each trellis partition is N/K. In some embodiments, N/K is greater than 100, or is greater than 200, or is greater than 500, or is from 100 to 1000, and the sub-optimal solution with parallel processing exhibits negligible performance degradation when compared to the optimal full-length trellis without parallel processing. In some embodiments, the receiver is implemented following the Forney channel model, and the partitions are completely independent (i.e., there is no overlap between the neighboring trellises). In other embodiments, the receiver is implemented following the Ungerboeck channel model, and the neighboring partitions overlap. In some embodiments, this overlap is about 10 symbols, or about 20 symbols, or about 50 symbols, or from 10 to 100 symbols. For example, when the neighboring partitions have lengths of 200 and overlap by 20 symbols, the overall system throughput increase is about (1-20/200) * K = 0.9 * K compared to the optimal BCJR (i.e., a 10% lower overall boost in throughput when compared to Forney channel model which achieves K-fold increase in throughput). In some embodiments, K is greater than 10, or greater than 100, or greater than 200, or greater than 300, or greater than 500, or is from 10 to 1000, or is from 50 to 500. In addition to the type of model used, the value of K that is possible depends on the partition size, and the LDPC codeword length. For example, given a partition size of 200 for the Forney model (or, 220 for the Ungerboeck model including the overhead), and an LDPC codeword size of 16200 or 64800, the value of K achieved can be 80 or 320, respectively. One tradeoff of boosting the overall system throughput by parallelizing the BCJR-based equalization, is that the system is required to have K times more hardware memory (e.g., on a FPGA/ASIC) to process all of the partitions in parallel. When windowed/partitioned BCJR is used in a turbo equalization loop, only in the first iteration of the turbo loop is equal likelihood assigned to each state at the initialization stage for each window/partition. After the first iteration of the turbo loop, likelihoods at the decoder output are assigned to each state at the initialization stage for each window/partition.

[0056] In some embodiments, the equalizer contains a BCJR variant algorithm, with reduced complexity compared to the full complexity optimal BCJR algorithm.

[0057] In some embodiments, the equalizer contains an I and Q (i.e., in-phase and quadrature) BCJR algorithm (e.g., in systems processing QPSK modulated signals). As described above, the BCJR complexity is M^L, which is a polynomial in the modulation alphabet M. If the modulation alphabet is higher than binary (e.g., higher than that using binary phase shift keying, or BPSK), the complexity can be reduced by introducing a sub-optimal solution which processes different parts of the alphabet separately. For example, the I and Q branches of the modulation alphabet (e.g., in QPSK schemes) can be processed separately. In that case, the overall complexity of the solution is $2 * M^L/2^L$ which dramatically simplifies the equalizer architecture, and hardware memory consumption on FPGA/ASIC. In some embodiments, replacing a single QPSK-based BCJR with 2 BPSK-based BCJRs (one for the I-branch another for the Q-branch) running in parallel, results in a negligible loss in the system performance (e.g., a negligible increase in bit error rate (BER)).

[0058] In some embodiments, channel shortening can be applied in the receiver processing chain prior to the equalizer (e.g., at the output of the receiving filter), enabling the use of a lower complexity equalizer. As described above, the BCJR complexity is M^L, where the complexity exponentially grows with the ISI length. A channel shortening process can be performed prior to the equalizer, which reduces the effective L enabling a reduction in the complexity of the equalizer. In some cases, the ISI memory elements at the edges of the ISI profile can be averaged, hence shortening the channel response and reducing the complexity (as described more completely in U.S. Patent No. 9,154,346). In other embodiments, a shortening filter based on minimum mean-squared error (MMSE) criteria is used to generate a shortened version of the channel impulse response prior to the equalizer (e.g., at the output of the receiving filter).

[0059] In some embodiments, the equalizer contains a BCJR variant algorithm, with reduced complexity compared to the full complexity optimal BCJR algorithm that is a MAX-BCJR algorithm. In each stage of the full complexity BCJR algorithm, a state metric update is conducted at each state by summing all of the branch metrics from the connecting states of the previous stage. Instead of the full complexity summation operation, MAX-BCJR uses only the maximum branch metric to update the state metric, which avoids a plurality of summation operations (i.e., saves arithmetic operations), thereby reducing the overall algorithm complexity.

[0060] FIG. 4 illustrates a turbo equalization loop, in accordance with some embodiments. Samples received from the channel are stored in the input buffer 210, which represents one input of the equalizer 230. The equalizer 230 in FIG. 4 corresponds to the equalization block 194 in FIG. 1. The extrinsic information produced by the ECC decoder 270, passed through the symbol mapper 220, is also taken to the input of the equalizer 230.

[0061] In some embodiments, the complexity of the trellis-based equalization process used by equalizer 230 is related to the cardinality of the linear modulation symbol alphabet (M) used, and the symbol memory length (L) induced by the BCET system. Complexity of the equalization process, and therefore hardware complexity, in such cases is proportional to M^L.

[0062] In some embodiments of turbo equalization loops, trellis-based equalizers, mainly BCJR and reduced complexity BCJR variants, like max-BCJR, M-BCJR, T-BCJR, forward-only BCJR, or windowed BCJR, are used. SOVA or even MMSE equalizer techniques can be used with restrictions as well. At the output of the BCJR-based equalizer, a soft demodulation block 240 is placed, which converts symbol likelihoods into the bit likelihoods.

[0063] In an alternative embodiment, and as a further complexity reduction, when pulse-shaping filter coefficients are real and 2-dimensional linear modulation is employed with cardinality M (for example QPSK, M=4), the pulse train can be modeled as two independent lower cardinality 1-dimensional modulation pulse trains (each with cardinality equal to $\log_2 M$), one on the I branch, and the other on the Q branch. The equalizer can then be formed by two lower complexity equalizers (complexity equal to $\log_2 M^L$ instead of M^L where L is the symbol memory length induced by the BCET system) operating in parallel, and this can significantly reduce hardware complexity and hardware resources without any loss in the receiver overall performance. These I/Q branch equalizers could use any trellis based equalizer architectures (e.g., BCJR, or a reduced complexity BCJR variant). In this case, there is a parallel-to-serial conversion of symbol likelihoods produced by two I/Q equalizers prior to soft demodulation block 240 which converts them to bit likelihoods.

[0064] Extrinsic information of BCJR is obtained when the input bit-level log-likelihood ratios (LLRs) are substracted from the output bit-level LLRs. The result is passed through deinterleaver 250. Interleavers can take the sequence of

symbols from its input and produce the identical symbols at the output, but in a different temporal order. In some embodiments, interleavers are used to disperse sequences in bit streams (or in streams of symbols) so as to minimize the effects of burst errors. The deinterleaver 250 and the ECC decoder 270 in FIG. 4 correspond to the deinterleaver/ECC decoder 196 in FIG. 1.

[0065] The use of reduced-complexity equalization techniques in turbo equalization schemes can significantly reduce the quality of the LLRs. The quality of the LLRs can strongly affect the system performance. In some embodiments, a non-linear function 260 can be optimized to transform a signal with low quality LLRs at the output of the deinterleaver 250, in order to maximize the effectiveness of the subsequent error control code optimization processes and iterative equalization and detection processes. For example, block 260 can be implemented in the form of a clipping circuit, an element that transforms a signal using a non-linear function that re-scales extrinsic LLRs, or an element that transforms a signal using a lookup table that incorporates a more elaborate distribution transformation. Non-linear LLR transformations can either be fixed from one turbo iteration to another, or can be adapted from iteration to iteration. Non-linear functions used by block 260 can be optimized based on different factors, for example: 1) estimated channel SNR; 2) pulse shaping response characteristics; 3) type of LDPC code applied; 4) decoding algorithm; and 5) other criteria. The non-linear transformation parameters can be pre-computed when an adaptive transformation law is applied, or they can be adapted on-the-fly based on the current codeword processed. Adaptation on the fly requires additional processing steps after the LDPC decoder block and adds to the overall complexity of the receiver 102. In some embodiments, the nonlinear operation can be precomputed and stored (e.g., as a look-up table, or map), which requires hardware memory space but does not result in an increase in system complexity. In other embodiments, the nonlinear operation can be computed on the fly, which increases the complexity of the system but does not require extra hardware memory. In some embodiments, a non-linear transformation is implemented in the form of an LLR clipping law. In these cases, threshold values can be pre-computed in advance by using Density evolution (DE) technique, so that the LDPC code employed has the largest DE threshold values.

[0066] Due to the serial nature of the trellis based equalizers, in order to achieve high throughput, in some embodiments, it is neccessary to highly parallelize

trellis based equalizers. In some embodiments, a received frame is divided into windows that are of equal length. And in some embodiments, the received frames are proccesed fully in parallel. In such cases, the number of windows can be chosen based on an optimization procedure with the criteria including: system throughput, hardware resources employed, and amount of degradation of the receiver performance compared to the a non-parallelized approach. Therefore, special attention should be paid to adequate interleaver design between the equalizer and the LDPC decoder in the receiver. In some embodiments, the interleaver supports a large number of equalizer windows, and is adapted to the layered LDPC decoder architecture, enabling fast transfer of LLRs between equalizer windows and LDPC decoder memories. In some cases, the interleaver is contention free. The underlying interleaving pattern can be deterministic, but can also emulate (or approximate) random pattern interleavers.

[0067] In some embodiments, an improved interleaver design is implemented. The interleaver can be designed with the following design goals: 1) include W equalizer windows and V LDPC memories (e.g., V=360 is an example of a possible LDPC parallelism level); 2) all LDPC memories are two port memories and each hardware memory is connected to two equalizer windows, and each hardware memory is divided in two hardware sub-memories, with each hardware sub-memory assigned to one equalizer window; 3) each equalizer window is connected to V/W hardware memories and serially sends data using a round-robin principle; and 4) the equalizer window address assignment is random. Since in a layered LDPC architecture, each LLR is read serially, LDPC reads a first location from the first hardware memory, then a first location from a second hardware memory and so on. In some embodiments, the above design goals can be modified to include more than two equalizer windows. The above described interealver design is a hybrid between random and block interleavers, and can achieve a high parallelism level with simple timing control. Simulations show that there are no losses in such systems compared to fully random interleavers.

[0068] Continuing with FIG. 4, the output of 260 defines input LLRs of the ECC decoder 270. In some embodiments, the code used as an ECC should be capacity approaching code and designed for attainment of performance closer to the constrained bandwidth channel capacity. In some embodiments, LDPC capacity approaching code is used as an ECC code.

[0069] In some embodiments, the LDPC code structure is optimized using the following requirements: 1) the code belongs to the irregular repeat accumulator (IRA) class of codes, that enables linear complexity of the encoding; 2) a parity check matrix can be rearranged in quasi-cyclic (QC) form, that enables layered decoding without hardware memory conflicts; 3) a degree distribution and parameters of the turbo loop are optimized for the known partial response channel and required level of parallelism; and 4) the designed code compensates imprecision caused by any reduction of the complexity of the equalization part of a turbo loop, as described above.

[0070] In some embodiments, the LDPC code is decoded using an iterative method using belief propagation or sum-product message passing (i.e., a message passing algorithm that is an optimal method for iterative decoding of LDPC codes). However, the optimality of sum-product message passing comes at the cost of a high complexity, numerical instability, and dependence on noise variance estimation (i.e., SNR estimation).

[0071] In some embodiments, a lower complexity LLR calculation in LDPC decoding can be used such as a min-sum algorithm (e.g., 3-min-sum, or 5-min-sum) that trade performance, or optimality for complexity of implementation. For the min-sum algorithm, complex computations in the sum-product algorithm are approximated using simpler comparison and summation operations (hence the "min-sum" name). 3-min-sum and 5-min-sum refer to versions of the algorithm with different numbers of elements used in the comparison logic of the algorithm. In some embodiments, a 5-min-sum algorithm is used in a BCET system with a turbo loop (i.e., iteration between the LDPC decoder and the equalizer), and negligible performance loss is observed compared to the same system using a sum-product solution.

[0072] In some embodiments, the LDPC code optimization process uses the distribution of the constituent variable node degrees and check node degrees, as well as the parameters of the non-linear function inside the turbo equalization loop (described above). The optimization can also be based on the density evolution for partial response channels, and on producing an optimized degree distribution that satisfies a predefined set of constraints that enable the construction of structured QC IRA codes (for a desired decoder complexity and level of parallelism).

[0073] In some embodiments, the parity check matrix in the LDPC code optimization process ensures that the QC structure is suitable for layered decoding. In

addition, enabling low complexity encoding is an important optimization constraint. In some embodiments, the above constraints on the LDPC code optimization process reduce the search area in which the optimization algorithm looks for the degree distribution of the irregular code that provides the minimal value of the SNR threshold, thereby reducing system complexity.

[0074] In some emobodiments, a layered LDPC decoder architecture is employed.

[0075] In some embodiments, the receiver performance of the BCET system depends on the number of iterations in the turbo loop and the internal LDPC decoder iterations in the receiver. Larger bandwidth constriction produces more severe ISI (or symbol memory) in the system. When there is a more severe ISI in the system, the turbo equalization scheme needs more iterations to remove the ISI and to achive the desried LDPC decoder performance (for a given SNR). The number of turbo iterations is a trade off between the required BCET performance, hardware complexity, and system throughput.

[0076] FIG. 5 illustrates an example of system Frame Error Rate (FER) performance with different number of turbo iterations. The FER versus SNR for a BCET system with a turbo loop (e.g., as shown in FIG. 4) are plotted in curves 510, 520 and 530, corresponding to 5, 10 and 25 turbo iterations in the recover, respectively.

[0077] As described above, bandwidth constrained equalized transport (BCET) systems (e.g., similar to those described in U.S. Pat. No. 8,155,530, and U.S. Patent Application Pub. No. 2014/0269894) increase spectral efficiency of the transmission by narrowing the transmission bandwidth, while retaining a constant information rate.

[0078] By stepping into the faster-than Nyquist (FTN) signaling realm, a BCET system relies on proper pulse shaping and equalization techniques to control the ISI. The present BCET systems additionally include error control coding techniques that enable reliable data transmission using practical hardware complexity. In some embodiments, the systems and methods described herein can increase the information rate in satellite communications, for example, using similar system parameters as in DVB-S2 and DVB-S2X standards, or using other wireless communication standards (e.g. 5G, WiFi, xDSL).

[0079] The low-density parity-check codes (LDPC) described in the DVB-S2 and DVB-S2X standards, optimized for additive white Gaussian noise (AWGN) channels, are not adequate solutions in BCET systems. In some embodiments, the present systems and methods are used to optimize the degree distribution for irregular LDPC codes, which satisfy requirements related to the impulse response of the partial response channel, required complexity of the equalizer, required information rate, and data throughput. In some embodiments, the degree distribution of both the variable nodes and the check nodes, as well as the parameters of the non-linear function in the turbo equalization loop are optimized together. This optimization can result in improved system performance for a given signal-to-noise ratio (SNR) and information rate. The value of the SNR that ensures that the FER is below a predetermined level can be denoted as a "turbo cliff". Therefore, in some embodiments the goal of the optimization is to minimize the turbo cliff (i.e., minimizing the SNR required to achieve a low FER) for a given information rate and for a particular (e.g., limited) complexity of a turbo equalizer. Optimizing for a particular system complexity is important, because typically processing power and hardware memory resources are limited. As the processing latency determines throughput, the optimization is performed for a limited number of iterations, in some embodiments.

[0080] Referring again to FIG. 1, in some embodiments, the ECC encoder 110 contains a cascade of two codes: an outer block encoder and an inner LDPC error-correction code encoder. The systems and methods described herein, such as the system shown in FIG. 1 and methods that can be performed using the system shown in FIG. 1, including the above ECC encoder description, are applicable to a wide range of transmission technologies and/or communication protocols. For example, the systems and methods described herein can be used for binary and/or multiary (M-ary) information streams, as well as in M-ary modulation modes. The systems and methods described herein are also applicable to BCET systems with any bandwidth narrowing factor and/or level of equalizer complexity.

[0081] Referring again to FIGs. 1 and 4, in some embodiments, ECC encoder (element 110 in FIG. 1) contains a cascade of two codes: an outer block encoder and an inner LDPC error-correction code encoder, and the ECC decoder (element 270 in FIG. 4) in the turbo equalization loop is an LDPC decoder. In this case, the extrinsic information produced by the LDPC decoder 270, is passed through the symbol mapper 220, and is taken to a second input of the equalizer 230. In some

embodiments, the equalizer 230 is a trellis-based equalizer, such as a BCJR equalizer and its reduced complexity variants (e.g., max-BCJR, M-BCJR, T-BCJR, forward-only BCJR, or windowed BCJR equalizers). In some embodiments, the equalizer 230 utilizes Viterbi or MMSE equalizer techniques. At the output of BCJR-based equalizer 230, soft demodulation block 240 is placed, which converts symbol likelihoods into the bit likelihoods.

[0082] Continuing with FIG. 4, extrinsic information from the BCJR equializer 230 is obtained when the input bit-level LLRs are substracted from the output bit-level LLRs. The result is passed through deinterleaver 250. Non-linear function 260 can then transform opportunistic LLRs (opportunism is a consequence of employing non-optimal equalization techniques) at the output of the deinterleaver 250 to an appropriate form, in order to maximize the effects of code optimization. The non-linear function block 260 can be optimized as well, can be implemented in the form of a clipping circuit, can utilize a polynomial function, sigmoidal function, or a function that re-scales extrinsic LLRs, or can utilize a lookup table that incorporates more elaborate distribution transformation, as described above. In the case that the ECC decoder 270 utilizes LDPC codes, the outputs of 260 are the input LLRs of the LDPC decoder 270. Furthemore, extrinsic information of the LDPC decoder 270 is obtained when the input LLRs are substracted from the output bit-level LLRs in block 275, which is after ECC decoder 270 and before interleaver 280. The result is passed through interleaver 280 to the symbol mapper 220, which closes the loop.

[0083] In some embodiments, the ECC encoder and decoder utilize LDPC codes, and an LDPC code optimization process is performed, which includes optimizing the distribution of the variable node degrees and check node degrees, as well as the parameters of the non-linear function. The optimization can be based on the density evolution for partial response channels, and the produced optimized degree distributions can satisfy a predefined set of constraints that enable the construction of structured QC IRA codes, for a desired complexity of the decoder and level of parallelism. An example of a process for LDPC code optimization is shown in FIG. 6, in accordance with some embodiments. The LDPC code optimization process can also depend on the type of pulse-shaping optimization procedure used in the system (examples of pulse-shaping optimization procedures for the present systems are described above).

[0084] In some embodiments, the parity check matrix has a QC structure that is suitable for layered decoding. Additionally, in some embodiments, the parity check matrix is designed to minimize the complexity of encoding. The constraints on the parity check matrix imposed by the above optimizations can be used to reduce the search area in which the optimization algorithm looks for the degree distribution of the irregular code that provides the minimal value of the SNR threshold.

[0085] In one possible optimization setup (mode 1), only a part of the variable degree distribution is optimized, while another part of the distribution is predefined. In such a case, the columns with weight equal to 2 can be placed in a double diagonal matrix only, the check node degrees can be fixed to two successive values, and the check node distribution can be determined with the code rate and structural properties of QC IRA codes. In another scenario (mode 2), the columns with weight equal to 2 can be placed in the double diagonal matrix, and can also be placed in the rest of the parity check matrix.

[0086] As shown in FIG. 6, the optimization process starts at step 300 by selecting the dimensions of a parity check matrix (that define a codeword length and a code rate), equalizer parameters, and a level of parallelism P, according to the system requirements.

[0087] Then, at step 310 the maximum variable degree is chosen, and set of the check node degrees is fixed. The optimization mode, as described above, is also selected in step 310. In step 320 the variable node distribution is initialized, and the distribution of check node degrees is calculated for the given input parameters. In other words, in step 320, for a given code rate and limitations of structured IRA codes (i.e., those selected in steps 300 and 310), the distributions of the check node degrees for the initial variable node degree are calculated.

[0088] Using a density evolution algorithm for partial response channels, the degree distribution and parameters of the non-linear function are optimized, and the corresponding threshold is calculated in step 330. In other words, in step 330, the optimal variable node degree distribution and nonlinear function parameters, along with the corresponding thresholds, are found using density evolution. The procedure in step 330 is repeated for an appropriate subset of initial conditions, and a database of the possible solutions for the various resulting sets of check node degrees is generated in step 340.

[0089] In some embodiments, the parity check matrix H contains two parts, a first part H_1 and a second part H_2, such that $H = [H_1 H_2]$, where H_2 is a double diagonal matrix and H_1 is the quasi-cyclic part of the parity check matrix with the structure determined by a random masking matrix that satisfies the degree distribution condition. Each binary zero in the masking matrix can correspond to a PxP zero submatrix in H_1, and every binary one in the masking matrix can correspond to a cyclically shifted eye submatrix with dimensions PxP. The corresponding values of the shifts in the cyclically shifted eye submatrices (e.g., in the range [0, 1,…, P-1]) are defined in a prototype matrix and can be generated by using an appropriate algorithm, as described in more detail herein. Starting from the degree distribution that corresponds to H, and taking into account a simple structure of H_2, the degree distribution that corresponds to H_1 is calculated, in some embodiments. By using this distribution, the random masking matrix is generated, and the prototype matrix is produced in step 350 (e.g., as will be described further below and in Fig. 7). This process is repeated for the appropriate set of check node degrees, and the solution that results with the lowest threshold is identified. In other words, the masking matrix and the prototype matrix that are generated in step 350 are optimized for the solution with the lowest threshold. At decision step 355, if it is not possible to construct a prototype matrix (e.g., if the maximal variable node degree was too large), then the maximal variable node degree is reduced and/or the set of check node degrees is redefined in step 360. After step 360, these new initial conditions are used to reoptimize the degree distribution by repeating steps 320 through 350. Steps 360, and 320 through 350 can be repeated until the prototype matrix is successfully generated (i.e., until the decision at step 355 is "YES").

[0090] The prototype matrix is an intermediate result before generating a parity check matrix. At decision step 355, if it is possible to construct a prototype matrix, then the parity check matrix suitable for layered decoding is generated at step 370. The parity check matrix is then represented in the form of the corresponding permutation matrix that is suitable for low complexity encoding at step 380, and the real degree distribution of the generated code is estimated and checked at step 390.

[0091] FIG. 7 is an example process for constructing the prototype matrix, in accordance with some embodiments. In some embodiments, the prototype matrix has nR/P columns and $(1-R)n/P$ rows, where R is the code rate (e.g., R=3/5), n is the codeword length (e.g., n=16200), and P is the level of paralelism (e.g., P=360). In

some embodiments, the prototype matrix is a matrix of integers, in which each element of the matrix denotes a cyclic shift of an eye PxP matrix in the H_1 part of the parity check matrix. In such cases, as a result, the prototype matrix is P times smaller than the H_1 matrix.

[0092] The prototype matrix can be generated in a few successive steps. In step 400, known optimal degree distributions for the parity check matrix (H) In step 410, the degree distribution is recalculated, to correspond to the first part of matrix H (denoted by H_1). In step 420, a binary masking matrix with size $(1-R)n/P \times nR/P$ is generated from the recalculated degree distribution. In step 430, the double diagonal matrix (denoted by H_2) is concatenated with the matrix H_1 such that $H = [H_1\ H_2]$, to complete the parity check matrix H.

[0093] Using the present systems and methods, the prototype matrix can directly determine the structure of matrix H. In some embodiments, both dimensions of the prototype matrix are P times less than those of the first part of the parity check matrix (H_1), and every element in the prototype matrix defines a number of cycle shifts in a corresponding submatrix with size P×P. For example, FIG. 8 shows a matrix H_2 with dimensions 6480×6480. The matrices H, H_1 and H_2 in FIG. 8 are shown using a compact description where the sizes are reduced by P times. In the example matrix H_2 in FIG. 8, every "0" corresponds to an eye matrix with site 360×360 (with no shifts), and the blank cells correspond to zero matrices with size 360×360 in the corresponding parity check matrix. The example matrices in FIG. 8 correspond to a parity check matrix for a code rate R=3/5, codeword length n=16200, and level of paralelism P=360, and is obtained by using the systems and methods described above. The matrix H has a size 6480×16000, and the maximum column and row degree are equal to 6 and 8, respectively.

[0094] FIG. 9 shows example error performance for a BCET system (e.g., the system shown in FIGs. 1 and 4) utilizing structured QC IRA codes with optimized degree distributions. The error performance is evaluated for partial response channel with the impulse response g=[0.0021 0.1252 0.3331 0.5329 0.5839 0.4461 0.2226], where the two first coefficients are ignored and renormalization is applied. The results are given for BPSK modulation (two paralel streams, one per each quadrature), codeword length n=64800, code rate R=1/2 and circulant size P=360. The total number of trellis states is $S=2^5=32$, and windowed BCJR with 80 segments is applied. Both the BER and FER are plotted for the standard control ("DVB-S2X, BER" 910

and "DVB-S2X, FER" 920), the optimized LDPC codes designed in mode 1 ("LDPC, mode 1, BER" 930 and "LDPC, mode 1, FER" 940), and the optimized LDPC codes designed in mode 2 ("LDPC, mode 2, BER" 950 and "LDPC, mode 2, FER" 960).

[0095] The data in FIG. 9 illustrates that the optimized LDPC code designed in mode 1 provides an error performance gain of approximately 0.7 dB compared with the corresponding code from DVB-S2X standard. The data in FIG. 9 also shows that the optimized LDPC codes designed in mode 2 provide an additional gain of about 1.4 dB. In both cases, a Bose, Chaudhuri, and Hocquenghem (BCH) code is used as an outer code, and corrects up to t=12 errors per codeword.

[0096] Two optimization modes (mode 1 and mode 2) are described above. In the first mode (mode 1), LDPC codes were designed to achieve excellent performance without using any outer code. In the second mode (mode 2), inner codes were designed that have good performance in the waterfall region, but with poor performance in the error floor region compared to general LDPC code properties. However, when the outer code that corrects up to t errors is applied, the codes designed in mode 2 can have even better performance that the codes designed in mode 1.

[0097] FIG. 10 illustrates an example performance for various LDPC code rates and spectral efficiency regions, for BCET systems described herein such as system 100 shown in FIG. 1. In the chart in FIG. 10, the data depicted using diamond and square symbols (labelled "DVB-S2X…" in the legend) use conventional LDPC encoders, while data depicted using triangle and circle symbols (labelled "BCET LDPC…" in the legend) use the improved LDPC encoders described herein. The different data points were also produced using different code rates ("R"), code word lengths ("n"), as shown in the legend of the graph in FIG. 10. All of the data shown in FIG. 10 was produced by systems with turbo equalization loops. The Shannon limit curve (labelled "AWGN Shannon capacity" in the legend) is shown as a dashed line, and the PSWF capacity (labelled "PSWF capacity" in the legend) is shown as a solid line. The PSWF capacity is the capacity of the system given a large number of turbo equalization loop iterations (e.g., 100 turbo iterations) and long code word lengths (e.g., $n=10^6$). FIG. 10 shows that the information rate (i.e., spectral efficiency) achieved by the present pulse-shaping optimization procedures, and bandwidth constriction in the transmitter, surpass the traditional Shannon capacity curve. FIG. 10 also shows that by using the current narrowband filtering coupled

with industry existing LDPC parity check matrices (e.g., which are optimized for use in traditional orthogonal communications systems with only AWGN present in the channel, and which are not optimized for the channel with inherent inter-symbol interference in the channel), system performance is very close to the traditional Shannon curve and even slightly above for larger code rates (operating points are represented with diamond and square symbols). This is due to inherent system capacity improvements obtained in systems with optimized transmitter side pulse-shaping and turbo equalizer loop architectures. FIG. 10 also shows that when the presently described optimized LDPC codes are applied, the system can operate well above the Shannon curve (operating points are represented with triangle and circle symbols). In other words, FIG. 10 shows that, using the systems described herein, narrowband filtering coupled with traditional LDPC codes is able to breach Shannon limit, and that narrowband filtering coupled with the improved LDPC codes described herein enables further improvements beyond the Shannon limit.

[0098] FIG. 10 shows the information rates that can be achieved for four code rates (i.e., R=1/2, R=3/5, R=22/30 and R=77/90). The numerical results in FIG. 10 are given for the channel with the same impulse response as in FIG. 9, a QC LDPC with the degree distribution optimized according to mode 2, with codeword length n=64800, and circulant size P=360. The data in FIG. 10 was generated using a BCET system (e.g., the system shown in FIGs. 1 and 4) including 15 turbo iterations and a windowed BCJR with 80 segments. The results are about 1.5 dB to 2 dB away from PSWF channel capacity, but more than 1 dB better than the capacity of the AWGN channel. For R=1/2, the optimization of the code degree distributions resulted in the performance gain of 2.8 dB compared with the DVB-S2X code with the same code rate.

[0099] FIG. 11 illustrates the dependency of the system performance on the number of turbo iterations in the receiver's turbo equalization loop, in some embodiments. The data depicted using diamonds (and labelled "DVB-S2X…" in the legend) use conventional LDPC encoders, while the data depicted using other symbols (i.e., circles, squares, stars, and triangles and labelled "BCET LDPC…" in the legend) use the improved LDPC encoders described herein. The different data points also use different code rates ("R"), code word lengths ("n"), and number of turbo iterations ("turbo it"). The Shannon capacity and the PSWF capacity are shown as they were in FIG. 10. The number of turbo iterations is a trade off between the

system performance, throughput, and the receiver hardware complexity. FIG. 11 shows that by allowing more turbo iterations in the loop, BCET systems can operate closer to inherent capacity (PSWF capacity) and surpass traditional Shannon capacity bounds.

[00100] FIG. 11 shows the information rates for BCET systems for different code rates, codeword lengths, and numbers of turbo iterations. The data in FIG. 11 shows that for codeword lengths approximately four times shorter (i.e., n=16560 compared to n=64800), the same information rate can be achieved for signal-to-noise ratio that is 0.7 dB smaller. For both codeword lengths and all code rates shown in FIG. 11, a reduction in the number of turbo iterations from 15 to 10 results in performance degradation of about 0.2 dB, and a further reduction to 5 turbo iterations corresponds to an additional degradation of approximately 1 dB.

[00101] Several embodiments of a transmitter in systems employing narrowband filtering (e.g., BCET systems) will now be described.

[00102] In some embodiments, a transmitter in a system employing narrowband filtering comprises: 1) a pulse shaping filter that is specifically designed for maximization of achievable information rates and high spectral efficiency, with different possible optimization criteria, such as lowest possible induced symbol memory (i.e., intentionally induced inter-symbol interference that can minimize receiver complexity); and 2) an error control code encoder used to append redundant information so as to avail information symbols' retrieval in the presence of noise and impairments, wherein the code structure is specifically designed along with the pulse-shaping design procedure (e.g., achieving performance closer to the achievable information rates than conventional systems). In some embodiments, the transmitter is for use in a digital communication system conveying information symbols at a certain symbol rate in which the information bearing waveforms are filtered to a bandwidth significantly narrower than the communication symbol rate; and wherein the apparatus achieves an improved energy performance and increased spectrum efficiency compared with systems not employing the bandwidth constraint.

[00103] In some embodiments, the system described above, further comprises a receiving filter. In some embodiments, the receiver further comprises an optional transmission impairments mitigating equalizer, which is prior to the information retrieving equalizer. In some embodiments, the receiver further comprises a channel response adjustment (or, impulse response adjustment) as an

optional additional processing block prior to information retrieving equalization. In some embodiments, the information retrieving equalizer outputs the reliability estimates, often referred to as the soft information of the information symbols. In some embodiments, the information receiving equalizer functions as a trellis-based equalizer (e.g., a BCJR or SOVA equalizer), or as a reduced complexity trellis-based equalizer (e.g., a M-BCJR, T-BCJR, or SOMA equalizer). In some embodiments, the information receiving equalizer is divided in two parallel independent equalizers, one processing an I demodulator branch and the other working on a Q demodulator branch of a signal, thus significantly reducing the complexity of each equalizer. In some embodiments, the information receiving equalizer functions as a windowed variation of a maximum a posteriori equalizer that can work fully in parallel. In some embodiments, the information receiving equalizer supports a very large number (e.g., 72, or up to 80, or up to 100, or greater than 100) of windowed MAP equalizers which are fully parallel and independent (or in a slight sliding window variant), thus achieving large system throughputs. In some embodiments, iterative detection is employed, wherein the information retrieving equalizer outputs likelihood estimates LLRs on the received symbols and pass it on to the error control decoder with the information retrieving equalizer and the error control decoder iteratively exchanging their estimates on the received information for a number of times (i.e., in a turbo equalization loop).

[00104] In some embodiments of the system described above, non-linear transformation of LLRs (e.g., low quality LLRs) is employed in order to transform them into an appropriate optimized form for turbo equalization loop constituents (i.e., equalizer and error control decoder), which can significantly improve overall system gain. In some embodiments, soft information LLRs are interleaved/deinterleaved between turbo equalization loop constituents. In some embodiments, the turbo equalization loop has a plurality of iterations (i.e., turbo iterations) and the number of iterations is optimized for attainment of performance closer to the optimized achievable information rates and overall system throughput. In some embodiments, turbo loop interleavers/deinterleavers are specifically designed to support a high level of parallelism of windowed equalizer and are quasi-random and contention free.

[00105] In some embodiments, a BCET communication system contains a transmitter that employs a pulse-shaping filter, and the filter response is designed using a numerical optimization procedure.

[00106] In some embodiments, a BCET communication system contains a receiver that employs joint channel symbol detection and error control code symbol detection that are combined using iterative decoding. In some embodiments, the error control code is obtained by a numerical optimization procedure.

[00107] In some embodiments, a BCET communication system contains an early termination criterion for LDPC codes to reduce the number of LDPC iterations, which in turn results in the overall reduction of the duration of the processing performed by the turbo equalization loop. This can be advantageous, for example, by enabling substantial power savings at the receiver.

[00108] In some embodiments, a BCET communication system contains an outer block code, such as a BCH code or a Reed-Solomon code.

[00109] In some embodiments, a method for optimizing LDPC codes in BCET systems includes: a) providing a parity check matrix of a low-density parity-check (LDPC) code, which is employed in error correction techniques in turbo-equalization-based bandwidth-constrained communication systems; and b) determining an optimized non-linear transformation of input log-likelihood ratios (LLRs) to the error correction decoder adjusted jointly with the parity check matrix.

[00110] In some embodiments, the method for optimizing LDPC codes in the BCET systems above further includes the utilization of an equalizer that operates using BCJR (Bahl-Cocke-Jelinek-Raviv) algorithms, Viterbi algorithms, reduced trellis states, and/or reduced trellis search variants of BCJR and Viterbi algorithms.

[00111] In some embodiments, the method for optimizing LDPC codes in the BCET systems above further includes the utilization of a plurality of equalizer complexity reduction techniques and/or partial response channel shortening.

[00112] In some embodiments, the method for optimizing LDPC codes in the BCET systems above further includes the utilization of pulse-shaping and receiving filters such as those described above and in U.S. Patent Application Pub. No. 2014/0269894, and U.S. Pat. No. 9,154,346.

[00113] In some embodiments, the method for optimizing LDPC codes in the BCET systems above results in the optimized transmission system

outperforming ISI-free transmission in terms of achievable information rate, for the same signal-to-noise ratio (SNR) and the same occupied bandwidth.

[00114] In some embodiments, the method for optimizing LDPC codes in the BCET systems above results in an optimized transmission system that outperforms the ISI-free transmission in terms of signal-to-noise ratio (SNR), for the same achievable information rate and the same occupied bandwidth.

[00115] FIG. 12 shows an example of a receiver processing architecture method 1200 that can be performed using the systems described above, in some embodiments. In some embodiments, a method comprises: a) jointly configuring a pulse-shaping transmission filter (in the transmitter), a receiving filter, and an optional channel impulse response adjustment block (in the receiver) in bandwidth-constrained communication systems (in step 1210); b) defining a set of constraints regarding occupied spectral bandwidth and methods for reducing complexity of the equalizer (in step 1220); and c) determining an optimized equivalent partial impulse response, which maximizes achievable information rate of a transmission system, based on pulse shapes with optimal time-bandwidth occupancies (e.g., using prolate spheroidal wave functions or Gaussian functions), and for the predefined other set of constraints (in step 1230). In some embodiments, the method described above further includes a pulse-shaping filter that satisfies a set of predefined constraints regarding the spectral mask, in the presence of non-linear distortion of the transmitted signal.

[00116] FIG. 13 shows an example of a method 1300 for optimizing LDPC codes that can be performed using the systems described above, in some embodiments. In some embodiments, a method comprises: a) performing an optimization procedure for optimizing a parity check matrix in a case in which the LDPC code is employed as an error correcting code (e.g., in the communication system described above) (in step 1310); b) performing an optimization procedure coupled with a specific information retrieving equalizer architecture, such as an optimal or reduced variant (in step 1320); and c) performing an optimization procedure based on a density evolution (DE) technique or extrinsic information transfer (EXIT) chart curve fitting technique (in step 1330).

[00117] In some embodiments, a communication system described above, when optimized using the methods described above, can produce a large number of operating points when performing close to or above traditional Shannon capacity bounds.

[00118] Reference has been made in detail to embodiments of the disclosed invention, one or more examples of which have been illustrated in the accompanying figures. Each example has been provided by way of explanation of the present technology, not as a limitation of the present technology. In fact, while the specification has been described in detail with respect to specific embodiments of the invention, it will be appreciated that those skilled in the art, upon attaining an understanding of the foregoing, may readily conceive of alterations to, variations of, and equivalents to these embodiments. For instance, features illustrated or described as part of one embodiment may be used with another embodiment to yield a still further embodiment. Thus, it is intended that the present subject matter covers all such modifications and variations within the scope of the appended claims and their equivalents. These and other modifications and variations to the present invention may be practiced by those of ordinary skill in the art, without departing from the scope of the present invention, which is more particularly set forth in the appended claims. Furthermore, those of ordinary skill in the art will appreciate that the foregoing description is by way of example only, and is not intended to limit the invention.

What is claimed is:

1. A bandwidth constrained equalized transport (BCET) communication system, comprising:

a transmitter that transmits a signal, comprising:

an error control code encoder;

a pulse-shaping filter; and

a first interleaver;

a communication channel that transports the signal; and

a receiver that receives the signal, comprising:

a receiving filter;

an information-retrieving equalizer;

a deinterleaver with an error control code decoder; and

a second interleaver;

wherein:

the error control code encoder appends redundant information onto the signal;

the pulse-shaping filter intentionally introduces memory into the signal in the form of inter-symbol interference;

the receiving filter is matched to the pulse-shaping filter;

the information-retrieving equalizer is a trellis-based equalizer;

the information-retrieving equalizer, the second interleaver, and the deinterleaver with the error control code decoder are joined in an iterative turbo equalization loop;

the communication system is bandwidth constrained;

the error control code encoder is a low-density parity-check (LDPC) error control code encoder;

the error control encoder comprises code that is optimized based on the intentionally introduced memory into the signal, a code rate, a signal-to-noise ratio, and an equalizer structure in the receiver; and

the signal comprises an information rate that is higher than for an equivalent system without intentional introduction of the memory at the transmitter.

2. The bandwidth constrained equalized transport (BCET) communication system of claim 1, wherein the error control code encoder further comprises:

code belonging to an irregular repeat accumulator (IRA) class of codes, that enables linear complexity of the encoding; and

a parity check matrix that can be rearranged in quasi-cyclic (QC) form, that enables layered decoding without hardware memory conflicts.

3. The bandwidth constrained equalized transport (BCET) communication system of claim 1, wherein the pulse-shaping filter utilizes prolate spheroid wave functions, or Gaussian wave functions, or digital, or discrete representations thereof.

4. The bandwidth constrained equalized transport (BCET) communication system of claim 1, wherein the pulse-shaping filter introduces a factor 3 or more of spectral compression compared to a square-root raised cosine (SRRC) power spectrum of the full response channel.

5. The bandwidth constrained equalized transport (BCET) communication system of claim 1, wherein the trellis-based equalizer comprises an algorithm that can accommodate colored noise, and is selected from the group consisting of a full Bahl-Cocke-Jelinek-Raviv (BCJR) equalizer, a soft output Viterbi algorithm (SOVA) equalizer, a max-BCJR equalizer, an M-BCJR equalizer, a T-BCJR equalizer, a forward-only BCJR equalizer, or a windowed BCJR equalizer.

6. The bandwidth constrained equalized transport (BCET) communication system of claim 1, wherein the information-retrieving equalizer contains a plurality of modules in a parallel arrangement, wherein each module contains a Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm that is windowed or partitioned, and wherein the system throughput is improved compared to a BCET communication system wherein the information-retrieving equalizer contains a single module containing a BCJR algorithm.

7. The bandwidth constrained equalized transport (BCET) communication system of claim 6, wherein the number of modules is from 10 to 100, or is 72.

8. The bandwidth constrained equalized transport (BCET) communication system of claim 1, further comprising a noise whitening filter before the information-retrieving equalizer in the receiver.

9. The bandwidth constrained equalized transport (BCET) communication of claim 1, wherein the iterative turbo equalization loop comprises from 3 to 15 turbo iterations.

10. The bandwidth constrained equalized transport (BCET) communication of claim 1, wherein the error control code encoder further comprises:

code belonging to an irregular repeat accumulator (IRA) class of codes, that enables linear complexity of the encoding;

a parity check matrix that can be rearranged in quasi-cyclic (QC) form, that enables layered decoding without hardware memory conflicts;

a degree distribution and parameters of the turbo equalization loop that are optimized for a known partial response channel and a required level of parallelism; and

the code compensates for imprecision that is due to a level of complexity of the turbo equalization loop.

11. A method comprising:

providing a signal comprising symbols;

encoding the symbols using an error control code encoder in a transmitter of a communication system to produce encoded symbols, wherein:

the error control code encoder appends redundant information onto the symbols; and

the error control code encoder is a low-density parity-check (LDPC) error control code encoder;

interleaving the encoded symbols using a first interleaver in the transmitter to produce interleaved symbols;

intentionally introducing memory into the interleaved symbols in the form of inter-symbol interference using a pulse-shaping filter in the transmitter to produce pulse-shaped symbols;

transmitting the pulse-shaped symbols to a receiver of the communication system over a physical memoryless channel with additive white Gaussian noise;

receiving the transmitted pulse-shaped symbols using a receiving filter in the receiver to produce a receiving filtered signal, wherein the receiving filter is matched to the pulse-shaping filter;

equalizing the receiving filtered signal using an information-retrieving equalizer in the receiver to produce equalized symbols, wherein the information-retrieving equalizer is a trellis-based equalizer;

deinterleaving the equalized symbols using a deinterleaver in the receiver to produce deinterleaved symbols;

processing the deinterleaved symbols using a non-linear function block in the receiver to produce a non-linear signal, wherein the non-linear function block transforms the deinterleaved symbols according to a non-linear function;

decoding the non-linear signal using an error control code decoder in the receiver to produce decoded symbols; and

iteratively updating the decoded symbols using a turbo equalization loop in the receiver to produce updated decoded symbols after each iteration, wherein the turbo equalization loop in the receiver comprises iteratively repeating:

equalizing iterated interleaved symbols using the information-retrieving equalizer to produce iterated equalized symbol likelihoods;

deinterleaving the iterated equalized symbol likelihoods using a deinterleaver in the turbo equalization loop to produce iterated deinterleaved symbol likelihoods;

transforming the iterated deinterleaved symbol likelihoods using the non-linear function to produce iterated non-linearly transformed symbol likelihoods;

decoding the iterated non-linearly transformed symbol likelihoods to produce updated decoded symbol likelihoods; and

interleaving the updated decoded symbol likelihoods using a second interleaver in the turbo equalization loop to produce an iterated interleaved signal comprising the updated decoded symbols;

wherein:

the error control encoder comprises code that is optimized based on the intentionally introduced memory into the signal, a code rate, a signal-to-noise ratio, and an equalizer structure in the receiver;

the communication system is bandwidth constrained; and

the transmitted signal comprises an information rate that is higher than for an equivalent system without intentional introduction of the memory at the transmitter.

12. The method of claim 11, further comprising optimizing a distribution of variable node degrees and check node degrees in the code of the low-density parity-check (LDPC) error control code encoder, and optimizing parameters of the non-linear function, based on a density evolution for partial response channels.

13. The method of claim 12, wherein the optimized distribution of the variable node degrees and check node degrees in the code of the low-density parity-check (LDPC) error control code encoder and the parameters of the non-linear function satisfy a predefined set of constraints that enable construction of structured quasi-cyclic (QC) irregular repeat accumulator (IRA) codes, for a desired complexity of the error control code decoder and level of parallelism.

14. A method comprising:

a. providing:

a bandwidth constrained equalized transport (BCET) communication system comprising a transmitter, a receiver, a partial channel response, a channel equalization structure, a low-density parity-check (LDPC) error control code encoder in the transmitter, and a non-linear function block in the receiver; and

input parameters comprising a codeword length, a code rate, a level of parallelism, and a maximum variable degree;

b. initializing a variable node degree distribution;

c. calculating a check node degree distribution for the provided input parameters;

d. optimizing a variable node degree distribution for the LDPC codes in the LDPC error control encoder, and non-linear parameters of a non-linear function using a density evolution algorithm for partial response channels;

e. calculating a corresponding threshold;

f. repeating steps b. – e. for different input parameters to generate a database of possible solutions; and

g. recalculating the variable node degree distribution and the check node degree distribution for a part of a parity check matrix (H_1) excluding a double diagonal matrix.

15. The method of claim 14, further comprising:

constructing a prototype matrix;

generating the parity check matrix from the prototype matrix, wherein the parity check matrix is suitable for layered decoding;

generating a corresponding permuted parity check matrix from the parity check matrix, wherein the permuted parity check matrix is suitable for low complexity encoding; and

estimating a real variable node degree distribution and a real check node degree distribution from the generated parity check matrix.

16. The method of claim 15, wherein the construction of the prototype matrix comprises:

providing a known optimal variable node degree distribution and a known optimal check node degree distribution for a prototype matrix (H), obtained previously by using the density evolution algorithm, wherein the prototype matrix H comprises the first part H_1 and a double diagonal matrix part H_2;

recalculating the variable node degree distribution and the check node degree distribution according to the known optimal variable node degree distribution and the known optimal check node degree distribution to correspond to H_1;

generating a binary masking matrix;

generating the prototype matrix with size $(1-R)n/P \times nR/P$ from the recalculated variable node degree distribution and check node degree distribution using any method for generating a prototype matrix of random low-density parity-

check (LDPC) codes, wherein R is the code rate, n is the codeword length, and P is the level of paralelism; and

concatenating the double diagonal matrix part (H_2) with the first part H_1 to complete the prototype matrix H, wherein $H = [H_1 H_2]$.

17. The method of claim 16, wherein:

R is greater than 0.25 and less than 1;

n is from 10000 to 1000000; and

P is from 1 to 720.

18. The method of claim 14, further comprising:

after recalculating the variable node degree distribution and the check node degree distribution for the first part of the parity check matrix H_1 excluding the double diagonal matrix, if it is not possible to construct the prototype matrix, then reducing the maximum variable degree and/or redefine check node degrees corresponding to the check node degree distribution;

repeating steps b. – g.;

constructing the prototype matrix;

generating the parity check matrix from the prototype matrix, wherein the parity check matrix is suitable for layered decoding;

generating a permutation matrix from the parity check matrix, wherein the permutation matrix is suitable for low complexity encoding; and

estimating a real variable node degree distribution and a real check node degree distribution from the permutation matrix.

19. The method of claim 18, wherein the constructing of the prototype matrix comprises:

providing a known optimal variable node degree distribution and a known optimal check node degree distribution for the prototype matrix (H), obtained previously by using the density evolution method, wherein the prototype matrix H comprises a first part H_1 and a double diagonal matrix part H_2;

recalculating the variable node degree distribution and the check node degree distribution according to the known optimal variable node degree distribution and known optimal check node degree distribution to correspond to H_1;

generating a binary masking matrix;

generating the prototype matrix with size (1-R)n/P × nR/P from the recalculated variable node degree distribution and the check node degree distribution using any method for generating a prototype matrix of random low-density parity-check (LDPC) codes, wherein R is the code rate, n is the codeword length, and P is the level of paralelism; and

concatenating the double diagonal matrix (H_2) with the first part H_1 to complete the prototype matrix H, wherein $H = [H_1\ H_2]$.

20. The method of claim 19, wherein:

R is greater than 0.25 and less than 1;

n is from 10000 to 1000000; and

P is from 1 to 720.

21. The method of claim 16, wherein the bandwidth constrained equalized transport (BCET) communication system transmits a signal comprising an information rate that is higher than for an equivalent system without intentional introduction of the memory at the transmitter.

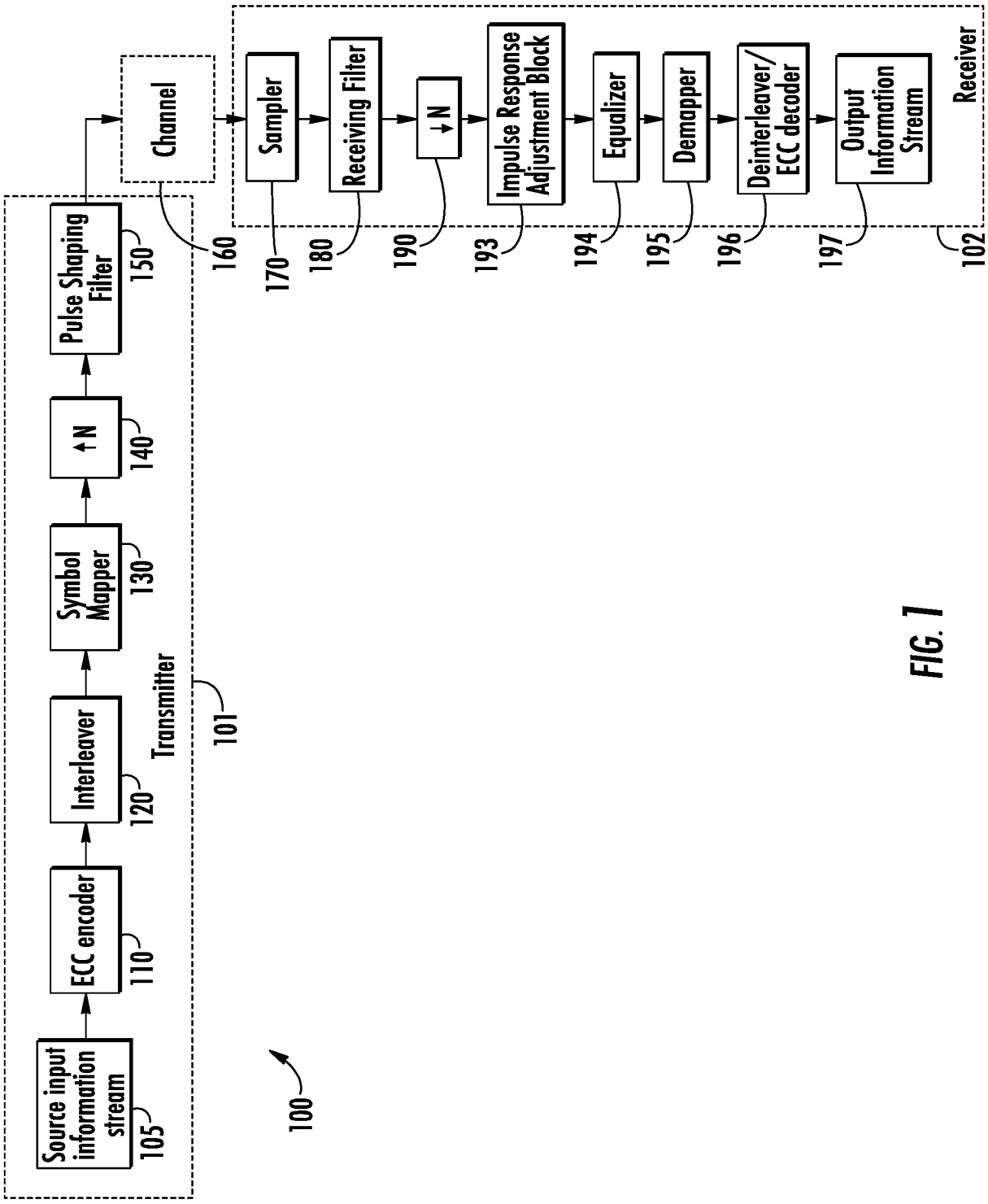
Source input information stream
105
ECC encoder
110
Interleaver
120
Symbol Mapper
130
↑N
140
Pulse Shaping Filter
150
Transmitter
101
100
Channel
160
Sampler
170
Receiving Filter
180
↓N
190
Impulse Response Adjustment Block
193
Equalizer
194
Demapper
195
Deinterleaver/ ECC decoder
196
Output Information Stream
197
Receiver
102

FIG. 1

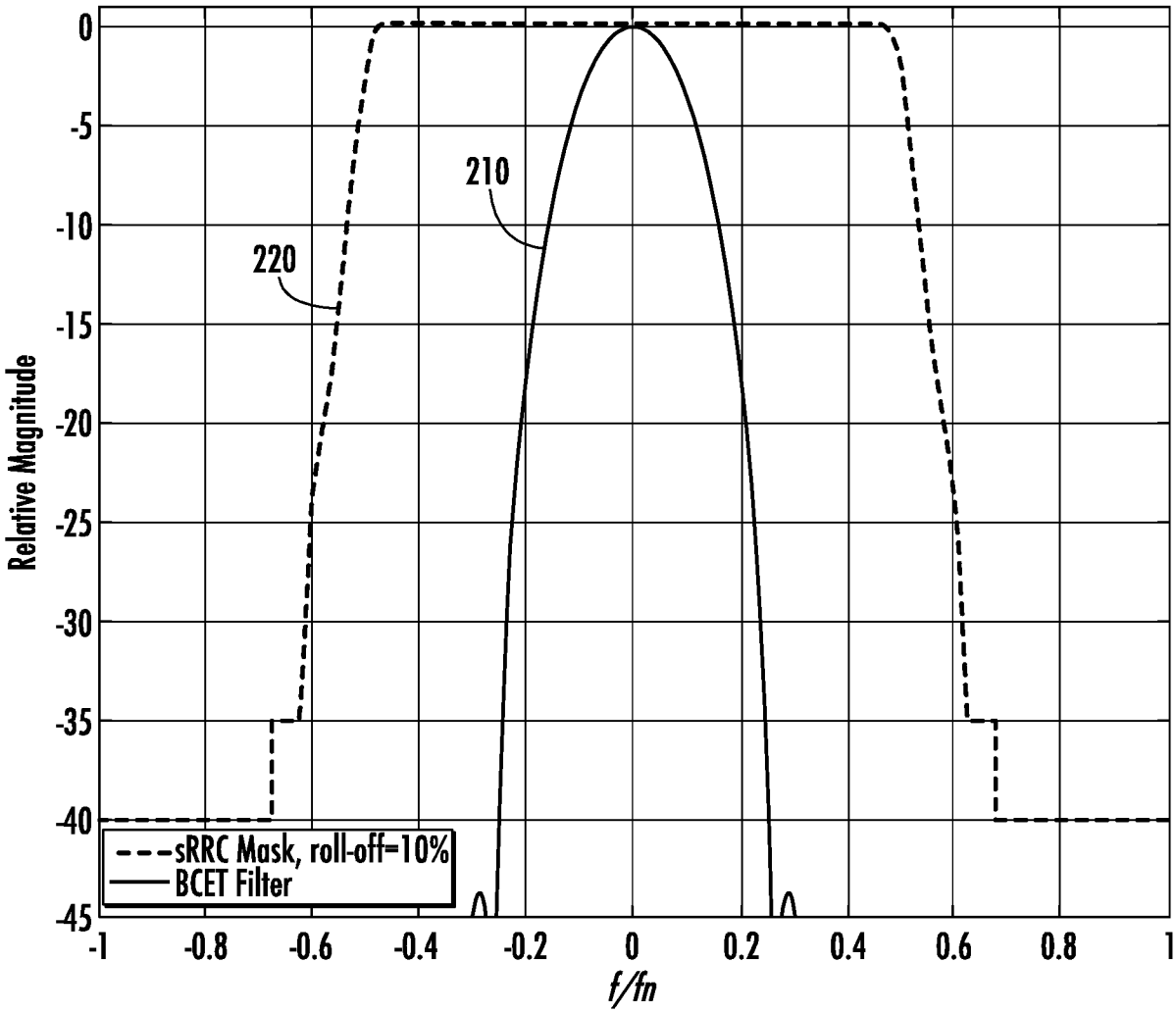
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
Relative Magnitude
210
220
sRRC Mask, roll-off=10%
BCET Filter
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1
f/fn

FIG. 2

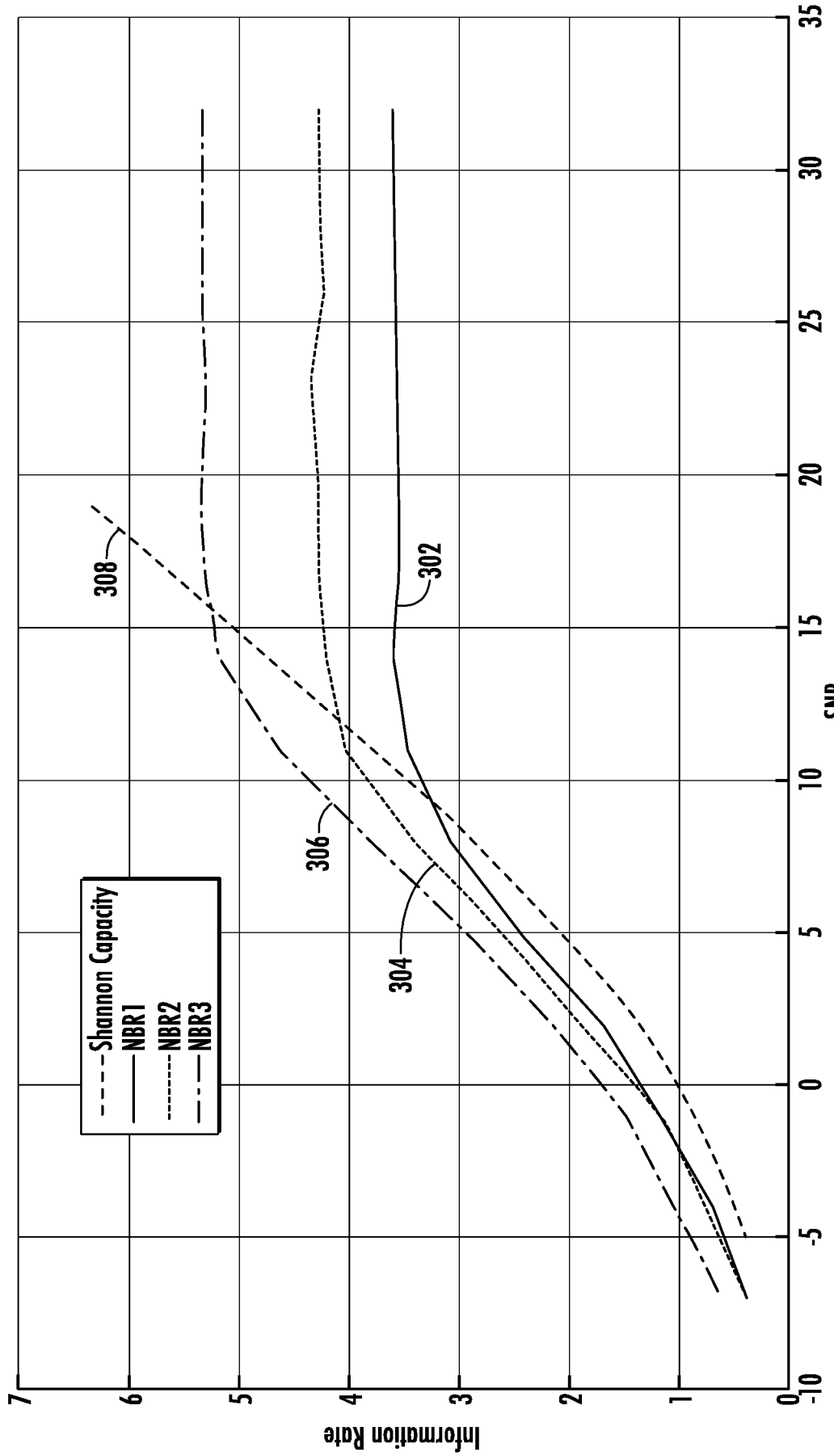
Information Rate
SNR
Shannon Capacity
NBR1
NBR2
NBR3
302
304
306
308
0
1
2
3
4
5
6
7
-10
-5
0
5
10
15
20
25
30
35

FIG. 3

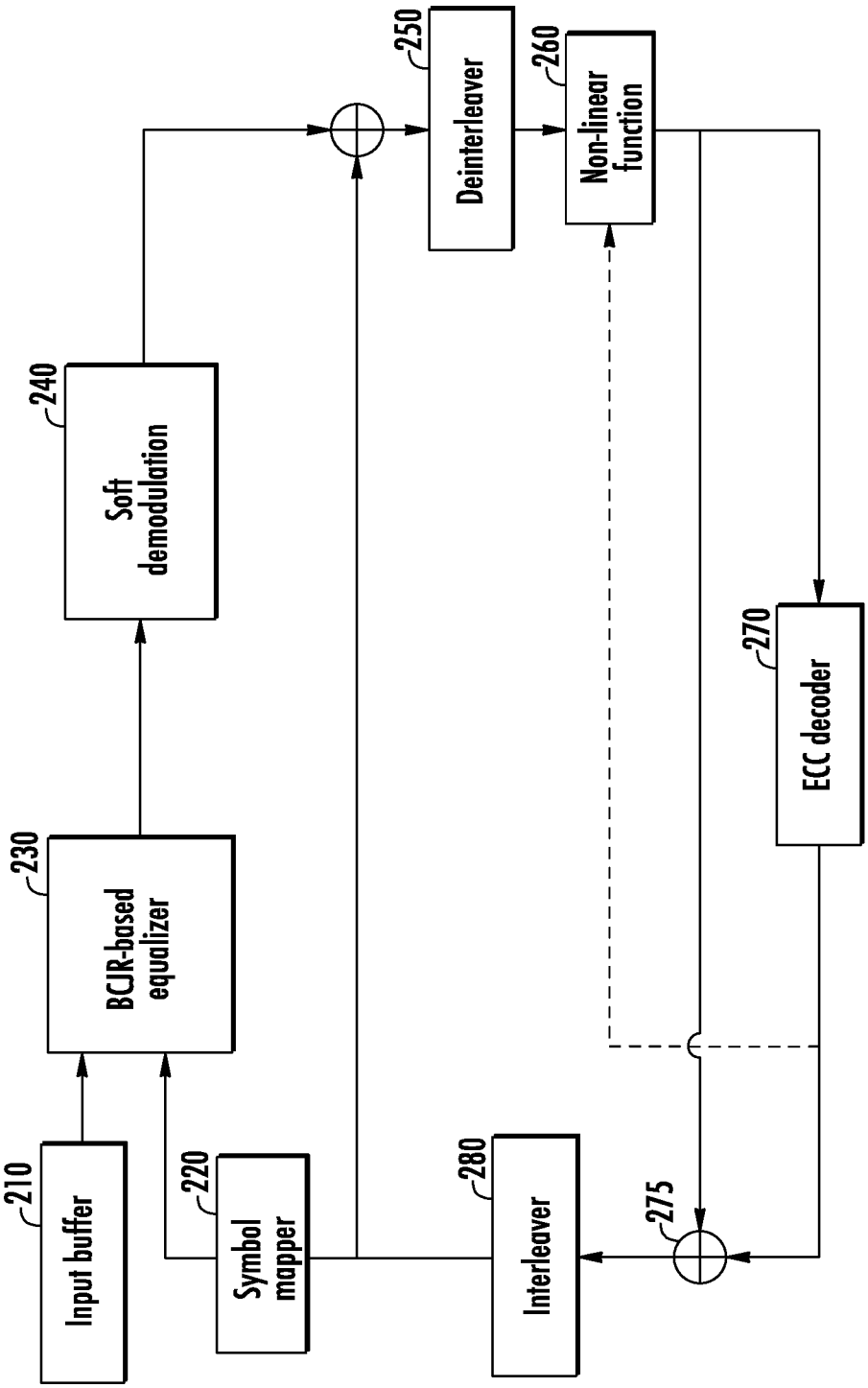
210
Input buffer
220
Symbol mapper
230
BCJR-based equalizer
240
Soft demodulation
250
Deinterleaver
260
Non-linear function
270
ECC decoder
275
280
Interleaver

FIG. 4

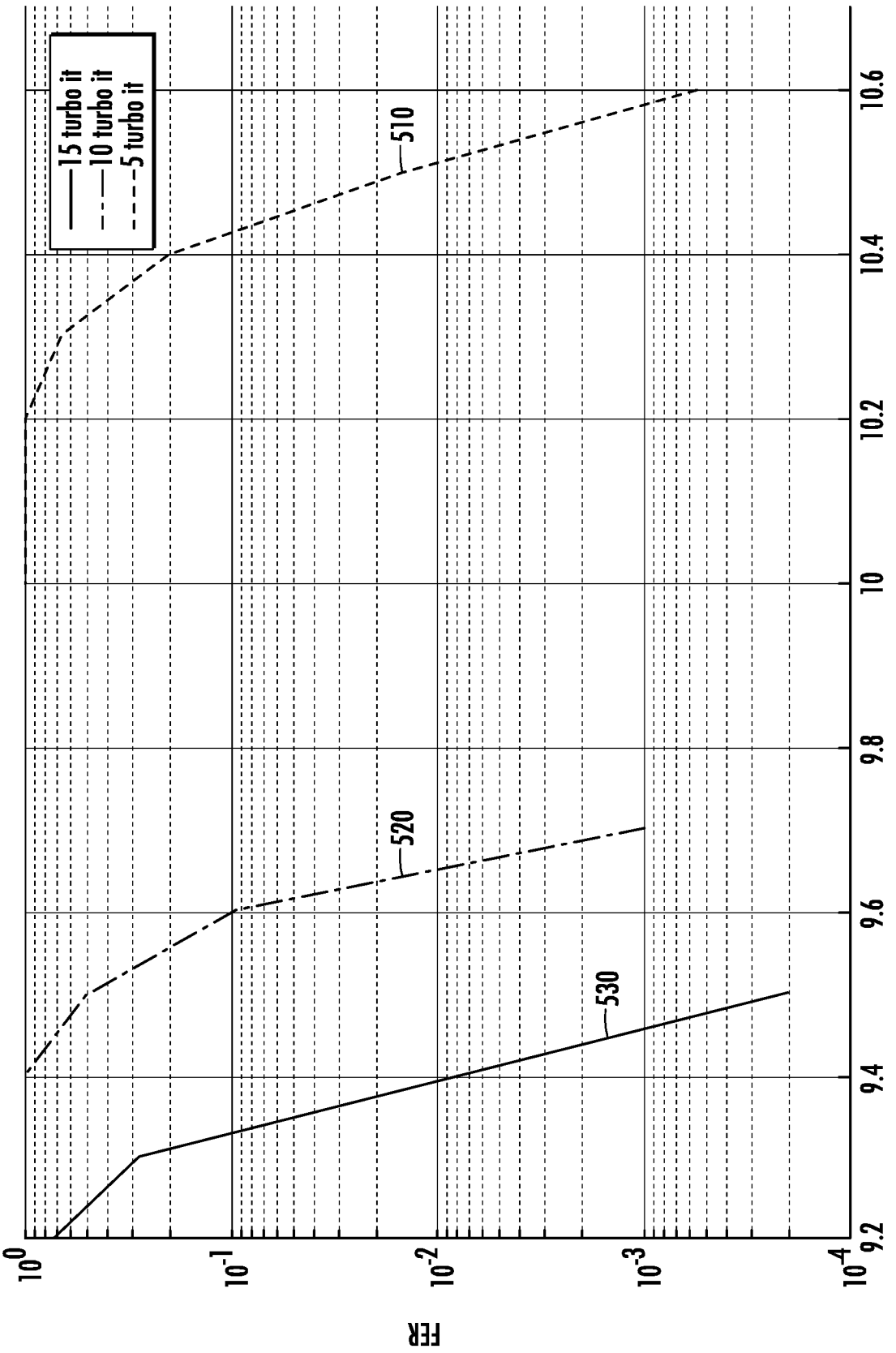
15 turbo it
10 turbo it
5 turbo it
510
520
530
FER
snr [dB]
10^0
10^-1
10^-2
10^-3
10^-4
9.2
9.4
9.6
9.8
10
10.2
10.4
10.6

FIG. 5

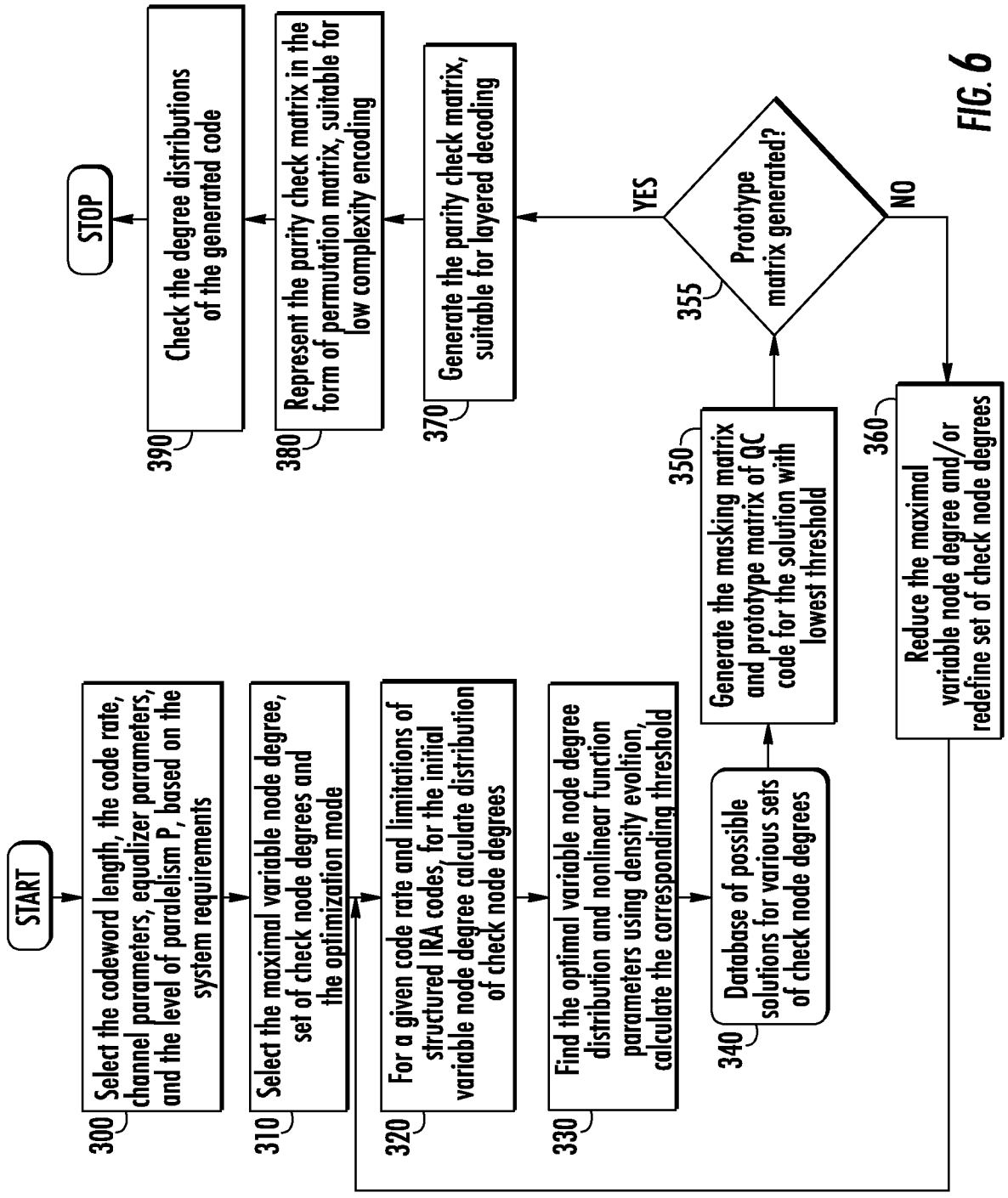
START
300 Select the codeword length, the code rate, channel parameters, equalizer parameters, and the level of parallelism P, based on the system requirements
310 Select the maximal variable node degree, set of check node degrees and the optimization mode
320 For a given code rate and limitations of structured IRA codes, for the initial variable node degree calculate distribution of check node degrees
330 Find the optimal variable node degree distribution and nonlinear function parameters using density evolution, calculate the corresponding threshold
340 Database of possible solutions for various sets of check node degrees
350 Generate the masking matrix and prototype matrix of QC code for the solution with lowest threshold
355 Prototype matrix generated?
YES
NO
360 Reduce the maximal variable node degree and/or redefine set of check node degrees
370 Generate the parity check matrix, suitable for layered decoding
380 Represent the parity check matrix in the form of permutation matrix, suitable for low complexity encoding
390 Check the degree distributions of the generated code
STOP

FIG. 6

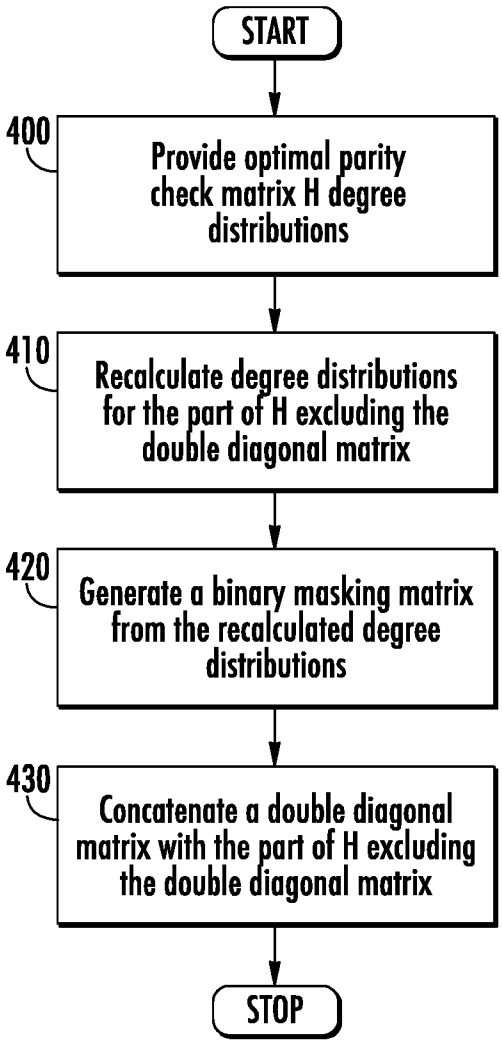
START
400
Provide optimal parity check matrix H degree distributions
410
Recalculate degree distributions for the part of H excluding the double diagonal matrix
420
Generate a binary masking matrix from the recalculated degree distributions
430
Concatenate a double diagonal matrix with the part of H excluding the double diagonal matrix
STOP

FIG. 7

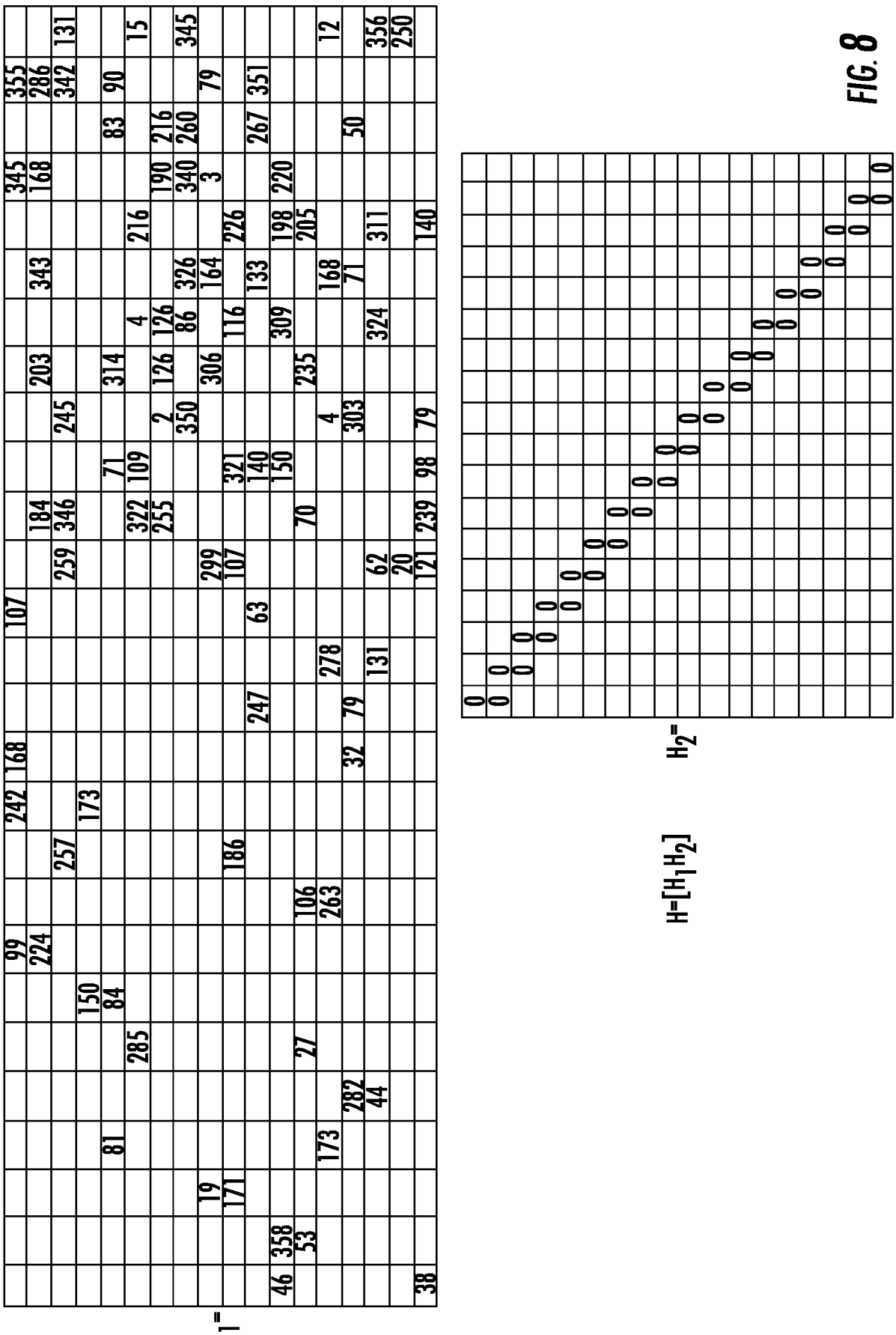

FIG. 8

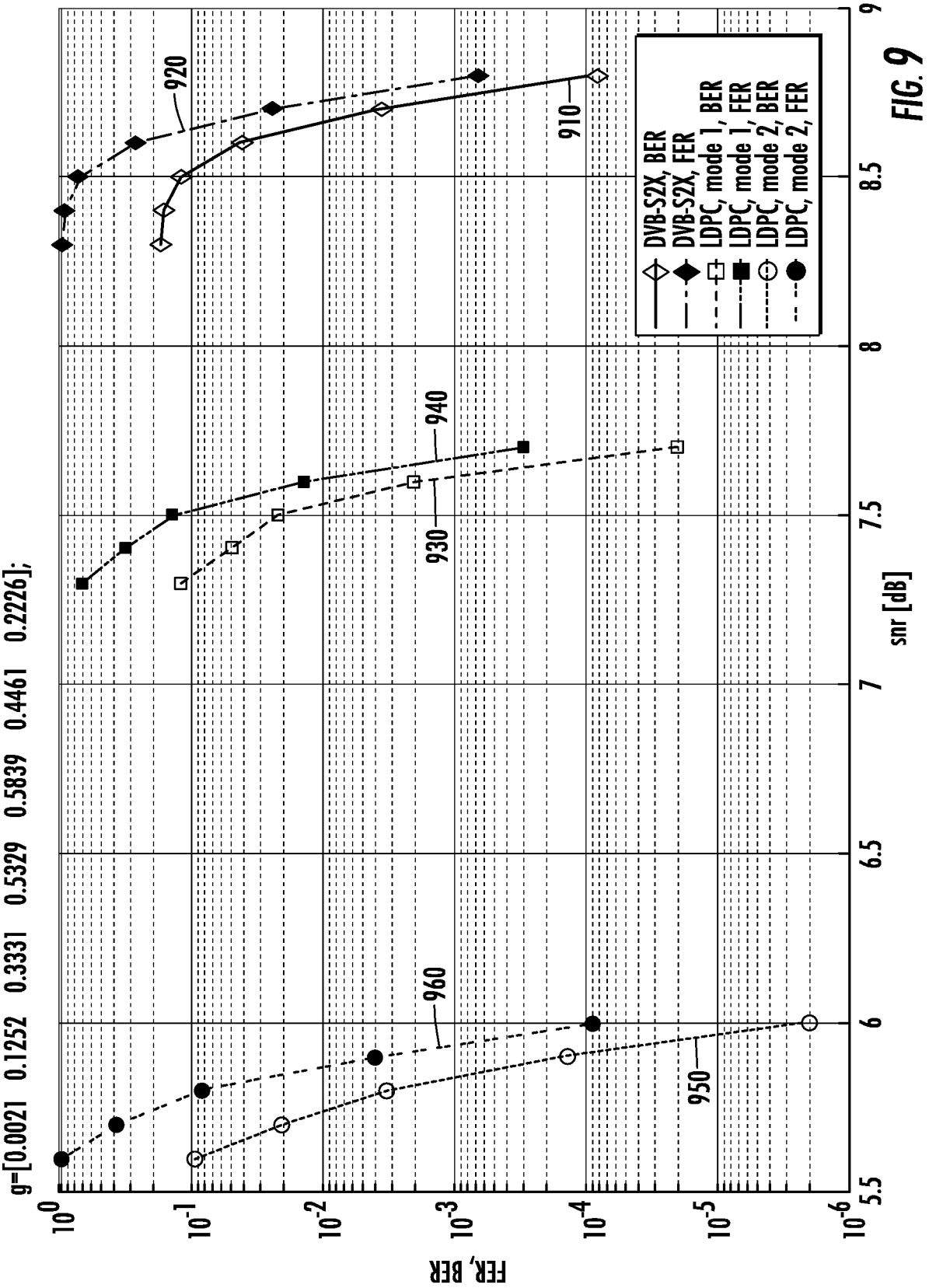
g=[0.0021 0.1252 0.3331 0.5329 0.5839 0.4461 0.2226];
FER, BER
snr [dB]
DVB-S2X, BER
DVB-S2X, FER
LDPC, mode 1, BER
LDPC, mode 1, FER
LDPC, mode 2, BER
LDPC, mode 2, FER
910
920
930
940
950
960

FIG. 9

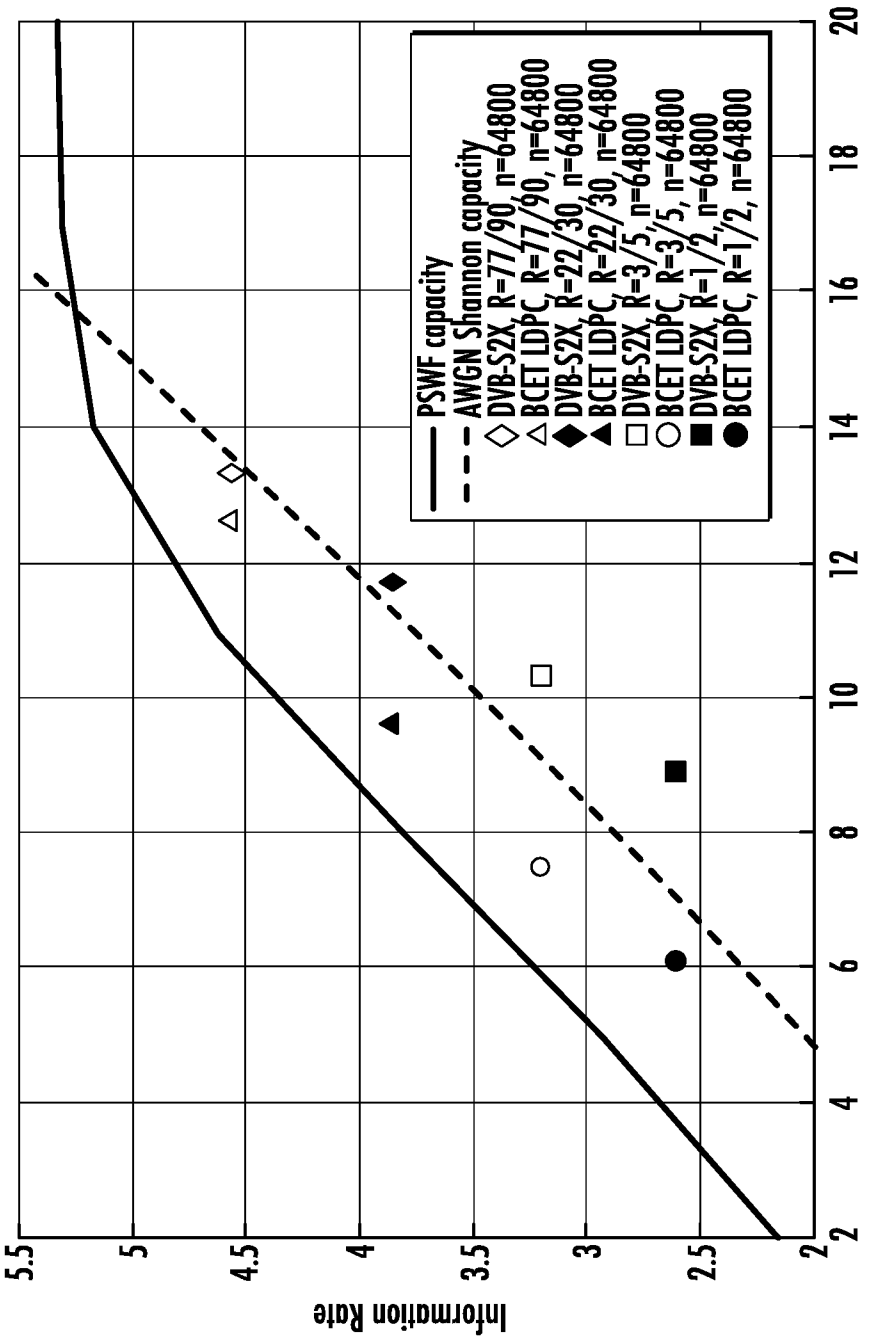
PSWF capacity
AWGN Shannon capacity
DVB-S2X, R=77/90, n=64800
BCET LDPC, R=77/90, n=64800
DVB-S2X, R=22/30, n=64800
BCET LDPC, R=22/30, n=64800
DVB-S2X, R=3/5, n=64800
BCET LDPC, R=3/5, n=64800
DVB-S2X, R=1/2, n=64800
BCET LDPC, R=1/2, n=64800
Information Rate
snr [dB]
5.5
5
4.5
4
3.5
3
2.5
2
2
4
6
8
10
12
14
16
18
20

FIG. 10

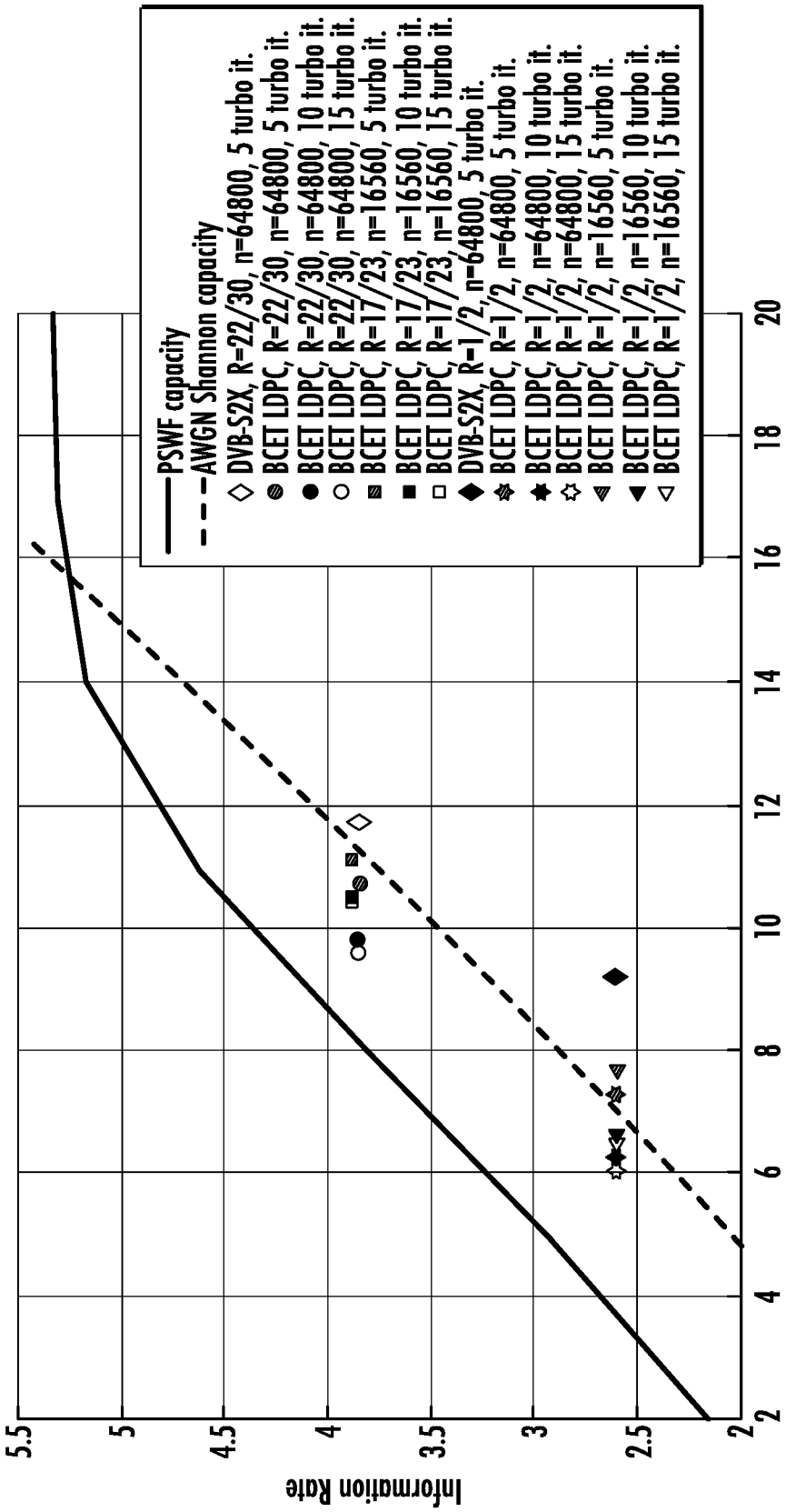
PSWF capacity
AWGN Shannon capacity
DVB-S2X, R=22/30, n=64800, 5 turbo it.
BCET LDPC, R=22/30, n=64800, 5 turbo it.
BCET LDPC, R=22/30, n=64800, 10 turbo it.
BCET LDPC, R=22/30, n=64800, 15 turbo it.
BCET LDPC, R=17/23, n=16560, 5 turbo it.
BCET LDPC, R=17/23, n=16560, 10 turbo it.
BCET LDPC, R=17/23, n=16560, 15 turbo it.
DVB-S2X, R=1/2, n=64800, 5 turbo it.
BCET LDPC, R=1/2, n=64800, 5 turbo it.
BCET LDPC, R=1/2, n=64800, 10 turbo it.
BCET LDPC, R=1/2, n=64800, 15 turbo it.
BCET LDPC, R=1/2, n=16560, 5 turbo it.
BCET LDPC, R=1/2, n=16560, 10 turbo it.
BCET LDPC, R=1/2, n=16560, 15 turbo it.
Information Rate
snr [dB]
5.5
5
4.5
4
3.5
3
2.5
2
2
4
6
8
10
12
14
16
18
20

FIG. 11

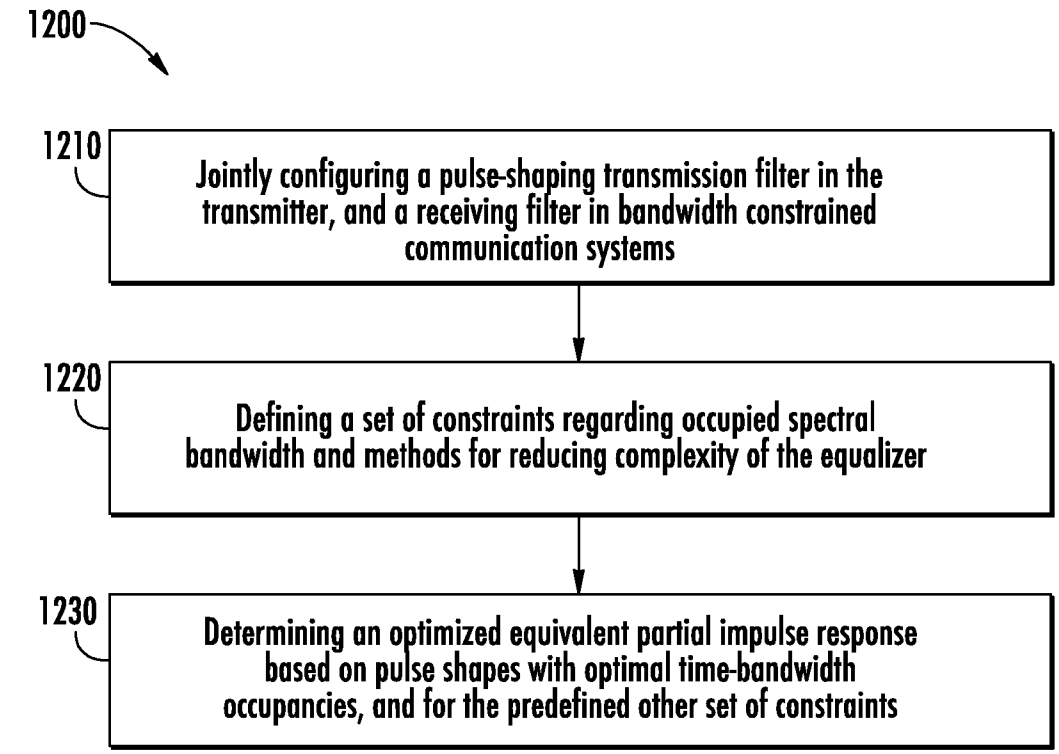
1200
1210
Jointly configuring a pulse-shaping transmission filter in the transmitter, and a receiving filter in bandwidth constrained communication systems
1220
Defining a set of constraints regarding occupied spectral bandwidth and methods for reducing complexity of the equalizer
1230
Determining an optimized equivalent partial impulse response based on pulse shapes with optimal time-bandwidth occupancies, and for the predefined other set of constraints

FIG. 12

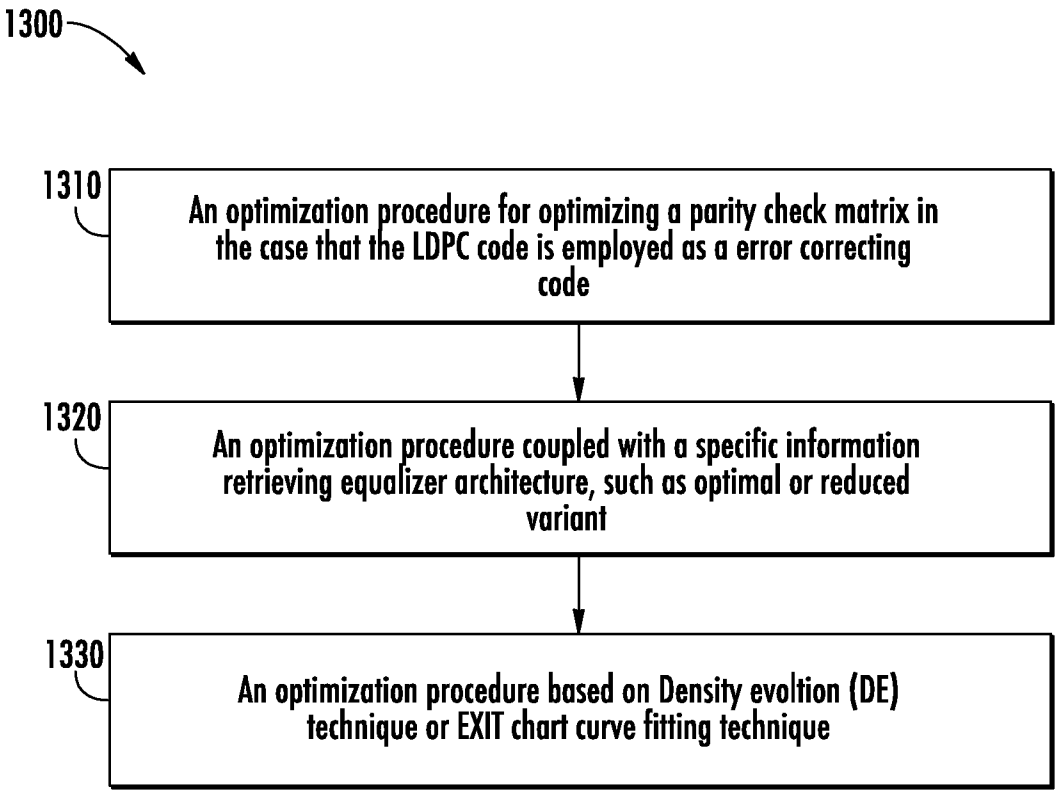
1300
1310
An optimization procedure for optimizing a parity check matrix in the case that the LDPC code is employed as a error correcting code
1320
An optimization procedure coupled with a specific information retrieving equalizer architecture, such as optimal or reduced variant
1330
An optimization procedure based on Density evoltion (DE) technique or EXIT chart curve fitting technique

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/033524

A. CLASSIFICATION OF SUBJECT MATTER

H03M 13/11(2006.01)i, H04L 1/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M 13/11; G06F 11/10; H03M 13/05; H04L 1/00; H04L 25/03; H04L 27/18; H04L 27/22; H04L 29/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: bandwidth constrained, equalize, pulse shaping, error control coding, LDPC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0269894 A1 (NIKOLA ALIC et al.) 18 September 2014 See claims 1,3 and fig. 1.	1-21
A	US 2016-0233979 A1 (MITSUBISHI ELECTRIC RESEARCH LABORATORIES, INC.) 11 August 2016 See claims 1-3 and fig. 1.	1-21
A	US 2012-0163489 A1 (STHANUNATHAN RAMAKRISHNAN) 28 June 2012 See claims 1-7 and fig. 1.	1-21
A	US 2015-0156041 A1 (MAGNACOM LTD.) 04 June 2015 See claims 21-30 and fig. 1.	1-21
A	US 2011-0276860 A1 (JING LEI et al.) 10 November 2011 See claims 1-5 and fig. 1.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 September 2019 (10.09.2019)	**10 September 2019 (10.09.2019)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/033524

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0269894 A1	18/09/2014	US 10020912 B2	10/07/2018
		US 10243690 B2	26/03/2019
		US 2018-0316459 A1	01/11/2018
US 2016-0233979 A1	11/08/2016	CN 107251439 A	13/10/2017
		EP 3248292 A2	29/11/2017
		JP 2017-533639 A	09/11/2017
		JP 6297215 B2	20/03/2018
		US 9722633 B2	01/08/2017
		WO 2016-129393 A2	18/08/2016
US 2012-0163489 A1	28/06/2012	US 9001948 B2	07/04/2015
US 2015-0156041 A1	04/06/2015	AU 2013-370955 A1	16/07/2015
		BR 112015015319 A2	11/07/2017
		CA 2896288 A1	03/07/2014
		CN 103516647 A	15/01/2014
		CN 104521141 A	15/04/2015
		CN 104521203 A	15/04/2015
		CN 104521204 A	15/04/2015
		CN 104769875 A	08/07/2015
		CN 104885088 A	02/09/2015
		CN 105007912 A	28/10/2015
		CR 20150386 A	07/10/2015
		EP 2865097 A2	29/04/2015
		EP 2865122 A2	29/04/2015
		EP 2865151 A2	29/04/2015
		EP 2938340 A1	04/11/2015
		HK 1216611 A1	25/11/2016
		IL 239593 A	31/08/2015
		JP 2016-504362 A	12/02/2016
		JP 2018-087241 A	07/06/2018
		KR 10-2015-0046003 A	29/04/2015
		KR 10-2015-0100903 A	02/09/2015
		MX 2015008361 A	11/03/2016
		NZ 630912 A	26/05/2017
		PH 12015501486 A1	21/09/2015
		RU 2015131141 A	03/02/2017
		RU 2663687 C2	08/08/2018
		SG 11201505111 A	30/07/2015
		US 2013-0343446 A1	26/12/2013
		US 2014-0003483 A1	02/01/2014
		US 2014-0133540 A1	15/05/2014
		US 2014-0301507 A1	09/10/2014
		US 2015-0131709 A1	14/05/2015
		US 2016-0254933 A1	01/09/2016
		US 8565363 B1	22/10/2013
		US 8665992 B1	04/03/2014
		US 8824572 B2	02/09/2014

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/033524

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 8972836 B2	03/03/2015
		US 8976853 B2	10/03/2015
		US 9137057 B2	15/09/2015
		WO 2013-190386 A2	27/12/2013
		WO 2014-016678 A3	15/05/2014
		ZA 201504762 B	26/10/2016
US 2011-0276860 A1	10/11/2011	CN 102349257 A	08/02/2012
		US 8537938 B2	17/09/2013
		WO 2010-083038 A2	22/07/2010