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(54) **SEMICONDUCTOR APPARATUS WITH VARIABLE RESISTOR HAVING TAPERED DOUBLE-LAYERED SIDEWALL SPACERS**

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(57) **ABSTRACT**

A method for fabricating a semiconductor apparatus includes forming a variable resistor region, and forming a spacer having a top linewidth and a bottom linewidth substantially equal to each other in the variable resistor region. The forming of the spacer includes forming a first insulating layer in the variable resistor region through a first method, forming a second insulating layer along a surface of the first insulating layer in the variable resistor region through a second method for providing step coverage superior to the first method, and etching the first and second insulating layers.

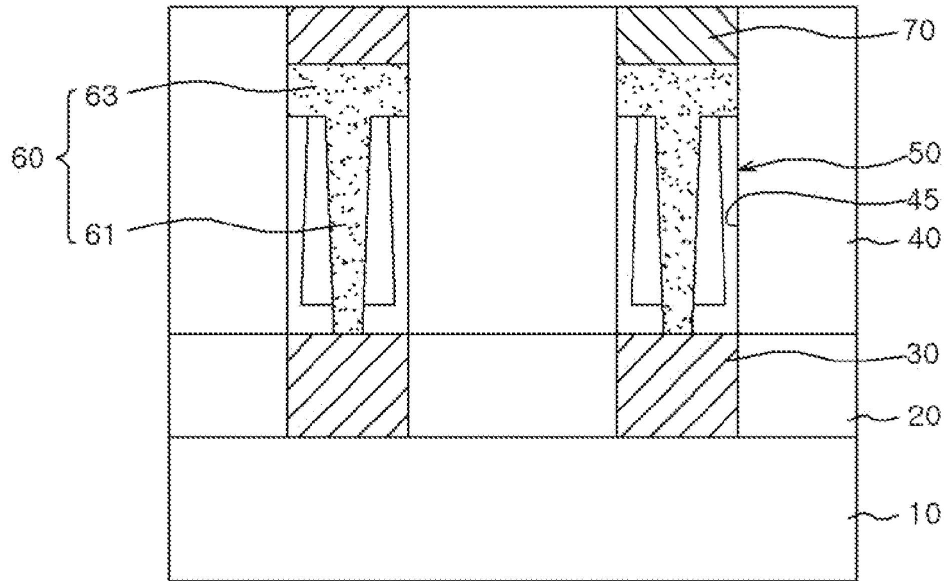


FIG.1

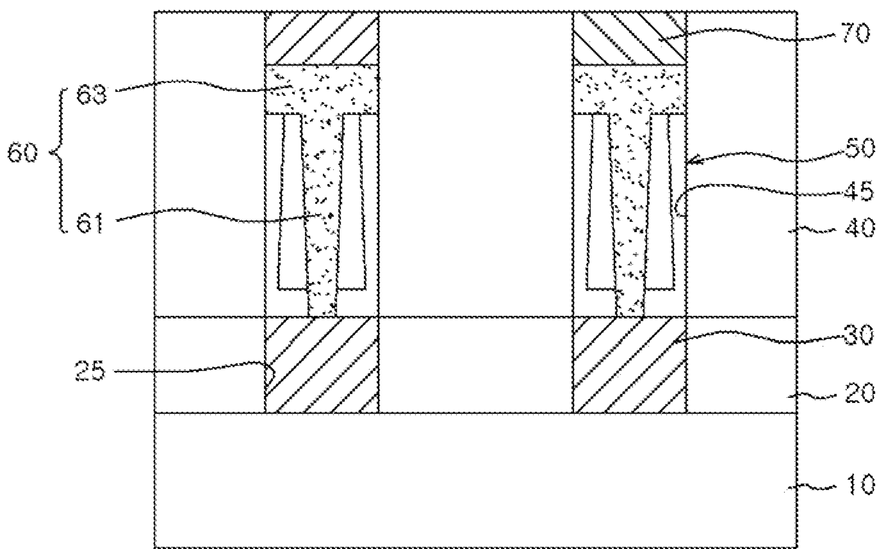


FIG.2

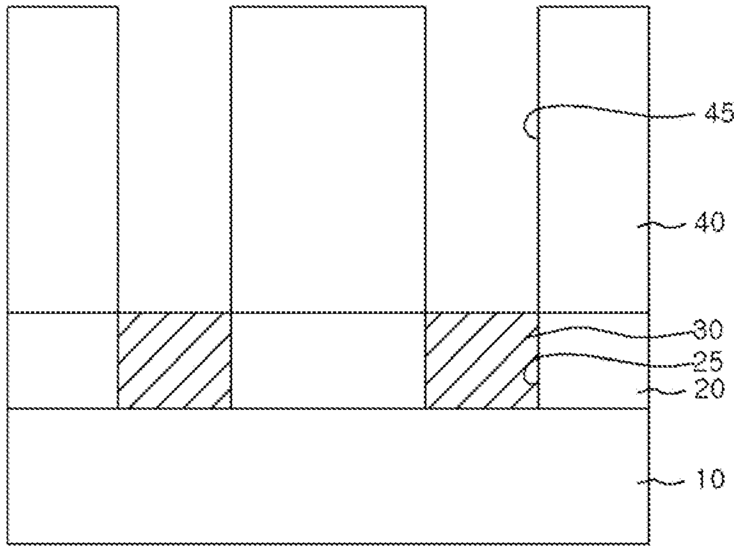


FIG.3

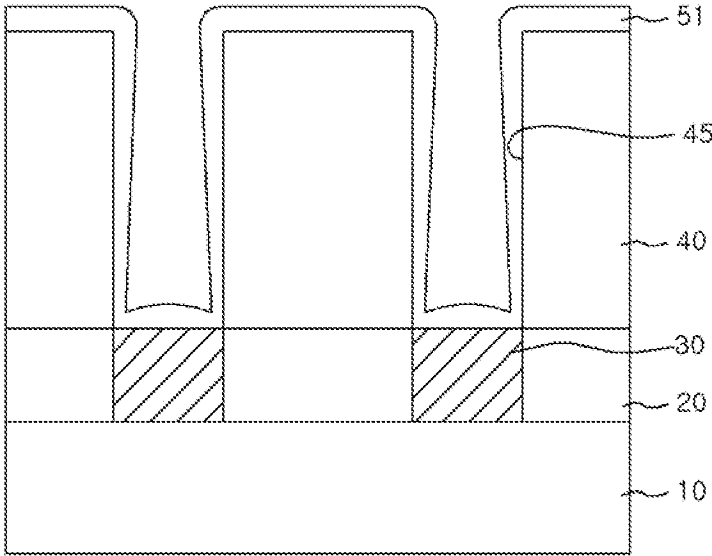


FIG.4

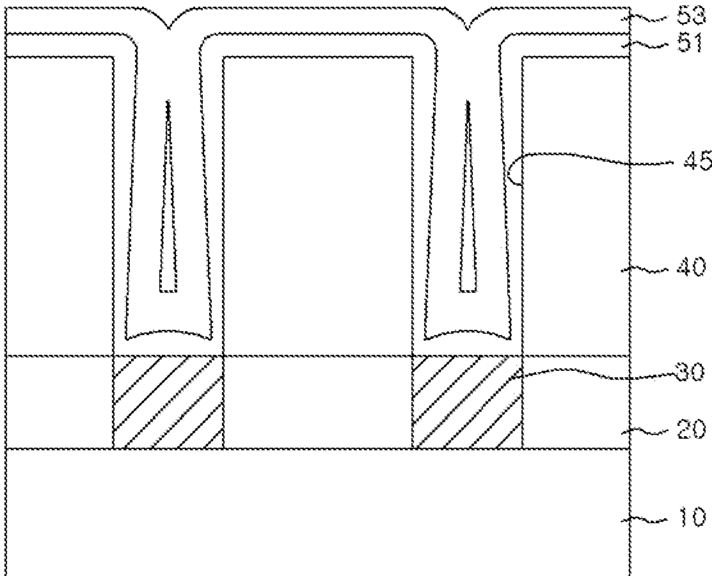


FIG.5

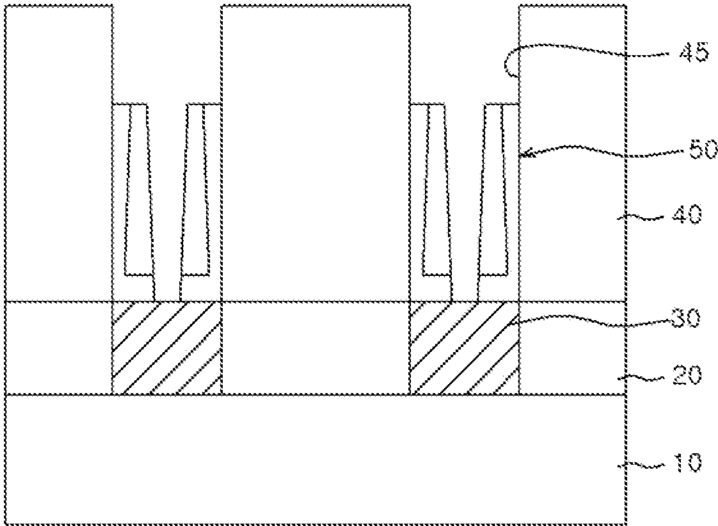


FIG.6

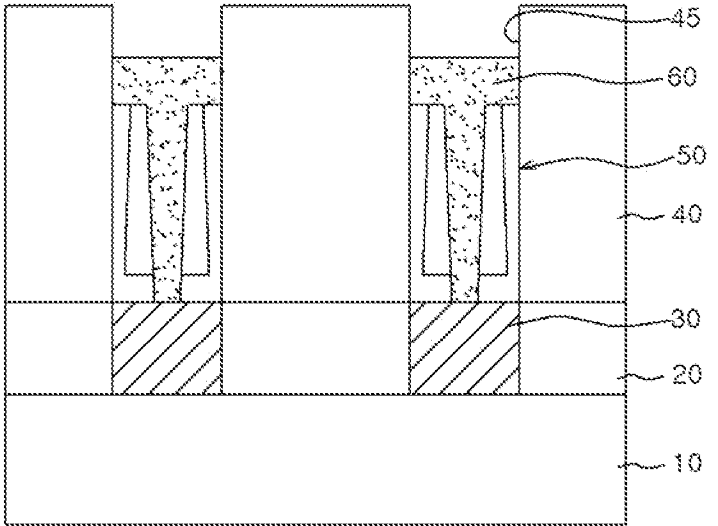
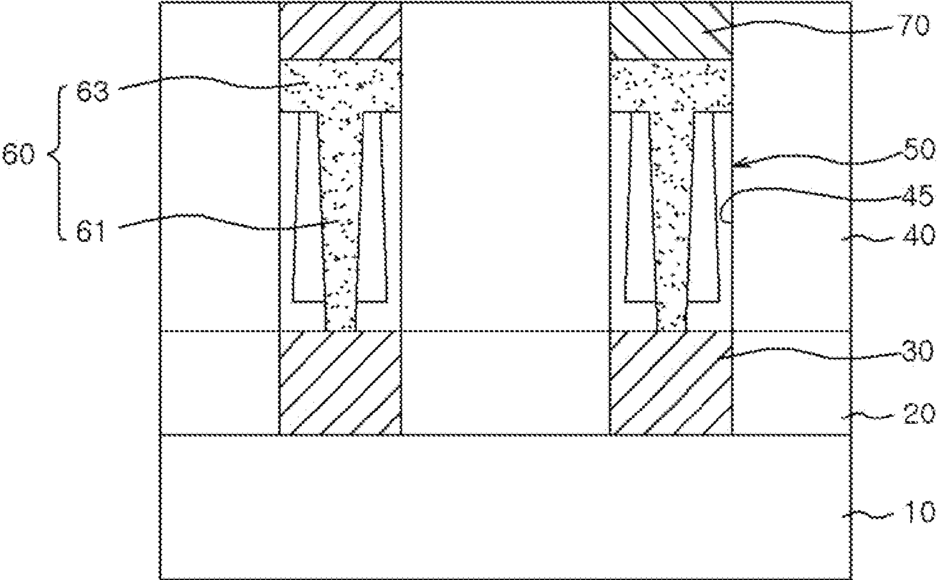


FIG.7



SEMICONDUCTOR APPARATUS WITH VARIABLE RESISTOR HAVING TAPERED DOUBLE-LAYERED SIDEWALL SPACERS

CROSS-REFERENCES TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. 119(a) to Korean application No. 10-2014-0120373, filed on Sep. 11, 2014, in the Korean intellectual property Office, which is incorporated by reference in its entirety as set forth in full.

BACKGROUND

[0002] 1. Technical Field

[0003] Various embodiments of the inventive concept relate to a semiconductor apparatus having resistance variable characteristics, and a method for fabricating the same.

[0004] 2. Related Art

[0005] With the rapid development of mobile and digital information communication and consumer-electronic industries, studies on existing electronic charge-controlled devices may encounter limitations. Thus, new functional memory devices other than the existing electronic charge-controlled devices need to be developed. In particular, next-generation memory devices with large capacity, ultra-high speed, and ultra-low power need to be developed to satisfy demands on large capacity of memories in main information apparatuses.

[0006] Currently, variable resistive memory devices using a resistance material as a memory medium have been suggested as the next-generation memory devices. Typically examples of the resistance variable memory device are phase-change random access memories (PCRAMs), resistive RAMs (ReRAMs), magneto-resistive RAMs (MRAMs), and spin-transfer torque magnetoresistive RAMs (STTMRAMs).

[0007] The variable resistive memory device may include a semiconductor substrate having a switching device a lower electrode, a variable resistor device, and an upper electrode. As the design rule is scaled down, the lower electrode, the variable resistor device, and the upper electrode may be formed in a hole having a fine size.

[0008] For example, the variable resistor device may be mainly formed through a method of forming an interlayer insulating layer the semiconductor substrate including the lower electrode, forming a hole in the interlayer insulating layer, and gap-filling the hole with a variable resistance material. In particular, technology for reducing a reset current through reduction in a contact area between the variable resistor device and the lower electrode had been suggested in the related art.

[0009] However, in the variable resistive memory device of the related art, the variable resistor device is formed in the hole, and thus the process of forming the variable resistor device is complicated.

SUMMARY

[0010] One or more exemplary embodiments are to provide a semiconductor apparatus and a method for fabricating the same, which easily form a variable resistor device.

[0011] According to an embodiment, there is provided a method for fabricating a semiconductor apparatus. The method may include forming a variable resistor region, and forming a spacer having a top linewidth and a bottom linewidth substantially equal to each other in the variable resistor region.

[0012] The forming of the spacer may include forming a first insulating layer in the variable resistor region through a first method, forming a second insulating layer along a surface of the first insulating layer in the variable resistor region through a second method for providing step coverage superior to the first method, and etching the first and second insulating layers.

[0013] According to an embodiment, there is provided semiconductor apparatus. The semiconductor apparatus may include a lower electrode, a variable resistor device including a first variable resistor device formed on the lower electrode and having a top linewidth and a bottom linewidth substantially equal to each other and a second variable resistor device formed on the first variable resistor device and having a linewidth larger than that of the first variable resistor device, and a spacer formed on an outer circumference of the first variable resistor device.

[0014] These and other features, aspects and embodiments are described below in the section entitled "DETAILED DESCRIPTION".

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The above and other aspects, features and advantages of the subject matter of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0016] FIG. **1** is a cross-sectional view illustrating a semiconductor apparatus according to an embodiment of the inventive concept;

[0017] FIG. **2** is a cross-sectional view illustrating a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept;

[0018] FIG. **3** is a cross-sectional view illustrating a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept;

[0019] FIG. **4** is a cross-sectional view illustrating a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept;

[0020] FIG. **5** is a cross-sectional view illustrating a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept;

[0021] FIG. **6** is a cross-sectional view illustrating a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept; and

[0022] FIG. **7** is a cross-sectional view illustrating a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept.

DETAILED DESCRIPTION

[0023] Exemplary embodiments will be described in greater detail with reference to the accompanying drawings. Exemplary embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of exemplary embodiments (and intermediate structures). As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but may

include deviations in shapes that result, for example, from manufacturing. In the drawings lengths and sizes of layers arid regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements. It is also understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other or substrate, or intervening layers may also be presents It is also noted that in this specification, "connected/coupled" refers to one component not only directly coupling another component but also indirectly coupling another component through an intermediate component. In addition, a singular form may include a plural form, and vice versa as long as it is not specifically mentioned.

[0024] The inventive concept is described herein with reference to cross-section and/or plan illustrations that are schematic illustrations of idealized embodiments of the inventive concept. However, embodiments of the inventive concept should not be limited construed as limited to the inventive concept Although a few embodiments of the inventive concept will be shown and described, it will be appreciated by those of ordinary skill in the art that changes may be made in these exemplary embodiments without departing from the principles and spirit of the inventive concept.

[0025] FIG. **1** is a cross-sectional view illustrating a semiconductor apparatus according to an embodiment.

[0026] Referring to FIG. **1**, a semiconductor apparatus according to an embodiment may include a semiconductor substrate **10**, a lower electrode **30**, a variable resistor device **60**, and an upper electrode **70** which are sequentially formed over the semiconductor substrate **10**.

[0027] A switching device (not shown) may be formed between the semiconductor substrate **10** and the lower electrode **30**. The switching device is a well-known device, and thus, a detailed description thereof will be omitted.

[0028] The lower electrode **30** may be formed in a hole **25** of a first interlayer insulating layer **20**, which is formed over the semiconductor substrate **10**. The lower electrode **30** may be electrically coupled to the switching device. The lower electrode **30** may include a doped polysilicon layer or a metal material having high resistivity. For example, the lower electrode **30** may include titanium nitride (TiN).

[0029] The variable resistor device **60** may be formed in the hole **45**, which is formed in a second interlayer insulating layer **40** to be electrically coupled to the lower electrode **30**. A variable resistance material for the variable resistor device **60** may include various materials such as a PCMO ($Pr_{1-x}Ca_xMnO_3$) layer for a ReRAM, a chalcogenide layer for a PCRAM a magnetIc layer for a MRAM, a magnetization reversal device layer for a STTMRAM, or a polymer layer for a polymer RAM (PoRAM). However, the material for the variable resistor device **60** is not limited thereto, and may include any material having a variable resistance characteristic in which the variable resistor device is switched between different resistance states according to a voltage or current applied thereto.

[0030] The variable resistor device **60** may include a first variable resistor device **61** and a second variable resistor device **63**. The first variable resistor device **61** is formed within the spacer **50**. The spacer **50** has a ring shape and is formed in the hole **45**. A second variable resistor device **63** is formed on the spacer **50** and the first variable resistor device **61** is formed in the hole **45**. In an embodiment, the first variable resistor device **61** and the second variable resistor device **63** may be coupled to each other. In an embodiment, the first variable resistor device **61** and the second variable resistor device **63** may be formed in a single body, but the first variable resistor device **61** and the second variable resistor device **63** may have different widths from each other. The first variable resistor device **61** is switched between different resistance states according to voltages or currents applied thereto, exhibiting variable resistance characteristics.

[0031] A spacer **50** may be formed in the hole **45** and formed in a ring shape as described above. In other words, the spacer **50** has a uniform width from a top to a bottom of the spacer **50**. To rephrase, a top width and a bottom width of the spacer **50** are substantially the same as each other, and thus the ring-shaped spacer **50** has a uniform inner diameter.

[0032] Since the spacer **50** has a substantially uniform inner diameter, the first variable resistor device **61**, which is formed inside the spacer **50**, also has a substantially uniform diameter. That is, the spacer **50** serves to reduce a bottom cross-sectional area of the variable resistor device **60**, which is in contact with the lower electrode **30**, thus reducing the reset current.

[0033] The upper electrode **70** may be formed on the variable resistor device **60** in a hole **45**. The upper electrode **70** may also include a doped polysilicon layer or a metal material having high resistivity like tile lower electrode **30**. For example, the upper electrode **70** may include titanium nitride (TiN).

[0034] FIGS. **2** to **7** are cross-sectional views illustrating a method for fabricating a semiconductor apparatus according to an embodiment.

[0035] Referring to FIG. **2**, a first interlayer insulating layer **20** is formed on a semiconductor substrate **10** and a predetermined portion of the first interlayer insulating layer **20** is etched to form a hole **25**. A conductive material is gap-filled in the hole **25** to form a lower electrode **30**. At this time, the lower electrode **30** may be electrically coupled to a switching device (not shown) formed in the semiconductor substrate **10**.

[0036] A second interlayer insulating layer **40** is formed on the semiconductor substrate in which the lower electrode **30** is formed, and then etched to form a hole **45** so that a surface of the lower electrode **30** is exposed. The hole **45** may correspond to a variable resistor region in which a variable resistor device (see **60** of FIG. **6**) is formed.

[0037] Referring to FIG. **3**, a first insulating layer **51** is thinly deposited on the semiconductor substrate in which the hole **45** is formed. The first insulating layer **51** may include a material including silicon nitride or nitride, but the material for the first insulating layer **51** is not limited thereto.

[0038] The first insulating layer **51** may be deposited through a first method. The first method may be a physical vapor deposition (PVD) method. The first insulating layer **51** disposed through the above-described PVD method may have a shape in which a width of the first insulating layer **51** tapers (i.e., gets thinner) going from a top toward a bottom of the first insulating layer **51**. However, the first insulating layer **51** is formed not to block a top of the hole **45**.

[0039] Referring to FIG. **4**, a second insulating layer **53** is deposited on the semiconductor substrate in which the first insulating layer **51** is formed. The second insulating layer **53** may include a material having substantially the same etch selectivity as the first insulating layer **51**. For example, the second insulating layer **53** may include a material including

a silicon nitride or nitride, but the material for the second insulating layer **53** is not limited thereto.

[0040] The second insulating layer **53** may be deposited through a second method for providing step coverage superior to the first insulating layer **51**. The second method may be a chemical vapor deposition (CVD) method or an atomic layer deposition (ALD) method.

[0041] The second insulating layer **53** deposited trough a CVD method or an ALD method has step coverage superior to the first insulating layer **51** deposited through the PVD method, and thus the second insulating layer **53** may be formed to a uniform width in the hole **45**. More specifically, the second insulating layer **53** may be deposited along a surface of the first insulating layer **51** in the hole **45** to a uniform width. As a result, a space or a seam may be formed within the second insulating layer **53**. The seam may increase in size going from a top toward a bottom of the hole **45**.

[0042] Referring to FIG. **5** the first insulating layer **51** and the second insulating layer **53** are anisotropically etched to form a sparer **50** on a sidewall of the hole **45**. Further, the first insulating layer **51** and the second insulating layer **53** may be etched so that the spacer **50** may have a height lower than that of the hole **45**. The spacer **50** may be formed in a ring shape. The spacer **50** may be formed to have a substantially uniform width from a top to a bottom of the spacer **50**, thus creating a ring structure with a uniform inner diameter.

[0043] The process of forming the spacer **50** in a ring shape having a substantially uniform inner diameter as described above will be described in detail.

[0044] Generally, when the spacer **50** is formed, since upper portions of the first and second insulating layers **51** and **53** are exposed to an etching gas more than lower portions of the first and second insulating layers **51** and **53** the upper portions of the first and second insulating layers **51** and **53** are etched relatively more, and the lower portions of the first and second insulating layers **51** and **53** are etched relatively less.

[0045] In an embodiment, the space or the seam formed inside the first and second insulating layers **51** and **53** may have a width that increases toward the bottom of the hole **45**. Therefore, even when the lower portions of the first and second insulating layers **51** and **53** are etched relatively less, compared to the upper portions of the first and second insulating layers **51** and **53** in the anisotropic etching process of the first and second insulating layers **51** and **53**, the spacer **50** in a ring shape with a substantially uniform inner diameter can be obtained.

[0046] Referring to FIG. **6** a variable resistance material is gap-filled in the hole **45** in which the spacer **50** is formed and then etched back to predetermined height, and thus a variable resistor device **60** is formed.

[0047] Referring to FIG. **7**, a conductive material is formed on the semiconductor substrate in which the variable resistor device **60** is formed, and then planarized to expose a surface of the second interlayer insulating layer **40**, and thus an upper electrode **70** is formed.

[0048] As described above, in the semiconductor apparatus according to an embodiment, the first insulating layer **51** is formed in the hole **45** through a PVD method, and the second insulating layer **53** is formed along a surface of the first insulating layer **51** through a CVD method or an ALD method. Then, the first and second insulating layers **51** and **53** may be etched to form the spacer **50**. Then, the variable resistor device **60** may be formed in the hole **45** in which the spacer **50** is formed.

[0049] In the semiconductor apparatus fabricated through the above-described method, even when the variable resistor device **60** is formed in a fine hole **45**, the fabrication process is simple. In particular, in the embodiment, the process of forming the spacer **50** in the hole **45** is simplified, and thus the semiconductor apparatus may be easily fabricated.

[0050] In the semiconductor apparatus according to an embodiment of the inventive concept, the variable resistor device **60** including the first variable resistor device **61** may be formed using the spacer **50** having substantially a uniform inner diameter. In other words, the first variable resistor device **61**, which is a region in which the resistance is switched may be formed to have a top linewidth and a bottom linewidth substantially equal to each other. When the first variable resistor device **61** is formed to have the top linewidth and the bottom line width substantially equal to each other as described above, the resistance for activating the first variable resistor device **61** is increased, and thus the resistance may be easily varied even in the low current. That is the reset current flowing through the variable resistor device may be reduced.

[0051] The above embodiment of the present invention is illustrative and not limitative. Various alternatives and equivalents are possible. The invention is not limited by the embodiments described herein. Nor is the invention limited to any specific type of semiconductor device. Other additions, subtractions, or modifications are obvious in view of the present disclosure and are intended to fall within the scope of the appended claims.

1-10. (canceled)

11. A semiconductor apparatus comprising:

a lower electrode;

a variable resistor device including a first variable resistor device and a second variable resistor device, wherein the first variable resistor device is formed over and coupled to the lower electrode and has a substantially uniform width from a top to a bottom of the first variable resistor device, wherein the second variable resistor device is formed over an upper surface of and coupled to the first variable resistor device and has a width larger than that of the first variable resistor device; and

a spacer formed over an outer circumference of the first variable resistor device.

12. The semiconductor apparatus of claim **11**, further comprising:

an upper electrode formed over and coupled to the second variable resistor device.

13. The semiconductor apparatus of claim **11**, further comprising:

a semiconductor substrate; and

an interlayer insulating layer having a hole formed over the semiconductor substrate,

wherein the spacer and the variable resistor device are formed in the hole.

14. The semiconductor apparatus of claim **13**, wherein the spacer includes:

a first insulating layer having a non-uniform width in the hole, and

a second insulating layer formed over a surface of the first insulating layer and having a substantially uniform width.

15. The semiconductor apparatus of claim **14**, wherein the first insulating layer has substantially the same etch selectivity as the second insulating layer.

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