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(54) INTEGRATED CIRCUIT DEVICE INCLUDING INTERCONNECTION STRUCTURE

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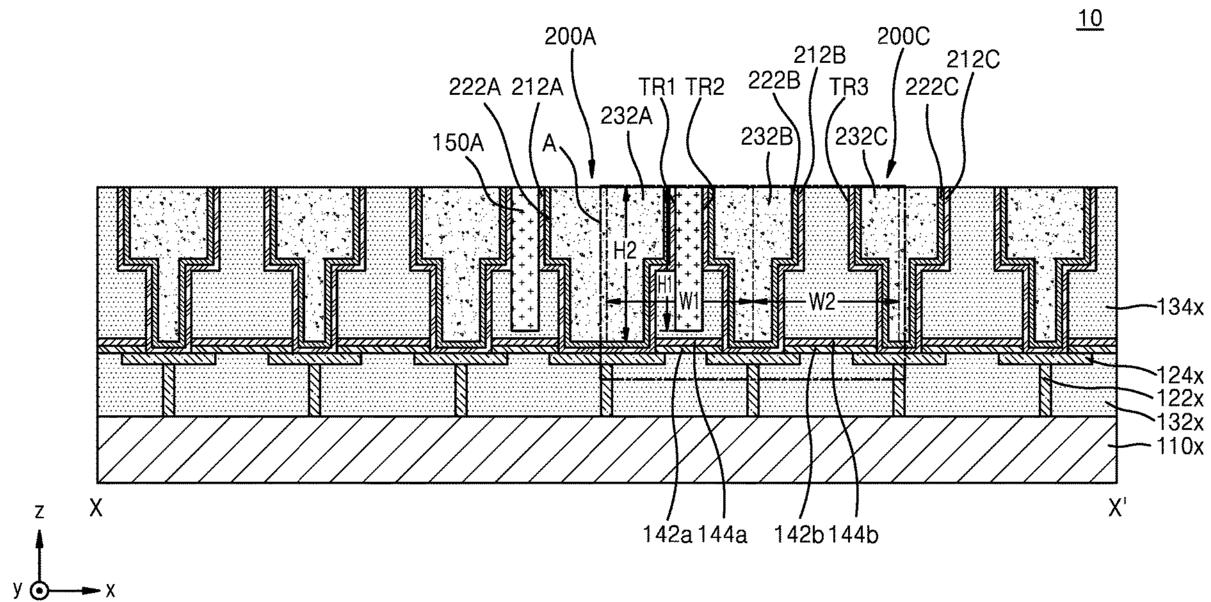
(57) **ABSTRACT**

An integrated circuit device includes an interconnection structure that includes: an interlayer insulating layer arranged on a substrate and having a plurality of trenches; a first conductive layer formed inside a first trench of the plurality of trenches; a second conductive layer formed inside a second trench of the plurality of trenches, wherein the second trench is spaced apart from the first trench; a third conductive layer formed inside a third trench of the plurality of trenches, wherein the third trench is spaced apart from the second trench; and a dielectric layer formed between the first conductive layer and the second conductive layer, wherein a portion of interlayer insulating layer is disposed between the second conductive layer and the third conductive layer, and wherein a first width of the first conductive layer is greater than a second width of the second conductive layer.



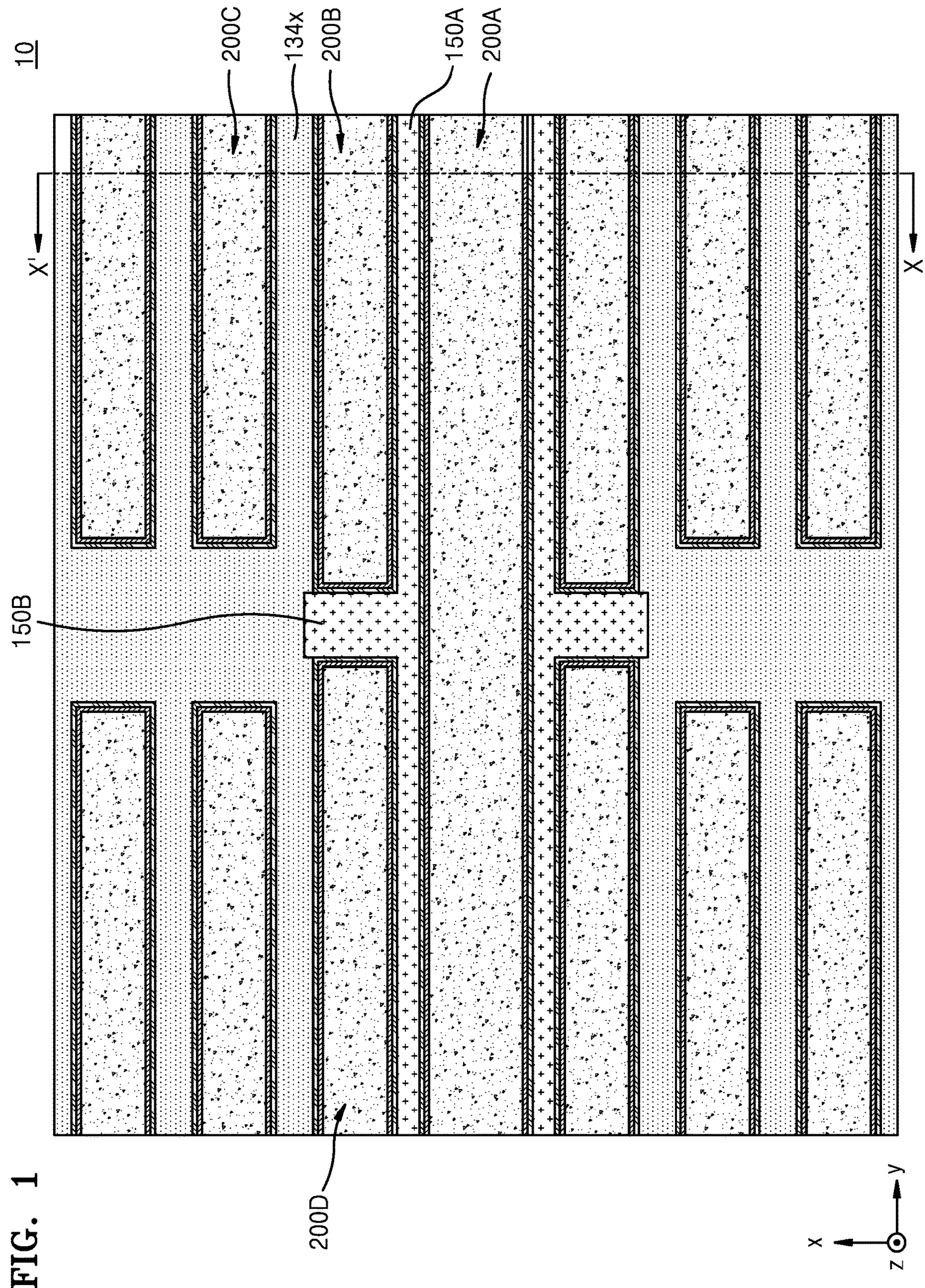


FIG. 1

FIG. 2

FIG. 3

FIG. 4

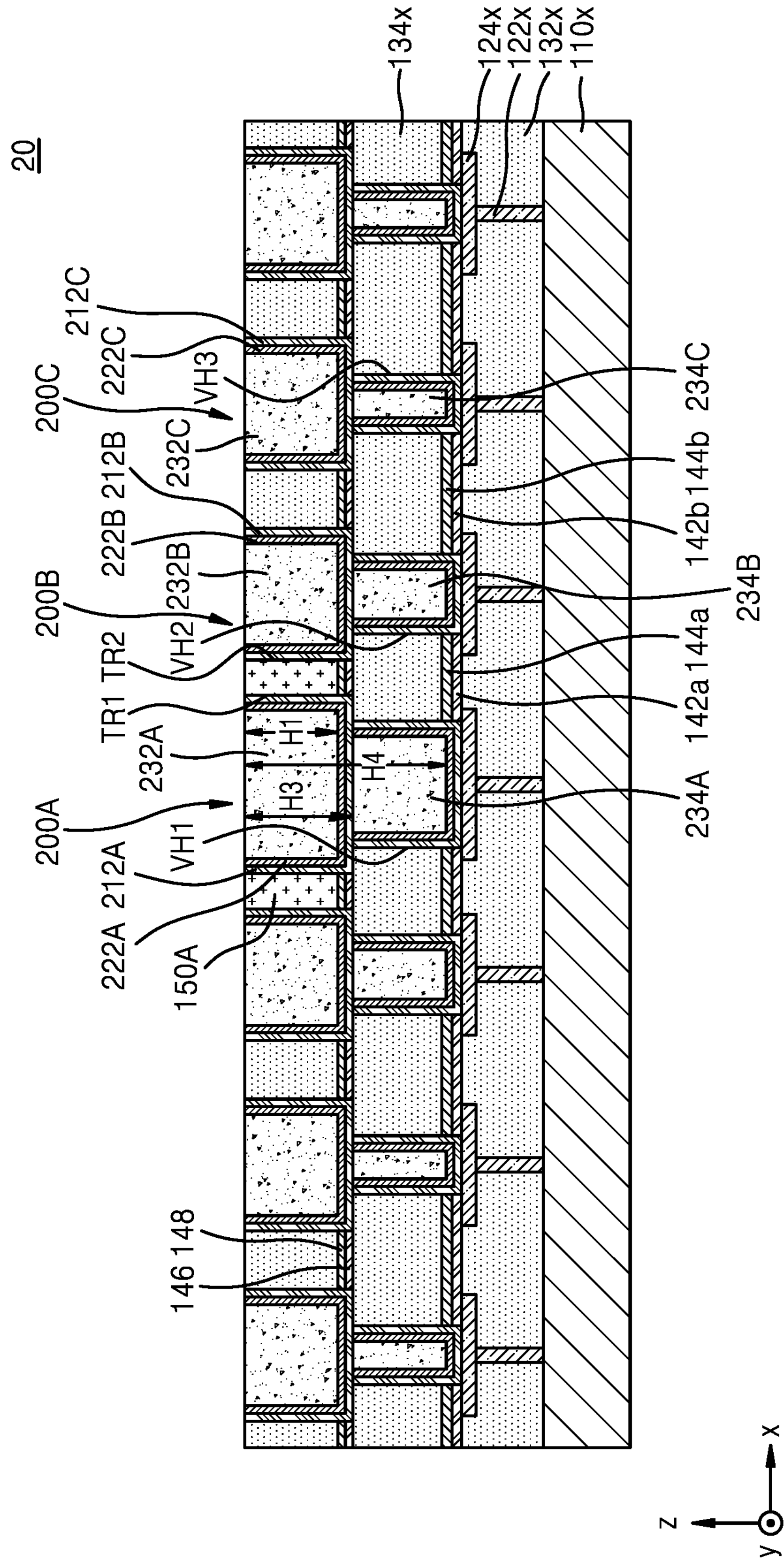


FIG. 5

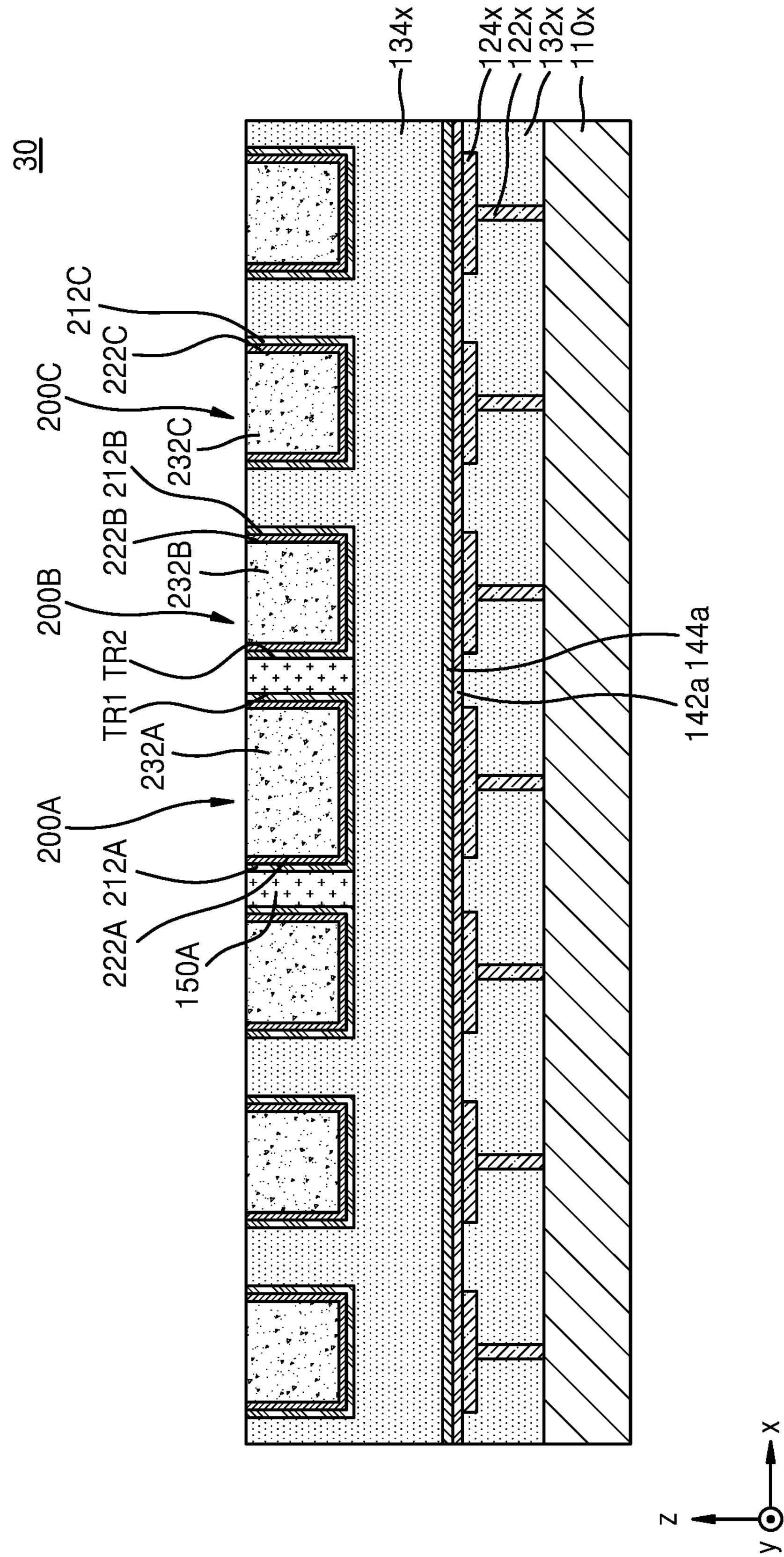


FIG. 6

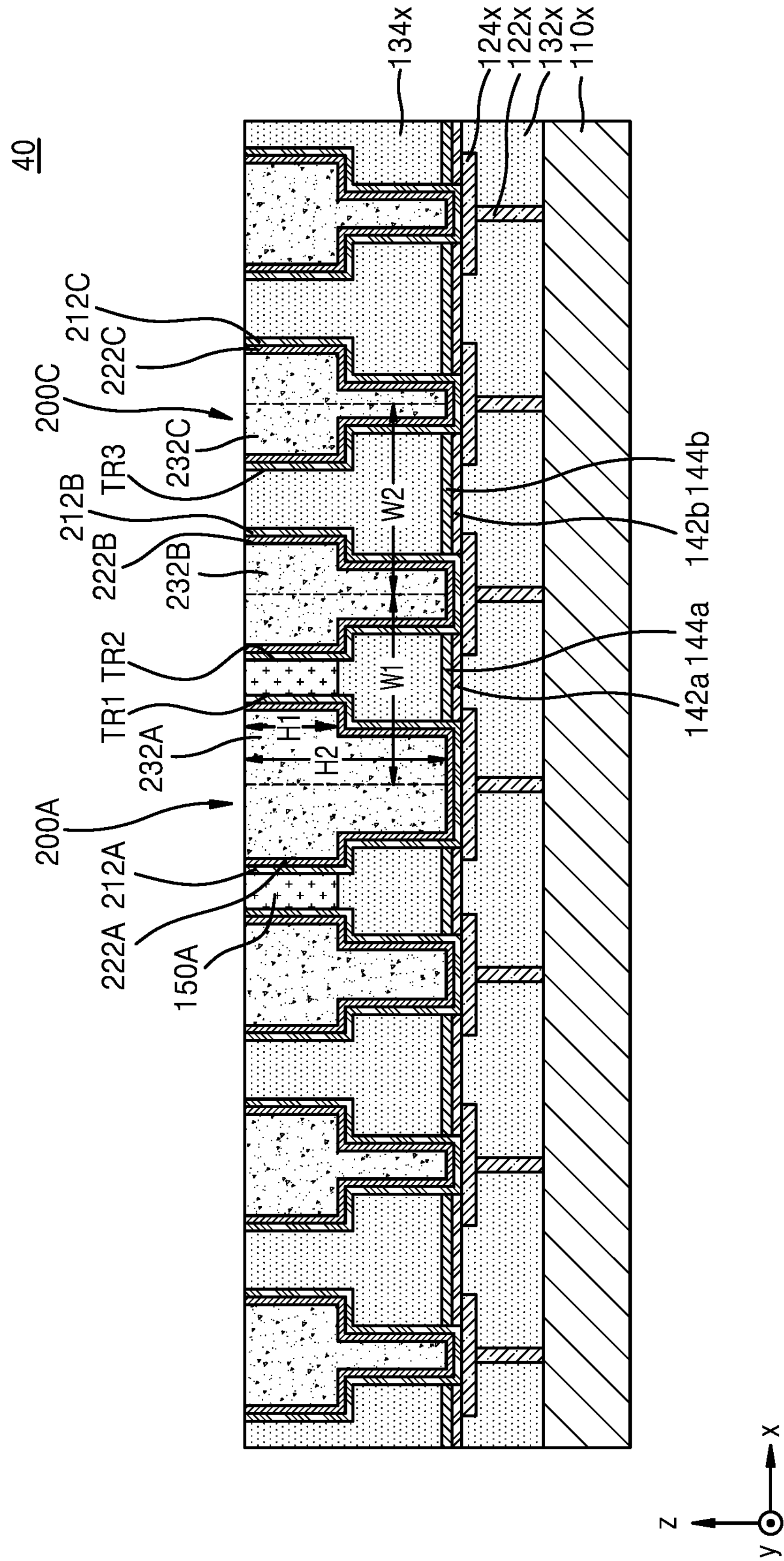
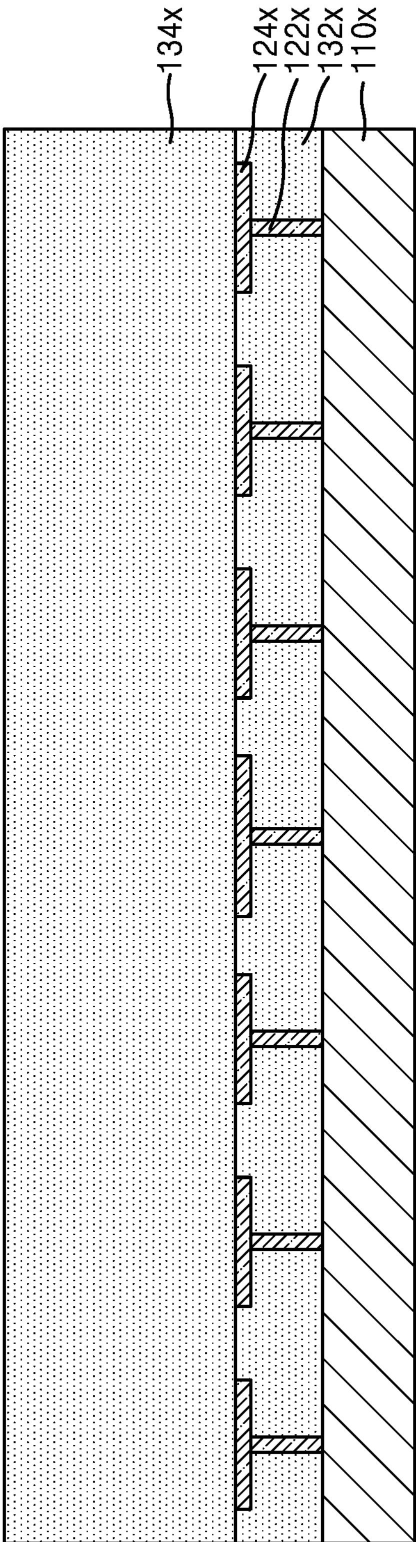


FIG. 7



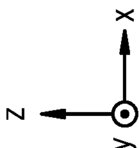


FIG. 8

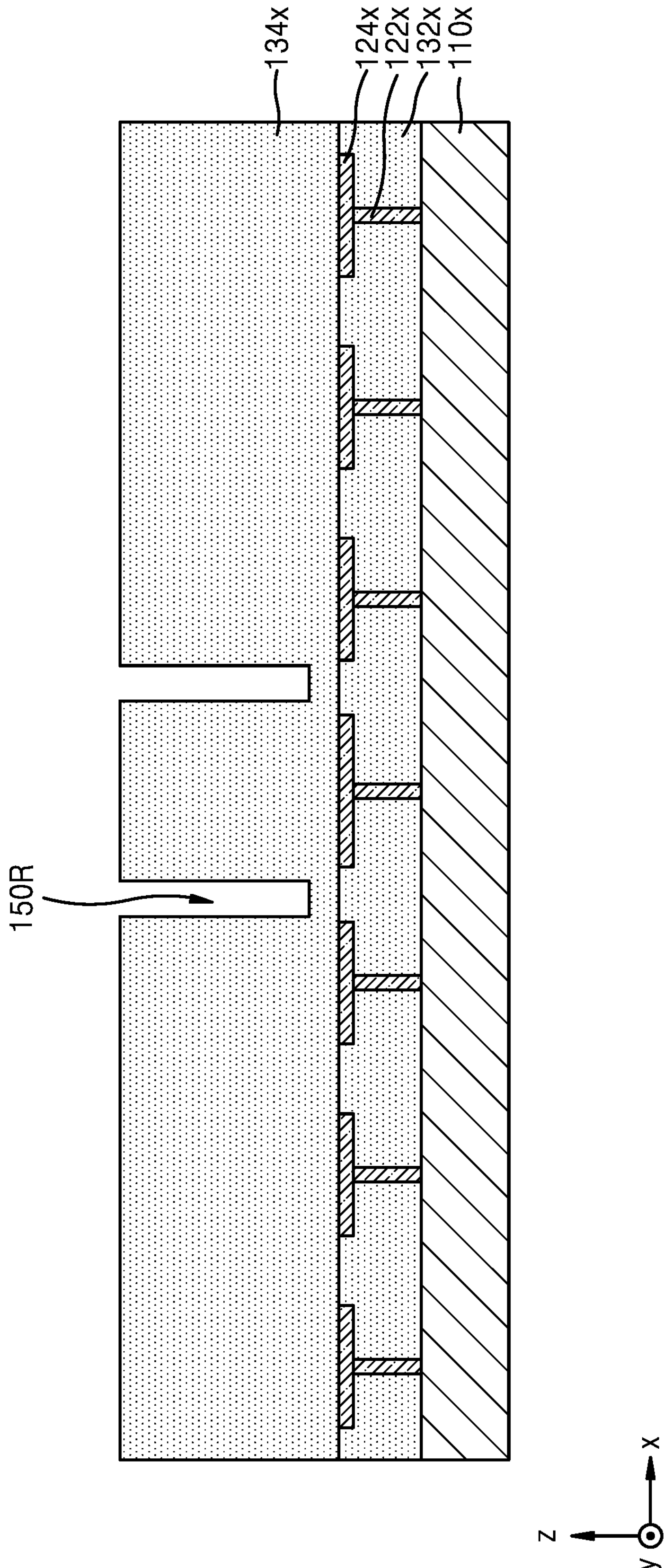


FIG. 9

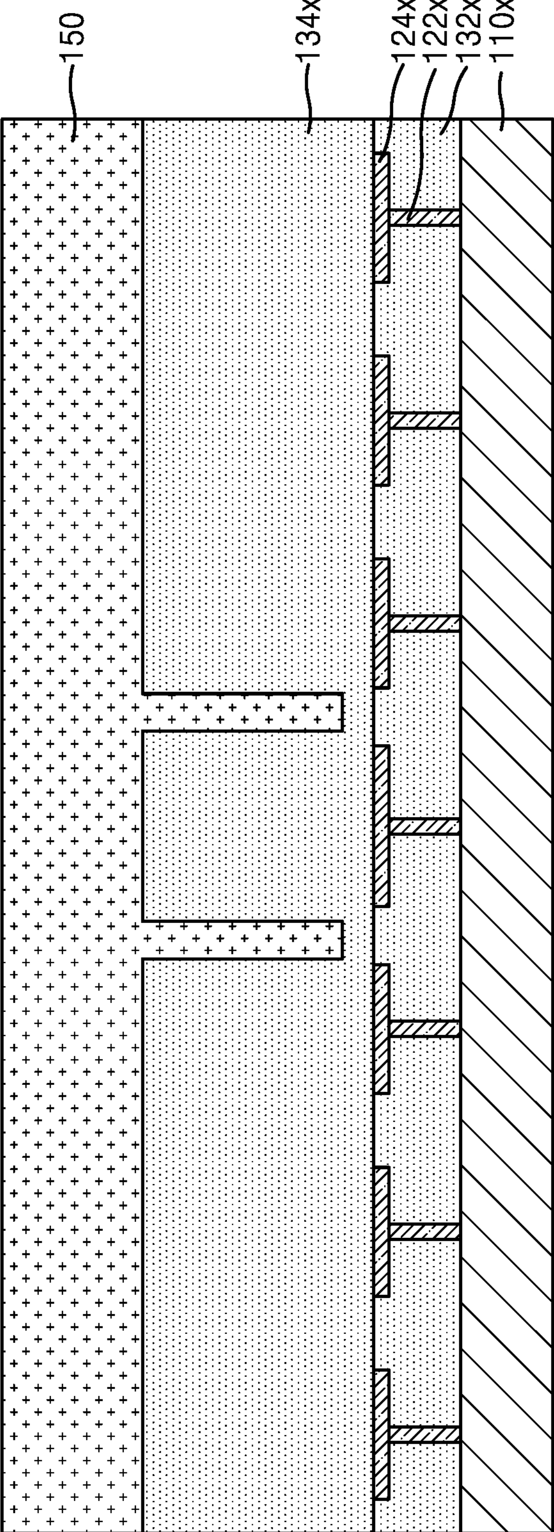


FIG. 10

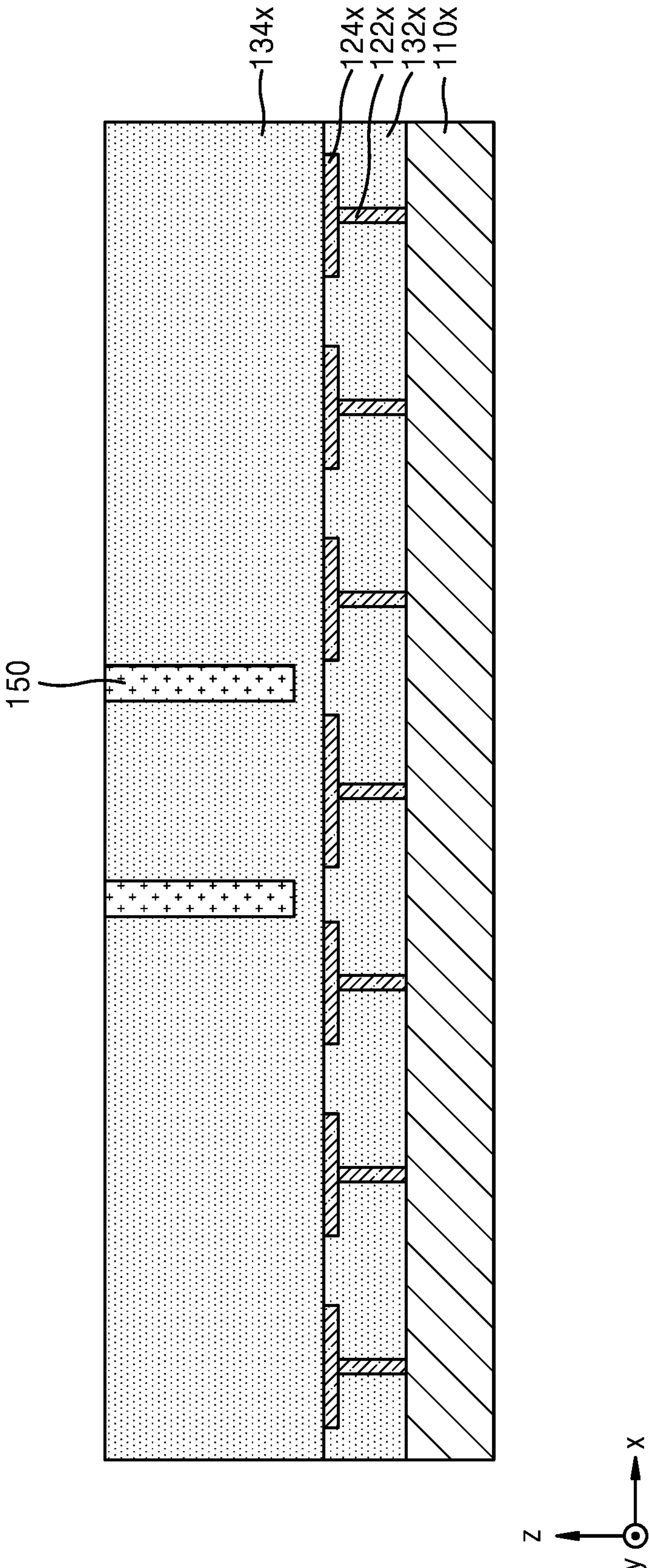


FIG. 11

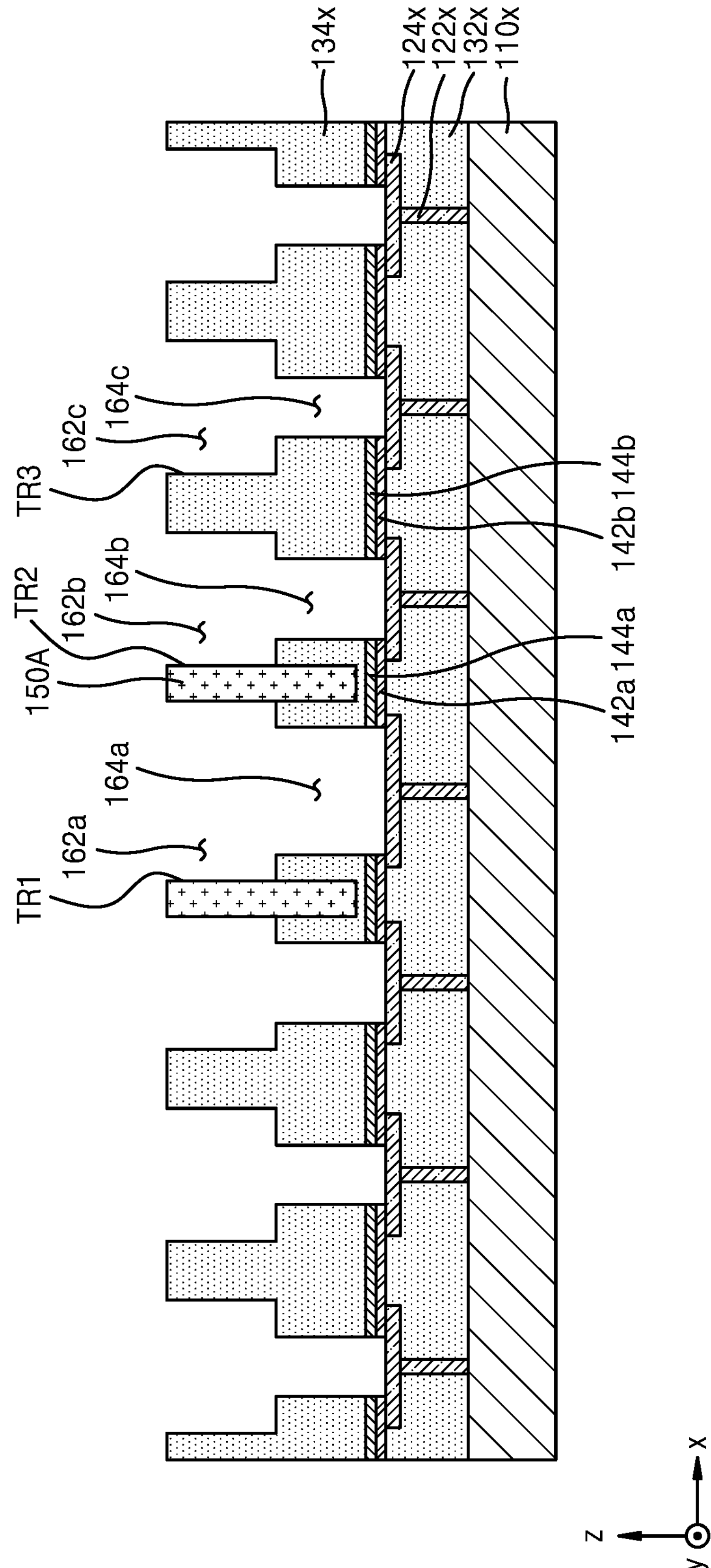


FIG. 12

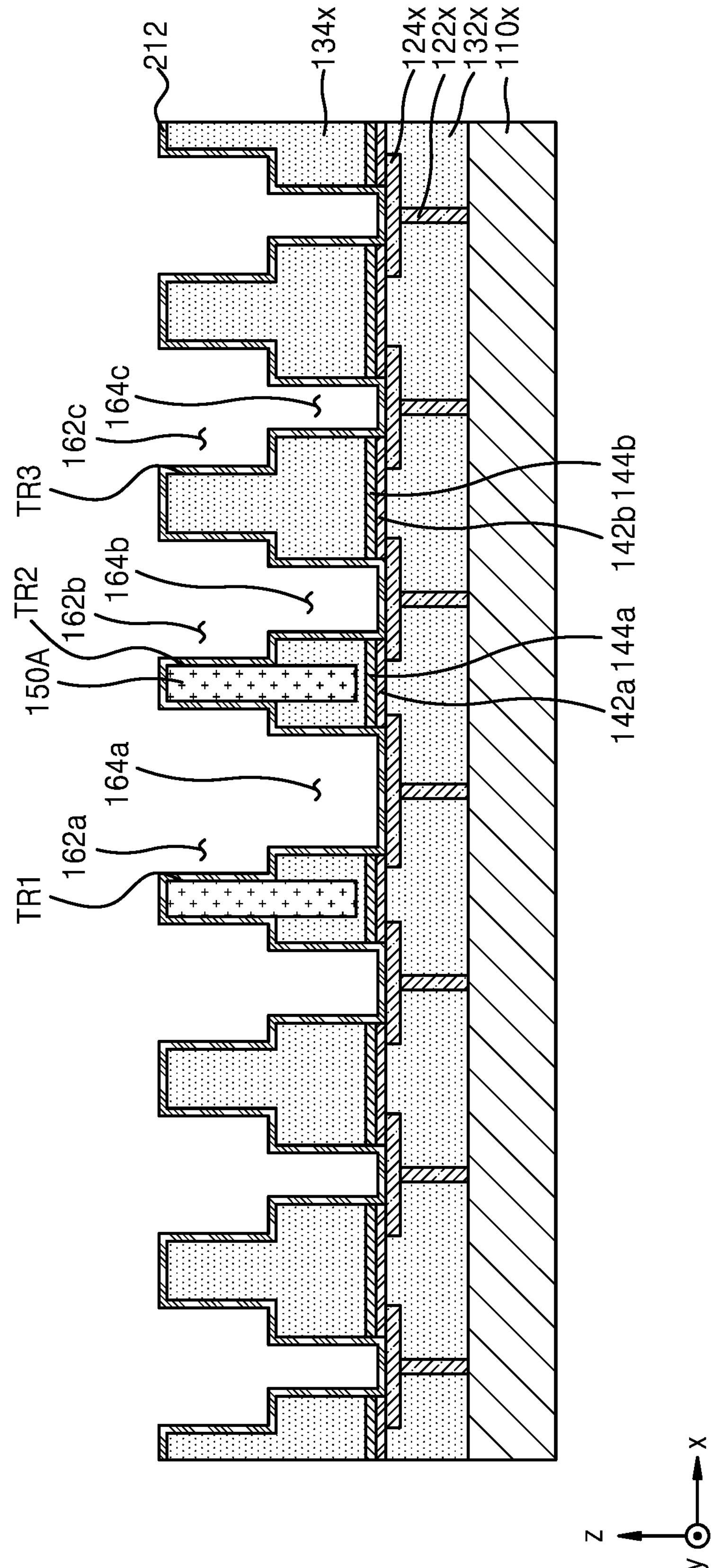


FIG. 13

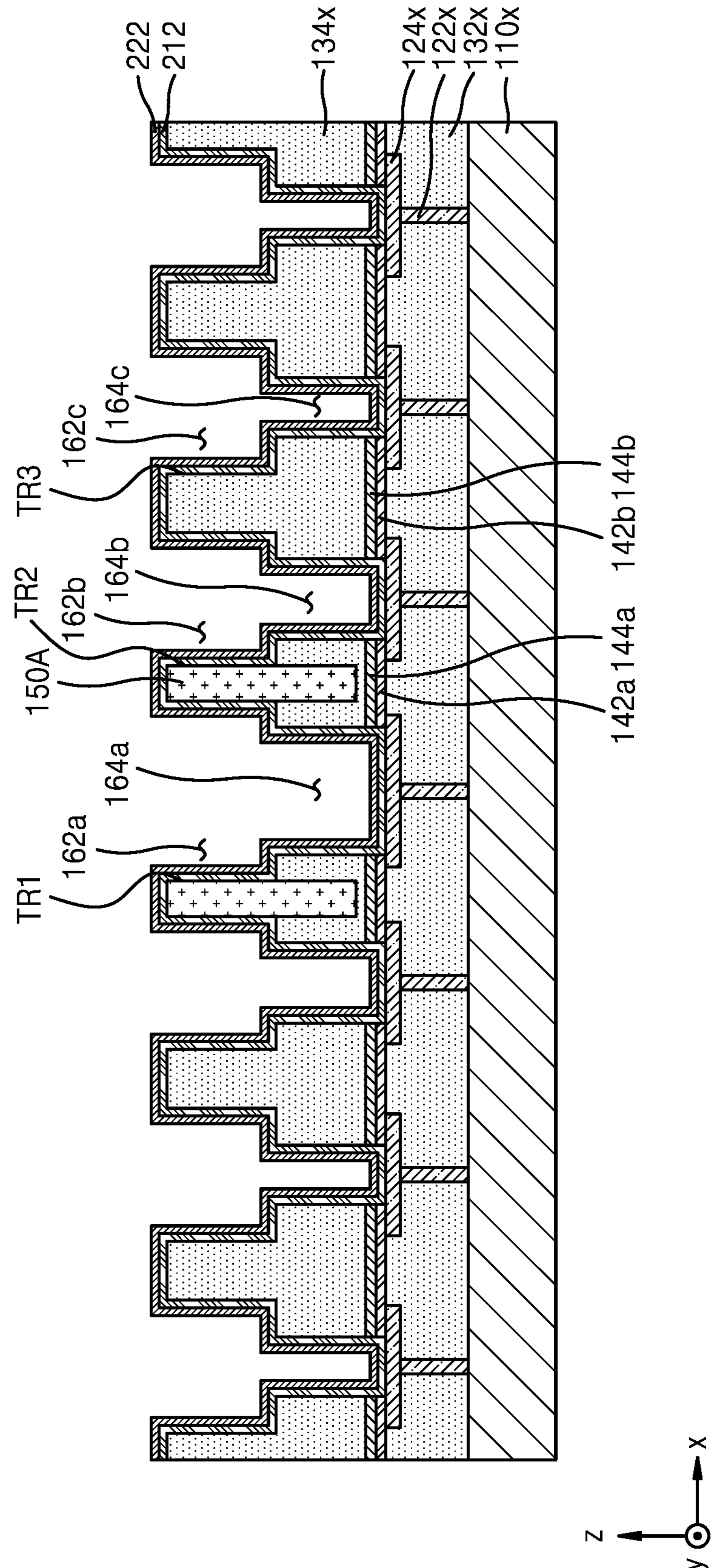
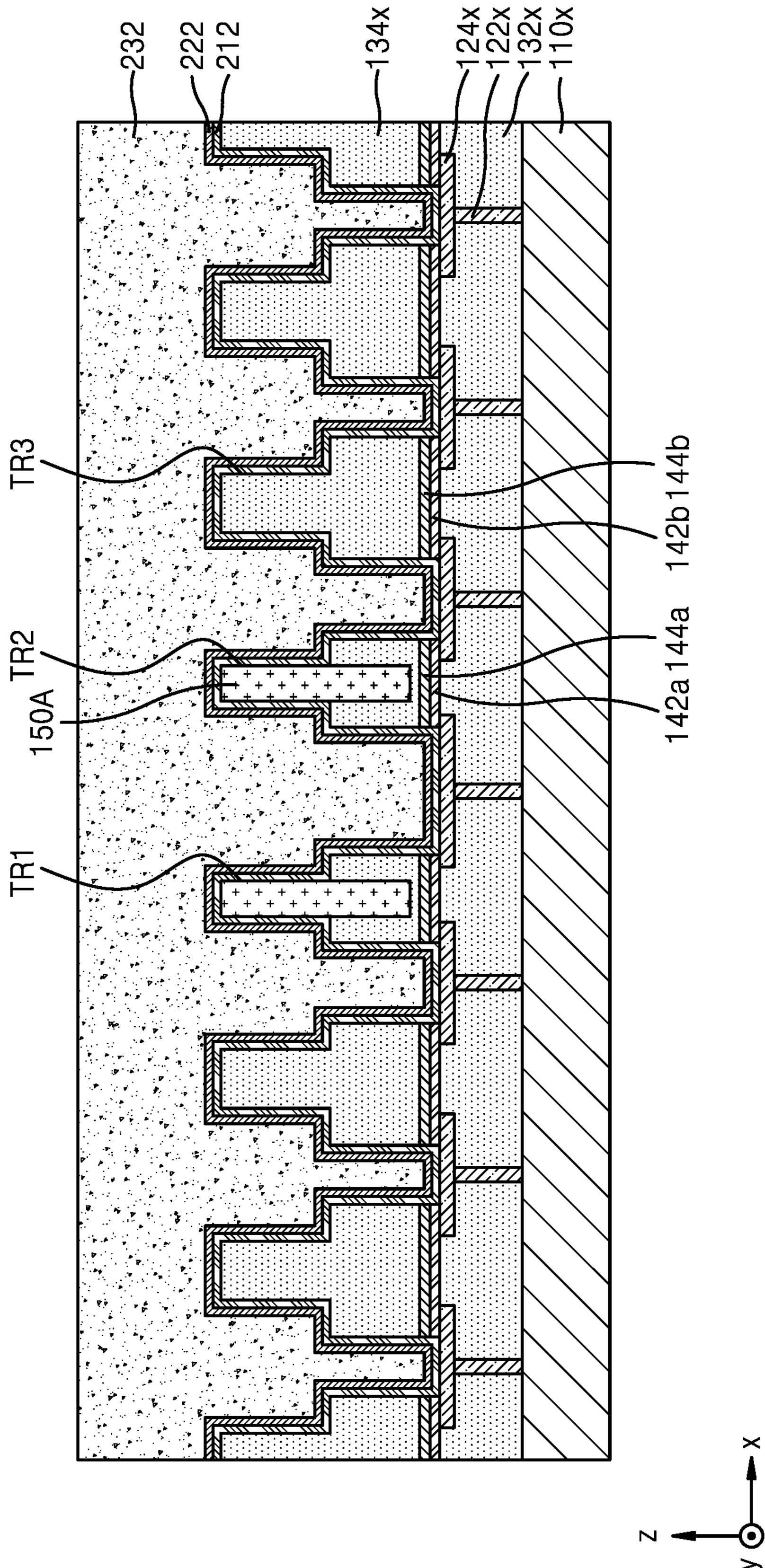


FIG. 14



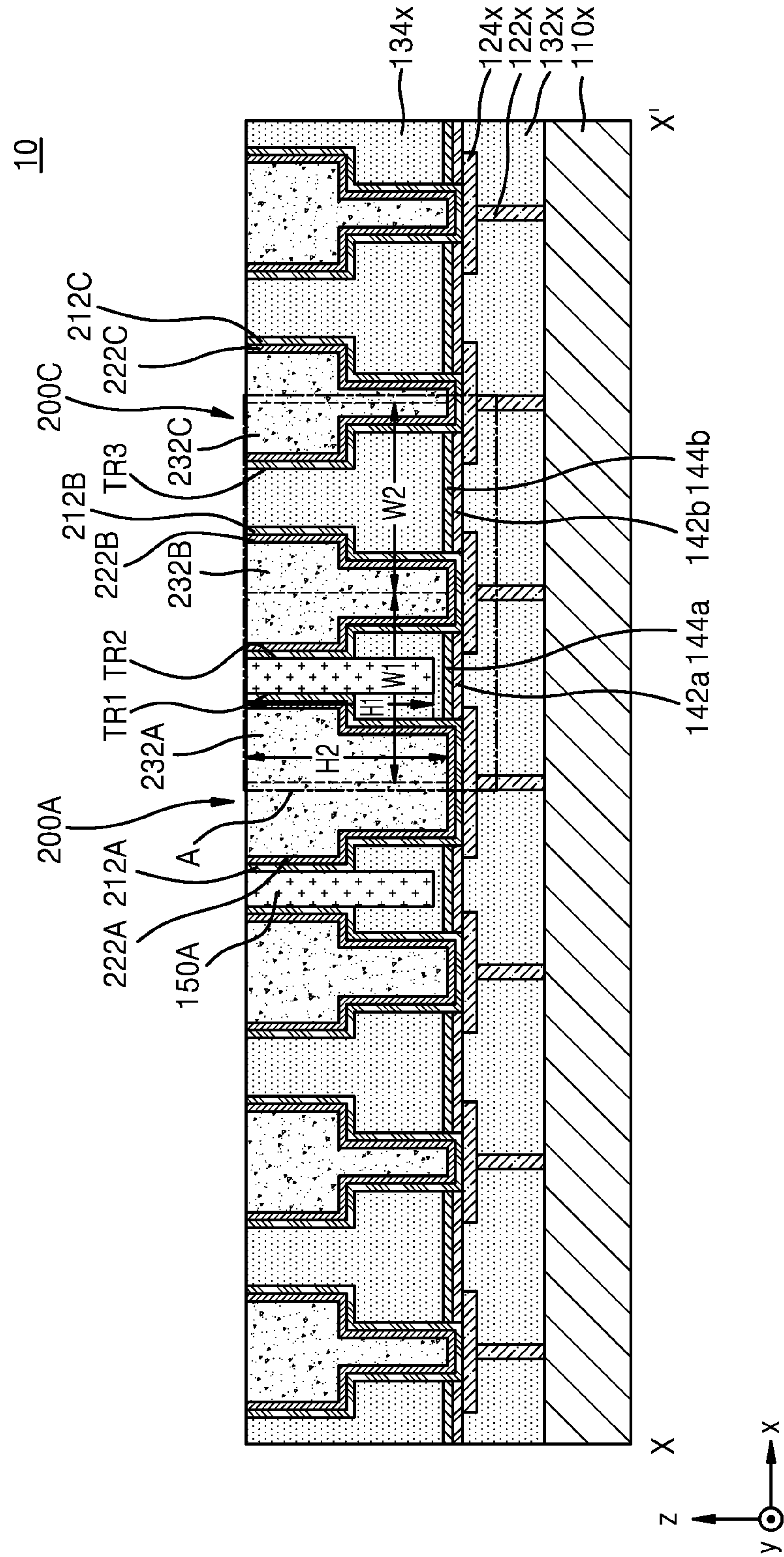


FIG. 15

INTEGRATED CIRCUIT DEVICE INCLUDING INTERCONNECTION STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2022-0105776, filed on Aug. 23, 2022, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The present inventive concept relates to an integrated circuit device, and more particularly, to an integrated circuit device including an interconnection structure.

DISCUSSION OF THE RELATED ART

[0003] An interconnection structure, of an integrated circuit device, for implementing the integrated circuit device has been under development to have a reduced size. However, it is difficult to reduce a distance between metal wirings due to the limitation of a photolithography process. With this limitation, the difficulty of a process for reducing the resistance of the metal wiring is increased.

SUMMARY

[0004] The present inventive concept provides an interconnection structure of an integrated circuit device in which a distance between metal wirings is reduced.

[0005] According to an embodiment of the present inventive concept, an integrated circuit device includes an interconnection structure, wherein the interconnection structure includes: an interlayer insulating layer arranged on a substrate and having a plurality of trenches formed in the interlayer insulating layer; a first conductive layer formed inside a first trench of the plurality of trenches; a second conductive layer formed inside a second trench of the plurality of trenches, wherein the second trench is spaced apart from the first trench of the plurality of trenches in a first direction; a third conductive layer formed inside a third trench of the plurality of trenches, wherein the third trench is spaced apart from the second trench of the plurality of trenches in the first direction; and a dielectric layer formed between the first conductive layer and the second conductive layer, wherein a portion of interlayer insulating layer is disposed between the second conductive layer and the third conductive layer, and wherein a first width of the first conductive layer in the first direction is greater than a second width of the second conductive layer in the first direction.

[0006] According to an embodiment of the present inventive concept, an integrated circuit device includes an interconnection structure, wherein the interconnection structure includes: a lower conductive layer formed on a substrate; an interlayer insulating layer formed on the lower conductive layer and having a first trench therein; a first via layer passing through portions of the interlayer insulating layer under the first trench; a first conductive layer electrically connected to the lower conductive layer through the first via layer; a second conductive layer formed on a second via layer, wherein the second via layer is spaced apart from the first via layer in a first direction; a third conductive layer formed on a third via layer, wherein the third via layer is spaced apart from the second via layer in the first direction; and a dielectric layer formed between the first conductive layer and the second conductive layer, wherein a portion of the interlayer insulating layer is formed between the second conductive layer and the third conductive layer, and wherein a first width of the first conductive layer in the first direction is greater than a second width of the second conductive layer in the first direction.

[0007] According to an embodiment of the present inventive concept, an integrated circuit device includes an interconnection structure, wherein the interconnection structure includes: an interlayer insulating layer arranged on a substrate and having a plurality of trenches formed in the interlayer insulating layer, wherein the interlayer insulating layer includes silicon oxide; a first conductive layer formed inside a first trench of the plurality of trenches; a second conductive layer formed inside a second trench of the plurality of trenches, wherein the second trench is spaced apart from the first trench of the plurality of trenches in a first direction; a third conductive layer formed inside a third trench of the plurality of trenches, wherein the third trench is spaced apart from the second trench of the plurality of trenches in the first direction; and a dielectric layer formed between the first conductive layer and the second conductive layer and including silicon nitride, silicon oxynitride (SiON), silicon carbon nitride (SiCN), aluminum oxide (Al_2O_2), aluminum nitride (AlN), titanium oxide (TiO_2), or a combination thereof, which have an etch selectivity with respect to the interlayer insulating layer, wherein the interlayer insulating layer includes silicon oxide, and a portion of the interlayer insulating layer is formed between the second conductive layer and the third conductive layer, wherein a first width of the first conductive layer in the first direction is greater than a second width of the second conductive layer in the first direction, and a first separation distance between the first conductive layer and the second conductive layer in the first direction is less than or equal to a second separation distance between the second conductive layer and the third conductive layer in the first direction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The above and other aspects of the present inventive concept will become more apparent by describing in detail embodiments thereof, with reference to the accompanying drawings, in which:

[0009] FIG. **1** is a cross-sectional view illustrating an interconnection structure of an integrated circuit device according to an embodiment of the present inventive concept;

[0010] FIG. **2** is a cross-sectional view of the interconnection structure of the integrated circuit device taken along a line X-X' of FIG. **1**;

[0011] FIG. **3** is an enlarged view of portion "A" of FIG. **2**;

[0012] FIG. **4** is a cross-sectional view illustrating an interconnection structure of an integrated circuit device according to an embodiment of the present inventive concept;

[0013] FIG. **5** is a cross-sectional view illustrating an interconnection structure of an integrated circuit device according to an embodiment of the present inventive concept;

[0014] FIG. **6** is a cross-sectional view illustrating an interconnection structure of an integrated circuit device according to an embodiment of the present inventive concept; and

[0015] FIGS. **7**, **8**, **9**, **10**, **11**, **12**, **13**, **14** and **15** are cross-sectional views illustrating a process of manufacturing the interconnection structure of the integrated circuit device shown in FIG. **1** according to an embodiment of the present inventive concept.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0016] Hereinafter, embodiments of the present inventive concept will be described in detail with reference to the accompanying drawings. However, the present inventive concept is not intended to be limited to the embodiments set forth herein and may be embodied in different forms.

[0017] FIG. **1** is a cross-sectional view illustrating an interconnection structure **10** of an integrated circuit device according to an embodiment of the present inventive concept.

[0018] Referring to FIG. **1**, the interconnection structure **10** of the integrated circuit device may include a plurality of electrode structures **200**A, **200**B, **200**C, and **200**D, and dielectric layers **150**A and **150**B and a second interlayer insulating layer **134***x*, which are formed between the plurality of electrode structures **200**A, **200**B, **200**C, and **200**D. The plurality of electrode structures **200**A, **200**B, and **200**C may be spaced apart from each other in a first direction (e.g., an x-direction) on a substrate. The width, in the first direction, of the first electrode structure **200**A may be largest among the plurality of electrode structures **200**A, **200**B, and **200**C. The widths of the second electrode structure **200**B and the third electrode structure **200**C may be substantially the same as each other. FIG. **1** illustrates that seven electrode structures are arranged. However, the number of electrode structures is not limited to the above-described number.

[0019] The second electrode structure **200**B and the fourth electrode structure **200**D may be spaced apart from each other in a second direction (e.g., a y-direction) substantially perpendicular to the first direction on the substrate.

[0020] According to an embodiment of the present inventive concept, a first direction (e.g., the x-direction) distance between the first electrode structure **200**A and the second electrode structure **200**B may less than a first direction (e.g., the x-axis direction) distance between other electrode structures of plurality of electrode structures **200**B, **200**C, and **200**D. The dielectric layer **150**A may be formed between the first electrode structure **200**A and the second electrode structure **200**B, and the dielectric layer **150**A may include a material having an etch selectivity with respect to the second interlayer insulating layer **134***x*. Thus, through an etching process using the etch selectivity of the dielectric layer **150**A, the first direction (e.g., the x-axis direction) distance between the first electrode structure **200**A and the second electrode structure **200**B may be relatively small. A detailed description of a process using the etch selectivity of the dielectric layer **150**A is provided later.

[0021] According to an embodiment of the present inventive concept, a second direction (e.g., a y-axis direction) distance between the second electrode structure **200**B and the fourth electrode structure **200**D may less than a second direction (e.g., the y-axis direction) distance between other electrode structures of plurality of electrode structures. The dielectric layer **150**B may be formed between the second electrode structure **200**B and the fourth electrode structure **2001**), and the dielectric layer **150**B may include a material having an etch selectivity with respect to the second interlayer insulating layer **134***x*. Thus, through an etching process using the etch selectivity of the dielectric layer **150**B, the second direction (e.g., the y-axis direction) distance between the second electrode structure **200**B and the fourth electrode structure **200**D may be relatively small. A detailed description of a process using the etch selectivity of the dielectric layer **150**B is provided later.

[0022] FIG. **1** illustrates that a space between the second electrode structure **200**B and the fourth electrode structure **200**D is greater than each of a space between the first electrode structure **200**A and the second electrode structure **200**B and/or a space between the second electrode structure **200**B and the third electrode structure **200**C. However, the present inventive concept is not necessarily limited thereto.

[0023] FIG. **2** is a cross-sectional view of the interconnection structure of the integrated circuit device taken along a line X-X of FIG. **1**. FIG. **3** is an enlarged view of portion "A" of FIG. **2**.

[0024] The interconnection structure **10** of the integrated circuit device shown in FIG. **2** may be a dual damascene structure formed by a dual damascene process. For example, a via hole etching process for forming via holes and a trench etching process for forming trenches TR**1** TR**2**, and TR**3** may be simultaneously performed on the dual damascene structure.

[0025] Referring to FIG. **2**, the interconnection structure **10** of the integrated circuit device may include a multi-layered wiring layer for connecting a lower conductive layer **124***x* to conductive layers **232**A, **232**B, and **232**C. The interconnection structure **10** of the integrated circuit device may include a substrate **110***x*. For example, the substrate **110***x* may be formed from a single crystal wafer. The substrate **110***x* may be, for example, a silicon wafer. Various electronic elements, such as transistors and/or capacitors, may be formed in the substrate **110***x*.

[0026] A first interlayer insulating layer **132***x* may be formed on the substrate **110***x*. The first interlayer insulating layer **132***x* may include, for example, silicon oxide. A conductive plug **122***x* and the lower conductive layer **124***x* may be arranged inside the first interlayer insulating layer **132***x*.

[0027] The lower conductive layer **124***x* may be a conductive material layer formed of at least one of, for example, copper (Cu), tungsten (W), aluminum (Al), or a combination thereof. The conductive plug **122***x* may be electrically connected to electrical elements formed in the substrate **110***x*.

[0028] A second interlayer insulating layer **134***x* and etch-stop layers **142***a* and **144***b* may be formed on the lower conductive layer **124***x*. The second interlayer insulating layer **134***x* may include, for example, silicon oxide. The etch-stop layers **142***a* and **142***b* may include materials having an etch selectivity with respect to the second interlayer insulating layer **134***x*. Thus, the etch-stop layers **142***a* and **142***b* may include materials having an etch selectivity with respect to silicon oxide. The etch-stop layers **142***a* and **144***b* are shown as double layers for convenience; however, the etch-stop layers **142***a* and **144***b* may include a single layer or a plurality of layers having a triple layer or more.

[0029] A first trench TR**1** may be formed inside the etch-stop layers **142***a* and **144***a* and the second interlayer insulating layer **134***x*. The bottom of the first trench TR**1** may be formed at a position lower than that of the bottom surface of the second etch-stop layer **142***a*. For example, a top surface of the lower conductive layer **124***x* may be exposed at the bottom portion of the first trench TR**1**.

[0030] Other trenches TR**2** and T**3** plurality of trenches TR**1**, TR**2** and TR**3** may be spaced apart from each other in a first direction based on the first trench TR**1**. The other trenches TR**2** and TR**3** may be formed inside the etch-stop layers **142***b* and **144***b* and the second interlayer insulating layer **134***x*.

[0031] A first barrier **212**A, a first seed layer **222**A, and a first conductive layer **232**A may be included in the first trench TR**1**. The first barrier **212**A may be formed with a substantially uniform thickness along the surface of the first trench TR**1**. A second barrier **212**B, a second seed layer **222**B, and a second conductive layer **232**B may be included in the second trench TR**2**. The second barrier **212**B may be formed with a substantially uniform thickness along the surface of the second trench TR**2**. A third barrier **212**C, a third seed layer **222**C, and a third conductive layer **232**C may be included in the third trench TR**3**. The third barrier **212**C may be formed with a substantially uniform thickness along the surface of the third trench TR**3**. Each of the first barrier **212**A, the second barrier **212**B, and the third barrier **212**C may include, for example, ruthenium (Ru), cobalt (Co), tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W), tungsten nitride (WN), ruthenium (Ru), or a combination thereof (e.g., an alloy or a stacked structure). Each of the plurality of barrier layers **212**A, **212**B, and **212**C, may respectively surround the conductive layers **232**A, **232**B, and **232**C, and the dielectric layer **150**A may be in contact with a first barrier **212**A and a second barrier **212**B.

[0032] The first seed layer **222**A may be formed with a substantially uniform thickness along the surface of the first barrier **212**A inside the first trench TR**1**. The second seed layer **222**B may be formed with a substantially uniform thickness along the surface of the second barrier **212**B inside the second trench TIC. The third seed layer **222**C may be formed with a substantially uniform thickness along the surface of the third barrier **212**C inside the third trench TR**3**. Each of the first seed layer **222**A, the second seed layer **222**B, and the third seed layer **222**C may include, for example, copper (Cu), platinum (Pt), palladium (Pd), nickel (Ni), silver (Ag), ruthenium (Ru), and the like.

[0033] The first conductive layer **232**A may be formed on the first seed layer **222**A and inside the first trench TR**1**. The first seed layer **222**A may at least partially surround the first conductive layer **232**A. For example, the bottom surface and both sidewalls of the first conductive layer **232**A may be surrounded by the first seed layer **222**A. Thus, the first conductive layer **232**A may be spaced apart from the dielectric layer **150**A so as not to contact the dielectric layer **150**A. The first barrier **212**A may prevent a material for forming the first conductive layer **232**A from being diffused into the first interlayer insulating layer **132***x* and the lower conductive layer **124***x*. The first barrier **212**A may have conductivity and may be configured to reduce an ohmic resistance of the first conductive layer **232**A and the lower conductive layer **124***x*. The first conductive layer **232**. A may include, for example, Cu, Pt, Pd, Ni, Au, Ag, Ru, and the like.

[0034] The dielectric layer **150**A may be formed between the first conductive layer **232**A, which is included in the first electrode structure **200**A, and the second conductive layer **232**B, which is included in the second electrode structure **200**B. The dielectric layer **150**A may include a material having an etch selectivity with respect to the interlayer insulating layers **132***x* and **134***x*. The dielectric layer **150**A may include, for example, silicon nitride (SiN), silicon oxynitride (SiON), silicon carbon nitride (SiCN), aluminum oxide (Al_2O_2), aluminum nitride (AlN), titanium oxide (TiO_2), or a combination thereof. Because the dielectric layer **150**A includes a material having an etch selectivity with respect to the interlayer insulating layers **132***x* and **134***x*, the dielectric layer **150**A may be etched at a relatively low speed or may be hardly etched in a process of etching the interlayer insulating layers **132***x* and **134***x*. In addition, the interlayer insulating layers **132***x* and **134***x* may be etched at a relatively low speed or may be hardly etched in a process of etching the dielectric layer **150**A.

[0035] A second conductive layer **232**B and a third conductive layer **232**C may be spaced apart from each other in a first direction based on the first trench TR**1** and may be formed inside the second trench TR**2** and the third trench TR**3**, respectively. The second conductive layer **232**B may be formed on the second seed layer **222**B and inside the second trench TR**2**, and the third conductive layer **232**C may be formed on the third seed layer **222**C and inside the third trench TR**31** The second seed layer **222**B may at least partially surround the second conductive layer **232**B, and the third seed layer **222**C may at least partially surround the third conductive layer **232**C. For example, the bottom surface and both sidewalls of the second conductive layer **232**B may be surrounded by the second seed layer **222**B. Thus, the second conductive layer **232**B may be spaced apart from the dielectric layer **150**A and the second interlayer insulating layer **134***x* so as not to contact the dielectric layer **150**A and the second interlayer insulating layer **134***x*. As an additional example, the bottom surface and both sidewalls of the third conductive layer **232**C may be surrounded by the third seed layer **222**C. Thus, the third conductive layer **232**C may be spaced apart from the second interlayer insulating layer **134***x* so as not to contact the second interlayer insulating layer **134***x*. The second barrier **212**B and the third barrier **212**C may prevent materials for forming the second conductive layer **232**B and the third conductive layer **232**C from being diffused into the first and second interlayer insulating layers **132***x* and **134***x* and the lower conductive layer **124***x* that is arranged under the second barrier **212**B and the third barrier **212**C. The second barrier **212**B and the third barrier **212**C may have conductivity and may reduce an ohmic resistance between the second conductive layer **232**B and the lower conductive layer **124***x* and an ohmic resistance between the third conductive layer **232**C and the lower conductive layer **124***x*.

[0036] According to an embodiment of the present inventive concept, a first width of the first conductive layer **232**A included in the first trench TR**1** in the first direction (e.g., the x-direction) may be greater than a second width of the second conductive layer **232**B included in the second trench TR**2**. In addition, the second width of the second conductive layer **232**B included in the second trench TR**2** in the first direction (e.g., the x-direction) may be greater than a third width of the third conductive layer **232**C included in the third trench TR**3**.

[0037] According to an embodiment of the present inventive concept, a first distance W**1** between the center of the first conductive layer **232**A, included in the first trench TR**1**, in the first direction (e.g., the x-direction) and the center of the second conductive layer **232**B, included in the second trench TR**2**, may be greater than or equal to a second distance W**2** between the second conductive layer **232**B, included in the second trench TR**2**, in the first direction (e.g., the x-direction) and the center of the third conductive layer **232**C, included in the third trench TR**3**, in the first direction (e.g., the x-direction).

[0038] According to an embodiment of the present inventive concept, based on top surfaces of the first conductive layer **232**A and the dielectric layer **150**A, a vertical length of the dielectric layer **150**A may be less than or equal to a vertical length of the first conductive layer **232**A. In this case, the vertical length of the dielectric layer **150**A may be less than or equal to each of a vertical length of the second conductive layer **232**B and a vertical length of the third conductive layer **232**C as well as the vertical length of the first conductive layer **232**A.

[0039] According to an embodiment of the present inventive concept, a first separation distance between the first conductive layer **232**A and the second conductive layer **2323** in the first direction (e.g., the x-direction) may be less than or equal to a second separation distance between the second conductive layer **232**B and the third conductive layer **232**C in the first direction (e.g., the x-direction). For example, the first separation distance may be a distance between the first electrode structure **200**A and the second electrode structure **200**B, and the second separation distance may be a distance between the second electrode structure **200**B and the third electrode structure **200**C. For example, the first separation distance may be a width of the dielectric layer **150**A located between the first electrode structure **200**A and the second electrode structure **200**B, and the second separation distance may be a width of the second interlayer insulating layer **134***x* located between the second electrode structure **200**B and the third electrode structure **200**C. In other words, the first separation distance may refer to a distance between tipper sidewalls of the first conductive layer **232**A, which face the second conductive layer **232**B, and upper sidewalls of the second conductive layer **232**B, which face the first conductive layer **232**A, or a minimum distance between the first conductive layer **232**A and the second conductive layer **232**B. In addition, the third separation distance ray refer to a distance between upper sidewalls of the second conductive layer **232**B, which face the third conductive layer **232**C, and upper sidewalls of the third conductive layer **232**C, which face the second conductive layer **232**B, or a minimum distance between the second conductive layer **232**B and the third conductive layer **232**C. The dielectric layer **150**A including a material, which has an etch selectivity with respect to the second interlayer insulating layer **134***x*, between the first electrode structure **200**A and the second electrode structure **200**B may be formed so that the first separation distance may be less than or equal to the second separation distance. According to an embodiment of the present inventive concept, a width of the dielectric layer **150**A in the first direction (e.g., the x-direction) may be smaller than a width of the first conductive layer **232**A in the first direction (e.g., the x-direction).

[0040] Referring to FIGS. **2** and **3**, a second interlayer insulating layer **134***x* may be formed between the second conductive layer **232**B, which is included in the second electrode structure **200**B, and the third conductive layer **232**C, which is included in the third electrode structure **200**C. Based on the center of each of the first conductive layer **232**A, the second conductive layer **232**B, and the third conductive layer **232**C, a distance W**1** between the center of the first conductive layer **232**A and the center of the second conductive layer **232**B may be greater than or equal to a distance W**2** between the center of the second conductive layer **232**B and the center of the third conductive layer **232**C.

[0041] In addition, based on top surfaces of the first conductive layer **232**A and the dielectric layer **150**A, a vertical length H**1** of the dielectric layer **150**A may be less than or equal to a vertical length H**2** of the first conductive layer **232**A.

[0042] Because the dielectric layer **150**A includes a material having an etch selectivity with respect to the interlayer insulating layers **132***x* and **134***x*, the dielectric layer **150**A may be etched at a relatively low speed or may be hardly etched in a process of etching the interlayer insulating layers **132***x* and **134***x*. In addition, the interlayer insulating layers **132***x* and **134***x* may be etched at a relatively low speed or may be hardly etched in a process of etching the dielectric layer **150**A. Thus, a distance W**1** or a first separation distance between the first conductive layer **232**A and the second conductive layer **232**B may be reduced through a process using an etch selectivity despite the limit of the photolithography process. Thus, the first separation distance between the first conductive layer **232**A and the second conductive layer **232**B in the first direction (e.g., the x-direction) may be less than or equal to the second separation distance between the second conductive layer **232**B and the third conductive layer **232**C in the first direction (e.g., the x-direction).

[0043] Referring to FIG. **1** together, a fourth electrode structure **2001**) may be formed to be spaced apart from the second electrode structure **200**B in a second direction (e.g., the y-direction) substantially perpendicular to the first direction (e.g., the x-direction). The fourth electrode structure **200**D may further include a fourth conductive layer formed inside a fourth trench. In addition, a dielectric layer **150**B may be formed between the second conductive layer **232**B and the fourth conductive layer.

[0044] FIG. **4** is a cross-sectional view illustrating an interconnection structure **20** of an integrated circuit device according to an embodiment of the present inventive concept.

[0045] The interconnection structure **20** of the integrated circuit device shown in FIG. **4** may be a single damascene structure formed by a single damascene process. The single damascene structure may be formed by performing a via hole etching process, which is for forming via holes VH, and a trench etching process, which is for forming trenches TR separately.

[0046] Components shown in FIG. **2** that may be assumed as being similar to components of the interconnection structure **20** of the integrated circuit device shown in FIG. **4** may perform the same or similar functions.

[0047] When comparing FIGS. **2** and **4** with each other, same reference numerals may refer to same elements. Thus, a description of the same elements as those of FIG. **2** may be omitted or briefly discussed.

[0048] The interconnection structure **20** of the integrated circuit device may pass through portions of the second interlayer insulating layer **134***x* that is disposed under the plurality of trenches TR**1**, TR**2**, and TR**3** to form a plurality of via holes VH**1**, VH**2**, and VH**3** in the second interlayer insulating layer **134***x*. A plurality of via layers **234**A, **234**B, and **234**C may be formed inside the plurality of via holes VH**1**, VH**2**, and VH**3**. The plurality of conductive layers **232**A, **232**B, and **232**C may be electrically connected to a lower conductive layer **124***x* through the plurality of via layers **234**A, **234**B, and **234**C, respectively.

[0049] A first barrier **212**A, a first seed layer **222**A, and a first via layer **234**A may be formed in the first via hole VH**1**. The first barrier **212**A may be formed with a substantially uniform thickness along the surface of the first via hole VH**1**, and the first seed layer **222**A may be disposed on the first barrier layer **212**A. The first via layer **234**A may be disposed on the first seed layer **222**A. A second barrier **212**B, a second seed layer **222**B, and a second via layer **234**B may be included in the second via hole VH**2**. The second barrier **212**B may be formed with a substantially uniform thickness along the surface of the second via hole VH**2**, and the second seed layer **222**B may be disposed on the second barrier layer **212**B. The second via layer **234**B may be disposed on the second seed layer **222**B. A third barrier **212**C, a third seed layer **222**C, and a third via layer **234**C may be included in the third via hole VH**3**. The third barrier **212**C may be formed with a substantially uniform thickness along the surface of the third via hole VH**3**, and the third seed layer **222**C may be disposed on the third barrier layer **212**C. The third via layer **234**C may be disposed on the third seed layer **222**C.

[0050] The second conductive layer **232**B may be formed on the second via layer **234**B, which is spaced apart from the first via layer **234**A in the first direction (e.g., the x-direction). The third conductive layer **232**C may be formed on the third via layer **234**C that is spaced apart from the second via layer **234**B in the first direction (e.g., the x-direction). The dielectric layer **150**A may be formed in a space between the first conductive layer **232**A and the second conductive layer **232**B, and the second interlayer insulating layer **134***x* may be formed in a space between the second conductive layer **232**B and the third conductive layer **232**C In this case, a bottom surface of the dielectric layer **150**A may be at a higher position than or on the same plane as the top surfaces of the first via layer **234**A, the second via layer **234**B, and the third via layer **234**C. For example, the bottom surface of the dielectric layer **150**A may be at a higher position than the top surfaces of the first via layer **234**A, the second via layer **234**B, and the third via layer **234**C. For example, the bottom surface of the dielectric layer **150**A may be at a higher position than or on the same plane as the bottom surfaces of the first conductive layer **232**A, the second conductive layer **232**B, and the third conductive layer **232**C. According to an embodiment of the present inventive concept, the bottom surface of the dielectric layer **150**A may be at a lower position than the bottom surfaces of the first conductive layer **232**A, the second conductive layer **232**B, and the third conductive layer **232**C.

[0051] Based on the center of each of the first conductive layer **232**A, the second conductive layer **232**B, and the third conductive layer **232**C, a distance W**1** between the center of the first conductive layer **232**A and the center of the second conductive layer **232**B may be greater than or equal to a distance W**2** between the center of the second conductive layer **232**B and the center of the third conductive layer **232**C.

[0052] In an embodiment of the present inventive concept, the first separation distance between the first conductive layer **232**A and the second conductive layer **232**B in the first direction (e.g., the x-direction) may be less than or equal to the second separation distance between the second conductive layer **232**B and the third conductive layer **232**C in the first direction (e.g., the x-direction). Here, the first separation distance may refer to a distance between upper sidewalls of the first conductive layer **232**A, which face the second conductive layer **232**B, and tipper sidewalls of the second conductive layer **232**B, which face the first conductive layer **232**A, or a minimum distance between the first conductive layer **232**A and the second conductive layer **232**B. In addition, the third separation distance may refer to a distance between upper sidewalls of the second conductive layer **232**B, which face the third conductive layer **232**C, and upper sidewalls of the third conductive layer **232**C, which face the second conductive layer **232**B, or a minimum distance between the second conductive layer **2323** and the third conductive layer **232**C.

[0053] Because the dielectric layer **150**A includes a material having an etch selectivity with respect to the interlayer insulating layers **132***x* and **134***x*, the dielectric layer **150**A may be etched at a relatively low speed or may be hardly etched in a process of etching the interlayer insulating layers **132***x* and **134***x*. In addition, the interlayer insulating layers **132***x* and **134***x* may be etched at a relatively low speed or may be hardly etched in a process of etching the dielectric layer **150**A. Thus, a distance W**1** or a first separation distance between the first conductive layer **232**A and the second conductive layer **232**B may be reduced through a process using an etch selectivity despite the limit of the photolithography process.

[0054] The dielectric layer **150**A may be formed between the first conductive layer **232**A included in the first electrode structure **200**A and the second conductive layer **232**B included in the second electrode structure **200**B. The dielectric layer **150**A may include a material having an etch selectivity with respect to the interlayer insulating layers **132***x* and **134***x*. The dielectric layer **150**A may include, for example, SiN, AlN, molybdenum disulfide (MoS_2), hexagonal-Boron nitride, or a combination thereof. Because the dielectric layer **150**A includes a material having an etch selectivity with respect to the interlayer insulating layers **132***x* and **134***x*, the dielectric layer **150**A may be etched at a relatively low speed or may be hardly etched in a process of etching the interlayer insulating layers **132***x* and **134***x*. In addition, the interlayer insulating layers **132***x* and **134***x* may be etched at a relatively low speed or may be hardly etched in a process of etching the dielectric layer **150**A.

[0055] A second interlayer insulating layer **134***x* and etch-stop layers **142***b* and **144***b* may be formed on the lower conductive layer **124***x* and the first interlayer insulating layer **132***x*. The etch-stop layers **142***b* and **144***b* may be arranged in a space between the first via layer **234**A and the second via layer **234**B and in a space between the second via layer **234**B and the third via layer **234**C. The second interlayer insulating layer **134***x* may include, for example, a silicon oxide. The etch-stop layers **142***a* and **142***b* may include materials having an etch selectivity with respect to the second interlayer insulating layer **134***x*. Thus, the etch-stop

layers **142**a and **142**b may include materials having an etch selectivity with respect to silicon oxide. The etch-stop layers **142**a and **144**b are shown as double layers for convenience, however, may include a single layer or a plurality of layers having a triple layer or more.

[0056] Upper etch-stop layers **146** and **148** may be formed on the second interlayer insulating layer **134**x. The upper etch-stop layers **146** and **148** may be arranged in a space between the plurality of trenches TR**1**, TR**2**, and TR**3**. The second interlayer insulating layer **134**x may include, for example, a silicon oxide. The upper etch-stop layers **146** and **148** may include materials having an etch selectivity with respect to the second interlayer insulating layer **134**x. Thus, the upper etch-stop layers **146** and **148** may include materials having an etch selectivity with respect to silicon oxide. The upper etch-stop layers **146** and **148** are shown as double layers for convenience, however, may include a single layer or a plurality of layers having a triple layer or more.

[0057] In an embodiment of the present inventive concept, the second interlayer insulating layer **134**x may include a first sub insulating layer, in which the plurality of via holes VH**1**, VH**2**, and VH**3** may be formed, and a second sub insulating layer, in which the plurality of trenches TR**1**, TR**2** and TR**3** may be formed.

[0058] A first trench TR**1** may be formed inside the upper etch-stop layers **146** and **148** and the second interlayer insulating layer **134**x. The bottom of the first trench TR**1** may be formed on the same plane as the bottom surface of the first upper etch-stop layer **146** or at a position lower than the bottom surface of the first upper etch-stop layer **146**. The first trench TR**1** may vertically overlap the first via hole VH**1**. The first trench TR**1** may be a trench recessed from the top surface of the second interlayer insulating layer **134**x to a level substantially equal to a level of the bottom surface of the first upper etch-stop layer **146** by a third height H**3**. The combined height of the first trench TR**1** and the first via hole VH**1** may extend from the top surface of the second interlayer insulating layer **134**x to the top surface of lower conductive layer **124**x and may be a fourth height H**4**.

[0059] Second and third trenches TR**2** and TR**3** may be spaced apart from each other in the first direction (x-direction) based on the first trench TR**1**. The second and third trenches TR**2** and TR**3** may be formed inside the tipper etch-stop layers **146** and **148** and the second interlayer insulating layer **134**x. The second and third trenches TR**2** and TR**3** may vertically overlap the second via hole VH**2** and the third via hole VH**3**, respectively.

[0060] A first barrier **212**A, a first seed layer **222**A, and a first conductive layer **232**A may be included in the first trench TR**1**. The first barrier **212**A may be formed with a substantially uniform thickness along the surface of the first trench TR**1**. A second barrier **212**B, a second seed layer **222**B, and a second conductive layer **232**B may be included in the second trench TR**2**. The second barrier **212**B may be formed with a substantially uniform thickness along the surface of the second trench TR**2**. A third barrier **212**C, a third seed layer **222**C, and a third conductive layer **232**C may be included in the third trench TR**3**. The third barrier **212**C may be formed with a substantially uniform thickness along the surface of the third trench TR**3**. The first barrier **212**A, the second barrier **212**B, and the third barrier **212**C: may each include, for example, ruthenium (Ru), cobalt (Co), tantalum (Ta), tantalum nitride (TaN) titanium (Ti), titanium nitride (TiN), tungsten (W), tungsten nitride (WN), ruthenium (Ru), or a combination thereof (e.g., an alloy or a stacked structure). Each of the plurality of barrier layers **212**A, **212**B, and **212**C; may at least partially surround the conductive layers **232**A, **232**B, and **232**C, and the dielectric layer **150**A may come into contact with a first barrier **212**A and a second barrier **212**B.

[0061] Referring to FIG. **1** together, a fourth electrode structure **200**D may be formed to be spaced apart from the second electrode structure **200**B in a second direction (e.g., the y-direction) substantially perpendicular to the first direction (e.g., the x-direction). The fourth electrode structure **200**D may further include a fourth conductive layer formed inside a fourth trench that is overlapping a fourth via hole that is filled with a fourth via layer. For example, a fourth conductive layer may be formed on the fourth via layer spaced apart from the second via layer **234**B in the second direction (e.g., the y-direction) substantially perpendicular to the first direction (e.g., the x-direction). In addition, a dielectric layer **150**B may be formed between the second conductive layer **232**B and the fourth conductive layer.

[0062] FIG. **5** is a cross-sectional view illustrating an interconnection structure **30** of an integrated circuit device according to an embodiment of the present inventive concept.

[0063] For example, the interconnection structure **30** of the integrated circuit device may be substantially the same as the interconnection structure **10** of the integrated circuit device of FIGS. **1** to **4**, except that the interconnection structure **30** does not include a via layer. The reference numerals of FIG. **5** that are the same as those of FIGS. **1** through **4** refer to same elements. Thus, a description of the same elements as those of FIGS. **1** through **4** may be briefly described or omitted.

[0064] According to an embodiment of the present inventive concept, the interconnection structure **30** of the integrated circuit device may include an interlayer insulating layer **134**x formed on the lower etch-stop layers **142**a and **144**b. A plurality of trenches TR**1**, TR**2**, and TR**3** may be formed inside the interlayer insulating layer **134**x, and conductive layers **232**A, **232**B, and **232**C may be respectively formed inside the plurality of trenches TR**1**, TR**2**, and TR**3**.

[0065] The plurality of trenches TR**1**, TR**2**, and TR**3** may be spaced apart from the lower etch-stop layers **142**a and **142**b. The interconnection structure **30** of the integrated circuit device may include a dielectric layer **150**A having an etch selectivity with respect to the interlayer insulating layer **134**x between the first conductive layer **232**A, which is formed inside the first trench TR**1**, and the second conductive layer **232**B, which is formed inside the second trench TR**2**.

[0066] FIG. **6** is a cross-sectional view illustrating an interconnection structure **40** of an integrated circuit device according to an embodiment of the present inventive concept.

[0067] For example, the interconnection structure **40** of the integrated circuit device may be substantially the same as the interconnection structure **10** of the integrated circuit device of FIGS. **1** to **4**, except that the height of the dielectric layer **150**A is relatively small. The reference numerals of FIG. **6** that are the same as those of FIGS. **1** through **4** refer to the same elements. Thus, a description of the same element as those of FIGS. **1** through **3** may be briefly described or omitted.

[0068] According to an embodiment of the present inventive concept, the interconnection structure **40** of the integrated circuit device may include a dielectric layer **150**A having an etch selectivity with respect to the interlayer insulating layer **134**x between the first conductive layer **232**A, which is formed inside the first trench TR**1**, and the second conductive layer **232**B, which is formed inside the second trench TR**2**. In this case, the lower cross-section of the dielectric layer **150**A may be at a higher position than upper cross-sections of lower etch-stop layers **142**a and **144**b.

[0069] FIGS. **7** through **15** are cross-sectional views for illustrating a process of manufacturing the interconnection structure **10** of the integrated circuit device shown in FIG. **1** according to an embodiment of the present inventive concept.

[0070] Referring to FIG. **7**, a first interlayer insulating layer **132**x may be formed on a semiconductor substrate **110**x. The first interlayer insulating layer **132**x may include, for example, silicon oxide. A conductive plug **122**x and a lower conductive layer **124**x may be arranged inside the first interlayer insulating layer **132**x.

[0071] In an embodiment of the present inventive concept, the lower conductive layer **124**x may be a conductive material layer including W or Al. In an embodiment of the present inventive concept, the lower conductive layer **124**x may be a conductive material layer including Cu. The conductive plug **122**x may be electrically connected to electrical elements formed in the substrate **110**x.

[0072] A second interlayer insulating layer **134**x and etch-stop layers **142**a and **144**b may be formed on the first conductive layer **107**. The second interlayer insulating layer **109** and the third interlayer insulating layer **123** may include, for example, silicon oxide layers. The etch-stop layers **142**a and **144**a may include materials having an etch selectivity with respect to the second interlayer insulating layer **134**x. The etch-stop layers **142**a and **144**a may, for example, include silicon nitride layers.

[0073] Referring to FIGS. **8** and **9**, a recess region **150**R in which a dielectric layer **150** may be formed, may be formed by removing portions of the second interlayer insulating layer **134**x. In FIG. **8**, two recess regions are formed. However, embodiments of the present inventive concept are not limited to the above-described number, and three or more recess regions may be formed. The recess region **150**R may be formed by using photography and etching methods. The recess region **150**R may be formed by trench first via last (TFVL) or via first trench last (VFTL).

[0074] After the recess region **150**R is formed, the dielectric layer **150** may be deposited on sidewalls of the recess region **150**R and the second interlayer insulating layer **134**x. The dielectric layer **150** may be formed by using physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma-enhanced CVD, or atomic layer deposition (ALD). The dielectric layer **150** may include a material having an etch selectivity with respect to the second interlayer insulating layer **134**x. The dielectric layer **150** may include, for example, silicon nitride (SiN), silicon oxynitride (SiON), silicon carbon nitride (SiCN), aluminum oxide (Al_2O_2), aluminum nitride (AlN), titanium oxide (TiO_2), or a combination thereof.

[0075] Referring to FIG. **10**, the dielectric layer **150** deposited on the second interlayer insulating layer **134**x may be etched A process of etching the dielectric layer **150** may be a process using an etch selectivity. For example, while the second interlayer insulating layer **134**x is hardly removed, the dielectric layer **150** may be etched at a relatively high speed. Thus, the dielectric layer **150** may be completely etched, and only the second interlayer insulating layer **134**x may be exposed in the region of the second interlayer insulating layer **134**x in which no recess is formed.

[0076] Referring to FIG. **11**, by etching portions of the second interlayer insulating layer **134**x and the dielectric layer **150**, a first upper recess region **162**a formed between a plurality of dielectric layers **150**, a second tipper recess region **162**b formed between the dielectric layer **150** and the second interlayer insulating layer **134**x, and a third upper recess region **162**c formed between a plurality of second interlayer insulating layers **134**x may be formed.

[0077] In an embodiment of the present inventive concept, a process of etching portions of the second interlayer insulating layer **134**x and a process of etching portions of the dielectric layer **150** may be different processes. The process of etching portions of the second interlayer insulating layer **134**x and the process of etching portions of the dielectric layer **150** may be processes using an etch selectivity.

[0078] For example, the process of etching the second interlayer insulating layer **134**x may be performed first, and the second interlayer insulating layer **134**x may be etched at a relatively high speed while the dielectric layer **150** is hardly removed. The process of etching portions of the dielectric layer **150** may be performed after the process of etching the second interlayer insulating layer **134**x is performed. While the second interlayer insulating layer **134**x is hardly removed, the dielectric layer **150** may be etched at a relatively high speed.

[0079] Because the dielectric layer **150** includes a material having an etch selectivity with respect to the interlayer insulating layers **132**x and **134**x, the dielectric layer **150** may be etched at a relatively low speed or may be hardly etched in a process of etching the interlayer insulating layers **132**x and **134**x. In addition, the interlayer insulating layers **132**x and **134**x may be etched at a relatively low speed or may be hardly etched in the process of etching the dielectric layer **150**. Thus, a distance between the first conductive layer **232**A and the second conductive layer **232**B may be reduced through a process using an etch selectivity despite the limit of the photolithography process.

[0080] Subsequently, portions of the dielectric layer **150** may be etched to laterally expand a first upper recess region **162**a between the plurality of dielectric layers **150**. The process of etching portions of the dielectric layer **150** may be a process using an etch selectivity. The width of the first upper recess region **162**a formed between the plurality of dielectric layers **150** may be greater than a width of the second upper recess region **162**b formed between the dielectric layer **150** and the second interlayer insulating layer **134**x and/or a width of the third upper recess region **162**c formed between the plurality of second interlayer insulating layers **134**x.

[0081] Subsequently, portions of the second interlayer insulating layer **134**x may be etched to form lower recess regions **164**a, **164**b, and **164**c. The first lower recess region **164**a may be formed between portions of the plurality of dielectric layers **150**. The second lower recess region **164**b may be formed between portions of the dielectric layer **150** and portions of the second interlayer insulating layer **134**x. The third lower recess region **164**c may be formed between

portions of the plurality of second interlayer insulating layers **134***x*. The first lower recess region **164***a*, the second lower recess region **164***b*, and the third lower recess region **164***c* may have, for example, shapes of holes each having a circular horizontal cross-sectional shape. Each of widths of the first lower recess region **164***a*, the second lower recess region **164***b*, and the third lower recess region **164***c* may be less than each of widths of the first upper recess region **162***a*, the second upper recess region **162***b*, and the third upper recess region **162***c*.

[0082] Subsequently, portions of the dielectric layer **150** may be etched to form the first trench TR**1**. For example, portions of the dielectric layer **150** may be etched to laterally expand the first lower recess region **164***a* between the plurality of dielectric layers **150**. In this case, the first trench TR**1** may be a region including the first upper recess region **162***a* and the first lower recess region **164***a*. The second trench TR**2** may be a region including the second upper recess region **162***b* and the second lower recess region **164***b*. The third trench TR**3** may be a region including the third upper recess region **162***c* and the third lower recess region **164***c*.

[0083] The second trench TR**2** may be spaced apart from the first trench TR**1** in the first direction (e.g., the x-direction). The third trench TR**3** may be spaced apart from the second trench TR**2** in the first direction (e.g., the x-direction). The first trench TR**1** may at least partially surround portions of the dielectric layer **150** and portions of the second interlayer insulating layer **134***x*. The second trench TR**2** may at least partially surround portions of the dielectric layer **150** and portions of the second interlayer insulating layer **134***x*. The third trench TR**3** may at least partially surround portions of the second interlayer insulating layer **134***x*.

[0084] Referring to FIG. **12**, a barrier **212** may be formed on the uppermost surface of the dielectric layer **150** and sidewalls and bottom (e.g., bottom surface) of the first trench TR**1**. In addition, the barrier **212** may be formed on the uppermost surface of the second interlayer insulating layer **134***x*, the sidewalls and bottom of the second trench TR**2**, and the sidewalls and the bottom of the third trench TR**3**. The barrier **212** may be formed using, for example, PVD, CVD, plasma-enhanced CVD, or ALD. The barrier **212** may include ruthenium (Ru), cobalt (Co), tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), W, tungsten nitride (WN), or a combination thereof (e.g., an alloy or stack structure).

[0085] Referring to FIG. **13**, a seed layer **222** may be formed on the barrier **212**. The seed layer **222** may be formed using, for example, PVD, CVD, plasma-enhanced CVD, or ALD. The seed layer **222** may include Cu, Pt, Pd, Ni, Au, Ag, Ru, and the like.

[0086] Referring to FIG. **14**, a conductive layer **232** may be formed on the seed layer **222**. The conductive layer **232** may fill the first trench TR**1**, the second trench TR**2**, and the third TR**3**.

[0087] The seed layer **222** may serve to facilitate the formation of the conductive layer **232**. The conductive layer **232** may be formed using, for example, electroplating or PVD, CVD, plasma-enhanced CVD, or ALD. The conductive layer **232** may include at least one of, for example, Cu, Pt, Pd, Ni, Au, Ag, Ru, and the like.

[0088] Referring to FIG. **15**, the barrier **212**, the seed layer **222**, and the conductive layer **232** may be planarized using etch back or chemical mechanical polishing (CMP) to form a first electrode structure **200**A, a second electrode structure **200**B, and a third electrode structure **200**C. The first electrode structure **200**A may be arranged between portions of the plurality of dielectric layers **150**A. The first electrode structure **200**A may include a first barrier **212**A, a first seed layer **222**A formed on the first barrier **212**A, and a first conductive layer **232**A formed on the first seed layer **222**A. The second electrode structure **200**B may be arranged between portions of the dielectric layer **150** and portions of the second interlayer insulating layer **134***x*. The second electrode structure **200**B may include a second barrier **212**B, a second seed layer **222**B formed on the second barrier **212**B, and a second conductive layer **232**B formed on the second seed layer **222**B. The third electrode structure **200**C may be arranged between portions of the second interlayer insulating layer **134***x*. The third electrode structure **200**C may include a third barrier **212**C, a third seed layer **222**C formed on the third barrier **212**C, and a third conductive layer **232**C formed on the third seed layer **222**C.

[0089] As described above, embodiments of the present inventive concept have been disclosed in the drawings and the specification. Although embodiments have been described in the specification by using specific terms, this is merely used for the purpose of describing embodiments of the present inventive concept and is not used to limit the scope of the present inventive concept.

[0090] While the present inventive concept has been described with reference to embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made thereto without departing from the spirit and scope of the present inventive concept.

What is claimed is:

1. An integrated circuit device comprising an interconnection structure, wherein the interconnection structure comprises:

an interlayer insulating layer arranged on a substrate and having a plurality of trenches formed in the interlayer insulating layer;

a first conductive layer formed inside a first trench of the plurality of trenches;

a second conductive layer formed inside a second trench of the plurality of trenches, wherein the second trench is spaced apart from the first trench of the plurality of trenches in a first direction;

a third conductive layer formed inside a third trench of the plurality of trenches, wherein the third trench is spaced apart from the second trench of the plurality of trenches in the first direction; and

a dielectric layer formed between the first conductive layer and the second conductive layer,

wherein a portion of interlayer insulating layer is disposed between the second conductive layer and the third conductive layer, and

wherein a first width of the first conductive layer in the first direction is greater than a second width of the second conductive layer in the first direction.

2. The integrated circuit device of claim **1**, wherein the dielectric layer comprises a material having an etch selectivity with respect to the interlayer insulating layer.

3. The integrated circuit device of claim **1**, wherein a first distance between a center of the first conductive layer in the first direction and a center of the second conductive layer in

the first direction is greater than or equal to a second distance between a center of the second conductive layer in the first direction and a center of the third conductive layer in the first direction.

4. The integrated circuit device of claim **1**, wherein, based on top surfaces of the first conductive layer and the dielectric layer, a vertical length of the dielectric layer is less than or equal to a vertical length of the first conductive layer.

5. The integrated circuit device of claim **1**, wherein the interlayer insulating layer comprises silicon oxide.

6. The integrated circuit device of claim **1**, wherein the dielectric layer comprises silicon nitride (SiN), silicon oxynitride (SiON), silicon carbon nitride (SiCN), aluminum oxide (Al_2O_2), aluminum nitride (AlN), titanium oxide (TiO_2), or a combination thereof.

7. The integrated circuit device of claim **1**, further comprising a fourth conductive layer formed inside a fourth trench of the plurality of trenches, wherein the fourth trench is spaced apart from the second trench of the plurality of trenches in a second direction substantially perpendicular to the first direction, wherein the dielectric layer is formed between the second conductive layer and the fourth conductive layer.

8. The integrated circuit device of claim **1**, further comprising a first seed layer and a second seed layer, wherein the first seed layer at least partially surrounds the first conductive layer, wherein the second seed layer at least partially surrounds the second conductive layer, and wherein the dielectric layer covers the first seed layer and the second seed layer.

9. The integrated circuit device of claim **1**, wherein a first separation distance between the first conductive layer and the second conductive layer in the first direction is less than or equal to a second separation distance between the second conductive layer and the third conductive layer in the first direction.

10. An integrated circuit device comprising an interconnection structure, wherein the interconnection structure comprises:

a lower conductive layer formed on a substrate;

an interlayer insulating layer formed on the lower conductive layer and having a first trench therein;

a first via layer passing through portions of the interlayer insulating layer under the first trench;

a first conductive layer electrically connected to the lower conductive layer through the first via layer;

a second conductive layer formed on a second via layer, wherein the second via layer is spaced apart from the first via layer in a first direction;

a third conductive layer formed on a third via layer, wherein the third via layer is spaced apart from the second via layer in the first direction; and

a dielectric layer formed between the first conductive layer and the second conductive layer,

wherein a portion of the interlayer insulating layer is formed between the second conductive layer and the third conductive layer, and

wherein a first width of the first conductive layer in the first direction is greater than a second width of the second conductive layer in the first direction.

11. The integrated circuit device of claim **10**, wherein the dielectric layer comprises a material having an etch selectivity with respect to the interlayer insulating layer.

12. The integrated circuit device of claim **10**, further comprising a first seed layer and a second seed layer, wherein the first seed layer at least partially surrounds the first conductive layer, wherein the second seed layer at least partially surrounds the second conductive layer, and wherein the dielectric layer covers the first seed layer and the second seed layer.

13. The integrated circuit device of claim **10**, wherein a bottom surface of the dielectric layer is at a higher position than a bottom surface of the first via layer.

14. The integrated circuit device of claim **10**, wherein a width of the dielectric layer in the first direction is smaller than a width of the first conductive layer in the first direction.

15. The integrated circuit device of claim **10**, wherein a first separation distance between the first conductive layer and the second conductive layer in the first direction is less than or equal to a second separation distance between the second conductive layer and the third conductive layer in the first direction.

16. The integrated circuit device of claim **10**, wherein the interlayer insulating layer comprises silicon oxide.

17. The integrated circuit device of claim **10**, wherein the dielectric layer comprises silicon nitride (SiN), silicon oxynitride (SiON), silicon carbon nitride (SiCN), aluminum oxide (Al_2O_2), aluminum nitride (AlN), titanium oxide (TiO_2), or a combination thereof.

18. The integrated circuit device of claim **10**, further comprising a fourth conductive layer formed on a fourth via layer, wherein the fourth via layer is spaced apart from the second via layer in a second direction substantially perpendicular to the first direction, wherein the dielectric layer is formed between the second conductive layer and the fourth conductive layer.

19. An integrated circuit device comprising an interconnection structure, wherein the interconnection structure comprises:

an interlayer insulating layer arranged on a substrate and having a plurality of trenches formed in the interlayer insulating layer, wherein the interlayer insulating layer includes silicon oxide;

a first conductive layer formed inside a first trench of the plurality of trenches;

a second conductive layer formed inside a second trench of the plurality of trenches, wherein the second trench is spaced apart from the first trench of the plurality of trenches in a first direction;

a third conductive layer formed inside a third trench of the plurality of trenches, wherein the third trench is spaced apart from the second trench of the plurality of trenches in the first direction; and

a dielectric layer formed between the first conductive layer and the second conductive layer and including silicon nitride, silicon oxynitride (SiON), silicon carbon nitride (SiCN), aluminum oxide (Al_2O_2), aluminum nitride (AlN), titanium oxide (TiO_2), or a combination thereof, which have an etch selectivity with respect to the interlayer insulating layer,

wherein the interlayer insulating layer includes silicon oxide, and a portion of the interlayer insulating layer is formed between the second conductive layer and the third conductive layer,

wherein a first width of the first conductive layer in the first direction is greater than a second width of the second conductive layer in the first direction, and

a first separation distance between the first conductive layer and the second conductive layer in the first direction is less than or equal to a second separation distance between the second conductive layer and the third conductive layer in the first direction.

20. The integrated circuit device of claim **19**, further comprising a fourth conductive layer formed inside a fourth trench of the plurality of trenches, wherein the fourth trench is spaced apart from the second trench of the plurality of trenches in a second direction substantially perpendicular to the first direction, wherein the dielectric layer is formed between the second conductive layer and the fourth conductive layer.

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