(19) **United States**
(12) **Patent Application Publication**
IWASAKI et al.
(10) **Pub. No.: US 2019/0279961 A1**
(43) **Pub. Date: Sep. 12, 2019**

(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **Toyota Jidosha Kabushiki Kaisha**, Toyota-shi (JP)

(72) Inventors: **Shingo IWASAKI**, Toyota-shi (JP); **Kaisei Satou**, Miyoshi-shi (JP); **Yuri Imai**, Miyoshi-shi (JP)

(73) Assignee: **Toyota Jidosha Kabushiki Kaisha**, Toyota-shi (JP)

(21) Appl. No.: **16/269,242**

(22) Filed: **Feb. 6, 2019**

(30) **Foreign Application Priority Data**

Mar. 6, 2018 (JP) 2018-039925

Publication Classification

(51) **Int. Cl.**

H01L 25/065	(2006.01)
H01L 23/498	(2006.01)
H01L 23/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 25/0655*** (2013.01); ***H01L 24/49*** (2013.01); ***H01L 23/49811*** (2013.01); ***H01L 23/49844*** (2013.01)

(57) **ABSTRACT**

A semiconductor device may include a first semiconductor chip, a second semiconductor chip, an encapsulant encapsulating the first and second semiconductor chips, a first signal terminal extending over inside and outside of the encapsulant and connected to the first semiconductor chip inside the encapsulant, and a second signal terminal extending over the inside and the outside of the encapsulant and connected to the second semiconductor chip inside the encapsulant. The first and second signal terminals may protrude from the encapsulant in a same direction. The first signal terminal may include, inside the encapsulant, a section where the first signal terminal extends farther away from the second signal terminal along a direction toward the first semiconductor chip. The second signal terminal may include, inside the encapsulant, a section where the second signal terminal extends farther away from the first signal terminal along a direction toward the second semiconductor chip.

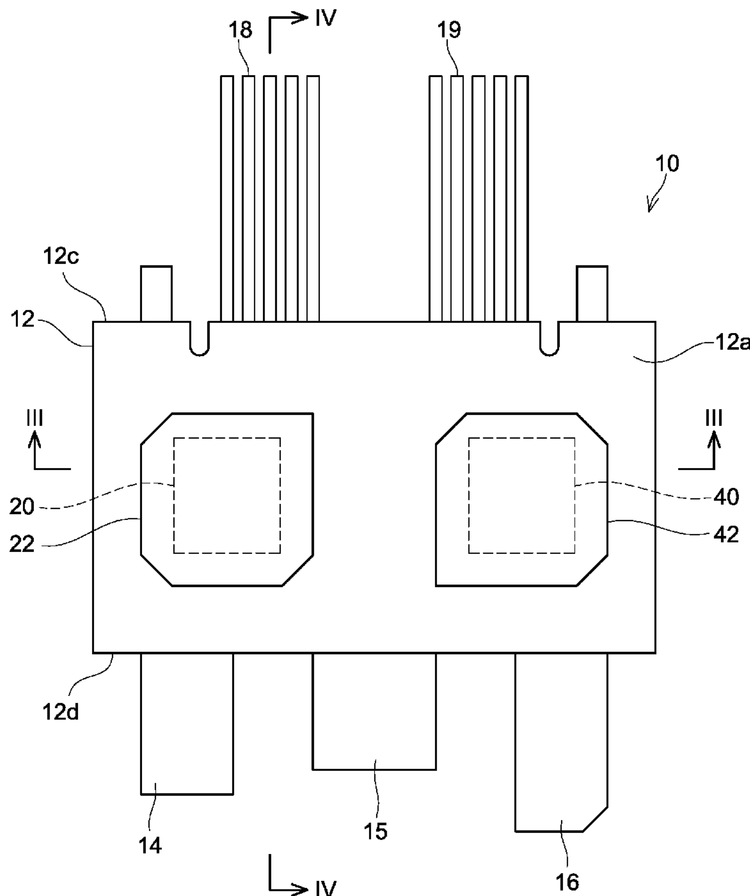


FIG. 1

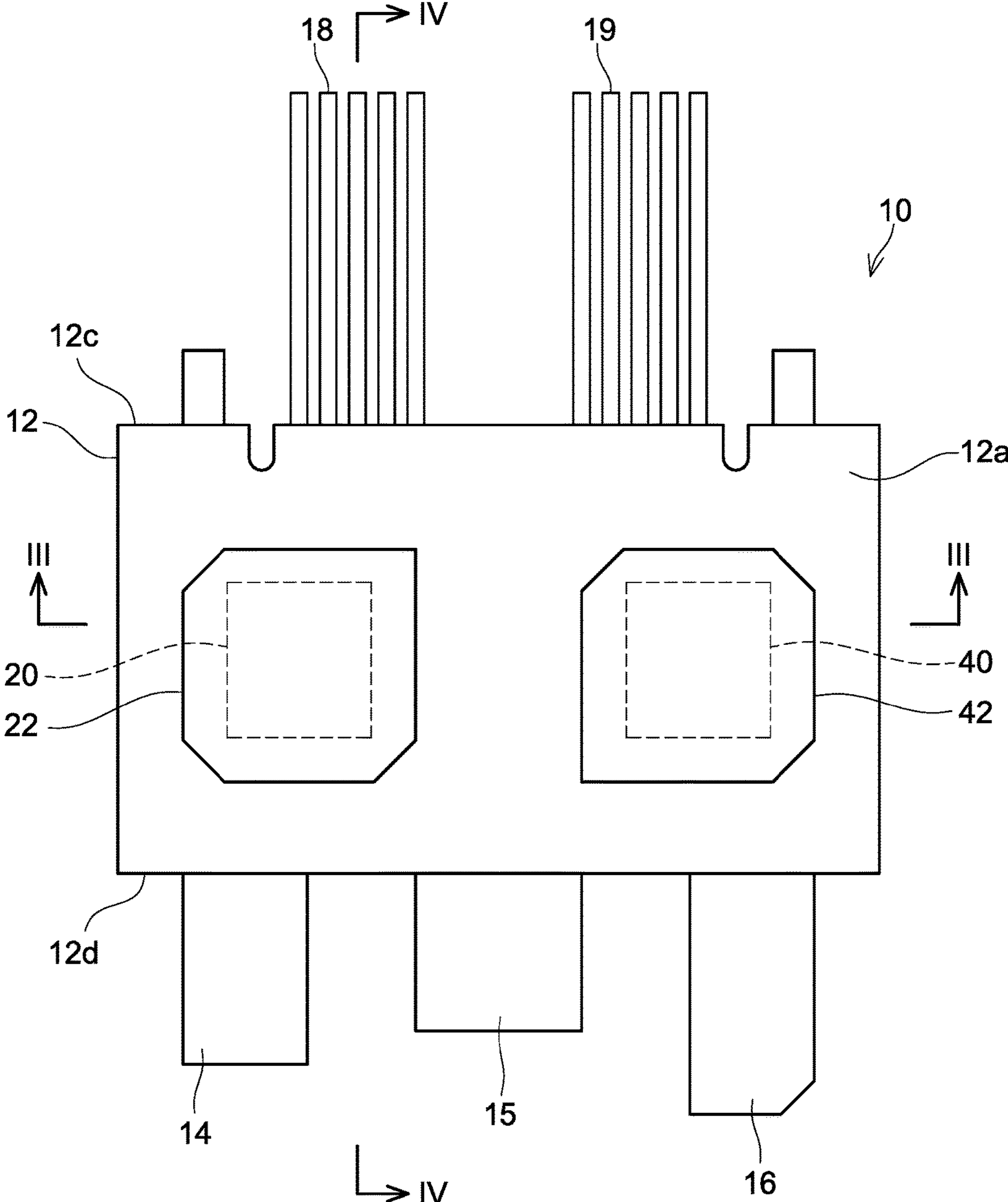


FIG. 2

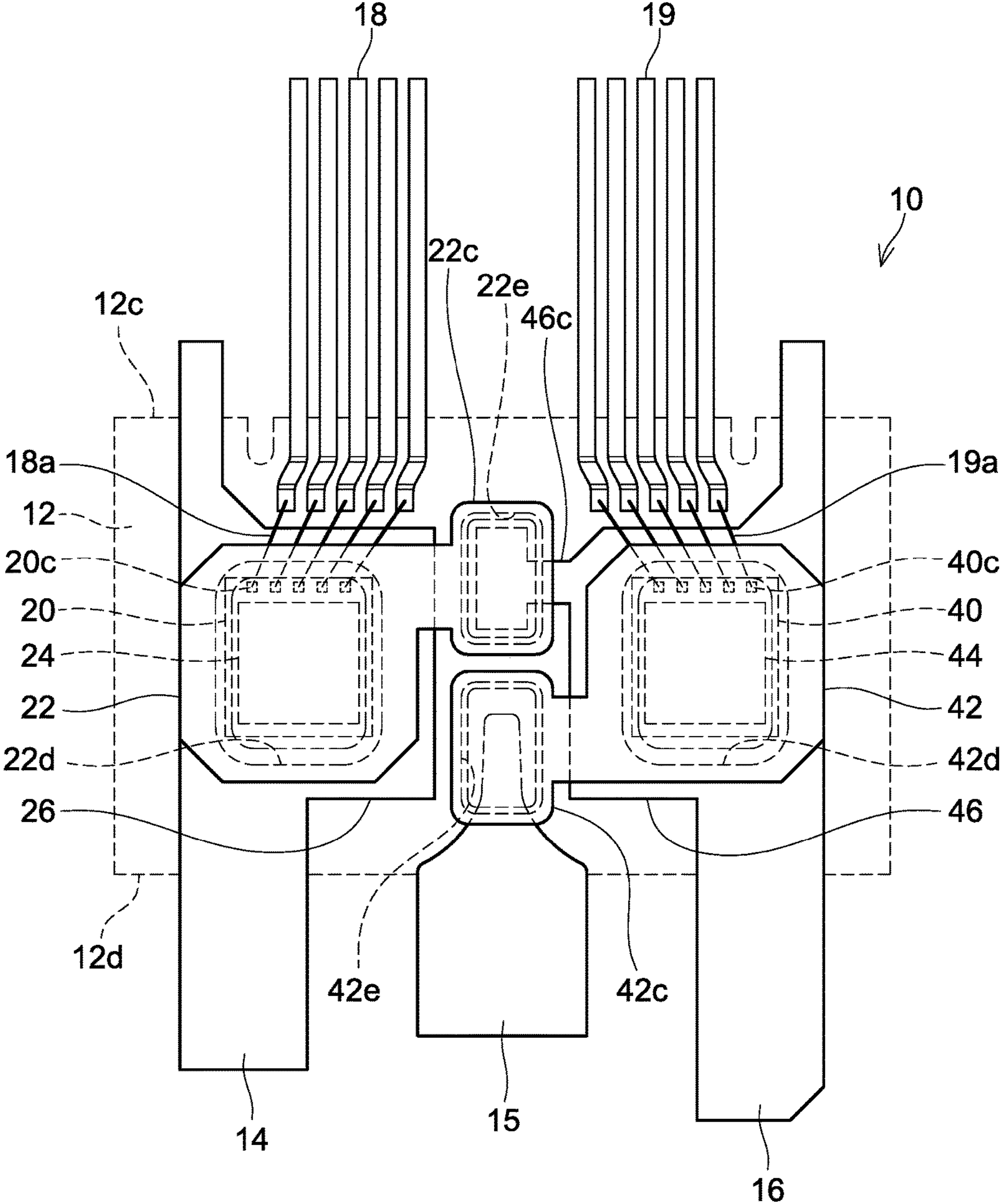


FIG. 3

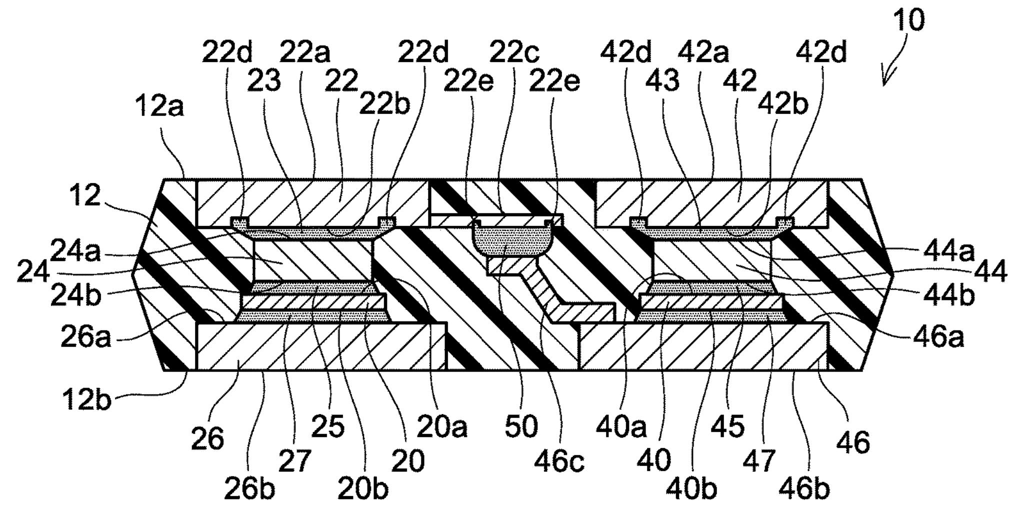
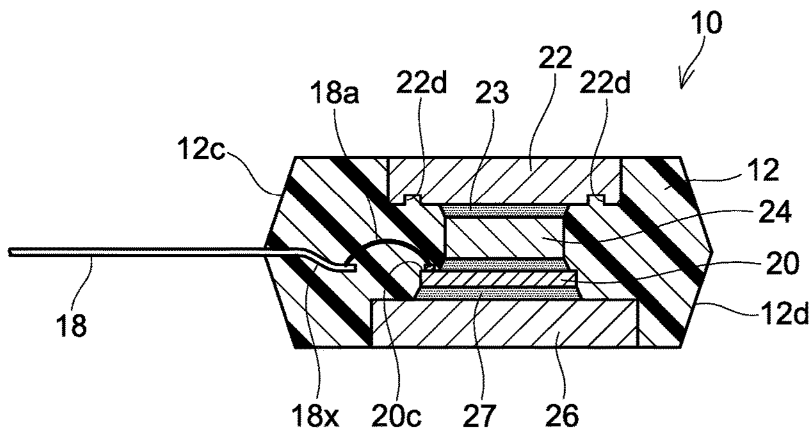


FIG. 4



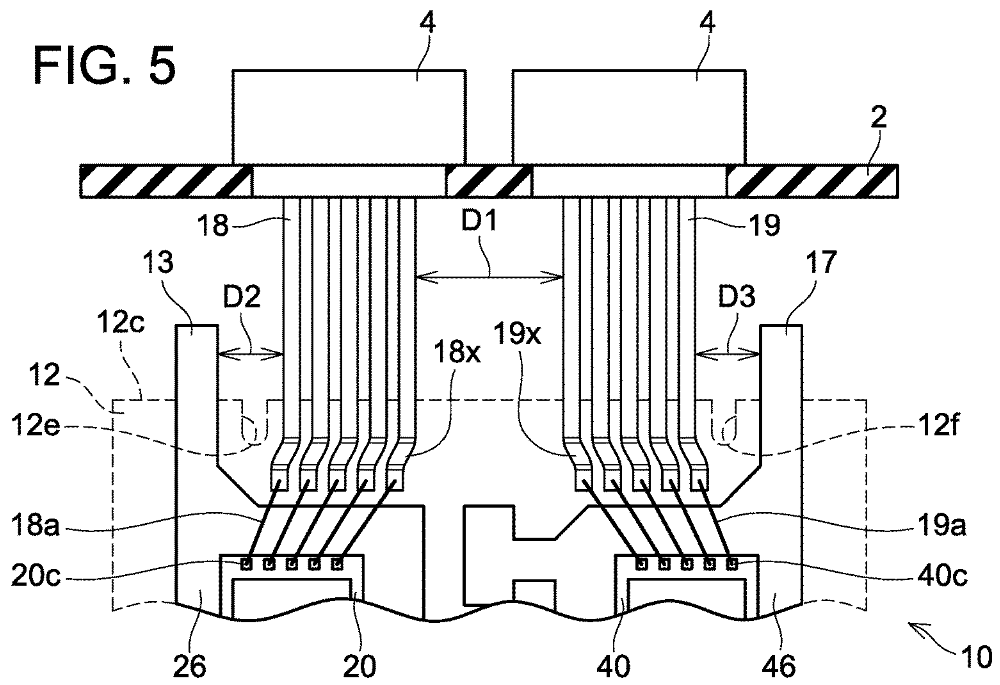


FIG. 5
4
4
2
18
19
D1
13
17
D2
D3
12c
19x
18x
12
12e
12f
18a
19a
20c
40c
26
20
40
46
10

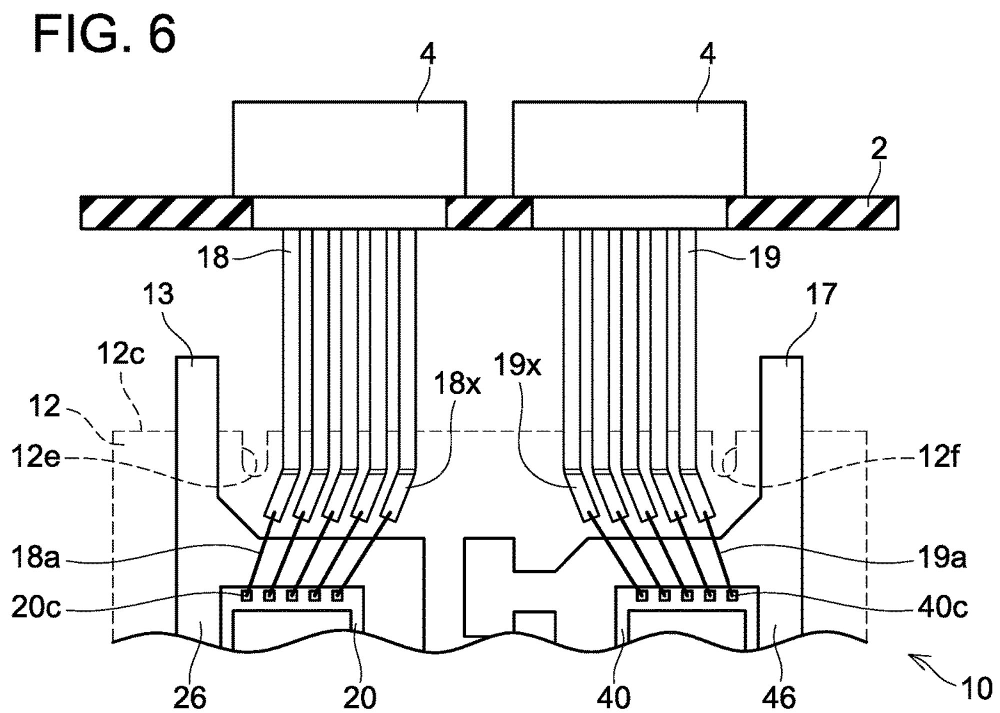


FIG. 6
4
4
2
18
19
13
17
12c
19x
18x
12
12e
12f
18a
19a
20c
40c
26
20
40
46
10

FIG. 7

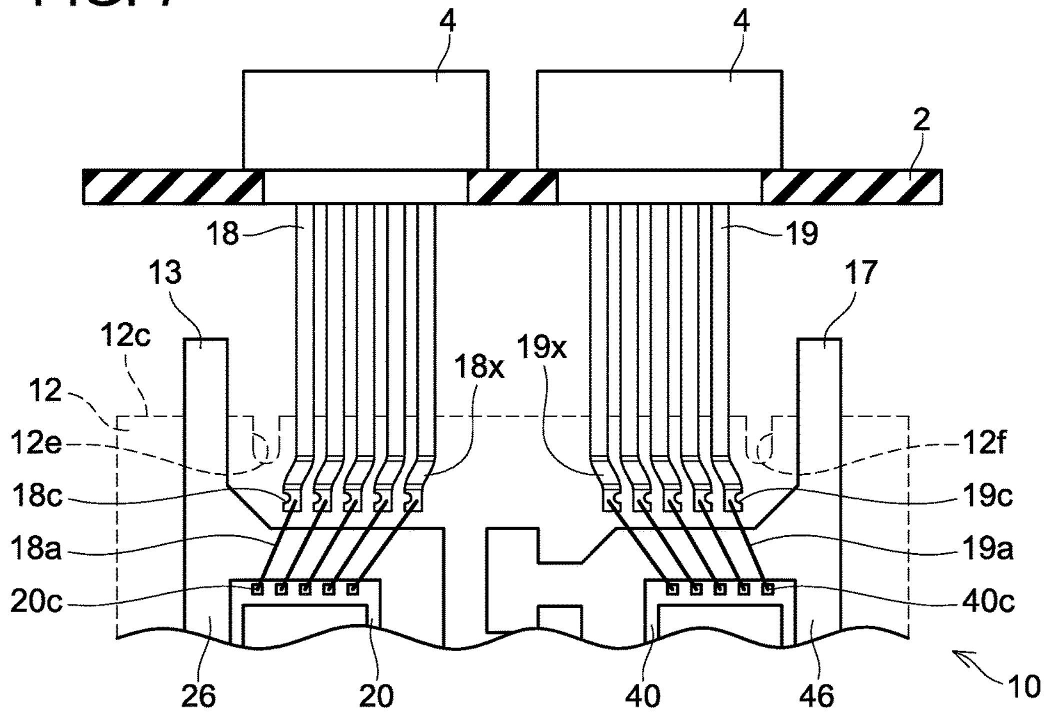


FIG. 8

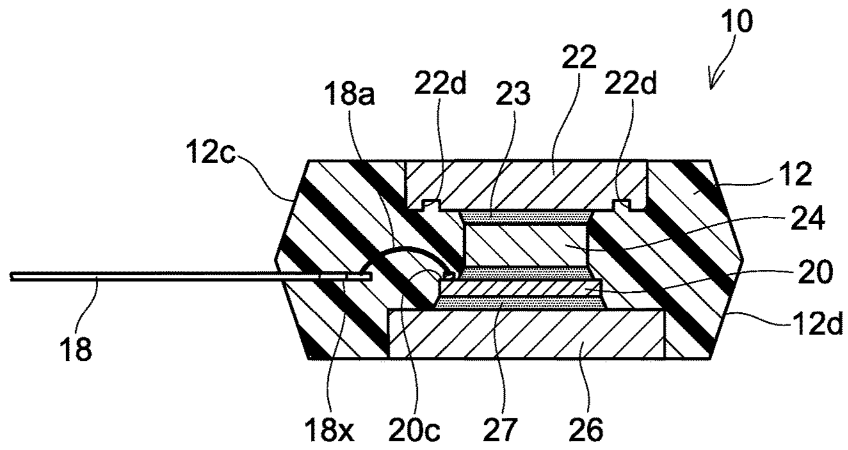


FIG. 9

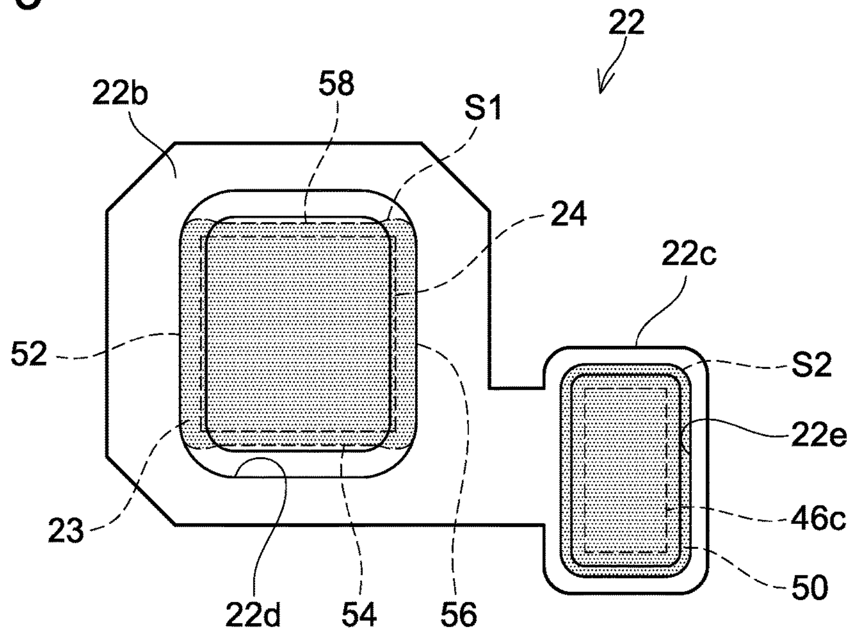


FIG. 10

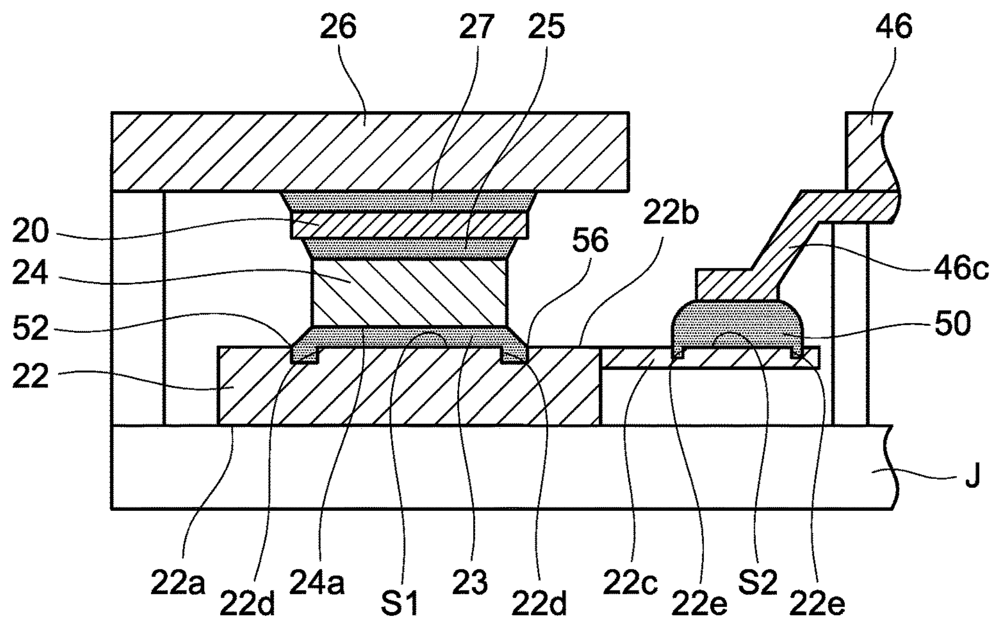


FIG. 11

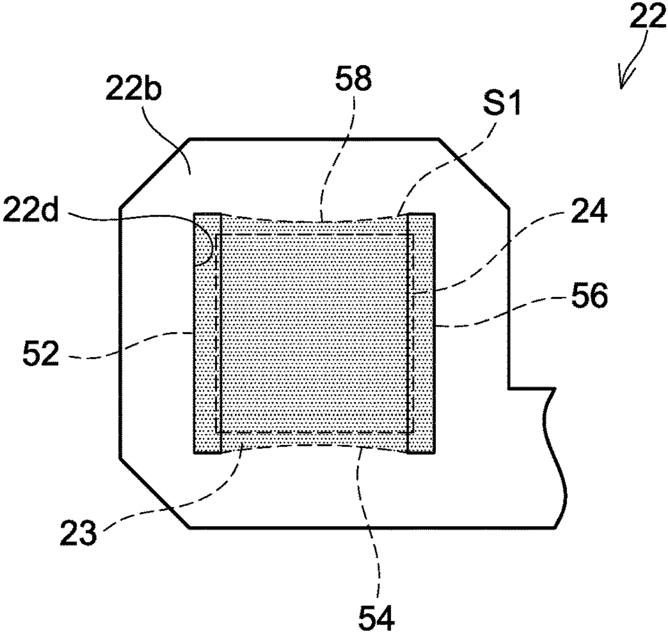


FIG. 12

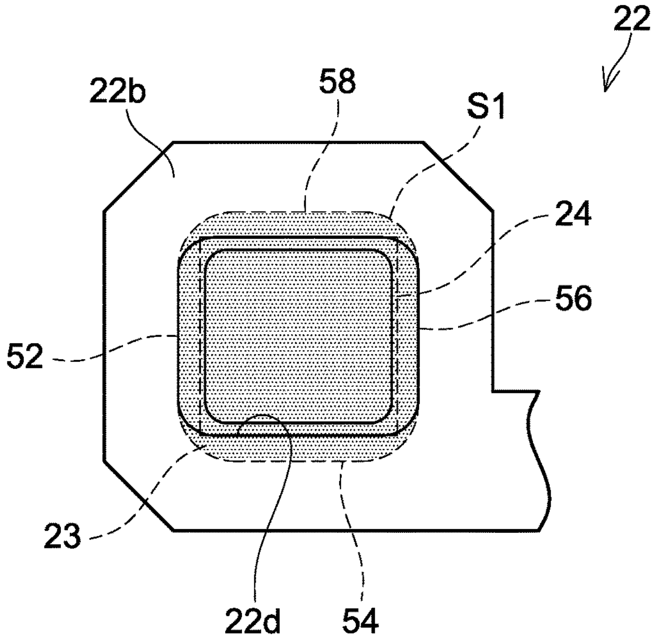


FIG. 13

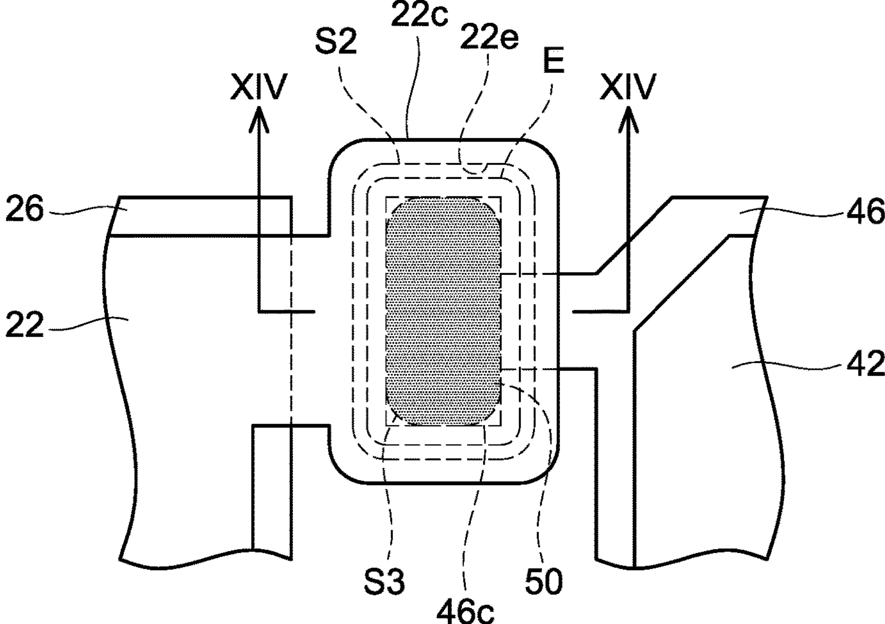


FIG. 14

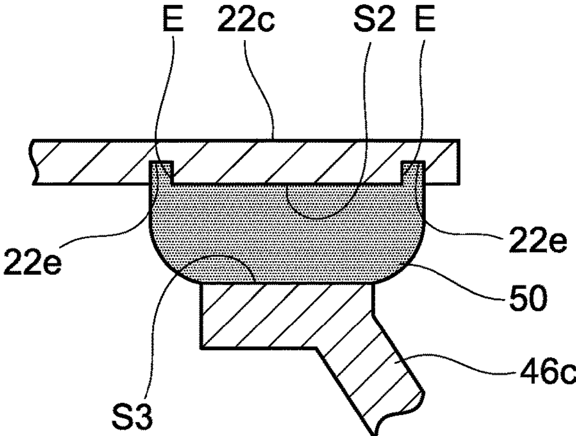


FIG. 15

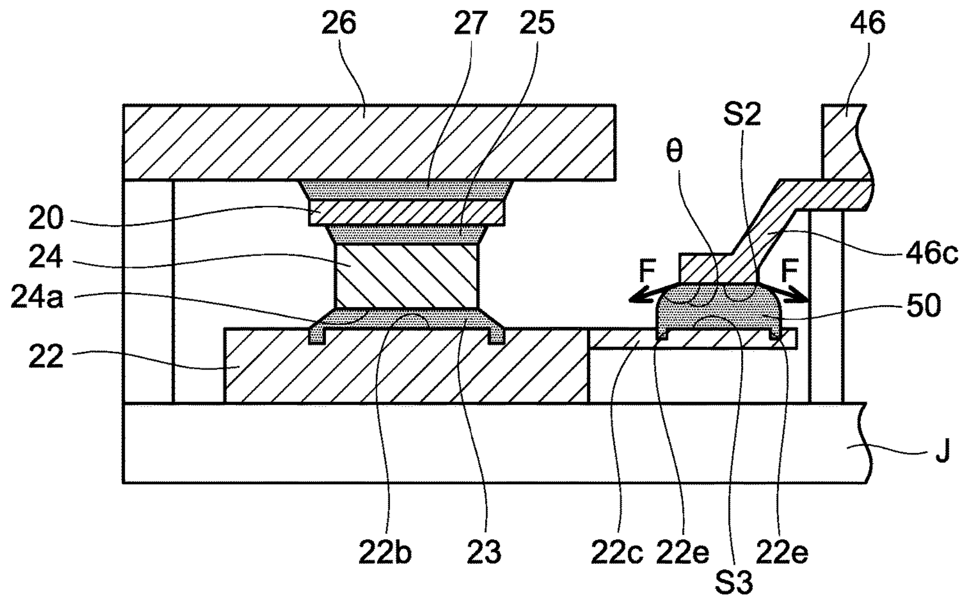


FIG. 16

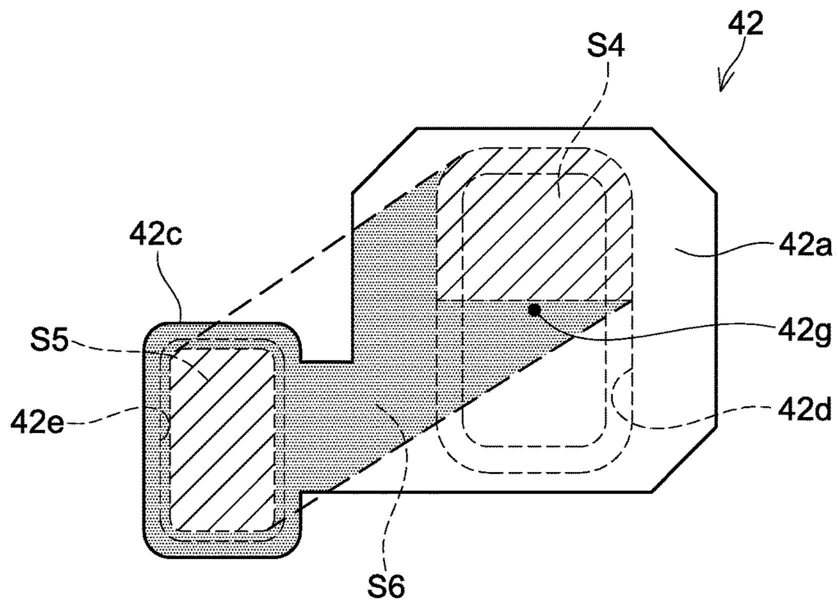


FIG. 17

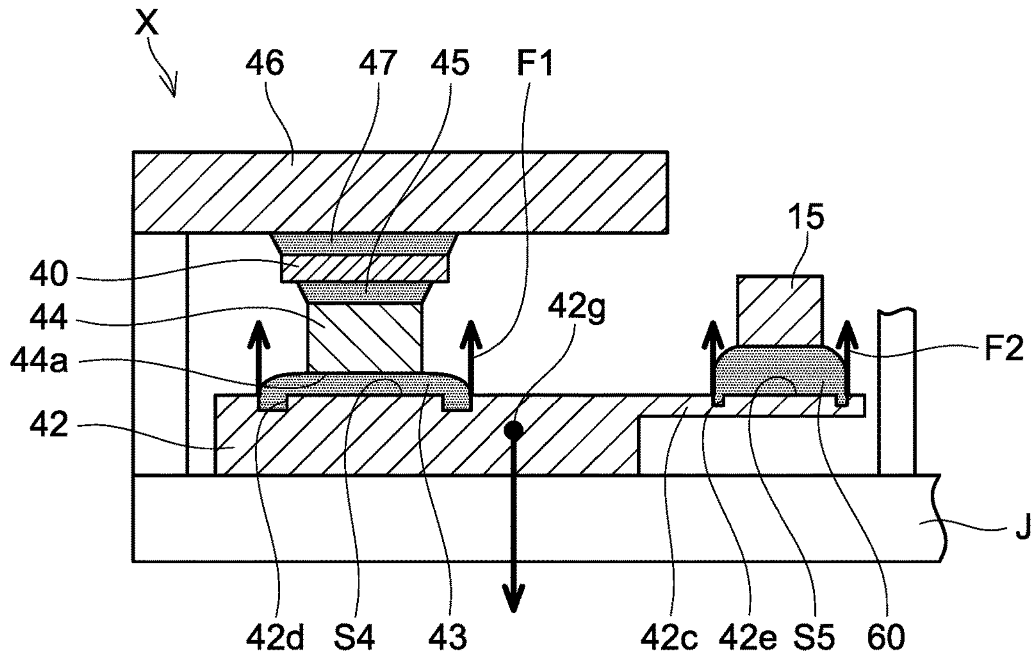


FIG. 18

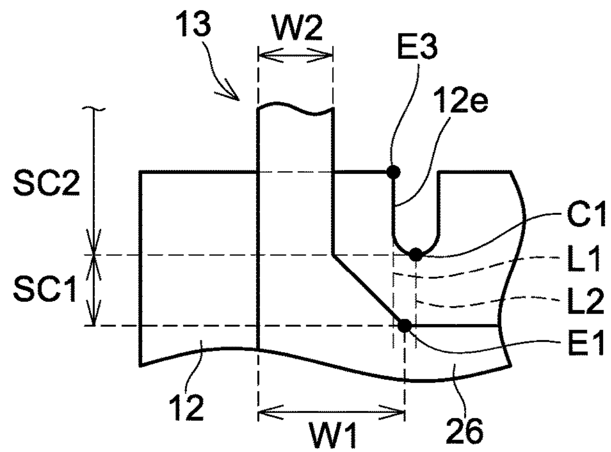


FIG. 19(A)

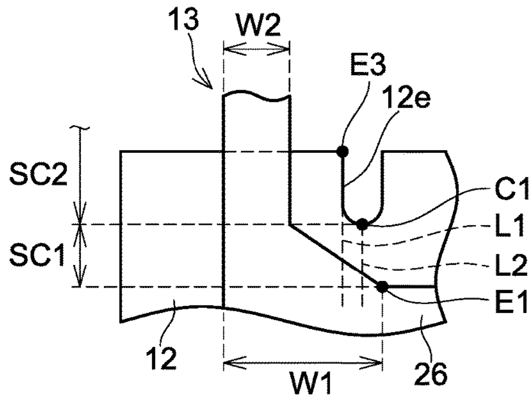


FIG. 19(B)

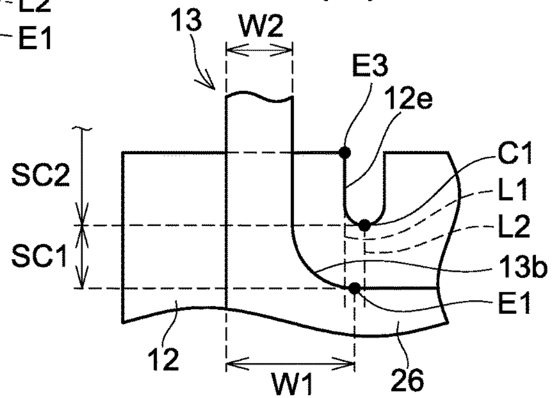


FIG. 19(C)

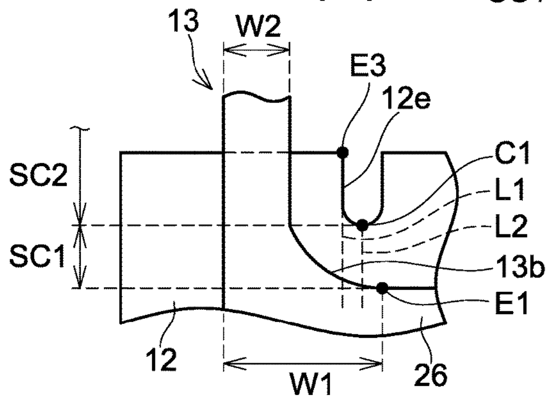


FIG. 19(D)

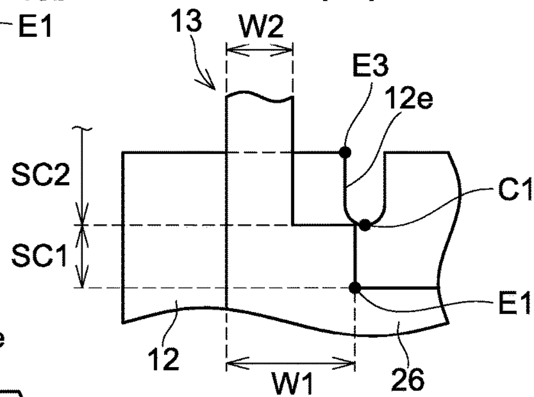


FIG. 19(E)

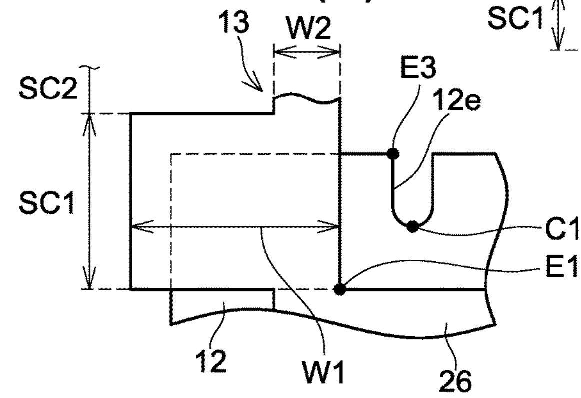


FIG. 20

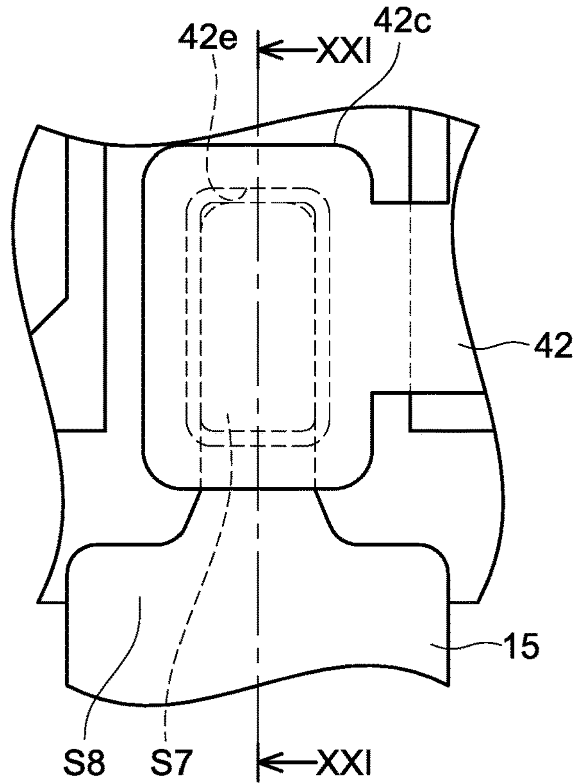
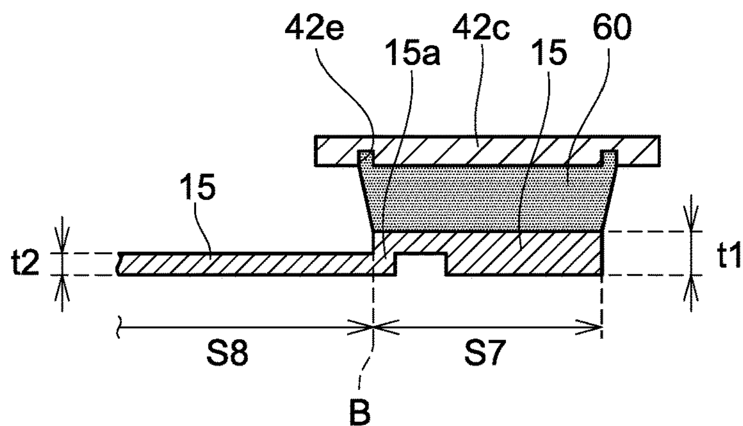


FIG. 21



SEMICONDUCTOR DEVICE

CROSS-REFERENCE

[0001] This application claims priority to Japanese Patent Application No. 2018-039925, filed on Mar. 6, 2018, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] A technology disclosed herein relates to a semiconductor device.

BACKGROUND

[0003] Japanese Patent Application Publication No. 2015-130465 describes a semiconductor device. This semiconductor device includes a first semiconductor chip and a second semiconductor chip, an encapsulant encapsulating the first semiconductor chip and the second semiconductor chip, and a first signal terminal and a second signal terminal both extending over inside and outside of the encapsulant. The first signal terminal is connected to the first semiconductor chip via a bonding wire inside the encapsulant. The second signal terminal is connected to the second semiconductor chip via a bonding wire inside the encapsulant. The first signal terminal and the second signal terminal protrude from the encapsulant in a same direction.

SUMMARY

[0004] The first signal terminal and the second signal terminal, which protrude from the encapsulant in the same direction, are usually connected to external equipment such as a control substrate. Therefore, to avoid increasing a size of the external equipment, it is desirable to set a distance (spacing) between the first signal terminal and the second signal terminal to be relatively small. On the other hand, a distance between the first semiconductor chip and the second semiconductor chip cannot be set to be small much due to design constraints inside the encapsulant, and the like. Due to this, when a distance between the first signal terminal and the second signal terminal is designed to be small, the first signal terminal and the second signal terminal are apart from the first semiconductor chip and the second semiconductor chip, respectively, inside the encapsulant. Consequently, the bonding wire that connects the first signal terminal and the first semiconductor chip, and the bonding wire that connects the second signal terminal and the second semiconductor chip are made longer. Longer bonding wires cause higher impedance, for example, and thus greater degradation or loss in signal transmission may be caused thereby. Alternatively, longer bonding wires are more likely to be displaced in a process of forming the encapsulant, and thus a risk of, for example, an electrical short circuit becomes higher. The disclosure herein provides a technology capable of shortening or omitting a bonding wire.

[0005] The technology disclosed herein is embodied by a semiconductor device. This semiconductor device may comprise a first semiconductor chip and a second semiconductor chip, an encapsulant encapsulating the first semiconductor chip and the second semiconductor chip, a first signal terminal extending over inside and outside of the encapsulant and connected to the first semiconductor chip inside the encapsulant, and a second signal terminal extending over the inside and the outside of the encapsulant and connected to the second semiconductor chip inside the encapsulant. The first signal terminal and the second signal terminal may protrude from the encapsulant in a same direction. The first signal terminal may comprise, inside the encapsulant, a section where the first signal terminal extends farther away from the second signal terminal along a direction toward the first semiconductor chip. The second signal terminal may comprise, inside the encapsulant, a section where the second signal terminal extends farther away from the first signal terminal along a direction toward the second semiconductor chip.

[0006] According to the above configuration, a distance (spacing) between the first signal terminal and the second signal terminal can be made small outside the encapsulant, and the first signal terminal and the second signal terminal can be made close to the first semiconductor chip and the second semiconductor chip, respectively, inside the encapsulant. As described before, when the distance between the first signal terminal and the second signal terminal is small outside the encapsulant, increase in a size of external equipment to which they are connected can be avoided. Alternatively, in a case where another terminal exists adjacent to the the first signal terminal or the second signal terminal, an insulating property from the other terminal can be enhanced by making a distance from the other terminal large. Inside the encapsulant, on the other hand, the first signal terminal is made close to the first semiconductor chip, and the second signal terminal is made close to the second semiconductor chip, by which a bonding wire (or another connecting member) that connects the first signal terminal and the first semiconductor chip, and a bonding wire (or another connecting member) that connects the second signal terminal and the second semiconductor chip can be shortened or omitted.

BRIEF DESCRIPTION OF DRAWINGS

[0007] FIG. **1** is a plan view of a semiconductor device **10** in an embodiment.

[0008] FIG. **2** is a plan view showing an internal structure of the semiconductor device **10**.

[0009] FIG. **3** is a cross-sectional view taken along a line III-III in FIG. **1**, which shows the internal structure of the semiconductor device **10**.

[0010] FIG. **4** is a cross-sectional view taken along a line IV-IV in FIG. **1**, which shows the internal structure of the semiconductor device **10**.

[0011] FIG. **5** shows structures of first signal terminals **18** and second signal terminals **19** inside an encapsulant **12**.

[0012] FIG. **6** shows a variant of the first signal terminals **18** and the second signal terminals **19**.

[0013] FIG. **7** shows another variant of the first signal terminals **18** and the second signal terminals **19**.

[0014] FIG. **8** shows still another variant of the first signal terminals **18** and the second signal terminals **19**.

[0015] FIG. **9** shows a variant related to a solder absorbing groove ***22d*** in a first upper heat dissipating plate **22**.

[0016] FIG. **10** is a diagram that shows soldering between the first upper heat dissipating plate **22** and a first conductor spacer **24**, in which the solder absorbing groove ***22d*** in the variant shown in FIG. **9** is adopted in the first upper heat dissipating plate **22**.

[0017] FIG. **11** shows another variant related to the solder absorbing groove ***22d***.

[0018] FIG. **12** shows still another variant related to the solder absorbing groove **22***d.*

[0019] FIG. **13** shows a variant of a solder absorbing groove **22***e* in a first joint **22***c*.

[0020] FIG. **14** shows a cross-sectional view taken along a line XIV-XIV in FIG. **13**.

[0021] FIG. **15** is a diagram that shows soldering between the first upper heat dissipating plate **22** and the first conductor spacer **24**, in which the solder absorbing groove **22***e* in the variant shown in FIGS. **13**, **14** is adopted in the first joint **22***c* of the first upper heat dissipating plate **22**.

[0022] FIG. **16** shows a variant related to solder joint areas S4, S5 of a second upper heat dissipating plate **42**.

[0023] FIG. **17** is a diagram that shows soldering between the second upper heat dissipating plate **42** and a second conductor spacer **44**, in which the solder joint areas S4, S5 of the second upper heat dissipating plate **42** satisfy a positional relation shown in FIG. **16**.

[0024] FIG. **18** shows a variant related to a suspended terminal **13**.

[0025] FIGS. **19**(A) to **19**(E) show other variants related to the suspended terminal **13**.

[0026] FIG. **20** shows a variant related to an N terminal **15**.

[0027] FIG. **21** shows a cross-sectional view taken along a line XXI-XXI in FIG. **20**.

DETAILED DESCRIPTION

[0028] In an embodiment of the present technology, at least one of the first signal terminal and the second signal terminal may extend linearly outside the encapsulant. According to such a configuration, deformation of the first signal terminal and/or the second signal terminal can be avoided when the first signal terminal and/or the second signal terminal are/is connected to, for example, a connector of a control substrate. In other words, if the first signal terminal and/or the second signal terminal are/is bent outside the encapsulant, the first signal terminal and/or the second signal terminal are/is likely to deform when connected to, for example, a connector of a control substrate.

[0029] In an embodiment of the present technology, at least one of the first signal terminal and the second signal terminal may comprise, inside the encapsulant, a crank shape that includes at least two bends. According to such a configuration, the first signal terminal and/or the second signal terminal can be fixed firmly to the encapsulant.

[0030] In an embodiment of the present technology, the first signal terminal and the second signal terminal may comprise plane-symmetrical shapes to each other. According to such a configuration, designing and manufacturing of the semiconductor device can be facilitated. Moreover, local generation of high stress (i.e., stress concentration) in the semiconductor device can be suppressed by having the structural symmetry.

[0031] In an embodiment of the present technology, at least one of the first signal terminal and the second signal terminal may comprise a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant. According to such a configuration, the first signal terminal and/or the second signal terminal can be fixed more firmly to the encapsulant.

[0032] Representative, non-limiting examples of the present invention will now be described in further detail with reference to the attached drawings. This detailed description is merely intended to teach a person of skill in the art further details for practicing preferred aspects of the present teachings and is not intended to limit the scope of the invention. Furthermore, each of the additional features and teachings disclosed below may be utilized separately or in conjunction with other features and teachings to provide improved semiconductor devices, as well as methods for using and manufacturing the same.

[0033] Moreover, combinations of features and steps disclosed in the following detailed description may not be necessary to practice the invention in the broadest sense, and are instead taught merely to particularly describe representative examples of the invention. Furthermore, various features of the above-described and below-described representative examples, as well as the various independent and dependent claims, may be combined in ways that are not specifically and explicitly enumerated in order to provide additional useful embodiments of the present teachings.

[0034] All features disclosed in the description and/or the claims are intended to be disclosed separately and independently from each other for the purpose of original written disclosure, as well as for the purpose of restricting the claimed subject matter, independent of the compositions of the features in the embodiments and/or the claims. In addition, all value ranges or indications of groups of entities are intended to disclose every possible intermediate value or intermediate entity for the purpose of original written disclosure, as well as for the purpose of restricting the claimed subject matter.

Embodiments

[0035] With reference to the drawings, a semiconductor device **10** in an embodiment will be described. The semiconductor device **10** in the present embodiment can be used for a power conversion circuit such as a converter or an inverter, in an electrically-operated vehicle such as an electric vehicle, a hybrid vehicle, and a fuel-cell vehicle. It should be noted that no particular limitation is imposed on application purposes of the semiconductor device **10**. The semiconductor device **10** can be adopted widely for various devices and circuits.

[0036] As shown in FIGS. **1** to **4**, the semiconductor device **10** includes a first semiconductor chip **20**, a second semiconductor chip **40**, an encapsulant **12**, and a plurality of terminals **14**, **15**, **16**, **18**, **19**. The first semiconductor chip **20** and the second semiconductor chip **40** are power semiconductor chips, and are encapsulated inside the encapsulant **12**. The encapsulant **12** is constituted of a thermosetting resin such as epoxy resin, but is not particularly limited thereto. The encapsulant **12** in the present embodiment has a generally plate shape, and includes an upper surface **12***a*, a lower surface **12***b* positioned opposite to the upper surface **12***a*, a first end surface **12***c* adjacent to the upper surface **12***a* and the lower surface **12***b*, and a second end surface **12***d* adjacent to the upper surface **12***a* and the lower surface **12***b* and positioned opposite to the first end surface **12***c*. It should be noted that the shape of the encapsulant **12** is not limited to the one exemplified in the present embodiment, and can be modified as appropriate.

[0037] Each of the terminals **14**, **15**, **16**, **18**, **19** extends over outside and inside of the encapsulant **12**, and is electrically connected to at least one of the first semiconductor chip **20** and the second semiconductor chip **40** inside the encapsulant **12**. As an example, the plurality of terminals

14, **15**, **16**, **18**, **19** includes a P terminal **14**, an N terminal **15**, and an O terminal **16** for power, and a plurality of first signal terminals **18** and a plurality of second signal terminals **19** for signals. The P terminal **14**, the N terminal **15**, and the O terminal **16** protrude from the second end surface **12***d* of the encapsulant **12**, and extend parallel to one another along a same direction. The plurality of first signal terminals **18** and the plurality of second signal terminals **19** protrude from the first end surface **12***c* of the encapsulant **12**, and extend parallel to one another along a same direction. The plurality of first signal terminals **18** and the plurality of second signal terminals **19** are respectively connected to, for example, connectors **4** of an external control substrate **2** (see FIG. **5**).

[0038] The first semiconductor chip **20** includes an upper surface electrode **20***a*, a lower surface electrode **20***b*, and a plurality of signal electrodes **20***c*. The upper surface electrode **20***a* and the plurality of signal electrodes **20***c* are positioned at an upper surface of the first semiconductor chip **20**, and the lower surface electrode **20***b* is positioned at a lower surface of the first semiconductor chip **20**. The first semiconductor chip **20** is a vertical-type semiconductor chip including a pair of the upper and lower electrodes **20***a*, **20***b*. The signal electrodes **20***c* are electrodes for inputting and outputting various signals such as a drive signal for the first semiconductor chip **20**, a temperature signal that indicates a temperature of the first semiconductor chip **20**, and a current signal that indicates a current in the first semiconductor chip **20**. Similarly, the second semiconductor chip **40** includes an upper surface electrode **40***a*, a lower surface electrode **40***b*, and a plurality of signal electrodes **40***c*. The upper surface electrode **40***a* and the plurality of signal electrodes **40***c* are positioned at an upper surface of the second semiconductor chip **40**, and the lower surface electrode **40***b* is positioned at a lower surface of the second semiconductor chip **40**. In other words, the second semiconductor chip **40** is also a vertical-type semiconductor chip including a pair of the upper and lower electrodes **40***a*, **40***b*. The first semiconductor chip **20** and the second semiconductor chip **40** in the present embodiment are semiconductor chips of a same type, and specifically are reverse conducting insulated gate bipolar transistor (RC-IGBT) chips each provided with an insulated gate bipolar transistor (IGBT) and a diode therein.

[0039] It should be noted that each of the first semiconductor chip **20** and the second semiconductor chip **40** is not limited to an RC-IGBT chip, and may be another power semiconductor chip such as a metal-oxide-semiconductor field-effect transistor (MOSFET) chip. Alternatively, each of the first semiconductor chip **20** and the second semiconductor chip **40** may be replaced by two or more semiconductor chips such as a diode chip and an IGBT chip (or a MOSFET chip). No particular limitation is imposed on a specific configuration of each of the first semiconductor chip **20** and the second semiconductor chip **40**, and various semiconductor chips can be adopted. In this case, the first semiconductor chip **20** and the second semiconductor chip **40** may be semiconductor chips of different types from each other. Moreover, each of the first semiconductor chip **20** and the second semiconductor chip **40** can be constituted of various semiconductor materials, for example, silicon (S**1**), silicon carbide (SiC), or gallium nitride (GaN). No particular limitation is imposed on materials that constitute the upper surface electrode **20***a* and the lower surface electrode **20***b* of the first semiconductor chip **20**, however, aluminum-based metal or another metal, for example, can be adopted. Similarly, no particular limitation is imposed on materials that constitute the upper surface electrode **40***a* and the lower surface electrode **40***b* of the second semiconductor chip **40**, however, aluminum-based metal or another metal, for example, can be adopted.

[0040] The semiconductor device **10** further includes a first upper heat dissipating plate **22**, a first conductor spacer **24**, and a first lower heat dissipating plate **26**. The first conductor spacer **24** is constituted of an electrically-conductive material, for example, copper or another metal. The first conductor spacer **24** is a member that has a generally plate shape or block shape, and includes an upper surface **24***a* and a lower surface **24***b* positioned opposite to the upper surface **24***a*. The first conductor spacer **24** is positioned in the encapsulant **12**. The upper surface **24***a* of the first conductor spacer **24** is joined to the first upper heat dissipating plate **22** via a solder layer **23**. The lower surface **24***b* of the first conductor spacer **24** is joined to the upper surface electrode **20***a* of the first semiconductor chip **20** via a solder layer **25**. In other words, the first conductor spacer **24** is electrically connected to the first semiconductor chip **20**. The first conductor spacer **24** is not necessarily needed, but ensures a space for connecting the first signal terminals **18** to the first semiconductor chip **20**.

[0041] Each of the first upper heat dissipating plate **22** and the first lower heat dissipating plate **26** is constituted of a material superior in heat conductivity, for example, copper, aluminum, or another metal. The first upper heat dissipating plate **22** is a member that has a generally rectangular parallelepiped shape or plate shape, and includes an upper surface **22***a* and a lower surface **22***b* positioned opposite to the upper surface **22***a*. The upper surface **22***a* of the first upper heat dissipating plate **22** is exposed to the outside at the upper surface **12***a* of the encapsulant **12**. Moreover, the lower surface **22***b* of the first upper heat dissipating plate **22** is joined to the aforementioned upper surface **24***a* of the first conductor spacer **24** via the solder layer **23**. In other words, the first upper heat dissipating plate **22** is electrically and thermally connected to the first semiconductor chip **20** via the first conductor spacer **24**. Thus, the first upper heat dissipating plate **22** configures a part of an electric circuit of the semiconductor device **10** as well as functions as a heat dissipating plate that dissipates heat of the first semiconductor chip **20** to the outside.

[0042] The first lower heat dissipating plate **26** is a member that has a generally rectangular parallelepiped shape or plate shape, and includes an upper surface **26***a* and a lower surface **26***b* positioned opposite to the upper surface **26***a*. The lower surface **26***b* of the first lower heat dissipating plate **26** is exposed to the outside at the lower surface **12***b* of the encapsulant **12**. Moreover, the upper surface **26***a* of the first lower heat dissipating plate **26** is joined to the lower surface electrode **20***b* of the first semiconductor chip **20** via a solder layer **27**. In other words, the first lower heat dissipating plate **26** is electrically and thermally connected to the first semiconductor chip **20**. Thus, the first lower heat dissipating plate **26** also configures a part of the electric circuit of the semiconductor device **10** as well as functions as a heat dissipating plate that dissipates heat of the first semiconductor chip **20** to the outside. As such, the semiconductor device **10** in the present embodiment includes a double-side cooling structure in which the first upper heat

dissipating plate **22** and the first lower heat dissipating plate **26** are exposed at the surfaces **12***a*, **12***b* of the encapsulant **12**, respectively.

[0043] The semiconductor device **10** further includes a second upper heat dissipating plate **42**, a second conductor spacer **44**, and a second lower heat dissipating plate **46**. The second conductor spacer **44** is constituted of an electrically-conductive material, for example, copper or another metal. The second conductor spacer **44** is a member that has a generally plate shape or block shape, and includes an upper surface **44***a* and a lower surface **44***b* positioned opposite to the upper surface **44***a*. The second conductor spacer **44** is positioned in the encapsulant **12**. The upper surface **44***a* of the second conductor spacer **44** is joined to the second upper heat dissipating plate **42** via a solder layer **43**. The lower surface **44***b* of the second conductor spacer **44** is joined to the upper surface electrode **40***a* of the second semiconductor chip **40** via a solder layer **45**. In other words, the second conductor spacer **44** is electrically connected to the second semiconductor chip **40**. The second conductor spacer **44** is not necessarily needed, but ensures a space for connecting the second signal terminals **19** to the second semiconductor chip **40**.

[0044] Each of the second upper heat dissipating plate **42** and the second lower heat dissipating plate **46** is constituted of a material superior in heat conductivity, for example, copper, aluminum, or another metal. The second upper heat dissipating plate **42** is a member that has a generally rectangular parallelepiped shape or plate shape, and includes an upper surface **42***a* and a lower surface **42***b* positioned opposite to the upper surface **42***a*. The upper surface **42***a* of the second upper heat dissipating plate **42** is exposed to the outside at the upper surface **12***a* of the encapsulant **12**. Moreover, the lower surface **42***b* of the second upper heat dissipating plate **42** is joined to the upper surface **44***a* of the aforementioned second conductor spacer **44** via the solder layer **43**. In other words, the second upper heat dissipating plate **42** is electrically and thermally connected to the second semiconductor chip **40** via the second conductor spacer **44**. Thus, the second upper heat dissipating plate **42** configures a part of the electric circuit of the semiconductor device **10** as well as functions as a heat dissipating plate that dissipates heat of the second semiconductor chip **40** to the outside.

[0045] The second lower heat dissipating plate **46** is a member that has a generally rectangular parallelepiped shape or plate shape, and includes an upper surface **46***a* and a lower surface **46***b* positioned opposite to the upper surface **46***a*. The lower surface **46***b* of the second lower heat dissipating plate **46** is exposed to the outside at the lower surface **12***b* of the encapsulant **12**. Moreover, the upper surface **46***a* of the second lower heat dissipating plate **46** is joined to the lower surface electrode **40***b* of the second semiconductor chip **40** via a solder layer **47**. In other words, the second lower heat dissipating plate **46** is electrically and thermally connected to the second semiconductor chip **40**. Thus, the second lower heat dissipating plate **46** also configures a part of the electric circuit of the semiconductor device **10** as well as functions as a heat dissipating plate that dissipates heat of the second semiconductor chip **40** to the outside. As such, the semiconductor device **10** in the present embodiment includes a double-side cooling structure in which the second upper heat dissipating plate **42** and the second lower heat dissipating plate **46** are exposed at the surfaces **12***a*, **12***b* of the encapsulant **12**, respectively. The second lower heat dissipating plate **46** is connected to the first upper heat dissipating plate **22** via a first joint **22***c* and a second joint **46***c*, which will be described later.

[0046] As described above, the semiconductor device **10** includes the P terminal **14**, the N terminal **15**, and the O terminal **16**, as external connection terminals. The P terminal **14**, the N terminal **15**, and the O terminal **16** in the present embodiment are constituted of copper. It should be noted that the material that constitutes the P terminal **14**, the N terminal **15**, and the O terminal **16** is not limited to copper, and may be another conductor. The P terminal **14** is connected to the upper surface **26***a* of the first lower heat dissipating plate **26** inside the encapsulant **12**. The N terminal **15** is connected to the lower surface **42***b* of the second upper heat dissipating plate **42** inside the encapsulant **12**. The O terminal **16** is connected to the upper surface **46***a* of the second lower heat dissipating plate **46**. As an example, the P terminal **14** and the O terminal **16** are configured integrally with the first lower heat dissipating plate **26** and the second lower heat dissipating plate **46**, respectively. It should be noted that one or both of the P terminal **14** and the O terminal **16** may be joined to the first lower heat dissipating plate **26** or/and the second lower heat dissipating plate **46**, respectively, by, for example, welding. Moreover, the N terminal **15** is joined to a third joint **42***c* of the second upper heat dissipating plate **42** by soldering, which will be described later.

[0047] The first signal terminals **18** are connected to the signal electrodes **20***c* of the first semiconductor chip **20** inside the encapsulant **12**, respectively. In the present embodiment, each of the first signal terminals **18** and corresponding one of the signal electrodes **20***c* of the first semiconductor chip **20** are connected via a bonding wire **18***a*. It should be noted that the first signal terminals **18** and the signal electrodes **20***c* may be connected directly without the bonding wires **18***a* or other connecting members interposed therebetween. Similarly, the second signal terminals **19** are connected to the signal electrodes **40***c* of the second semiconductor chip **40** inside the encapsulant **12**, respectively. Each of the second signal terminals **19** and corresponding one of the signal electrodes **40***c* of the second semiconductor chip **40** are also connected via a bonding wire **19***a*. It should be noted that the second signal terminals **19** and the signal electrodes **40***c* may be connected directly without the bonding wires **19***a* or other connecting members interposed therebetween.

[0048] As shown in FIGS. **2** and **3**, the first upper heat dissipating plate **22** of the semiconductor device **10** further includes the first joint **22***c* constituted of a conductor. Similarly, the second lower heat dissipating plate **46** also further includes the second joint **46***c* constituted of a conductor. The first joint **22***c* and the second joint **46***c* are positioned inside the encapsulant **12**. The first joint **22***c* of the first upper heat dissipating plate **22** is joined to the second joint **46***c* of the second lower heat dissipating plate **46** via a solder layer **50**. In other words, the first joint **22***c* and the second joint **46***c* electrically connect the first upper heat dissipating plate **22** and the second lower heat dissipating plate **46** to each other. The first semiconductor chip **20** and the second semiconductor chip **40** are thereby connected in series via the first joint **22***c* and the second joint **46***c*. The first joint **22***c* and the second joint **46***c* can be constituted of, for example, copper. The first joint **22***c* and the first upper heat dissipating plate **22** may be configured integrally or

may be joined to each other. In a case of joining them, no particular limitation is imposed on the joining technique, and they may be joined by welding, for example. Similarly, the second joint **46**c and the second lower heat dissipating plate **46** may be configured integrally or may be joined to each other. In a case of joining them, no particular limitation is imposed on the joining technique, either, and they may be joined by welding, for example.

[0049] The second upper heat dissipating plate **42** of the semiconductor device **10** includes the third joint **42**c constituted of a conductor. The third joint **42**c is positioned inside the encapsulant **12**, and is joined to the N terminal **15** via a solder layer **60** (see FIG. **17**). The second semiconductor chip **40** is thereby electrically connected to the N terminal **15** via the second upper heat dissipating plate **42** and the third joint **42**c. The third joint **42**c can be constituted of, for example, copper. The third joint **42**c and the second upper heat dissipating plate **42** may be configured integrally or may be joined to each other. In a case of joining them, no particular limitation is imposed on the joining technique, and they may be joined by welding, for example.

[0050] As shown in FIGS. **2** and **3**, the lower surface **22**b of the first upper heat dissipating plate **22** is provided with a solder absorbing groove **22**d such that the solder absorbing groove **22**d surrounds the solder layer **23**. This solder absorbing groove **22**d takes in excessive solder when the first conductor spacer **24** and the first upper heat dissipating plate **22** are soldered, by which wetting and spreading of the solder to an unintended range can be prevented. Similarly, the lower surface **42**b of the second upper heat dissipating plate **42** is provided with a solder absorbing groove **42**d such that the solder absorbing groove **42**d surrounds the solder layer **43**. This solder absorbing groove **42**d takes in excessive solder when the second conductor spacer **44** and the second upper heat dissipating plate **42** are soldered, by which wetting and spreading of the solder to an unintended range can be prevented. As an example, the semiconductor device **10** in the present embodiment adopts members having a same shape for the first upper heat dissipating plate **22** and the second upper heat dissipating plate **42**, respectively.

[0051] The first joint **22**c of the first upper heat dissipating plate **22** is also provided with a solder absorbing groove **22**e. The solder absorbing groove **22**e is provided to surround the solder layer **50** positioned between the first joint **22**c and the second joint **46**c. This solder absorbing groove **22**e takes in excessive solder when the first joint **22**c and the second joint **46**c are soldered, by which wetting and spreading of the solder to an unintended range can be prevented. Similarly, the third joint **42**c of the second upper heat dissipating plate **42** is also provided with a solder absorbing groove **42**e. The solder absorbing groove **42**e is provided to surround the solder layer **60** (see FIG. **17**) positioned between the third joint **42**c and the N terminal **15**. This solder absorbing groove **42**e takes in excessive solder when the third joint **42**c of the second upper heat dissipating plate **42** and the N terminal **15** are soldered, by which wetting and spreading of the solder to an unintended range can be prevented.

[0052] Next, details of the first signal terminals **18** and the second signal terminals **19** will be described. As shown in FIG. **5**, each of the first signal terminals **18** includes a displaced section **18**x which is bent inside the encapsulant **12** and displaced toward the first semiconductor chip **20**. In the displaced sections **18**x, the first signal terminals **18** extend farther away from the second signal terminals **19** along a direction toward the first semiconductor chip **20**. Similarly, each of the second signal terminals **19** includes a displaced section **19**x which is bent inside the encapsulant **12** and displaced toward the second semiconductor chip **40**. In the displaced sections **19**x, the second signal terminals **19** extend farther away from the first signal terminals **18** along a direction toward the second semiconductor chip **40**.

[0053] According to the above configuration, a distance D**1** between the plurality of first signal terminals **18** and the plurality of second signal terminals **19** can be made small outside the encapsulant **12**, and additionally, the first signal terminals **18** and the second signal terminals **19** can be made close to the first semiconductor chip **20** and the second semiconductor chip **40**, respectively, inside the encapsulant **12**. As described before, the plurality of first signal terminals **18** and the plurality of second signal terminals **19** are connected to the connectors **4** of the external control substrate **2**. Therefore, when the distance D**1** between the plurality of first signal terminals **18** and the plurality of second signal terminals **19** is small outside the encapsulant **12**, increase in the size of the control substrate **2** to which the plurality of first signal terminals **18** and the plurality of second signal terminals **19** are connected can be avoided.

[0054] Meanwhile, since the first signal terminals **18** are made close to the first semiconductor chip **20** inside the encapsulant **12**, the bonding wires **18**a (or other connecting members) that connect the first signal terminals **18** and the first semiconductor chip **20** can be shortened. Alternatively, the first signal terminals **18** and the first semiconductor chip **20** can also be connected directly without the bonding wires **18**a interposed therebetween. Similarly, the bonding wires **19**a (or other connecting members) that connect the second signal terminals **19** and the second semiconductor chip **40** can also be shortened or omitted.

[0055] Additionally, the semiconductor device **10** in the present embodiment includes a suspended terminal **13** adjacent to the plurality of first signal terminals **18**, and another suspended terminal **17** adjacent to the plurality of second signal terminals **19**. One of the terminals, namely, the suspended terminal **13** is connected to the first lower heat dissipating plate **26**, and thus needs to be electrically insulated from the first signal terminals **18**. Similarly, the other of the terminals, namely, the suspended terminal **17** is connected to the second lower heat dissipating plate **46**, and thus needs to be electrically insulated from the second signal terminals **19**. In this respect, when the distance D**1** between the plurality of first signal terminals **18** and the plurality of second signal terminals **19** is small, a distance D**2** between the plurality of first signal terminals **18** and the suspended terminal **13** and a distance D**3** between the plurality of second signal terminals **19** and the suspended terminal **17** can be made large. Due to this, an insulating property between the plurality of first signal terminals **18** and the suspended terminal **13**, and an insulating property between the plurality of second signal terminals **19** and the suspended terminal **17** can be enhanced. A recess **12**e is provided in the encapsulant **12** between the plurality of first signal terminals **18** and the suspended terminal **13** to increase a creepage distance therebetween. Similarly, a recess **12**f is provided in the encapsulant **12** between the plurality of second signal terminals **19** and the suspended terminal **17** to increase a creepage distance therebetween.

[0056] In the semiconductor device **10** in the present embodiment, each of the first signal terminals **18** and the

second signal terminals **19** extends linearly outside the encapsulant **12**. According to such a configuration, deformation of the first signal terminals **18** and the second signal terminals **19** can be avoided when the first signal terminals **18** and the second signal terminals **19** are connected to, for example, the connectors **4** of the control substrate **2**. It should be noted that one or more of the first signal terminals **18** and/or one or more of the second signal terminals **19** may be bent outside the encapsulant **12** in another embodiment.

[0057] In the semiconductor device **10** in the present embodiment, each of the first signal terminals **18** and the second signal terminals **19** includes, inside the encapsulant **12**, a crank shape including two bends with corresponding one of the displaced sections **18***x*, **19***x* interposed therebetween. According to such a configuration, the first signal terminals **18** and the second signal terminals **19** can be fixed firmly to the encapsulant **12**. It should be noted that, as shown in FIG. **6**, each of the first signal terminals **18** and the second signal terminals **19** only needs to include at least corresponding one of the displaced sections **18***x*, **19***x*, and may not necessarily include a crank shape, in another embodiment. In the example shown in FIG. **6**, each of the first signal terminals **18** and the second signal terminals **19** includes corresponding one of the displaced sections **18***x*. **19***x* that extend to tips of the signal terminals **18**, **19**.

[0058] As shown in FIG. **7**, at least one of the first signal terminals **18** and/or at least one of the second signal terminals **19** may be provided with, inside the encapsulant **12**, a notch **18***c* and/or a notch **19***c*. According to such a configuration, a part of the encapsulant **12** enters the notch **18***c* and/or the notch **19***c*, by which the first signal terminals **18** and/or the second signal terminals **19** are fixed more firmly to the encapsulant **12**. It should be noted that, in the semiconductor device **10** in the present embodiment, since the first signal terminals **18** and the second signal terminals **19** include the displaced sections **18***x*, **19***x*, respectively, they are fixed firmly to the encapsulant **12**. Therefore, the first signal terminals **18** and the second signal terminals **19** are not necessarily provided with the notches **18***c*, **19***c*. Omission of the notches **18***c*, **19***c* can, for example, reduce impedance of the first signal terminals **18** and the second signal terminals **19**.

[0059] In the semiconductor device **10** in the present embodiment, the first signal terminals **18** and the second signal terminals **19** comprise plane-symmetrical shapes to each other. According to such a configuration, designing and manufacturing of the semiconductor device **10** can be facilitated. Moreover, local generation of high stress (i.e., stress concentration) in the semiconductor device **10** can be suppressed by having the structural symmetry.

[0060] In the semiconductor device **10** in the present embodiment, each of the first signal terminals **18** and the second signal terminals **19** comprises a plate shape and is bent in a direction of thickness of corresponding one of the first and second signal terminals **18**, **19** inside the encapsulant **12**. According to such a configuration, the first signal terminals **18** and the second signal terminals **19** can be fixed more firmly to the encapsulant **12**. It should be noted that, as shown in FIG. **8**, one or more of the first signal terminals **18** and/or one or more of the second signal terminals **19** may not be bent in the direction of thickness of the first signal terminals **18** and/or the second signal terminals **19** inside the encapsulant **12** in another embodiment. In other words, one or more of the first signal terminals **18** and/or one or more of the second signal terminals **19** may be flat inside the encapsulant **12**.

[0061] (Variants Related to Solder Absorbing Grooves **22***d*, **42***d*)

[0062] As described before, the lower surface **22***b* of the first upper heat dissipating plate **22** is provided with the solder absorbing groove **22***d* such that the solder absorbing groove **22***d* surrounds the solder layer **23**. This solder absorbing groove **22***d* takes in excessive solder when the first conductor spacer **24** and the first upper heat dissipating plate **22** are soldered, by which wetting and spreading of the solder to an unintended range can be prevented. However, the amount of excessive solder varies among semiconductor devices, and hence when the amount of excessive solder is relatively small, for example, the excessive solder is taken in only in a section of the solder absorbing groove **22***d*. In this case, a part of a periphery of the solder layer **23** is positioned inside the solder absorbing groove **22***d*, whereas another part of the periphery of the solder layer **23** is positioned outside the solder absorbing groove **22***d*, which results in significantly different contact angles of the solder (fillet shapes of the solder) between these parts.

[0063] Here, when solder melts between two members, adsorption force caused by surface tension of the molten solder acts between the two members. A magnitude of this adsorption force varies in accordance with a contact angle of the solder. Therefore, in a state where excessive solder is taken in only in a section of the solder absorbing groove **22***d*, adsorption force that acts between the first conductor spacer **24** and the first upper heat dissipating plate **22** is caused unevenly. Consequently, relative positions and orientations between the first conductor spacer **24** and the first upper heat dissipating plate **22** may change, and dimensional accuracy of the semiconductor device **10** may decrease. In particular, if the solder contact angles (i.e., generated adsorption force) are different from each other in opposing two sides of the periphery of the solder layer **23**, relative positions and orientations of the two members are likely to change, and dimensional accuracy of the semiconductor device **10** is likely to decrease.

[0064] With respect to the above problem, the solder absorbing groove **22***d* can adopt a configuration described below. As shown in FIG. **9**, a region of the lower surface **22***b* of the first upper heat dissipating plate **22**, which is in contact with the solder layer **23** inserted between the lower surface **22***b* and the first conductor spacer **24**, is herein referred to as a first solder joint area S**1**. In this case, in a periphery of the first solder joint area S**1**, two sides **52**, **56** opposite to each other in a first direction (in a right-left direction in FIG. **9**) may be positioned inside the solder absorbing groove **22***d*, and additionally, other two sides **54**, **58** opposite to each other in a second direction (in an up-down direction in FIG. **9**) may be positioned outside the solder absorbing groove **22***d*. As an example, the first direction and the second direction may be orthogonal to each other.

[0065] As shown in FIG. **10**, according to the above configuration, a position where excessive solder is taken in in the solder absorbing groove **22***d* when the first upper heat dissipating plate **22** and the first conductor spacer **24** are soldered is restricted to the two opposite sides **52**, **56** of the first solder joint area S**1**. By restricting the position where excessive solder flows into the solder absorbing groove **22***d*

to a part of the periphery of the first solder joint area **S1**, the excessive solder is uniformly taken in in the solder absorbing groove **22***d* at the two sides **52**, **56** and contact angles of the solder **23** become approximately equal there, even if the amount of excessive solder fluctuates by a certain degree. Meanwhile, since the other two opposite sides **54**, **58** of the first solder joint area S**1** are positioned outside the solder absorbing groove **22***d*, contact angles of the solder **23** become approximately equal there.

[0066] The contact angles of the solder **23** become approximately equal at each pair of the two opposite sides (**52** and **56**, **54** and **58**) of the first solder joint area S**1**, so changes in relative positions and orientations between the first upper heat dissipating plate **22** and the first conductor spacer **24** are suppressed, and dimensional accuracy of the semiconductor device **10** is improved. The solder **23** at a manufacturing stage is to constitute the aforementioned solder layer **23** in the semiconductor device **10**, and hence they are herein assigned the same sign. Moreover, as shown in FIG. **10**, when the first upper heat dissipating plate **22** and the first conductor spacer **24** are soldered, a jig J may be utilized as needed. The aforementioned configuration relevant to the solder absorbing groove **22***d* can also be adopted for the solder absorbing groove **42***d* in the second upper heat dissipating plate **42**.

[0067] The configurations of the solder absorbing grooves **22***d*, **42***d* can be modified variously. For example, as shown in FIG. **11**, the lower surface **22***b* of the first upper heat dissipating plate **22** may be provided with two solder absorbing grooves **22***d* opposite to each other in the first direction, along the periphery of the first solder joint area S**1**. In other words, the solder absorbing groove **22***d* may not be provided in an annular shape. In this case as well, the two sides **52**, **56** opposite to each other in the first direction are positioned inside the solder absorbing grooves **22***d*, whereas the other two sides **54**, **58** opposite to each other in the second direction are positioned outside the solder absorbing grooves **22***d*, in the periphery of the first solder joint area S**1**.

[0068] Alternatively, as shown in FIG. **12**, the solder absorbing groove **22***d* may have different widths or different cross-sectional areas between at a pair of two opposing sections and at another pair of two opposing sections. Specifically, the width at two sections opposite to each other in the second direction may be made sufficiently smaller than the width at two sections opposite to each other in the first direction. Due to this, the cross-sectional area at the two sections opposite to each other in the second direction is reduced to a degree by which these two sections cannot take in excessive solder sufficiently. According to such a configuration, when the first upper heat dissipating plate **22** and the first conductor spacer **24** are soldered, the two sides **54**, **58** of the first solder joint area S**1**, which are opposite to each other in the second direction, cross over the solder absorbing groove **22***d* and are positioned outside the solder absorbing groove **22***d*. On the other hand, the two sides **52**, **56** of the first solder joint area S**1**, which are opposite to each other in the first direction, are positioned inside the solder absorbing groove **22***d*. In other words, with the configuration shown in FIG. **12** as well, the two sides **52**, **56** opposite to each other in the first direction are positioned inside the solder absorbing groove **22***d*, and the other two sides **54**, **58** opposite to each other in the second direction are positioned outside the solder absorbing groove **22***d*, in the periphery of the first solder joint area S**1**. The solder absorbing groove **22***d* may not be provided in an annular shape, and may be divided into, for example, the four sections mentioned above.

[0069] (Variant Related to Solder Absorbing Groove **22***e*)

[0070] As mentioned before, the first joint **22***c* of the first upper heat dissipating plate **22** and the second joint **46***c* of the second lower heat dissipating plate **46** are joined to each other via the solder layer **50**. The first joint **22***c* of the first upper heat dissipating plate **22** is provided with the solder absorbing groove **22***e* such that the solder absorbing groove **22***e* surrounds the solder layer **50**. When the first joint **22***c* of the first upper heat dissipating plate **22** and the second joint **46***c* of the second lower heat dissipating plate **46** are soldered to each other, adsorption force acts between the two joints **22***c*, **46***c*, due to surface tension of the molten solder. Here, the first joint **22***c* of the first upper heat dissipating plate **22** is positioned apart from a center of gravity of the first upper heat dissipating plate **22**, so the adsorption force that acts on the first joint **22***c* is likely to change the position and orientation of the first upper heat dissipating plate **22**. The same applies to the second lower heat dissipating plate **46**. As such, in a case of soldering two members to each other, if adsorption force caused by surface tension of the molten solder acts on a position apart from a center of gravity of at least one of the members, the relative positions and orientations of the two members are likely to change, and dimensional accuracy of the product may be decreased.

[0071] With respect to the above problem, the solder absorbing groove **22***e* in the first joint **22***c* can adopt a configuration described below. As shown in FIGS. **13** and **14**, a region of the first joint **22***c* of the first upper heat dissipating plate **22**, which is in contact with the solder layer **50**, is referred to as a second solder joint area S**2**, and a region of the second joint **46***c* of the second lower heat dissipating plate **46**, which is in contact with the solder layer **50**, is referred to as a third solder joint area S**3**. In this case, an inner periphery E of the solder absorbing groove **22***e* may be positioned outside the third solder joint area S**3** in a plan view (see FIG. **13**). In other words, the solder absorbing groove **22***e* in the first joint **22***c* may be provided such that an area of the second solder joint area S**2** in the first joint **22***c* is larger than an area of the third solder joint area S**3** in the second joint **46***c*. The plan view herein means observation along a direction vertical to the solder layer **50** that joins the first joint **22***c* and the second joint **46***c* to each other.

[0072] As shown in FIG. **15**, according to the above configuration, at the manufacturing stage of the semiconductor device **10**, a contact angle θ of the molten solder **50** relative to the second solder joint area S**2** becomes sufficiently larger than 90 degrees when the first joint **22***c* and the second joint **46***c* are soldered. As described before, when the solder **50** melts between the first joint **22***c* and the second joint **46***c*, adsorption force acts between the first joint **22***c* and the second joint **46***c*, due to surface tension F of the molten solder **50**. A magnitude of this adsorption force varies in accordance with the contact angle θ. In a range where the contact angle θ exceeds 90 degrees, the adsorption force becomes smaller with larger contact angle θ. With the small adsorption force that acts on the first joint **22***c* and the second joint **46***c*, changes in relative positions and orientations between the first upper heat dissipating plate **22** and the second joint **46***c* of the second lower heat dissipating plate **46** can be suppressed, and dimensional accuracy of the semiconductor device **10** can be improved. Here, the solder

50 at the manufacturing stage is to constitute the solder layer **50** in the semiconductor device **10**, and hence they are herein assigned the same sign.

[0073] (Variant Related to Second Upper Heat Dissipating Plate **42**)

[0074] In the semiconductor device **10** in the present embodiment, the second conductor spacer **44** and the N terminal **15** are soldered to the second upper heat dissipating plate **42**. FIG. **16** is a diagram of the second upper heat dissipating plate **42** in a plan view, and shows a fourth solder joint area S**4** and a fifth solder joint area S**5** of the second upper heat dissipating plate **42**. The fourth solder joint area S**4** is a range to which the second conductor spacer **44** is soldered, and is a range with which the solder layer **43** positioned between the second conductor spacer **44** and the second upper heat dissipating plate **42** is in contact. The fifth solder joint area S**5** is a range to which the N terminal **15** is soldered, and is a range with which the solder layer **60** positioned between the N terminal **15** and the second upper heat dissipating plate **42** is in contact. Here, a center of gravity **42***g* of the second upper heat dissipating plate **42** is positioned in a range S**6** that links the fourth solder joint area S**4** and the fifth solder joint area S**5** in the plan view. This range S**6** is a range positioned between the fourth solder joint area S**4** and the fifth solder joint area S**5**, and does not include the fourth solder joint area S**4** or the fifth solder joint area S**5**.

[0075] As shown in FIG. **17**, according to the above structure, the second conductor spacer **44** and the N terminal **15** can be simultaneously soldered to the second upper heat dissipating plate **42** when the semiconductor device **10** is manufactured. At this time, surface tensions F**1**. F**2** of the molten solder **43**, **60** act on the fourth solder joint area S**4** and the fifth solder joint area S**5**, respectively, in the second upper heat dissipating plate **42**. When external forces such as the surface tensions F**1**, F**2** act on two areas in the single second upper heat dissipating plate **42**, the position and orientation of the second upper heat dissipating plate **42** are likely to change, and dimensional accuracy of the semiconductor device **10** may be decreased. In particular, when the two surface tensions F**1**. F**2** act on the second upper heat dissipating plate **42** in an unbalanced manner with respect to the center of gravity **42***g*, the orientation of the second upper heat dissipating plate **42** is likely to change (i.e., is likely to tilt). In this respect, as described before, the semiconductor device **10** in the present embodiment has the center of gravity **42***g* of the second upper heat dissipating plate **42** positioned in the range S**6** that links the fourth solder joint area S**4** and the fifth solder joint area S**5** in the plan view. According to such a configuration, the surface tensions F**1**, F**2** of the molten solder respectively act on both sides relative to the center of gravity **42***g* of the second upper heat dissipating plate **42**, so changes in position and especially in orientation of the second upper heat dissipating plate **42** are suppressed. Consequently, dimensional accuracy of the semiconductor device **10** can be improved.

[0076] (Variants Related to Suspended Terminals **13**, **17**)

[0077] As described before, the semiconductor device **10** in the present embodiment includes the suspended terminals **13**, **17** (see FIG. **5**). Moreover, the encapsulant **12** is provided with the recesses **12***e*, **12***f* adjacent to the suspended terminals **13**, **17**, respectively. When the semiconductor device **10** operates and the semiconductor chips **20**, **40** generate heat, the encapsulant **12** thermally expands. At this time, stress is likely to locally increase at positions of the recesses **12***e*, **12***f*, so cracks may occur there.

[0078] With respect to the above problem, as shown in FIG. **18**, the suspended terminal **13** may have its width dimension W**2** increased at its base end inside the encapsulant **12**. According to such a configuration, the suspended terminal **13** is less likely to be displaced relative to the first lower heat dissipating plate **26** (i.e., increases its rigidity), and the thermal expansion of the encapsulant **12** is suppressed by the suspended terminal **13**. The stress generated in the encapsulant **12** is thereby mitigated at the recess **12***e* adjacent to the suspended terminal **13**, and generation of cracks at the recess **12***e* can be suppressed. Similarly, the other of the suspended terminals, namely, the suspended terminal **17** may also have its width dimension increased at its proximal end. The stress generated at the other of the recesses, namely, the recess **12***f* is thereby also mitigated.

[0079] As an example, in the example shown in FIG. **18**, the suspended terminal **13** includes a first section SC**1** that extends from the first lower heat dissipating plate **26** and a second section SC**2** that extends from the first section SC**1**. The first section SC**1** is a section provided inside the encapsulant **12**, and the second section SC**2** is a section that extends over the inside and the outside of the encapsulant **12**. The first section SC**1** has a width dimension W**1** larger than the width dimension W**2** of the second section SC**2**. In the first section SC**1**, the width dimension of the suspended terminal **13** gradually increases from W**2** to W**1** toward the first lower heat dissipating plate **26**. A similar configuration hereto can also be adopted for the other of the terminals, namely, the suspended terminal **17**, and the stress generated at the other of the recesses, namely, the recess **12***f* is also mitigated thereby.

[0080] The base end E**1** of the suspended terminal **13** may be positioned within a range formed by extending the recess **12***e* in its depth direction, but no particular limitation is imposed thereto. In other words, when a phantom line L**1** extends from an end E**3** of the recess **12***e* that is positioned on a suspended terminal **13** side along the depth direction of the recess **12***e*, the phantom line L**1** may intersect with the first section SC**1** of the suspended terminal **13**. According to such a configuration, the base end E**1** of the suspended terminal **13** is positioned in proximity to the recess **12***e*, so generation of cracks at the recess **12***e* in the encapsulant **12** can be effectively suppressed. On the other hand, when a phantom line L**2** extends from a center C**1** of the recess **12***e* along the depth direction of the recess **12***e*, the phantom line L**2** may not intersect with the first section SC**1** of the suspended terminal **13**. In another embodiment, however, the first section SC**1** of the suspended terminal **13** may be further enlarged to a position at which the first section SC**1** intersects with the phantom line L**2** extending from the center C**1** of the recess **12***e*. The shape of the first section SC**1** is not limited to the shapes described herein, and can be modified as appropriate.

[0081] When the semiconductor chips **20**, **40** generate heat during use of the semiconductor device **10**, the encapsulant **12** thermally expands mainly in a longitudinal direction of the encapsulant **12** (in a right-left direction in FIG. **1**). In this respect, the suspended terminals **13**, **17** extend vertically relative to the longitudinal direction of the encapsulant **12**, and thus the thermal expansion of the encapsulant **12** can effectively be suppressed by the suspended terminals **13**, **17**.

[0082] The structures of the suspended terminals **13**, **17** can be modified variously. FIG. **19** shows some variants of the suspended terminal **13**. Structures shown in FIGS. **19**(A) to **19**(E) can also be adopted for the other of the suspended terminals, namely, the suspended terminal **17**. In the suspended terminal **13** shown in FIG. **19**(A), the width dimension W**1** of the suspended terminal **13** at the base end E**1** is further increased such that when the phantom line L**2** extends from the center C of the recess **12***e* along the depth direction of the recess **12***e*, the phantom line L**2** intersects with the first section SC**1** of the suspended terminal **13**. According to such a configuration, the suspended terminal **13** is in contact with the encapsulant **12** by a larger area, and thus the thermal expansion of the encapsulant **12** can further be suppressed by the suspended terminal **13**. Due to this, the thermal expansion of the encapsulant **12** caused by heat generated in the semiconductor chips **20**, **40** is further suppressed, and the stress generated at the recess **12***e* can further be mitigated.

[0083] In the suspended terminal **13** shown in FIG. **19**(B), one lateral edge **13***b* of lateral edges of the suspended terminal **13** is curved in the first section SC**1**. According to such a configuration, stress concentration in the encapsulant **12** that is in contact with the lateral edge **13***b* of the suspended terminal **13** is mitigated, and the stress generated at the recess **12***e* positioned in proximity thereto can further be mitigated. In the suspended terminal **13** shown in FIG. **19**(C), the phantom line L**2**, which extends from the center C**1** of the recess **12***e* along the depth direction of the recess **12***e*, intersects with the first section SC**1** of the suspended terminal **13**. Furthermore, the one lateral edge **13***b* of the suspended terminal **13** is curved in the first section SC**1**. In other words, the suspended terminal **13** shown in FIG. **19**(C) includes both of the features of the suspended terminals **13** shown in FIGS. **19**(A) and **19**(B), and can effectively mitigate the stress generated at the recess **12***e*.

[0084] In the suspended terminal **13** shown in FIG. **19**(D), the width dimensions W**1**, W**2** of the suspended terminal **13** change discontinuously between the first section SC**1** and the second section SC**2**, and the width dimension W**1** in the first section SC**1** is constant. According to such a configuration, the suspended terminal **13** is in contact with the encapsulant **12** by a larger area, and thus the thermal expansion of the encapsulant **12** is further suppressed by the suspended terminal **13**. Due to this, the thermal expansion of the encapsulant **12** caused by heat generated in the semiconductor chips **20**, **40** is further suppressed, and the stress generated at the recess **12***e* can further be mitigated. In the suspended terminal **13** shown in FIG. **19**(E), the width dimension W**1** of the suspended terminal **13** in the first section SC**1** is increased toward an opposite side from the recess **12***e* (i.e., toward the left side in the figure). According to such a configuration, the width dimension W**1** of the suspended terminal **13** in the first section SC**1** can further be increased, without interfering with the recess **12***e* or the first signal terminals **18**. The suspended terminal **13** is thereby less likely to be displaced (i.e., enhances its rigidity), and thus the stress generated at the recess **12***e* can further be mitigated. Here, a part of the first section SC**1** of the suspended terminal **13** may be positioned outside the encapsulant **12**.

[0085] (Variant Related to N Terminal **15**)

[0086] As described before, in the semiconductor device **10** in the present embodiment, the N terminal **15** is joined to the third joint **42***c* of the second upper heat dissipating plate **42** via the solder layer **60**. In other words, at the manufacturing stage of the semiconductor device **10**, soldering is performed for the N terminal **15** and the third joint **42***c* of the second upper heat dissipating plate **42**. In this soldering, the molten solder layer **60** needs to be prevented from unintentionally spreading over a wide range in the N terminal **15** and the third joint **42***c*. With respect to this problem, the N terminal **15** can adopt a configuration described below.

[0087] As shown in FIGS. **20** and **21**, the N terminal **15** may include a bend **15***a* that bends in its thickness direction at a boundary B between a joint area S**7** that is in contact with the solder layer **60** and a non-joint area S**8** adjacent to the joint area S**7**. According to such a configuration, wetting and spreading of the solder layer **60**, which has fluidity, beyond the bend **15***a* is suppressed at the manufacturing stage of the semiconductor device **10**. Due to this, excessive wetting and spreading of the solder layer **60** beyond the intended boundary B between the joint area S**7** and the non-joint area S**8** can be suppressed.

[0088] The bend **15***a* can be formed easily by bending and the like at the manufacturing stage of the semiconductor device **10**. Therefore, the boundary B of the joint area S**7** in the N terminal **15** can be changed easily by changing the position where the bend **15***a* is formed. Therefore, by making the joint area S**7** correspond to the shape of the third joint **42***c* of the second upper heat dissipating plate **42** (or the position of the solder absorbing groove **42***e*), a joint area between the second upper heat dissipating plate **42** and the N terminal **15** can be maximized. Due to this, the bend **15***a* of the N terminal **15** and the third joint **42***c* of the second upper heat dissipating plate **42** further suppress wetting and spreading of the solder layer **60** at the manufacturing stage. The technology described here is not limited to the N terminal **15**, and can also be adopted for a power terminal of another type (or with another application purpose).

[0089] The N terminal **15** may include a thick-plate section and a thin-plate section, although no particular limitation is imposed thereto. As shown in FIG. **21**, the thick-plate section has a thickness dimension t**1** larger than a thickness dimension t**2** of the thin-plate section. In this case, the bend **15***a* may be positioned in the thin-plate section. The bend **15***a* positioned in the thin-plate section enables easy formation of the bend **15***a* by bending and the like. Therefore, even if the position of the solder absorbing groove **42***e* is changed, for example, the position of the bend **15***a* in the N terminal **15** can be easily made to correspond to the changed position of the solder absorbing groove **42***e*. Due to this, the joint area between the second upper heat dissipating plate **42** and the N terminal **15** can be maximized easily.

[0090] A larger joint area between the second upper heat dissipating plate **42** and the N terminal **15** causes larger thermal stress generated in the N terminal **15** when the first semiconductor chip **20** generates heat. In this respect, with the bend **15***a* provided at the N terminal **15**, the thermal stress can be mitigated by the bend **15***a*. Therefore, even if the joint area between the second upper heat dissipating plate **42** and the N terminal **15** is maximized, a decrease in reliability of the semiconductor device **10** can be prevented.

[0091] As described above, the joint area with the solder layer **60** (i.e., the area of the joint area S**7**) can be adjusted by changing the position of the bend **15***a* in the N terminal **15**. Here, a larger joint area with the solder layer **60** makes the position of the bend **15***a* closer to an outer surface of the

encapsulant **12** (i.e., the outside of the encapsulant **12**) along a longitudinal direction of the N terminal **15**. In this case, a distance from the outer surface of the encapsulant **12** to the joint portion with the solder layer **60** is shorter, so vibrations externally applied to the N terminal **15** are likely to be transferred to the joint portion with the solder layer **60**. When the external vibrations are likely to be transferred to the joint portion with the solder layer **60**, there may be a risk of a decrease in reliability, for example, generation of cracks in the solder layer **60**. However, with the bend **15***a* provided at the N terminal **15**, the vibrations can be mitigated by the bend **15***a*. Therefore, by providing the bend **15***a* at the N terminal **15**, the decrease in reliability of the semiconductor device **10** can be prevented, while increasing the joint area with the solder layer **60**.

1. A semiconductor device comprising:
- a first semiconductor chip and a second semiconductor chip;
- an encapsulant encapsulating the first semiconductor chip and the second semiconductor chip;
- a first signal terminal extending over inside and outside of the encapsulant and connected to the first semiconductor chip inside the encapsulant; and
- a second signal terminal extending over the inside and the outside of the encapsulant and connected to the second semiconductor chip inside the encapsulant,
- wherein
- the first signal terminal and the second signal terminal protrude from the encapsulant in a same direction,
- the first signal terminal comprises, inside the encapsulant, a section where the first signal terminal extends farther away from the second signal terminal along a direction toward the first semiconductor chip,
- the second signal terminal comprises, inside the encapsulant, a section where the second signal terminal extends farther away from the first signal terminal along a direction toward the second semiconductor chip.

2. The semiconductor device according to claim **1**, wherein at least one of the first signal terminal and the second signal terminal extends linearly outside the encapsulant

3. The semiconductor device according to claim **1**, wherein at least one of the first signal terminal and the second signal terminal comprises, inside the encapsulant, a crank shape that includes at least two bends.

4. The semiconductor device according to claim **1**, wherein the first signal terminal and the second signal terminal comprise plane-symmetrical shapes to each other.

5. The semiconductor device according to claim **1**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

6. The semiconductor device according to **2**, wherein at least one of the first signal terminal and the second signal terminal comprises, inside the encapsulant, a crank shape that includes at least two bends.

7. The semiconductor device according to claim **2**, wherein the first signal terminal and the second signal terminal comprise plane-symmetrical shapes to each other.

8. The semiconductor device according to claim **3**, wherein the first signal terminal and the second signal terminal comprise plane-symmetrical shapes to each other.

9. The semiconductor device according to claim **6**, wherein the first signal terminal and the second signal terminal comprise plane-symmetrical shapes to each other.

10. The semiconductor device according to claim **2**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

11. The semiconductor device according to claim **3**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

12. The semiconductor device according to claim **4**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

13. The semiconductor device according to claim **6**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

14. The semiconductor device according to claim **7**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

15. The semiconductor device according to claim **8**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

16. The semiconductor device according to claim **9**, wherein at least one of the first signal terminal and the second signal terminal comprises a plate shape and is bent in a direction of thickness of the at least one of the first and second signal terminals inside the encapsulant.

* * * * *