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(54) **METHOD OF FORMING LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTOR WITH PARTIALLY UNSILICIDED SOURCE/DRAIN**

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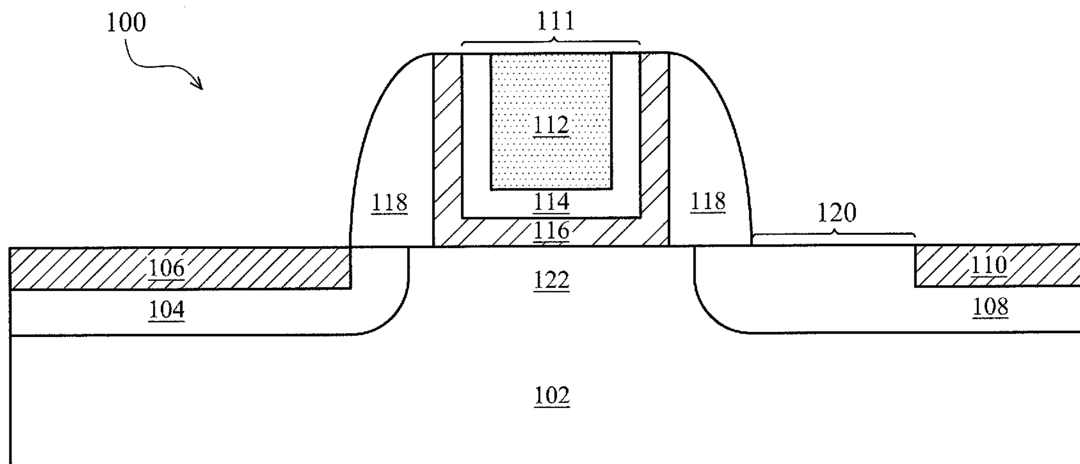
(57) **ABSTRACT**

A method of forming a semiconductor device comprises forming a gate over a substrate. The method also comprises forming a source and a drain on opposite sides of the gate. The source and the drain are formed such that the source and the drain are separated by a channel region beneath the gate. The source and the drain are positioned such that the channel region has a channel width with respect to a surface of the substrate greater than a width of the gate with respect to the surface of the substrate. The method further comprises forming a first silicide over a portion of the source. The method additionally comprises forming a second silicide over a portion of the drain such that the drain has an unsilicided region adjacent to the gate configured to provide a resistive region configured to sustain a voltage load in a high voltage laterally diffused metal oxide semiconductor (LDMOS) application.



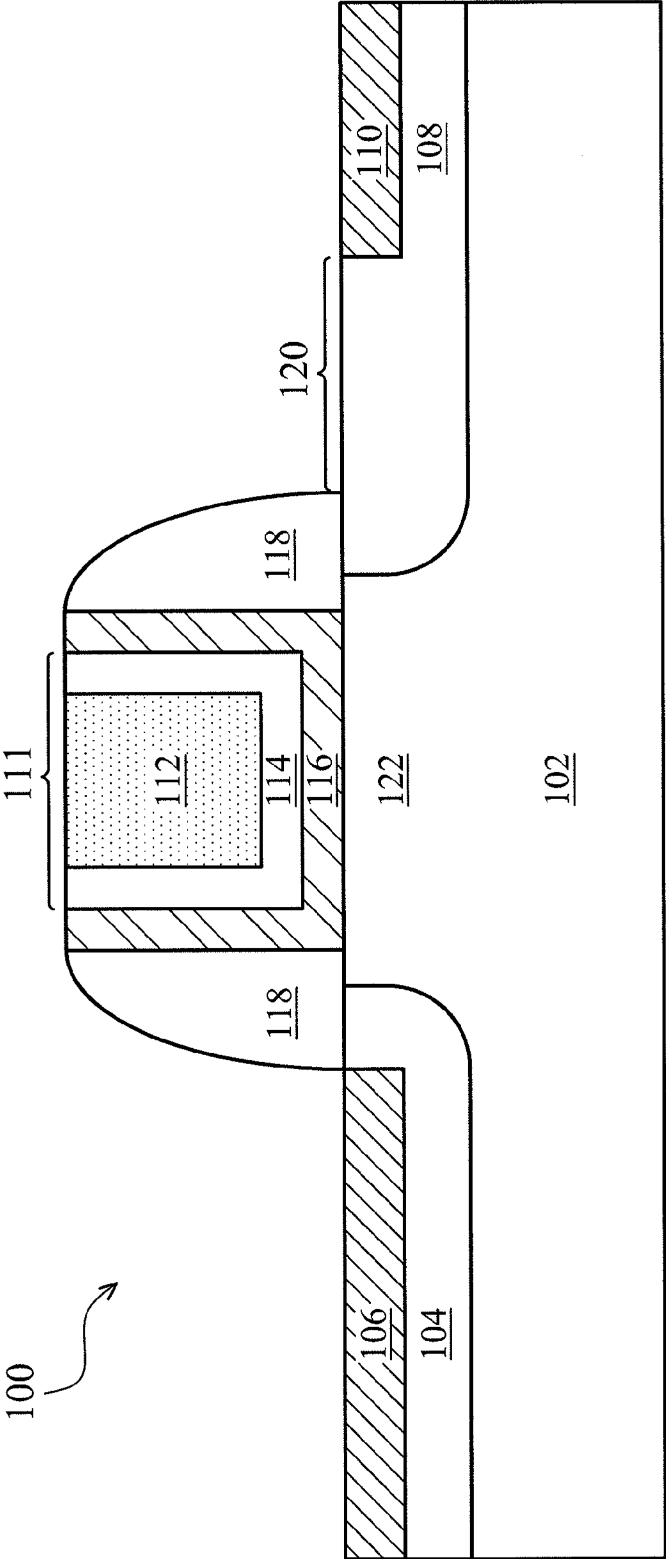


Fig. 1

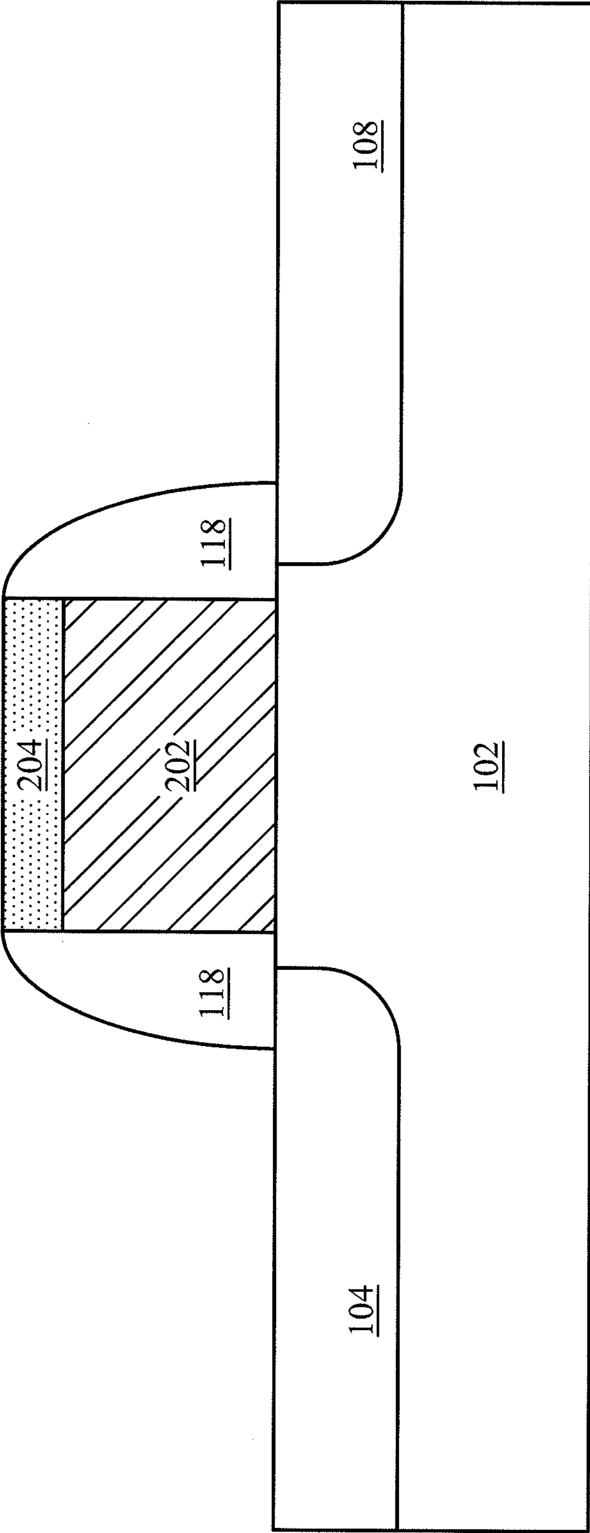


Fig. 2

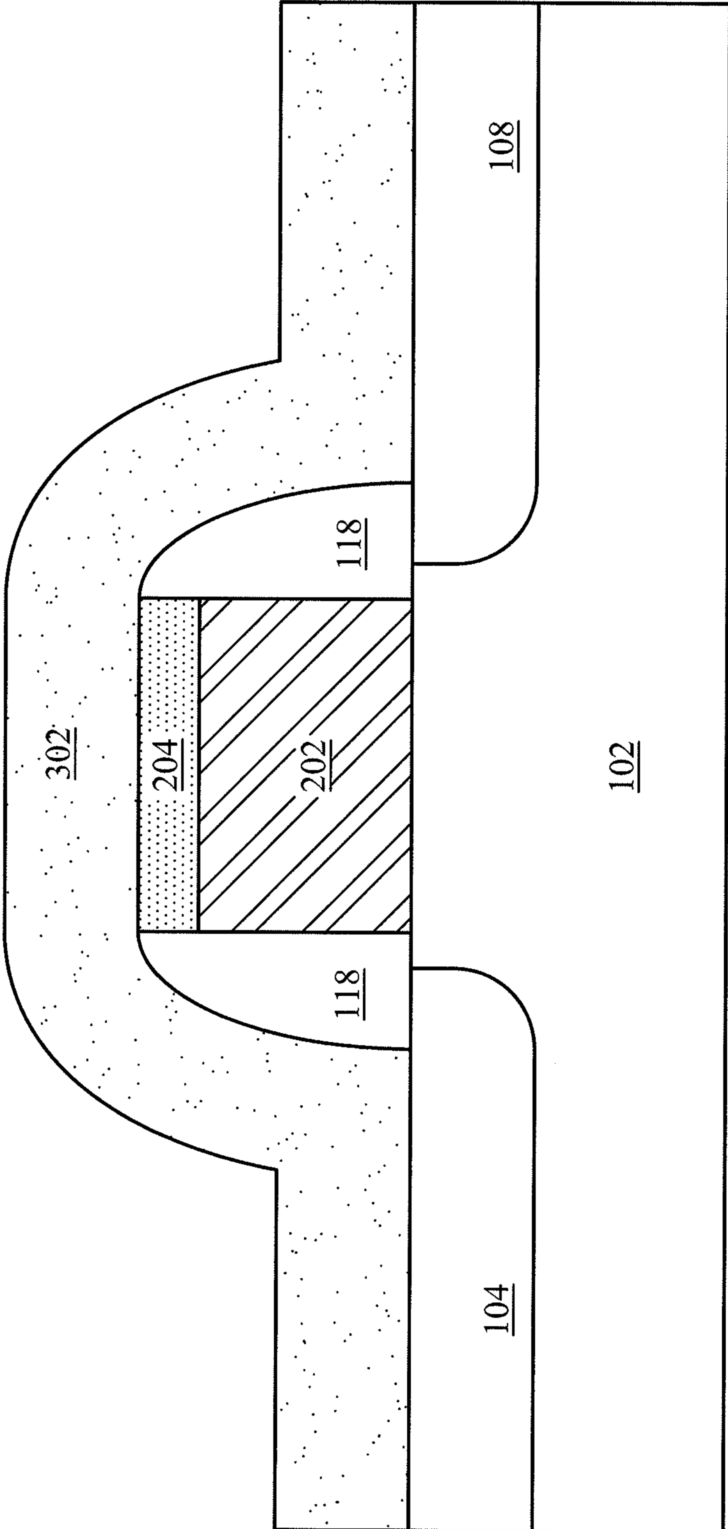


Fig. 3

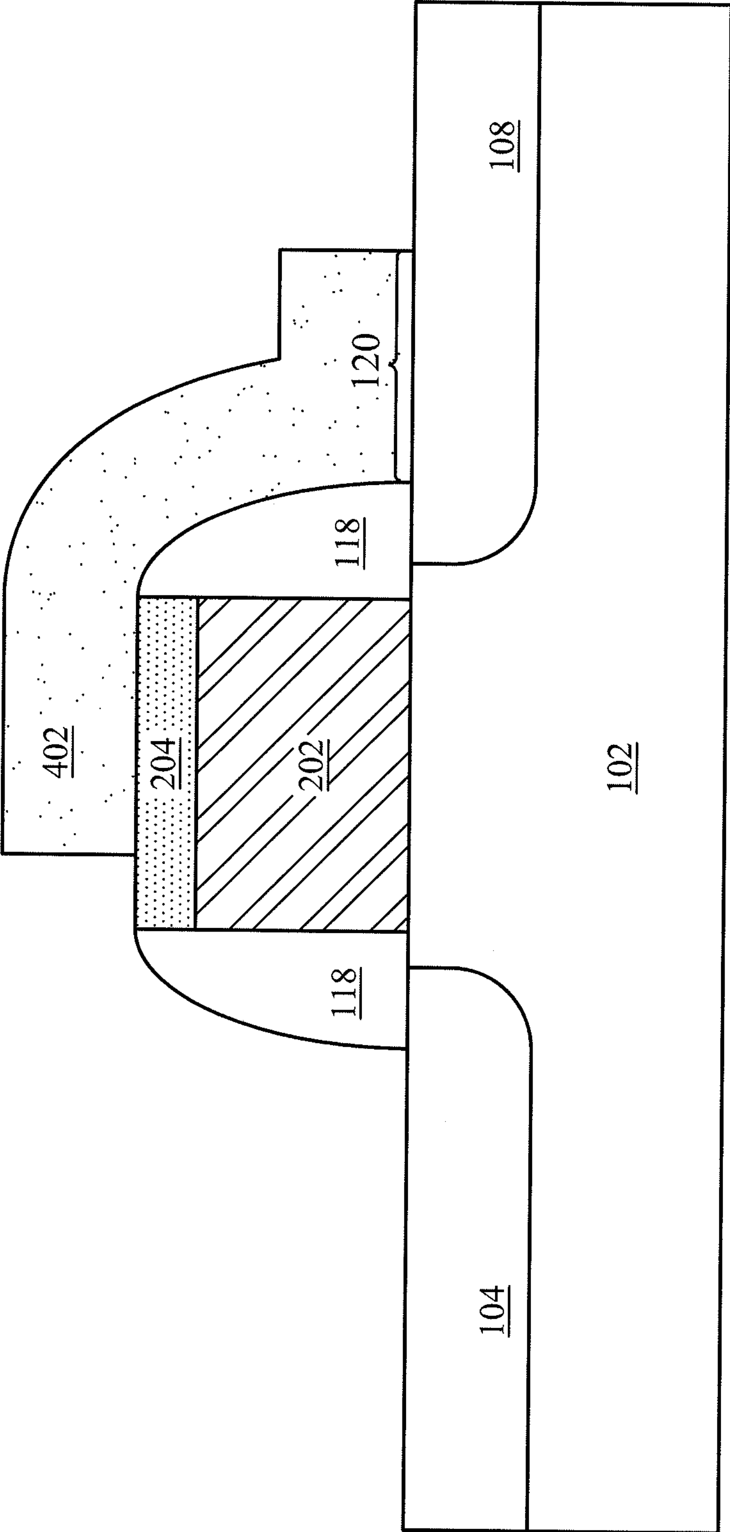


Fig. 4

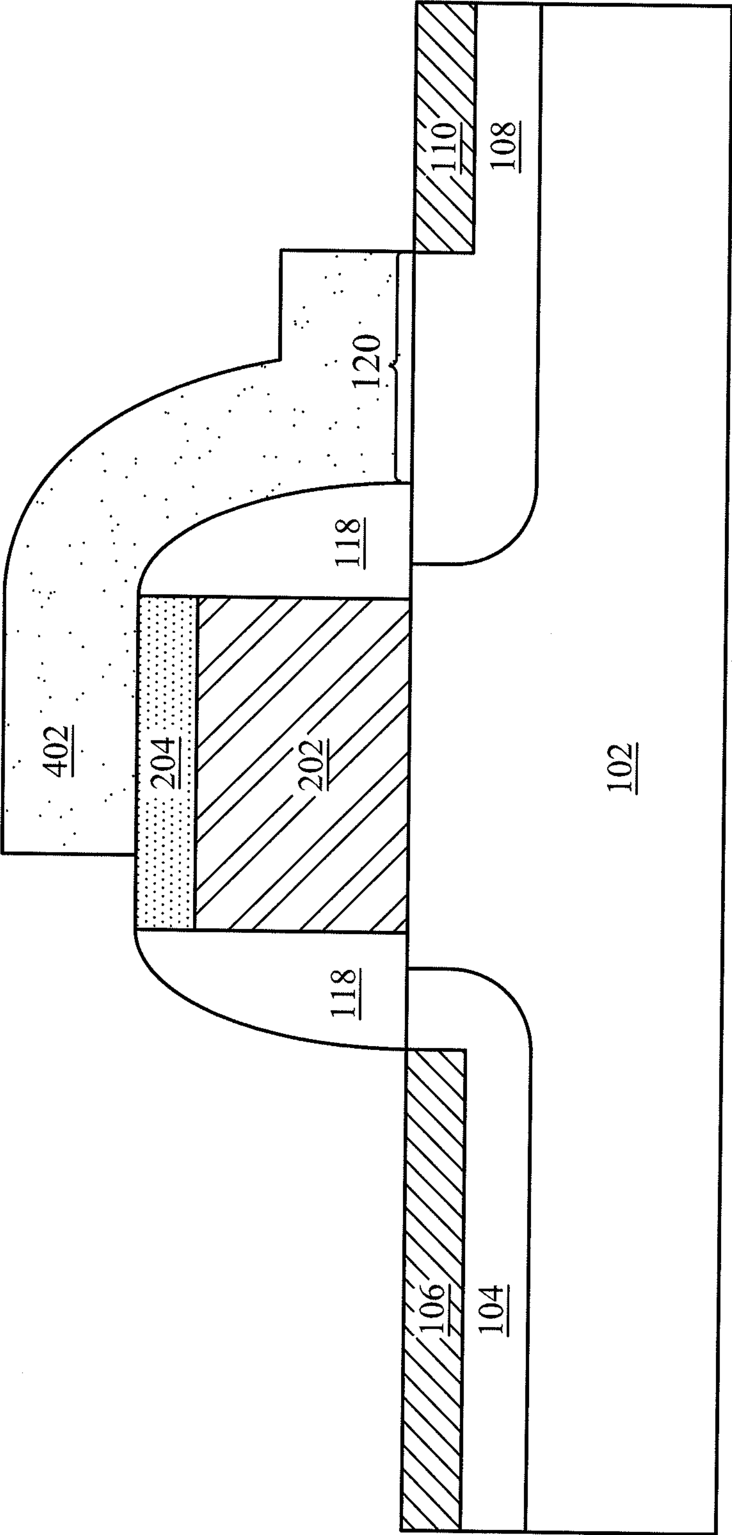


Fig. 5

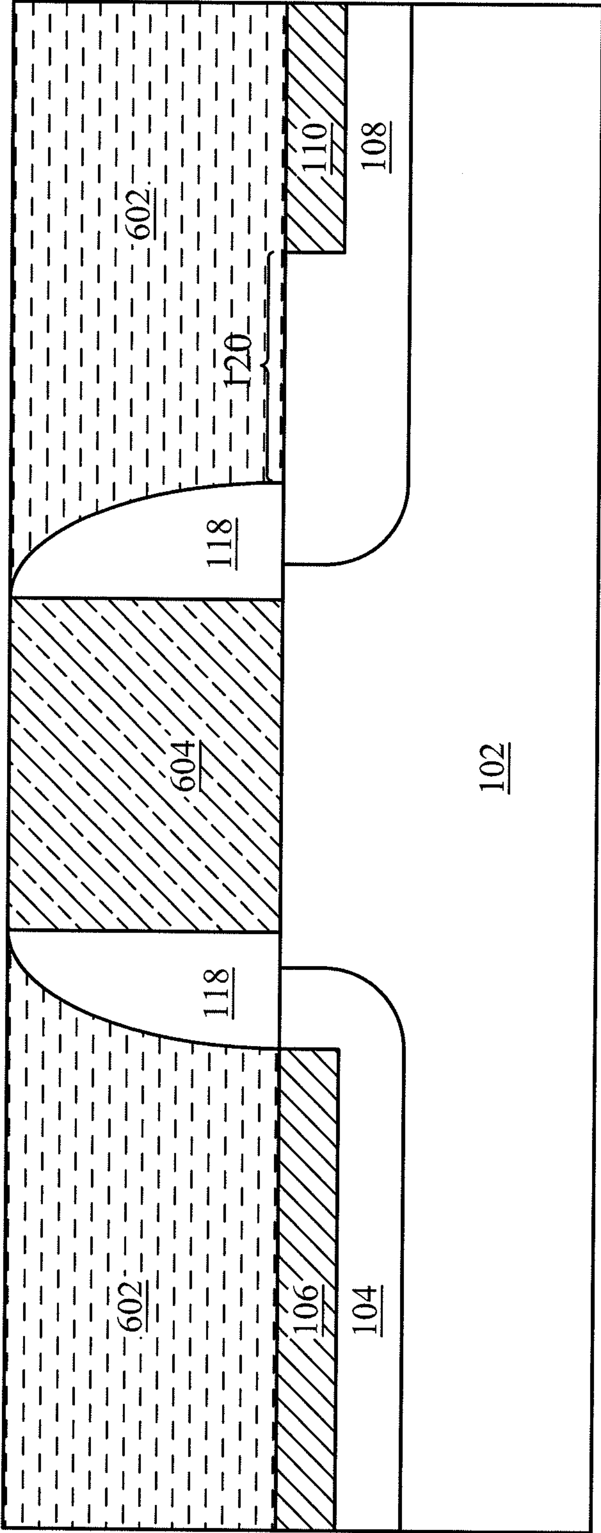


Fig. 6

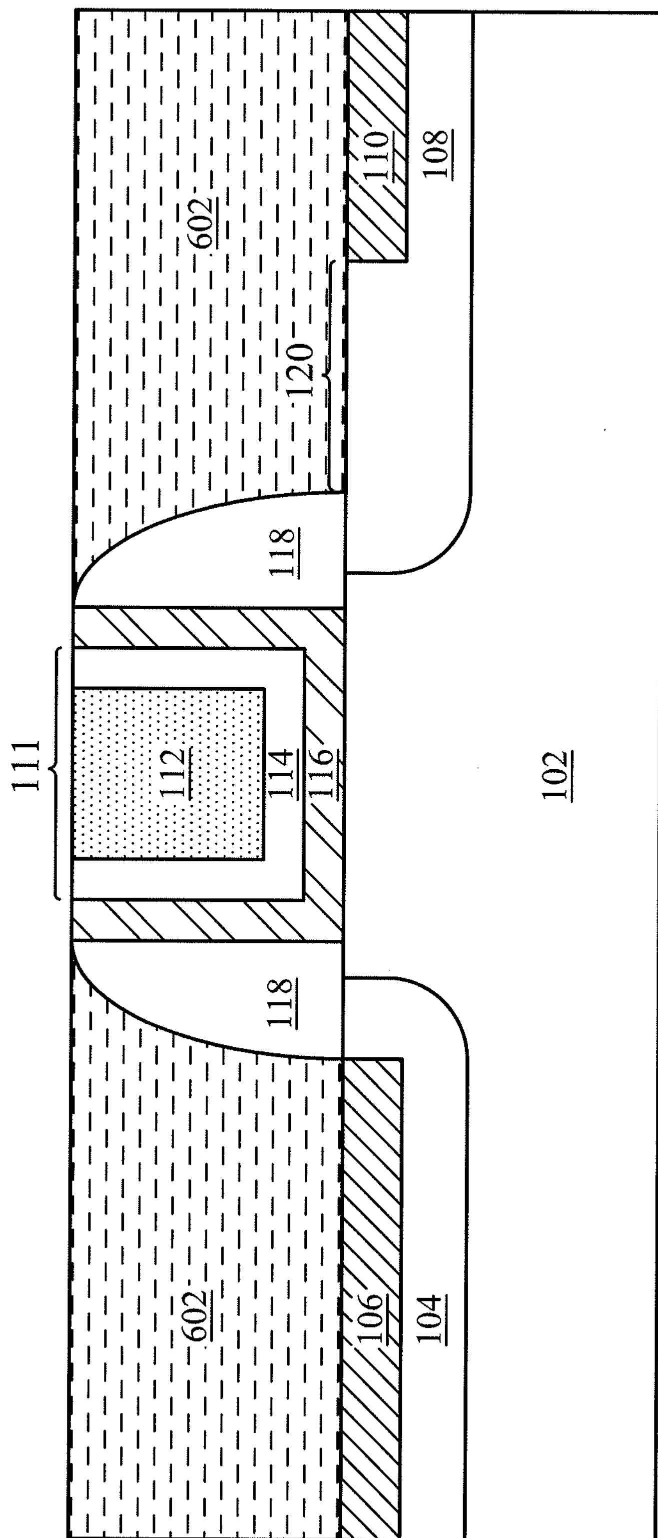


Fig. 7

METHOD OF FORMING LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTOR WITH PARTIALLY UNSILICIDED SOURCE/DRAIN

PRIORITY CLAIM

[0001] The present application is a continuation of U.S. application Ser. No. 13/711,054, filed Dec. 11, 2012, which is a divisional application of U.S. application Ser. No. 12/701, 824 filed Feb. 8, 2010, now U.S. Pat. No. 8,349,678, issued Jan. 8, 2013, the entire disclosures of which are incorporated by reference herein in their entireties.

TECHNICAL FIELD

[0002] The present disclosure relates generally to a method of forming an integrated circuit device and, more particularly, to method of forming a laterally diffused metal oxide semiconductor (LDMOS) transistor.

BACKGROUND

[0003] LDMOS transistors are used in radio frequency (RF)/microwave applications. For example, in power amplifier applications, high output power is required. Therefore, an LDMOS transistor that can handle a high voltage and an increased current is desirable. Also, an LDMOS transistor that uses a polysilicon/SiON gate stack has a control issue in the silicide formation on its gate, resulting in a partially silicided gate during the silicide process. Accordingly, new methods and structures for LDMOS transistors are desired.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] For a more complete understanding of embodiments of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0005] FIG. **1** illustrates a laterally diffused metal oxide semiconductor (LDMOS) transistor in accordance with one or more embodiments;

[0006] FIG. **2**-FIG. **7** illustrate various stages of an exemplary method of fabrication of the LDMOS transistor in accordance with one or more embodiments.

DETAILED DESCRIPTION

[0007] The making and using of various embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use, and do not limit the scope of the invention.

[0008] A structure for a laterally diffused metal oxide semiconductor (LDMOS) transistor is provided. FIG. **1** illustrates a laterally diffused metal oxide semiconductor (LDMOS) transistor in accordance with one or more embodiments. The LDMOS transistor 100 includes a substrate **102**, a metal gate **111** over the substrate **102**, and a source **104** and a drain **108** over the substrate **102** on opposite sides of the metal gate **111**. The substrate **102** may comprise a bulk silicon or silicon-on-insulator substructure. Alternatively, the substrate **102** may comprise other materials, which may or may not be combined with silicon, such as germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, or any other suitable material. A gate dielectric layer **116** is disposed over the substrate **102** and between the metal gate **111** and a channel **122** of the transistor **100**. Spacers **118** are also shown on opposite sides of the metal gate **111**.

[0009] A first silicide **106** is disposed on the source **104**. A second silicide **110** is disposed on the drain **108**. A silicide is an alloy of silicon and metals, used as contact materials in silicon device manufacturing, e.g., $TiSi_2$, $CoSi_2$, NiSi, other silicide, or any combinations thereof. The silicide combines advantageous features of metal contacts (e.g., significantly lower resistivity than polysilicon) and polysilicon contacts (e.g., no electromigration). The drain **108** has an unsilicided region **120** adjacent to the metal gate **111** to provide a resistive region capable of sustaining a voltage load suitable for a high voltage LDMOS application.

[0010] For example, LDMOS transistors are widely used in power amplifiers for base-stations that use a high output power with a corresponding drain to source breakdown voltage usually above 60 volts. Many high power RF applications use direct current (DC) supply voltages ranging from about 20 to about 50 volts.

[0011] In one example, the unsilicided region **120** can be defined between the spacer **118** and the silicide **110**. In some embodiments, the unsilicided region **120** has a length ranging from about 0.05 μm to about 1 μm. The gate dielectric layer **116** comprises a high-k gate dielectric material. The materials that may be used to make the high-k gate dielectric include hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or any other suitable material. The metal gate **111** can comprise more than one metal layers, e.g. a work function metal layer **114** and a trench fill metal layer **112**. The trench fill metal layer **112** can comprise tungsten, aluminum, titanium, titanium nitride, or any other suitable material.

[0012] Table 1 below shows a performance comparison between a LDMOS transistor using a polysilicon ("poly")/ SiON gate stack and a LDMOS transistor using a high-k dielectric/metal gate stack in accordance with one or more embodiments. The LDMOS transistors have the same equivalent oxide thickness (EOT) of 28 angstroms and the gate length Lg of 1 μm. The on-state current I_{on} of the LDMOS transistor using a high-k dielectric/metal gate stack in accordance with one or more embodiments shows about 4% increase compared to the on-state current I_{on} of the LDMOS transistor using the poly/SiON gate stack, due to the elimination of the poly depletion effect.

TABLE 1

LDMOS	Poly/SiON	HK/MG
$V_{t\ lin}$ (V)	0.256	0.257
$V_{t\ sat}$ (V)	0.251	0.251
Id lin (μA/μm)	19.6	20.1
Ion (μA/μm)	402.5	419.9
DIBL (mV)	5.4	5.3

The current $I_{d\ lin}$ in the linear region of the LDMOS transistor using the high-k dielectric/metal gate stack in accordance with one or more embodiments also has an increased value. The threshold voltages $V_{t\ lin}$ in the linear region and $V_{t\ sat}$ in

the saturation region for both the LDMOS transistors are similar to each other. The drain induced barrier lowering (DIBL) values are also similar to each other.

[0013] Regarding on-state resistance distribution, an exemplary embodiment of the LDMOS transistor using the high-k dielectric/metal gate stack showed a source resistance of 107 ohm-cm, which is about 4.3% of the total on-state resistance of the transistor. The channel resistance was 1460.2 ohm-cm, which is about 58.7% of the total on-state resistance of the transistor. The drain resistance was 920.4 ohm-cm, which is about 37% of the total on-state resistance of the transistor. These values are similar to the on-state resistance distribution of a LDMOS transistor using the poly/SiON gate stack.

[0014] FIG. **2**-FIG. **7** illustrate various stages of an exemplary method of fabrication of the LDMOS transistor in accordance with one or more embodiments. FIG. **2** shows a dummy gate **202** formed over the substrate **102**. In one example, the dummy gate **202** can comprise, for example, polysilicon. A hardmask **204** is formed over the dummy gate **202**. The hard mask **204** and the dummy gate **202** may be patterned by applying a photolithographic process and/or an etch process. In one example, the polysilicon dummy gate **202** has a thickness between about 100 and about 2,000 angstroms. The hardmask **204** may comprise silicon nitride, silicon dioxide and/or silicon oxynitride, and may have a thickness between about 100 and about 500 angstroms.

[0015] The spacers **118** are formed on opposite sides of the dummy gate **202**. The spacers **118** may comprise, for example, silicon nitride. After forming the spacers **118**, the source **104** and the drain **108** are formed over the substrate **102** on opposite sides of the dummy gate **202**. The source **104** and the drain **108** may be formed by implanting ions into the substrate **102**, followed by applying an appropriate anneal step. After the ion implantation and anneal steps, portions of the source **104** and the drain **108** may be converted to silicides as described below.

[0016] In FIG. **3**, a resist protect oxide (RPO) layer **302** is formed over the hardmask **204**, the dummy gate **202**, the spacers **118**, the source **104**, and the drain **108**. After covering all device area defined over the surface of the substrate **102** with the RPO layer **302**, the device area can be divided into an area that is to be silicided for electrical contacts and another area that is not to be silicided. In one example, the RPO layer **302** is formed using silicon dioxide.

[0017] In FIG. **4**, the RPO layer **302** (shown in FIG. **3**) is partially etched away, leaving the RPO layer **402** over at least a portion of the dummy gate **202**, extending over the drain **108**. The device area that is not to be silicided is covered with the RPO layer **402**. The RPO layer **402** can be defined by applying, for example, an oxide wet etch that partially removes the RPO layer **302**. This protects the areas under the RPO layer **402** from the silicide formation. The hardmask **204** also protects the dummy gate **202** from the silicide formation.

[0018] In FIG. **5**, a silicide process is performed to form the first silicide **106** and the second silicide **110**. The first silicide **106** is formed on the source **104**. The second silicide **110** is formed on the drain **108** so that the unsilicided region **120** of the drain **108** is left adjacent to the dummy gate **202**. The unsilicided region **120** of the drain **108** provides a highly resistive region capable of sustaining a voltage load suitable for a high voltage LDMOS application as described above. In one example, the unsilicided region **120** has a length ranging from about 0.05 μm to about 1 μm.

[0019] In FIG. **6**-FIG. **7**, a replacement gate process is performed on the dummy gate **202** (shown in FIG. **5**). In FIG. **6**, after forming the silicided regions **106** and **110** over the source **104** and the drain **108**, the RPO layer **402** (shown in FIG. **5**) can be removed and a dielectric layer **602** can be deposited over the device area. The dielectric layer **602** may comprise silicon dioxide, a low-k material, or any other suitable material. The dielectric layer **602** may be doped with phosphorus, boron, or other elements, and may be formed using a high-density plasma deposition process.

[0020] FIG. **6** shows the dielectric layer **602** after being polished for the replacement gate process. A chemical mechanical polishing (CMP) operation may be applied to remove a part of the dielectric layer **602**. After exposing the hardmask **204** (shown in FIG. **5**), the hardmask **204** is removed to expose the dummy gate **202**. In some embodiments, the hardmask **204** may be polished from the surface of the dummy gate **202** when dielectric layer **602** is polished. The dummy gate **202** (shown in FIG. **5**) that is bracketed by the spacers **118** is removed to create a trench **604** between the spacers **118**. A selective wet etch process can be applied to remove the dummy gate **202**.

[0021] In FIG. **7**, the gate dielectric layer **116** is formed over substrate **102** at the bottom of trench **604** after removing the dummy gate **202**. The trench **604** is filled with the metal gate **111** over the gate dielectric layer **116**. Although the gate dielectric layer **116** may comprise any material that may serve as a gate dielectric for a transistor that includes a metal gate electrode, the gate dielectric layer **116** can comprise a high-k dielectric material.

[0022] The gate dielectric layer **116** may be formed over the substrate **102** using a deposition method, e.g., a chemical vapor deposition (CVD), a low pressure CVD, or a physical vapor deposition (PVD) process. In many applications, a high-k gate dielectric layer can be less than about 60 angstroms in thickness. In some embodiments, to remove impurities from the gate dielectric layer **116** and to increase that layer's oxygen content, a wet chemical treatment may be applied to the gate dielectric layer **116**.

[0023] In some embodiments, the metal gate **111** can comprise more than one metal layers. For example, the work function metal layer **114** can be deposited over the gate dielectric layer **116**, and the trench fill metal layer **112** can be deposited over the work function metal layer **114**. The work function metal layer **114** for NMOS transistors can comprise hafnium, zirconium, titanium, tantalum, aluminum, their alloys, e.g., metal carbides that include these elements, i.e., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide, or any other suitable material. The work function metal layer **114** may be formed on the gate dielectric layer **116** using PVD and/or CVD processes, e.g., sputter and/or atomic layer CVD processes.

[0024] In some embodiments, the work function metal layer **114** for NMOS transistors can have a work function that is between about 3.9 eV and about 4.2 eV. The work function metal layer **114** can fill up the trench and have a thickness that is between about 100 angstroms and about 2,000 angstroms if no trench fill metal layer **112** is deposited. If the trench metal **112** is deposited over the work function metal **114** to fill the trench **604**, the trench fill metal layer **112** can comprise a material that may be easily polished, e.g., tungsten, aluminum, titanium, titanium nitride, and/or any other suitable

material. In such an embodiment, the work function metal layer **114** may have a thickness between about 50 and about 1,000 angstroms.

[0025] The work function metal layer **114** for PMOS transistors can comprise ruthenium, palladium, platinum, cobalt, nickel, conductive metal oxides, e.g., ruthenium oxide, or any other suitable material. In some embodiments, the work function metal layer **114** for PMOS transistors can have a work function that is between about 4.9 eV and about 5.2 eV.

[0026] In the embodiments specifically disclosed with respect to FIGS. **1-7**, the drain **108** outside the spacers **118** is partially unsilicided. However, in some other embodiments, the source **104** outside the spacers **118** is partially unsilicided, whereas the drain **108** outside the spacers **118** is fully silicided. In further embodiment, both the source **104** and the drain **108** outside the spacers **118** are partially unsilicided. A substantially same effect is achieved in that the unsilicided region(s) of the drain **108** and/or the source **104** provide(s) one or more highly resistive regions capable of sustaining a voltage load suitable for a high voltage LDMOS application as described above.

[0027] Embodiments of the fabrication process described above may provide improved process control of the gate region compared to a known process for a poly/SiON gate stack, because no silicide formation is necessary on the gate region. Also, the high-k dielectric/metal gate stack enables the structure to have less process variations. To reduce process cost and complexity, the LDMOS can be fabricated through a careful logic operation to define silicide area and manipulation of existing fabrication processes. A skilled person in the art will appreciate that there can be many embodiment variations of this invention.

[0028] In some embodiments, a transistor comprises a substrate, a gate over the substrate, a source and a drain over the substrate on opposite sides of the gate, a first silicide on the source, and a second silicide on the drain. Only one of the drain or the source has an unsilicided region adjacent to the gate to provide a resistive region.

[0029] In some embodiments, a transistor comprises a substrate, a gate over the substrate, a source and a drain over the substrate on opposite sides of the gate, a first spacer between the source and the gate, and a second spacer between the drain and the gate. One of the source and the drain has a silicided region extending from the corresponding spacer away from the gate. The other of the source and the drain has an unsilicided region extending from the corresponding spacer away from the gate.

[0030] In some embodiments, a laterally diffused metal oxide semiconductor (LDMOS) transistor comprises a substrate, a gate over the substrate, a source and a drain over the substrate on opposite sides of the gate, a first spacer between the source and the gate, a second spacer between the drain and the gate, a first silicide on the source and outside the spacers, and a second silicide on the drain and outside the spacers. Only one of the drain or the source has an unsilicided region adjacent to the corresponding spacer to provide a resistive region configured to sustain a voltage load in a high voltage LDMOS application.

[0031] An aspect of this description relates to a method of forming a semiconductor device. The method comprises forming a gate over a substrate. The method also comprises forming a source and a drain on opposite sides of the gate. The source and the drain are formed such that the source and the drain are separated by a channel region beneath the gate. The source and the drain are positioned such that the channel region has a channel width with respect to a surface of the substrate greater than a width of the gate with respect to the surface of the substrate. The method further comprises forming a first silicide over a portion of the source. The method additionally comprises forming a second silicide over a portion of the drain such that the drain has an unsilicided region adjacent to the gate configured to provide a resistive region configured to sustain a voltage load in a high voltage laterally diffused metal oxide semiconductor (LDMOS) application.

[0032] Another aspect of this description relates to a method of forming a transistor. The method comprises forming a gate over a substrate. The method also comprises forming a source and a drain on opposite sides of the gate. The source and the drain are formed such that the source and the drain are separated by a channel region beneath the gate separating the source from the drain. The source and the drain are positioned such that the channel region has a channel width with respect to a surface of the substrate greater than a width of the gate with respect to the surface of the substrate. The method further comprises forming a first silicide over a portion of the drain. The method additionally comprises forming a second silicide over a portion of the source such that the source has an unsilicided region adjacent to the gate configured to provide a resistive region configured to sustain a voltage load in a high voltage laterally diffused metal oxide semiconductor (LDMOS) application. The method also comprises forming a first spacer between the drain and the gate. The method further comprises forming a second spacer between the source and the gate.

[0033] A further aspect of this description relates to a method of forming a laterally diffused metal oxide semiconductor (LDMOS) transistor. The method comprises forming a source and a drain on opposite sides of a gate. The source and the drain are formed such that the source and the drain are separated by a channel region beneath the gate separating the source from the drain. The source and the drain are positioned such that the channel region has a channel width with respect to a surface of the substrate greater than a width of the gate with respect to the surface of the substrate. The method also comprises forming a first spacer between the source and the gate. The method further comprises forming a second spacer between the drain and the gate. The method additionally comprises forming a first silicide on the source and outside the first and second spacers. The method also comprises forming a second silicide on the drain and outside the first and second spacers. The second silicide is formed such that the drain has an unsilicided region adjacent to the second spacer configured to provide a resistive region configured to sustain a voltage load in a high voltage LDMOS application.

[0034] Although embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function and/or achieve substantially the

same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A method of forming a semiconductor device, the method comprising:

forming a gate over a substrate;

forming a source and a drain on opposite sides of the gate, the source and the drain being separated by a channel region beneath the gate, wherein the source and the drain are positioned such that the channel region has a channel width with respect to a surface of the substrate greater than a width of the gate with respect to the surface of the substrate;

forming a first silicide over a portion of the source; and

forming a second silicide over a portion of the drain such that the drain has an unsilicided region adjacent to the gate configured to provide a resistive region configured to sustain a voltage load in a high voltage laterally diffused metal oxide semiconductor (LDMOS) application.

2. The method of claim **1**, wherein the second silicide is formed such that the unsilicided region has a length ranging from about 0.05 μm to about 1 μm.

3. The method of claim **1**, further comprising:

forming a gate dielectric layer between the gate and the substrate.

4. The method of claim **3**, wherein the gate dielectric layer is formed comprising a high-k dielectric material.

5. The method of claim **1**, wherein the gate is formed by a replacement gate process on a dummy gate positioned over the substrate in a position corresponding to a position in which the gate is formed.

6. The method of claim **5**, further comprising:

forming a hardmask layer over the dummy gate.

7. The method of claim **5**, further comprising:

forming a resist protect oxide (RPO) layer over at least a portion of the dummy gate and over the unsilicided region to protect areas under the RPO layer from a silicide process used to form the first silicide and the second silicide.

8. The method of claim **1**, further comprising:

forming a first spacer on a first side of the gate; and

forming a second spacer on a second side of the gate opposite the first side of the gate.

9. The method of claim **8**, wherein the first spacer, the second spacer, and the second silicide are formed such that the unsilicided region is not covered by either of the first spacer or the second spacer.

10. A method of forming a transistor, the method comprising:

forming a gate over a substrate;

forming a source and a drain on opposite sides of the gate, the source and the drain being separated by a channel region beneath the gate separating the source from the drain, wherein the source and the drain are positioned such that the channel region has a channel width with respect to a surface of the substrate greater than a width of the gate with respect to the surface of the substrate;

forming a first silicide over a portion of the drain;

forming a second silicide over a portion of the source such that the source has an unsilicided region adjacent to the gate configured to provide a resistive region configured to sustain a voltage load in a high voltage laterally diffused metal oxide semiconductor (LDMOS) application;

forming a first spacer between the drain and the gate; and

forming a second spacer between the source and the gate.

11. The method of claim **10**, wherein the gate is formed by a replacement gate process on a dummy gate positioned over the substrate in a position corresponding to a position in which the gate is formed, and the replacement gate process comprises forming a gate dielectric layer between a metal gate and the substrate.

12. The method of claim **11**, wherein the gate dielectric layer is formed comprising a high-k dielectric material.

13. The method of claim **11**, wherein the replacement gate process further comprises depositing a work function metal over the gate dielectric layer.

14. The method of claim **13**, wherein the replacement gate process further comprises depositing a conductive material over the work function metal.

15. The method of claim **14**, wherein the conductive material is selected from the group consisting of tungsten, aluminum, titanium, and titanium nitride.

16. The method of claim **10**, wherein the first spacer, the second spacer, and the second silicide are formed such that the unsilicided region is exposed by either of the first spacer or the second spacer and the unsilicided region has a length ranging from about 0.05 μm to about 1 μm.

17. A method of forming a laterally diffused metal oxide semiconductor (LDMOS) transistor, the method comprising:

forming a source and a drain on opposite sides of a gate, the source and the drain being separated by a channel region beneath the gate separating the source from the drain, wherein the source and the drain are positioned such that the channel region has a channel width with respect to a surface of the substrate greater than a width of the gate with respect to the surface of the substrate;

forming a first spacer between the source and the gate;

forming a second spacer between the drain and the gate;

forming a first silicide on the source and outside the first and second spacers; and

forming a second silicide on the drain and outside the second spacer, the second silicide being formed such that the drain has an unsilicided region adjacent to the second spacer configured to provide a resistive region configured to sustain a voltage load in a high voltage LDMOS application.

18. The method of claim **17**, wherein the source and the drain are formed after the first spacer and the second spacer are formed, and the second silicide is formed such that the unsilicided region has a length ranging from about 0.05 micrometers (μm) to about 1 μm.

19. The method of claim **18**, further comprising:

forming a resist protect oxide (RPO) layer over at least a portion of the drain to protect areas under the RPO layer from a silicide process used to form the first silicide and the second silicide.

20. The method of claim **17**, further comprising:

forming a gate dielectric layer between a metal gate and the substrate by depositing a high-k gate dielectric material to a thickness less than about 60 angstroms.

* * * * *