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(54) OXIDATION RESISTANT BARRIER METAL PROCESS FOR SEMICONDUCTOR DEVICES

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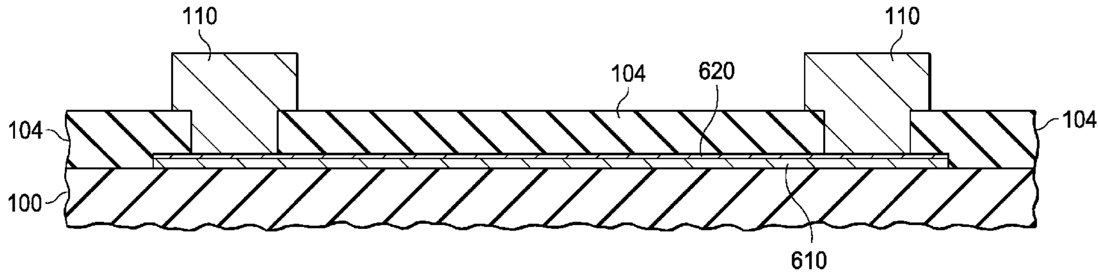
(57) **ABSTRACT**

An integrated circuit and method comprising an underlying metal geometry, a dielectric layer on the underlying metal geometry, a contact opening through the dielectric layer, an overlying metal geometry wherein a portion of the overlying metal geometry fills a portion of the contact opening, and an oxidation resistant barrier layer disposed between the underlying metal geometry and overlying metal geometry. The oxidation resistant barrier layer is formed of TaN or TiN with a nitrogen content of at least 20 atomic % and a thickness of at least 5 nm.



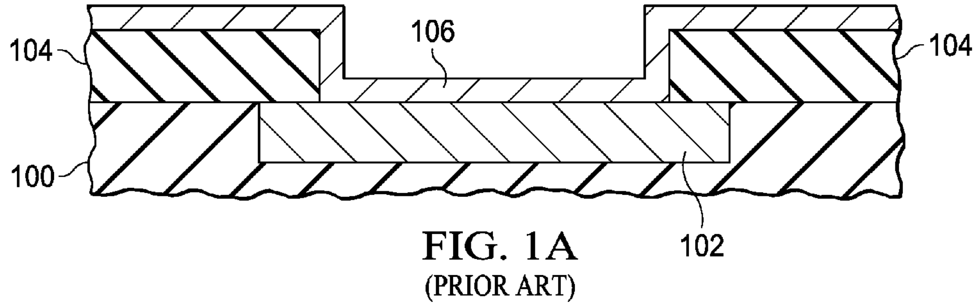


FIG. 1A
(PRIOR ART)

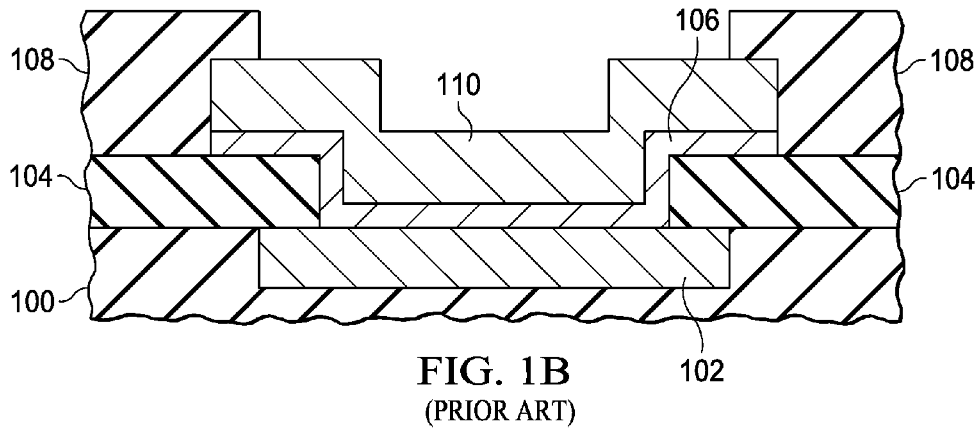


FIG. 1B
(PRIOR ART)

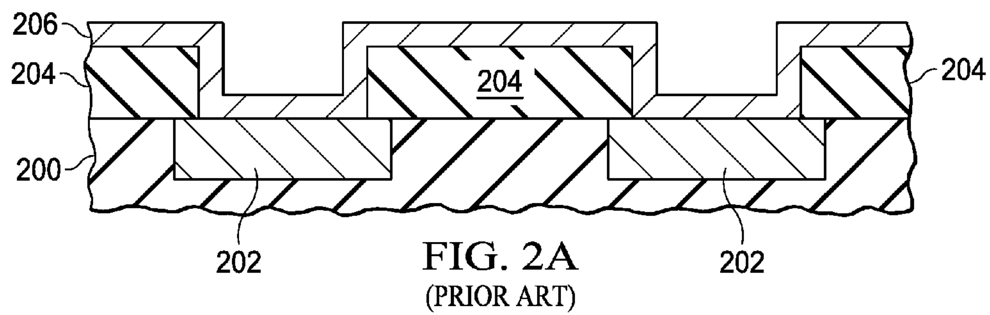


FIG. 2A
(PRIOR ART)

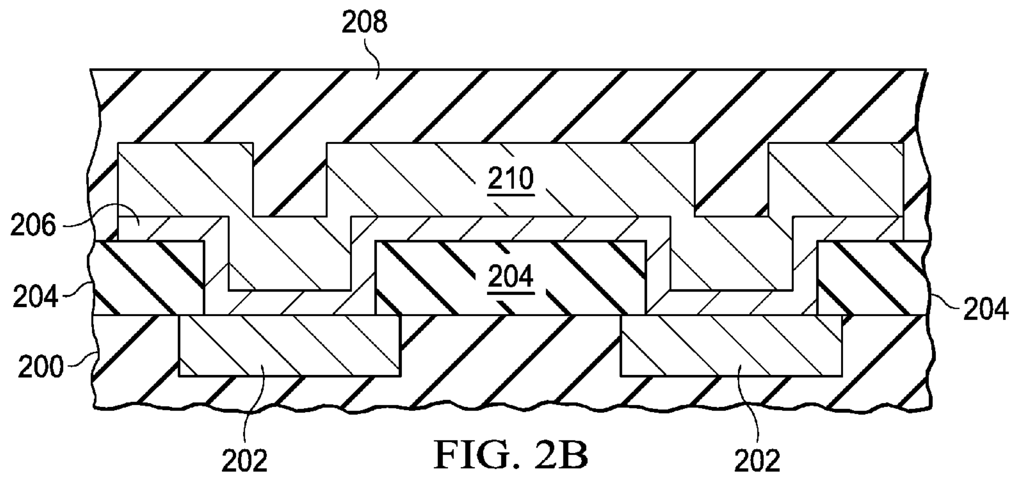


FIG. 2B
(PRIOR ART)

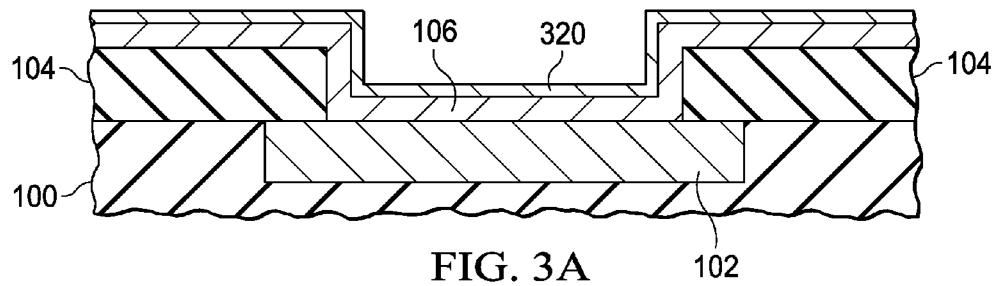


FIG. 3A

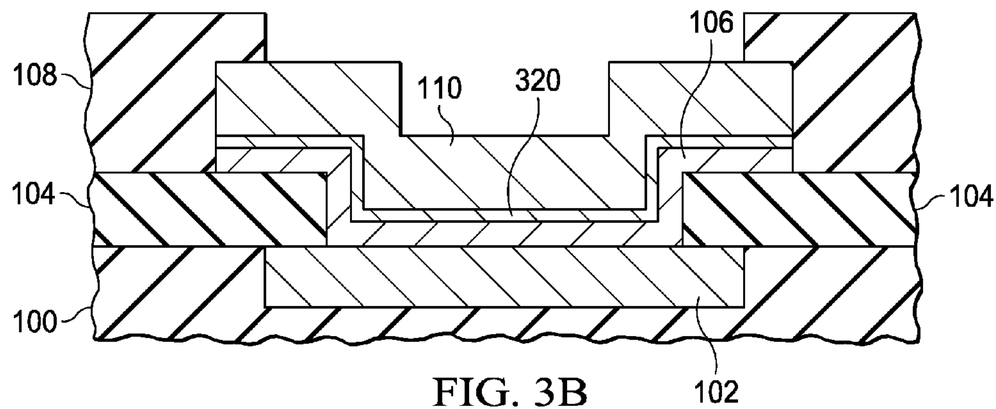


FIG. 3B

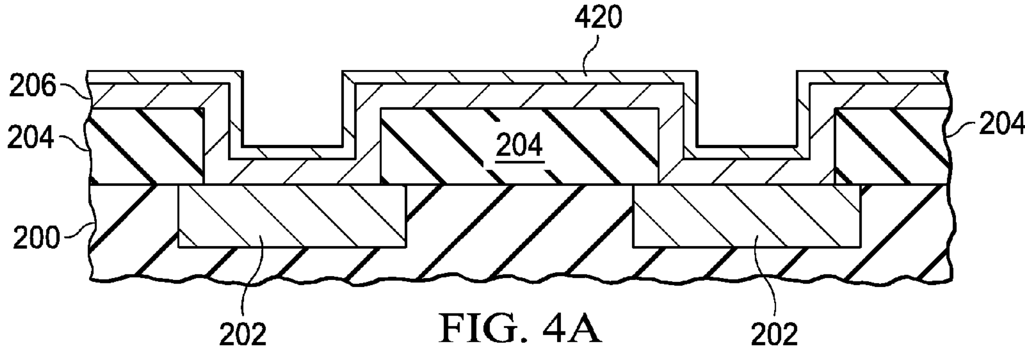


FIG. 4A

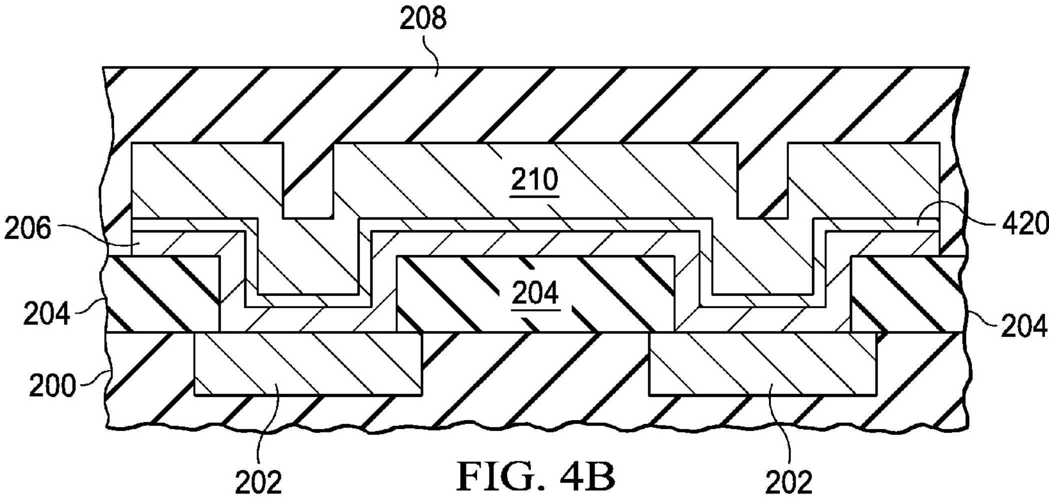


FIG. 4B

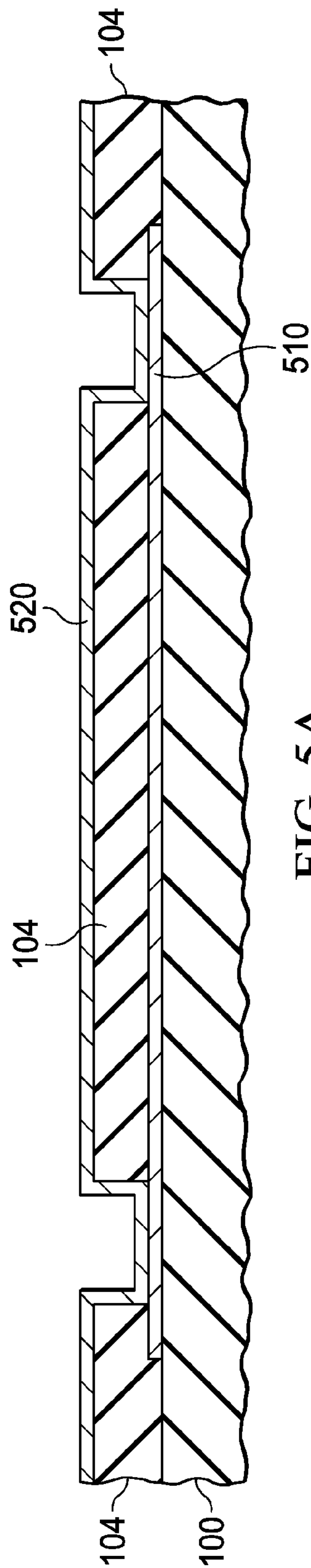


FIG. 5A

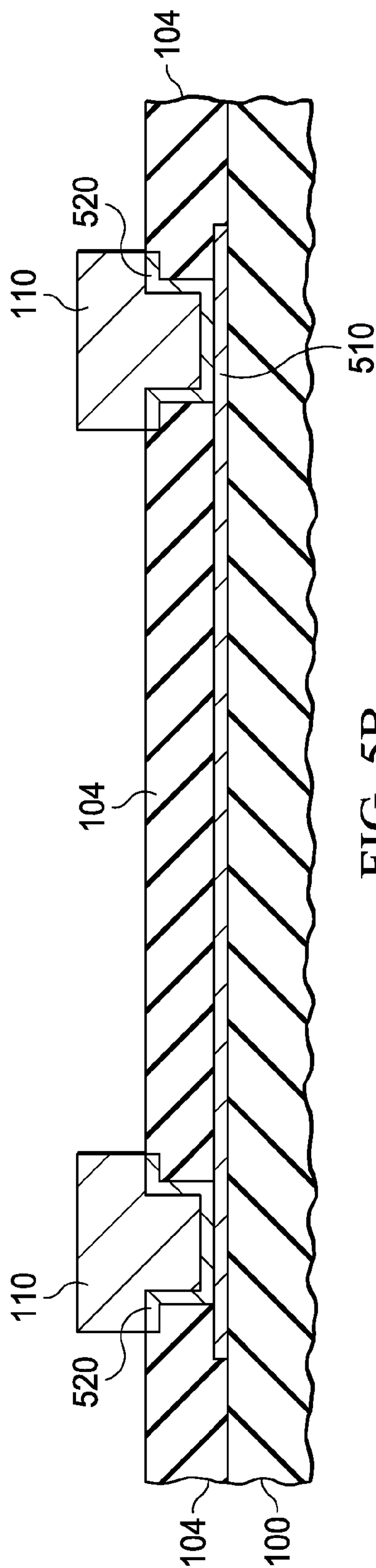


FIG. 5B

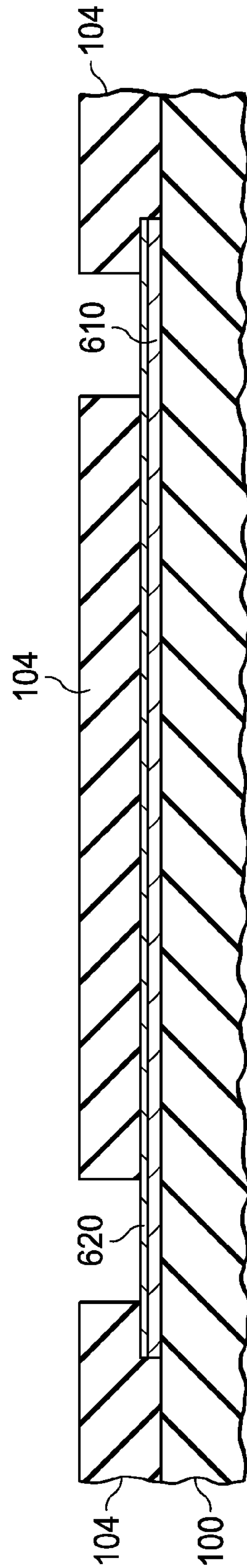


FIG. 6A

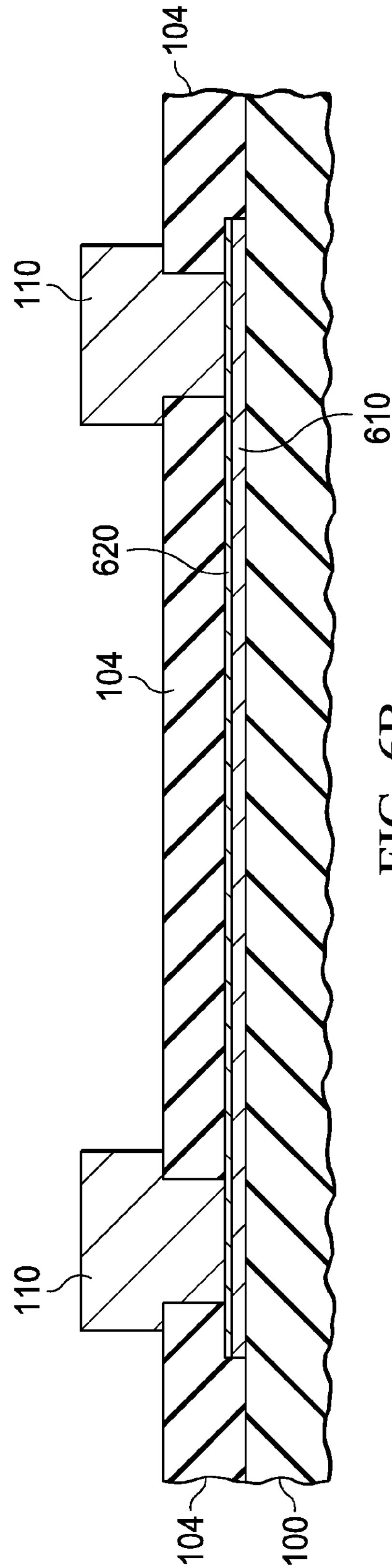


FIG. 6B

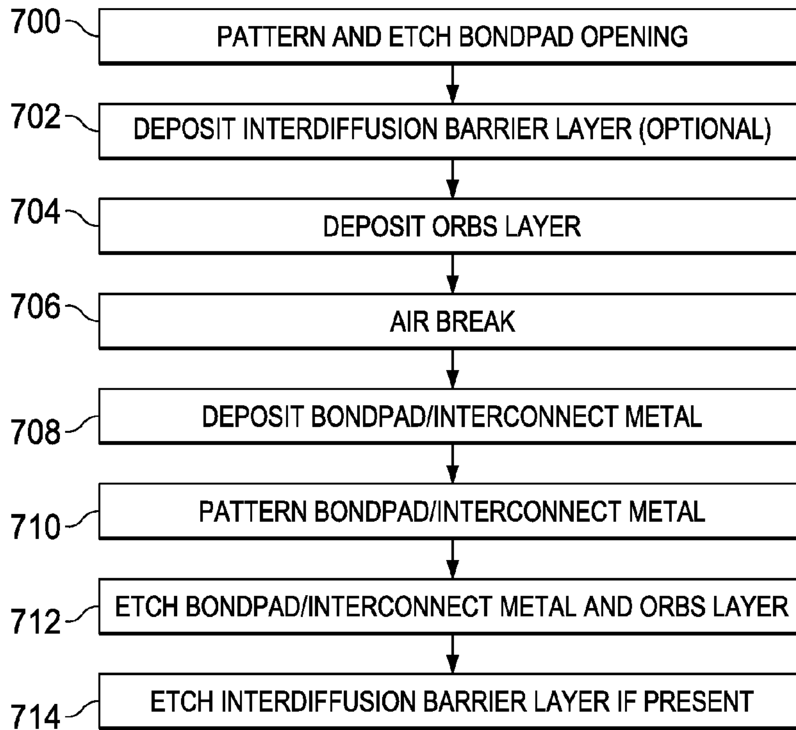


FIG. 7

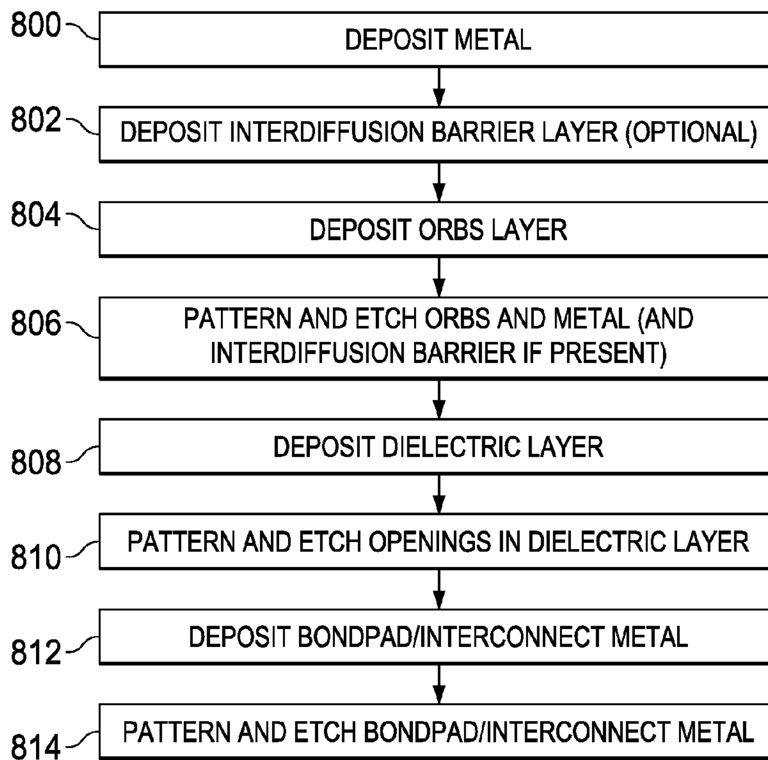


FIG. 8

OXIDATION RESISTANT BARRIER METAL PROCESS FOR SEMICONDUCTOR DEVICES

FIELD

[0001] This invention relates to the field of integrated circuits. More particularly, this invention relates to the formation of contacts with stable resistance in integrated circuits.

BACKGROUND

[0002] During processing of an integrated circuit, openings typically referred to as contacts or vias are made through dielectric overlying metal interconnect leads to form electrical contact to the leads. The metal interconnect that is exposed in the these contact or via openings may form a layer of metal oxide on the surface that increases the electrical contact resistance and also may cause significant variation in the electrical contact resistance in these openings across an integrated circuit chip or wafer.

[0003] A typical example of forming an aluminum bond pad **110** on a top layer of copper interconnect **102** is illustrated in FIG. **1**B. The underlying copper interconnect layer **102** is formed in a dielectric layer **100** using either a single or a dual damascene process. An opening is formed in dielectric layer **104** overlying the copper interconnect layer to form electrical connection to an overlying aluminum bondpad **110**. An interdiffusion barrier layer **106** of a material such as Ta or TaN is disposed between the underlying copper interconnect and the overlying aluminum bondpad **110** to prevent interdiffusion of copper and aluminum.

[0004] A typical example of forming an upper level of aluminum interconnect **210** on a lower layer of copper interconnect **202** is illustrated in FIG. **2**B. The underlying copper interconnect layer **202** is formed in a dielectric layer **200** using either a single or a dual damascene process. Contact or via openings are formed in dielectric layer **204** overlying the copper interconnect layer **202** to form electrical connection between the interconnect layers **202** and **210**. An interdiffusion barrier layer **206** of a material such as Ta or TaN is disposed between the underlying copper interconnect **202** and the overlying aluminum interconnect **210** to prevent interdiffusion of copper and aluminum.

[0005] As illustrated in TABLE 1, the Ta_xO_y (or $Ta_xN_yO_z$) layer that forms on the TaN interdiffusion barrier layer **106** (FIG. **1**A) and layer **206** (FIG. **2**A) causes the contact resistance to increase by 6× after 12 hours of exposure to air and by **10***x* after 24 hours of exposure to air. In addition, the increase in electrical contact resistance caused by the Ta_xO_y layer typically varies significantly from contact to contact. Those skilled in the art will recognize that the magnitude of the increase in electrical resistance depends on both the test structure and measurement technique used; TABLE 1 was generated from 4-point probe measurements to maximize sensitivity to interface resistance and is intended solely to provide a baseline reference for quantifying the improvement afforded by the invention.

TABLE 1

TaN in via exposure to air	Resistance Increase
12 hours	6x
24 hours	10x

[0006] The metal oxide layer may be removed by various means such as sputter etching prior to deposition of the aluminum bondpad metal **110** or the upper aluminum interconnect metal **210**, but this often causes other problems. For example if an argon sputter etch is used to remove the Ta_xO_y layer that forms on the TaN barrier layer **106** and **206** prior to AlCu **110** and **210** deposition, the sputter etch process introduces particles which reduces yield. In addition the presputter etch alters the morphology of the deposited AlCu, **110** or **210**, resulting in a decrease in electromigration resistance.

SUMMARY

[0007] The following presents a simplified summary in order to provide a basic understanding of one or more aspects of the invention. This summary is not an extensive overview of the invention, and is neither intended to identify key or critical elements of the invention, nor to delineate the scope thereof. Rather, the primary purpose of the summary is to present some concepts of the invention in a simplified form as a prelude to a more detailed description that is presented later.

[0008] An integrated circuit and method comprising an underlying metal geometry, a dielectric layer on the underlying metal geometry, a contact opening through the dielectric layer, an overlying metal geometry wherein a portion of the overlying metal geometry fills a portion of the contact opening, and an oxidation resistant barrier layer disposed between the underlying metal geometry and overlying metal geometry. The oxidation resistant barrier layer is formed of TaN or TiN with a nitrogen content of at least 20 atomic % and a thickness of at least 5 nm.

DESCRIPTION OF THE VIEWS OF THE DRAWINGS

[0009] FIGS. **1**A and **1**B (Prior art) are cross-sections of a lower copper interconnect to upper aluminum bondpad metal contact with an interdiffusion barrier in the bottom of the contact.

[0010] FIGS. **2**A and **2**B (Prior art) are cross-sections of a lower copper interconnect to upper aluminum interconnect metal contact with an interdiffusion barrier in the bottom of the contact.

[0011] FIGS. **3**A and **3**B are cross-sections of a lower copper interconnect to upper aluminum bondpad contact with an interdiffusion barrier plus an oxidation resistant barrier layer formed according to embodiments.

[0012] FIGS. **4**A and **4**B are cross-sections of a lower copper interconnect to upper aluminum interconnect contact with an interdiffusion barrier plus an oxidation resistant barrier layer formed according to embodiments.

[0013] FIGS. **5**A and **5**B are cross-sections of a lower metal to upper metal contact with an oxidation resistant barrier layer formed according to embodiments wherein the oxidation resistant barrier layer covers the sidewalls and the bottom of the contact.

[0014] FIGS. **6**A and **6**B are cross-sections of a lower metal to upper metal contact with an oxidation resistant barrier layer formed according to principles of the invention wherein the oxidation resistant barrier layer covers the lower metal geometry.

[0015] FIG. **7** is a flow diagram describing the primary manufacturing steps used to form the contact structures depicted in FIGS. **2**A, **2**B, **3**A, **3**B, **4**A, **4**B, **5**A, and **5**B.

[0016] FIG. **8** is a flow diagram describing the primary manufacturing steps used to form the contact structures depicted in FIGS. **6**A and **6**B.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0017] Embodiments of the invention are described with reference to the attached figures. The figures are not drawn to scale and they are provided merely to illustrate the invention. Several aspects of the embodiments are described below with reference to example applications for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide an understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details or with other methods. In other instances, well-known structures or operations are not shown in detail to avoid obscuring the invention. The embodiments are not limited by the illustrated ordering of acts or events, as some acts may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a methodology in accordance with the present invention.

[0018] An aluminum copper (AlCu) bondpad **110** to underlying copper interconnect **102** structure with an interdiffusion barrier layer **106** and with an embodiment oxidation resistant barrier layer **320** is illustrated in FIG. **3**B. A copper interconnect geometry **102** is formed in a dielectric layer **100** using a damascene process. A dielectric layer **104** with a contact opening to the copper interconnect geometry **102** overlies dielectric layer **100** and copper interconnect geometry **102**. A bondpad stack comprised of an interdiffusion barrier layer **106**, an embodiment oxidation resistant barrier surface (ORBS) layer **320** and aluminum or aluminum copper alloy **110** overlies the dielectric layer **104** and contacts the underlying copper interconnect geometry **102** through the contact opening in dielectric layer **104**. The interdiffusion barrier layer **106** may be a material such as TaN or TiN with a thickness between about 60 nm and 90 nm, and a nitrogen content between about 0 and 12 atomic percent. The ORBS layer **320** may be nitrogen rich tantalum nitride with nitrogen content in the range of about 20 to 35 atomic percent and a thickness in the range of about 5 nm to 15 nm. The ORBS layer **320** may also be a nitrogen rich titanium nitride with a thickness slightly higher than the nitrogen rich tantalum nitride oxidation resistant layer.

[0019] An aluminum copper (AlCu) interconnect **210** to underlying copper interconnect **202** structure with an interdiffusion barrier layer **206** and with an embodiment oxidation resistant barrier layer **420** is illustrated in FIG. **4**B. A copper interconnect geometry **202** is formed in a dielectric layer **200** using a damascene process. A dielectric layer **204** with contact or via openings to the copper interconnect geometries **202** overlies dielectric layer **200** and copper interconnect geometries **202**. A upper aluminum interconnect stack comprised of an interdiffusion barrier layer **206**, an embodiment oxidation resistant barrier surface (ORBS) layer **420** and aluminum or aluminum copper alloy **210** overlies the dielectric layer **204** and contacts the underlying copper interconnect geometries **202** through the contact or via openings in dielectric layer **204**. The interdiffusion barrier layer **206** may be a material such as TaN or TiN with a thickness between about 60 nm and 90 nm, and a nitrogen content between about 0 and 12 atomic percent. The ORBS layer **420** may be nitrogen rich tantalum nitride with nitrogen content in the range of about 20 to 35 atomic percent and a thickness in the range of about 5 nm to 15 nm. The ORBS layer **420** may also be a nitrogen rich titanium nitride with a thickness slightly higher than the nitrogen rich tantalum nitride oxidation resistant layer.

[0020] The ORBS layers **320** and **420** enable the IC to be exposed to air for 24 hours or longer prior to deposition of the bondpad metal **110** or the upper aluminum interconnect metal **210** with an increase in contact resistance of less than 2×. In addition with the ORBS layers **320** and **420** the resistance of many contacts or vias across the integrated circuit (IC) chip and across the IC wafer remains tightly distributed.

[0021] A copper interconnect interdiffusion barrier layer with an embodiment oxidation resistant barrier layer structure is used for illustration. In this structure, an interdiffusion barrier layer **106** or **206** is required to prevent interdiffusion of copper and aluminum. If the underlying interconnect layer is another material such as TiW or W which does not interdiffuse with AlCu, the barrier layer **106** or **206** may be omitted and the ORBS layer **320** or **420** may be deposited directly on the underlying interconnect.

[0022] Overlying aluminum or aluminum copper is used in FIGS. **3** and **4** for illustration. Other overlying metals such as nickel palladium alloy may be used for the overlying bondpad **110** or overlying interconnect **210** material instead of aluminum or aluminum copper.

[0023] When the underlying metal layer is formed by deposition, pattern, and etch instead of by a damascene process, two options for the embodiment ORBS layer are available. As with an underlying metal geometry formed using a damascene process, a contact opening may be formed in a dielectric layer that overlies the underlying metal layer and the ORBS layer may be deposited on the dielectric layer and into the contact opening as described above. Alternatively, for metal geometries formed by deposition, pattern, and etch the ORBS layer may be deposited on the underlying metal layer (or on a barrier layer on the underlying metal layer) prior to patterning and etching to form the underlying metal layer geometry. In this alternative structure a contact opening is etched through an overlying dielectric layer stopping on the ORBS layer. This contact opening with the ORBS layer in the bottom may be exposed to air for an extended time (up to 24 hours) with little (less than 2×) increase in contact resistance.

[0024] A structure in which the underlying metal layer **510** is deposited, patterned and etched and the embodiment oxidation resistant barrier layer **520** is deposited into a contact opening in a dielectric **104** overlying the underlying metal layer **510** is illustrated in FIG. **5**B. The underlying metal layer **510** to which contact is made may be a metal resistor or an electrical fuse (efuse) or a top plate of a metal-to-metal capacitor for example.

[0025] The oxidation resistant barrier layer **520** is deposited into openings in the dielectric **104** overlying the metal layer **510** to form electrical contact to underlying metal layer **510**, as shown in FIG. **5**A. Top metal **110** which overlies the oxidation resistant barrier **520** may be used to form a bondpad or may be used as an upper layer of interconnect.

In this example, a metal which does not require an interdiffusion barrier layer is used for illustration so the oxidation resistant barrier **520** may be deposited directly onto the underlying metal layer **510**.

[0026] The ORBS layer which may be nitrogen rich TaN as described previously provides low and consistent contact resistance across a wafer and also increases the span of time (process window) that the wafer may be exposed to air between oxidation resistant barrier layer **520** deposition and top metal **110** deposition thus improving manufacturability.

[0027] Another structure in which an embodiment oxidation resistant barrier layer **620** is deposited on the underlying metal layer **610** prior to patterning and etching to form the underlying metal layer **610** geometry is shown in FIG. **6**B. The lower metal layer **610** for example, may be a top capacitor plate or a metal resistor. An optional interdiffusion barrier layer may be deposited on the underlying metal layer **610** prior to deposition of the ORBS layer **620** if needed.

[0028] In this structure, contact or via openings are etched through an overlying dielectric layer **104** and stop on the ORBS layer **620** which is on top of the underlying metal layer **610**, as shown in FIG. **6**A. The top metal **110** is deposited directly onto the ORBS layer **620** that is exposed in the bottom of the contact or via openings. The ORBS layer **620** may be exposed to air for up to 24 hours with less than a **2***x* increase in resistance. In addition the distribution of contact or via resistance across contacts across an IC chip or across an IC wafer remains tightly distributed.

[0029] FIG. **7** is a process flow diagram for a method for forming contacts using an embodiment ORBS layer such as those shown in FIGS. **3**A, **3**B, **4**A, **4**B, and **5**A and **5**B.

[0030] In step **700** a contact pattern is formed on a dielectric layer **104** overlying the underlying metal **102** (FIG. **3**A) or **202** (FIG. **4**A) or **510** (FIG. **5**A) and openings are etched through the dielectric layer **104** (FIG. **3**A, **5**A) or **204** (FIG. **4**A) stopping on the underlying metal layer **102/202/510**.

[0031] In step **702** an optional interdiffusion barrier layer **106** (FIG. **3**A) or **206** (FIG. **4**B) may be deposited over the dielectric layer **104** or **204** and into the contact opening. A degas step (for example a bake at a temperature in the range of 250° C. to 400° C. under reduced pressure) and/or a presputter clean step (for example an argon presputter clean) or a reactive preclean (for example a high bias preclean with hydrogen plus argon or hydrogen plus helium) may be performed prior to the interdiffusion barrier layer **106** (FIG. **3**A) or **206** (FIG. **4**A) deposition. FIGS. **3**A and **4**A illustrate a process flow that incorporates the optional interdiffusion barrier layer **106** or **206**. FIG. **5**A illustrates a process flow that does not incorporate an interdiffusion barrier layer. The interdiffusion barrier layer may be TaN or TiN with a thickness between about 60 nm and 90 nm and a nitrogen content between about 0 atomic % and 12 atomic %.

[0032] In step **704** the embodiment oxidation resistance barrier surface (ORBS) layer, **320** (FIG. **3**A) or **420** (FIG. **4**A) is deposited. The ORBS layer, **320** (FIG. **3**A) or **420** (FIG. **4**A), may be a high nitrogen content TaN layer with a thickness between about 5 nm and 15 nm and a nitrogen content of about 20 atomic % to 35 atomic %. One tool that the ORBS film may be deposited in is an EnCoRel chamber on the Applied Endura platform. In this tool, the ORBS layer may be deposited at room temperature with a pressure between about 2.5 and 5 torr, a power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W and a flow rate of nitrogen in the range of about 115 to 125 sccm. The deposition time may vary depending upon the deposition conditions. A time sufficient to deposit a TaN film with a thickness in the range of 5 nm to 15 nm is used.

[0033] Other deposition tools with different deposition conditions may be utilized by those skilled in the art to produce an equivalent ORBS TaN film with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 atomic % to 35 atomic %.

[0034] In step **706** the ORBS film may be exposed to air for an extended length of time if desired. At least a short exposure to air may be desirable. The air exposure may affect the grain structure and electromigration resistance of subsequently deposited interconnect or bondpad metal. The ORBS film enables the IC wafer to be exposed to air for an extended period of time (24 hours) with less than a **2***x* increase in resistance. In addition the distribution of resistance of all the contacts across an IC chip and across an IC wafer remains tightly distributed.

[0035] In step **708** an upper metal used for either interconnect or bondpad formation is deposited on the oxidation resistant barrier surface (ORBS) layer.

[0036] In step **710** the upper metal used for either interconnect or bondpad formation is patterned.

[0037] In step **712** the upper metal used for either interconnect or bondpad formation is etched and the ORBS material is etched.

[0038] In step **714** the interdiffusion barrier layer is etched if it is present.

[0039] FIG. **8** is a process flow diagram for a method for forming contacts using an ORBS layer **620** (FIG. **6**A) that is deposited on an underlying metal layer **610** prior to patterning and etching to form the underlying metal geometry **610** is shown in FIGS. **6**A and **6**B.

[0040] In step **800** the underlying metal layer **610** is deposited.

[0041] In step **802** an optional interdiffusion barrier layer is deposited to prevent interdiffusion of the underlying metal layer **610** with the overlying metal layer **110** if it is needed. If it is not needed the embodiment ORBS layer **620** may be deposited directly on the underlying metal layer **610**. If the underlying metal layer has been exposed to air, a degas step may be used. The degas step (for example a bake at 250 C to 400 C under reduced pressure) and/or a presputter clean step (for examples an argon presputter clean) or a reactive preclean (for example a high bias preclean with hydrogen plus argon or hydrogen plus helium) may be performed prior to the ORBS layer **620** deposition.

[0042] In step **804** the ORBS layer **620** is deposited on the underlying metal layer **610**. The ORBS layer **620** may be a high nitrogen content TaN layer with a thickness between about 5 nm and 15 nm and a nitrogen content of about 20 atomic % to 35 atomic %. One tool that the ORBS film may be deposited in is an EnCoRel chamber on the Applied Endura platform. In this tool The ORBS layer may be deposited at room temperature with a pressure between about 2.5 to 5 torr, a power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W and a flow rate of nitrogen in the range of about 115 to 125 sccm. The deposition time may vary depending upon the deposition conditions. A time sufficient to deposit a TaN film with a thickness in the range of 5 nm to 15 nm is used.

[0043] Other deposition tools with different deposition conditions may be utilized by those skilled in the art to

produce an equivalent ORBS TaN film with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 atomic % to 35 atomic %.

[0044] In step **806** the underlying metal is patterned and etched to form the underlying interconnect geometry **610**. The ORBS layer **620** is etched first. The optional interdiffusion barrier layer is etched next if it is present. The underlying metal **610** is then etched.

[0045] In step **808** a dielectric layer **104** such as silicon dioxide or polyimide is deposited over the underlying dielectric **100** and metal layer **610**.

[0046] In step **810** a pattern is formed on the dielectric layer **104** with openings over the underlying metal geometry **610**. The dielectric material is etched out of the openings stopping on the ORBS layer **620**. The ORBS layer **620** enables the IC wafers to be exposed to air for an extended period of time (24 hours) with little (less than 2×) increase in resistance. In addition the ORBS layer **620** provides for a tight distribution of contact resistance across the IC chip and across the IC wafer.

[0047] In step **812** an upper metal used for either interconnect or bondpad formation is deposited on the dielectric layer **104** and on the oxidation resistant (ORBS) barrier layer in the bottom of the contact openings.

[0048] In step **814** the upper metal used for either interconnect or bondpad formation is patterned and etched to form the upper interconnect metal geometries **110**.

[0049] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only and not limitation. Numerous changes to the disclosed embodiments can be made in accordance with the disclosure herein without departing from the spirit or scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above described embodiments. Rather, the scope of the invention should be defined in accordance with the following claims and their equivalents.

1-7: (canceled)

8: A process of forming an integrated circuit, comprising the steps:

forming an underlying metal geometry on a first dielectric;

depositing a second dielectric layer over the underlying metal geometry and over the first dielectric;

forming a contact photo resist pattern on the second dielectric layer with a contact opening over the underlying metal geometry;

etching a contact opening through the second dielectric layer and stopping on the underlying metal geometry;

depositing an overlying metal layer in the contact opening in the second dielectric layer;

forming an oxidation resistant barrier layer between the underlying metal geometry and the overlying metal layer wherein the oxidation resistant barrier layer is TaN or TiN with a nitrogen content of at least 20 atomic percent and a thickness of at least 5 nm;

forming a photo resist pattern on the overlying metal layer with a geometry covering the contact opening; and

etching the overlying metal layer with the photo resist pattern to form an overlying metal geometry.

9: The process of claim **8**, wherein forming the oxidation resistant barrier layer comprises depositing an oxidation resistant barrier layer on the second dielectric layer and on the sides and bottom of the contact opening.

10: The process of claim **9**, wherein the oxidation resistant barrier layer is deposited on the underlying metal geometry prior to depositing the second dielectric layer.

11: The process of claim **8** further comprising the step of exposing the oxidation resistant barrier layer to air for a period of time up to 24 hours prior to the step of depositing the overlying metal layer.

12: The process of claim **8** further comprising the step of depositing an interdiffusion barrier layer prior to the step of depositing the oxidation resistant barrier layer.

13: The process of claim **12**, wherein the interdiffusion barrier layer is a TaN or TiN layer with a thickness between 60 nm and 90 nm and a nitrogen content in the range of 0 to 12 atomic percent.

14: The process of claim **8**, wherein the oxidation resistance barrier layer is a TaN layer with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 to 35 atomic percent.

15: The process of claim **8**, wherein the oxidation resistant barrier layer is TaN with a thickness in the range of 5 nm to 15 nm deposited at room temperature with a pressure between about 2.5 to 5 torr, a power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W, and a flow rate of nitrogen in the range of about 115 to 125 sccm.

16: A process of forming an integrated circuit, comprising the steps:

depositing an underlying metal layer on a first dielectric layer;

depositing an oxidation resistant barrier layer on the underlying metal layer wherein the oxidation resistant barrier layer is TaN or TiN with a nitrogen content of at least 20 atomic percent and a thickness of at least 5 nm.

forming a photo resist pattern on the oxidation resistant barrier layer;

etching the oxidation resistant barrier layer and etching the underlying metal layer to form an underlying metal geometry;

depositing a second dielectric layer over the underlying metal geometry and over the first dielectric layer;

forming a contact photo resist pattern on the second dielectric layer with a contact opening over the underlying metal geometry;

etching a contact opening through the second dielectric layer and stopping on the oxidation resistant barrier layer on the underlying metal geometry;

depositing an overlying metal layer wherein the overlying metal layer fills the contact opening in the second dielectric layer;

forming a photo resist pattern on the overlying metal layer; and

etching the overlying metal layer to form an overlying metal geometry which covers the contact opening in the second dielectric layer.

17: The process of claim **16**, wherein the oxidation resistant barrier layer is TaN with a thickness in the range of 5 nm to 15 nm deposited at room temperature with a pressure between about 2.5 to 5 torr, a power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W, and a flow rate of nitrogen in the range of about 115 to 125 sccm.

18: The process of claim **16**, further comprising the step of depositing an interdiffusion barrier layer prior to the step of depositing the oxidation resistant barrier layer.

19: The process of claim **18**, wherein the interdiffusion barrier layer is a TaN or TiN layer with a thickness between 60 nm and 90 nm and a nitrogen content in the range of 0 to 12 atomic percent.

20: The process of claim **16**, wherein the oxidation resistance barrier layer is a TaN layer with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 to 35 atomic percent.

21: A process of forming an integrated circuit, comprising the steps:

forming an underlying metal geometry over a first dielectric;

depositing a second dielectric layer over the first dielectric;

etching a contact opening through the second dielectric layer;

depositing an overlying metal layer in the contact opening;

forming an oxidation resistant barrier layer between the underlying metal geometry and the overlying metal layer wherein the oxidation resistant barrier layer is TaN or TiN with a nitrogen content of at least 20 atomic percent and a thickness of at least 5 nm; and

etching the overlying metal layer to form an overlying metal geometry.

22: The process of claim **21**, wherein forming the oxidation resistant barrier layer comprises depositing an oxidation resistant barrier layer on the second dielectric layer and on the sides and bottom of the contact opening.

23: The process of claim **21**, wherein the oxidation resistant barrier layer is deposited on the underlying metal geometry prior to depositing the second dielectric layer.

24: The process of claim **21**, further comprising the step of exposing the oxidation resistant barrier layer to air for a period of time up to 24 hours prior to the step of depositing the overlying metal layer.

25: The process of claim **21**, further comprising the step of depositing an interdiffusion barrier layer prior to the step of depositing the oxidation resistant barrier layer.

26: The process of claim **25**, wherein the interdiffusion barrier layer is a TaN or TiN layer with a thickness between 60 nm and 90 nm and a nitrogen content in the range of 0 to 12 atomic percent.

27: The process of claim **21**, wherein the oxidation resistance barrier layer is a TaN layer with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 to 35 atomic percent.

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