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(54) **CHIP STACK STRUCTURE USING CONDUCTIVE FILM BRIDGE ADHESIVE TECHNOLOGY**

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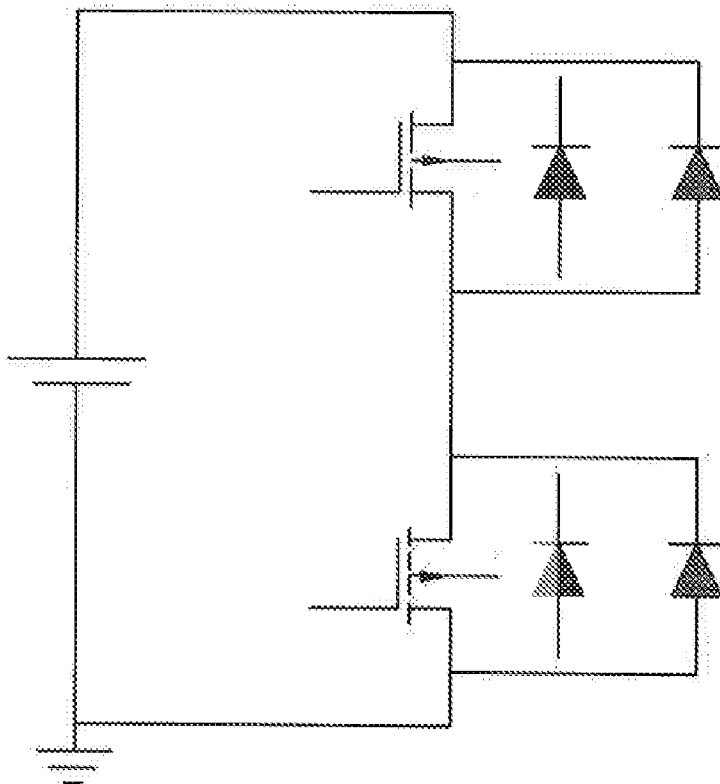
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(57) **ABSTRACT**

A chip stack structure using conductive film bridge adhesive technology comprises a substrate, a first chip, at least one bridge element, a conductive film, and a second chip. The first chip is electrically connected to a first electrode of the substrate. The at least one bridge element has a first bridge surface and a second bridge surface at two ends, and the first bridge surface and the second bridge surface are electrically connected to the first chip and a second electrode of the substrate, respectively. The conductive film is electrically connected to the first bridge surface of the at least one bridge element. The second chip is stacked and electrically connected to the conductive film. Thus, the structure of the present invention not only facilitates the ease of stacking the chips but also increases the effectiveness of the chips heat dissipation and ability of withstanding electrical current.



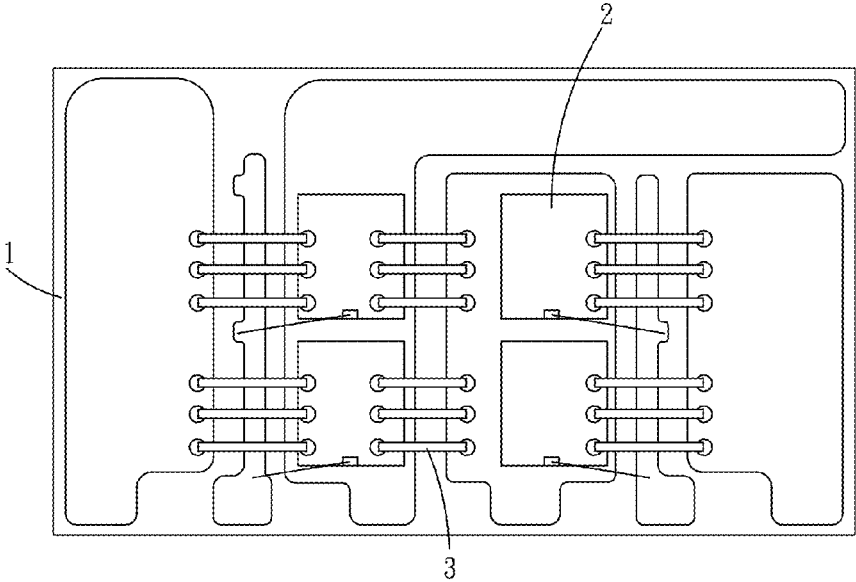


FIG. 1
PRIOR ART

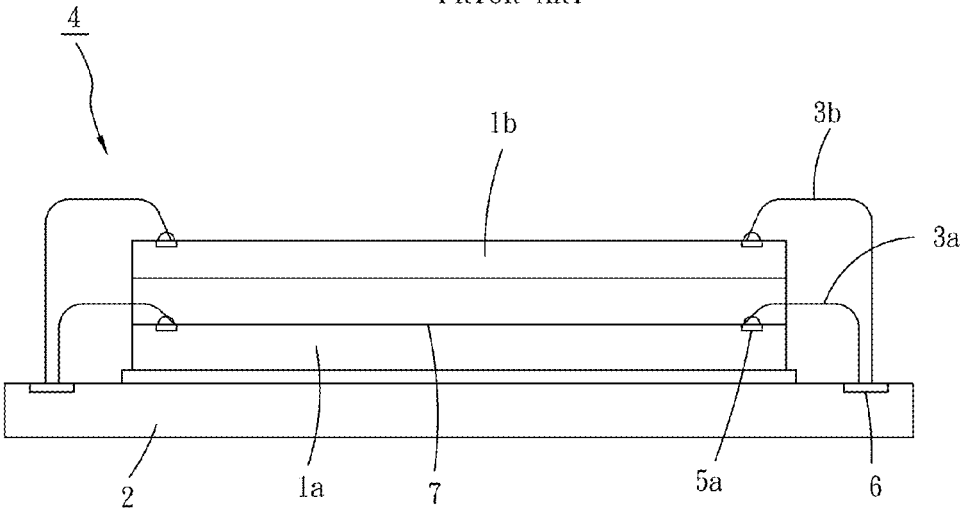


FIG. 2
PRIOR ART

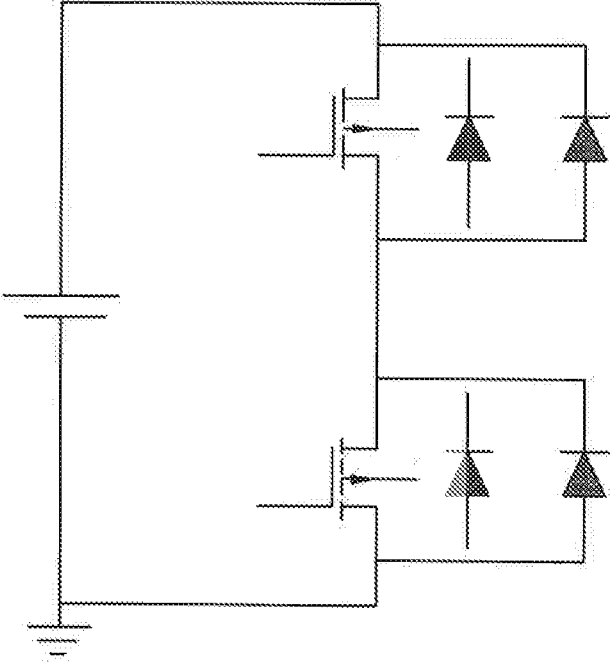


FIG. 3

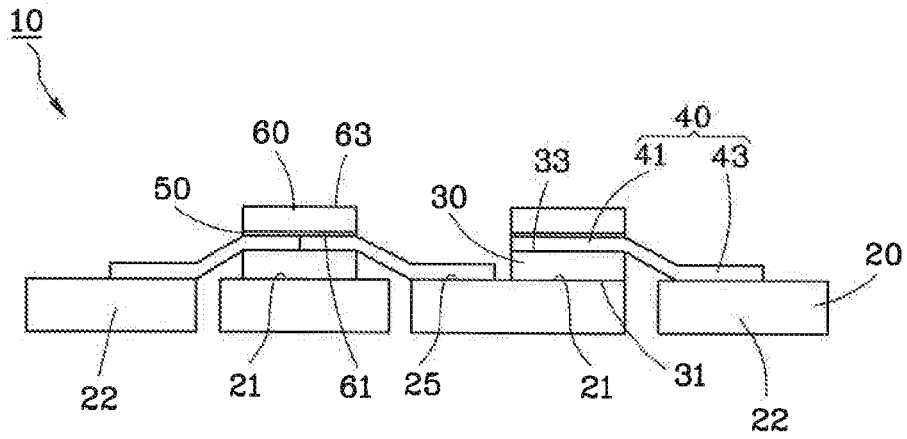


FIG. 4

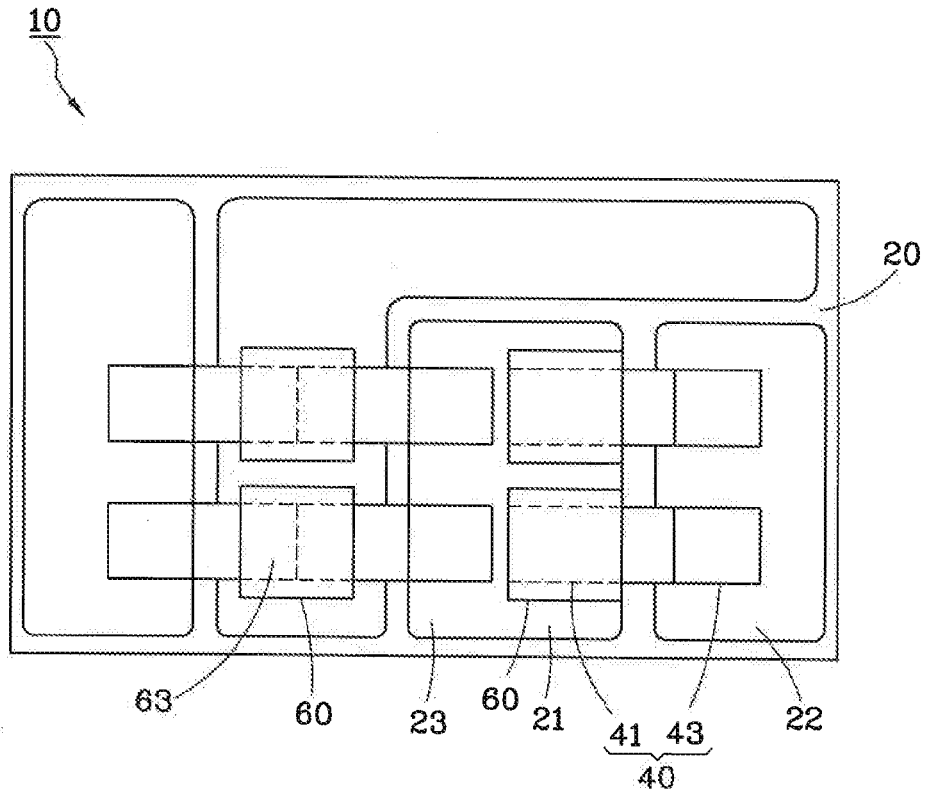


FIG. 5

CHIP STACK STRUCTURE USING CONDUCTIVE FILM BRIDGE ADHESIVE TECHNOLOGY

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention is related to chip stack structure, especially related to a chip stack structure using conductive film bridge adhesive technology.

[0003] 2. Description of Related Art

[0004] Since a single chip cannot withstand the electrical current of an entire system, it is generally required to use two or more chips to overcome this problem, however, the substrate area will be have to be increased due to placing the chips horizontally. As shown in FIG. 1, an integrated power module has a plurality of separated chips **1** disposed on a single substrate **2**, and then welding wires **3** are bonded to electrically connect the chips with each other. However, the overall size of the package increases because the chip **1** becomes more dense in this kind of structure.

[0005] With the advancement of technology, electronic products tend towards miniaturization and providing high performance to meet the needs of customers. In order to improve the performance and the capacity rate of a single package structure, three-dimensional (3D) package is widely adopted in the present day. Two or more chips **1** are stacked in a single package structure in order to provide a 3D package with compactly stacked and interconnected chips **1**. As shown in FIG. 2, a conventional chip stack structure **4** is disposed with a plurality of chips, which are stacked up and down on a substrate **2**. In the chip stack structure **4**, a first chip **1a** is adhered to the substrate **2** by an adhesive, and a plurality of first welding wires **3a** are bonded and electrically connected to first pads **5a** on the surface of the first chip **1a** and contacts **6** on the substrate **2**. Then, a second chip **1b** is disposed on the first chip **1a**. The adhesive **7** is applied between the first chip **1a** and the second chip **1b** in advance to adhere the second chip **1b** to the first chip **1a** and partially covers the first welding wires **3a**. The thickness of the adhesive **7** exceeds the arc height of the first welding wires **3a** in case of the first welding wires **3a** make contact with the second chip **1b**. After stacking the second chip **1b**, a plurality of second welding wires **3b** are bonded to and electrically connected to second pads **5b** of the second chip **1b** and the contacts **6** on the substrate **2**. Both this chip stack structure **4** and the one recited above use wire bonding for electrical connection between chips so there isn't any effective heat dissipation structure between the chips **1a**, **1b**. When the heat can't be timely dissipated, the effectiveness of the chips will decrease due to the increase in temperature. Moreover, the adhesive **7** in this case is easily interfered with due to high temperatures and welding wires, and there will be voids gathered in the adhesive **7**. Once the number of voids is reaches a critical capacity, the adhesive bond of the adhesive **7** will be greatly reduced, which leads to the chips **1a**, **1b** not being able to be stacked successfully.

[0006] To sum up the above, the conventional chip stack structure has the above drawbacks and needs to be improved.

BRIEF SUMMARY OF THE INVENTION

[0007] The main objective of the present invention is to provide a chip stack structure using conductive film bridge adhesive technology. The chip stack structure not only facili-

tates the case of stacking the chips but also increases the effectiveness of the chips heat dissipation and ability of withstanding electrical current.

[0008] In order to achieve the above objective, the present invention utilizes of the chip stack structure using conductive film bridge adhesive technology. The chip stack structure comprises a substrate, a first chip, at least one bridge element, a conductive film and a second chip. The substrate comprises a first electrode and a second electrode. The first chip is electrically connected to the first electrode of the substrate. The at least one bridge element has a first bridge surface and a second bridge surface at two ends, and the first bridge surface and the second bridge surface are electrically connected to the first chip and the second electrode of the substrate, respectively. The conductive film is electrically connected to the first bridge surface of the at least one bridge element. The second chip is stacked and electrically connected to the conductive film.

[0009] The first chip has a first connecting surface and a second connecting surface, the first connecting surface is disposed on the first electrode of the substrate, and the first bridge surface of the at least one bridge element is connected to the second connecting surface.

[0010] The substrate further comprises a third electrode, the second bridge surface of the at least one bridge element is electrically connected to the third electrode.

[0011] The conductive film is a tin film.

[0012] The first bridge surface and the second bridge surface of the at least one bridge element are flat surfaces.

[0013] The at least one bridge element is a copper film.

[0014] Thus, the structure of the present invention not only facilitates the ease of stacking the chips but also increases the effectiveness of the chips heat dissipation and ability of withstanding electrical current.

[0015] In order to facilitate the examiner to have a further knowledge and understanding of the present objectives of the present invention, technical features, and the effects, the embodiments corresponding to drawings are illustrated as follows.

[0016] In order to facilitate the examiner to have a further understanding of components, features, and objectives thereof, the embodiments corresponding to drawings are illustrated as follows. However, the following description is an embodiment provided only for illustrating the technical content and features of the present invention. Various simple modifications, replacements, or omitted components made by people skilled in this art without violating the spirit of the present invention after they understand the technical content and features should fall within the scope the present invention intends to protect.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] FIG. 1 is a top view of a conventional chip package structure, and it mainly shows that aluminum wires electrically connect the chips and the substrate by wire bonding in the conventional manner.

[0018] FIG. 2 is a cross-sectional view of a conventional chip stack structure, which mainly shows the arrangement relationship between the first chip and the second chip.

[0019] FIG. 3 is a circuit diagram of a half bridge module.

[0020] FIG. 4 is a cross-sectional view of a chip stack structure using conductive film bridge adhesive technology of

a preferred embodiment of the present invention, and it mainly shows the aspect that a plurality of chip stack structures.

[0021] FIG. 5 is a top view of a chip stack structure using conductive film bridge adhesive technology of a preferred embodiment of the present invention, and it mainly shows the change area after the plurality of chip are stacked.

DETAILED DESCRIPTION OF THE INVENTION

[0022] In order to describe the structure, technical features, and effects of the present invention in detail, a preferred embodiment corresponding to following drawings is illustrated as follows.

[0023] Please refer to FIG. 3 to FIG. 5, which show a chip stack structure 10 using conductive film bridge adhesive technology of a preferred embodiment of the present invention. The chip stack structure 10 comprises:

[0024] A substrate 20, which comprises a first electrode 21 and a second electrode 23.

[0025] A first chip 30, which is electrically connected to the first electrode 21 of the substrate 20.

[0026] At least one bridge element 40, which is a copper film and has a first bridge surface 41 and a second bridge surface 43 at two ends of the at least one bridge element 40. The first bridge surface 41 and the second bridge surface 43 are electrically connected to the first chip 30 and the second electrode 23 of the substrate 20, respectively. In the preferred embodiment of the present invention, the first bridge surface 41 and the second bridge surface 43 of the at least one bridge element 40 are flat surfaces. Since the bridge element 40 has a comparatively large conductive area, it replaces the conventional aluminum wire to improve the effect of withstanding electrical current.

[0027] A conductive film 50, which is a tin film and is electrically connected to the first bridge surface 41 of the at least one bridge element 40. Thereby, the conductive film 50 can be comparatively stably disposed on the first bridge surface 41 of the at least one bridge element 40.

[0028] A second chip 60, which is stacked and electrically connected to the conductive film 50. Since the conductive film 50 is a sheet-like structure, the second chip 60 can be placed plainly. Furthermore, because the second chip 60 conducts the first chip 30 and the at least one bridge element 40 through the tin conductive film 50, heat generated by the first and second chips 30, 60 can be quickly and efficiently dissipated to prevent overall performance degradation due to being unable to dissipate the heat in a timely manner.

[0029] It should be noted that the conductive film 50 of the chip stack structure of the present invention is a tin film. Therefore, there won't be any voids generated in the conductive film 50 during the melting process when the vacuum reflow furnace is welding. This way helps the adhesion and prevents the second chip 60 from peeling.

[0030] In addition, the numbers of chip stack layers of the chip stack structure 10 using the conductive film bridge adhesive technology and the bridge element 40 are not limited to the numbers of the abovementioned. The capacity of the structure can be improved by interlacing and stacking a plurality of the bridge elements 40, a plurality of the conductive films 50, and a plurality of the second chip 60 on the first chip 30. Or, as shown FIGS. 4 and 5, the substrate 20 further has a third electrode 25. The second surface 43 of the at least one second bridge element 40 is electrically connected to the third electrode 25. The first chip 30 has a first surface 31 and a

second connecting surface 33. The first connecting surface 31 is disposed on the first electrode 21 of the substrate 20. The first bridge surface 41 of the at least one bridge element 40 is connected to the second connecting surface 33. The second chip 60 has a first connecting surface 61 and a second connecting surface 63. The first connecting surface 61 of the second chip 60 is connected to the conductive film 50. The second connecting surface 63 of the second chip 60 can be continuously stacked with the bridge element 40 and the conductive film 50 as the aforesaid structure in order for provide various chip stack structures to achieve different circuit layouts.

[0031] In conclusion, the chip stack structure using conductive film bridge adhesive technology of the present invention utilizes the first bridge surface and the second bridge surface, which are both flat and have a large conductive area, of the bridge element, to improve the effectiveness of withstanding electrical current and to provide the conduction film to be disposed plainly. Thereby, the heat generated by each of the chips will be quickly and effectively dissipated to prevent overall performance degradation due to being unable to dissipate the heat in a timely manner. Moreover, because the conductive film is a tin film, there won't be any void generated in the conductive film during the melting process when the vacuum reflow furnace is welding. This way supports the adhesive bond and prevents the second chip from peeling.

[0032] The components disclosed in the abovementioned embodiment of the present invention are only illustrative and not intended to limit the scope of the present invention. Substitutions or changes of other equivalent elements should be covered by the claims of the present invention.

1. A chip stack structure using conductive film bridge adhesive technology, comprising:

a substrate comprising a first electrode and a second electrode;

a first chip, electrically connected to the first electrode of the substrate;

at least one bridge element having a first bridge surface and a second bridge surface at two ends, the first bridge surface and the second bridge surface being electrically connected to the first chip and the second electrode of the substrate, respectively;

a conductive film, electrically connected to the first bridge surface of the at least one bridge element; and

a second chip, stacked and electrically connected to the conductive film,

wherein the first chip has a first connecting surface and a second connecting surface, the first connecting surface is disposed on the first electrode of the substrate and the first bridge surface of the at least one bridge element is connected to the second connecting surface.

2. (canceled)

3. The chip stack structure using conductive film bridge adhesive technology in claim 1, wherein the substrate further comprises a third electrode, the second bridge surface of the at least one bridge element is electrically connected to the third electrode.

4. The chip stack structure using conductive film bridge adhesive technology in claim 1, wherein the conductive film is a tin film.

5. The chip stack structure using conductive film bridge adhesive technology in claim 1, wherein the first bridge surface and the second bridge surface of the at least one bridge element are flat surfaces.

6. The chip stack structure using conductive film bridge adhesive technology in claim 1, wherein the at least one bridge element is a copper film.

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