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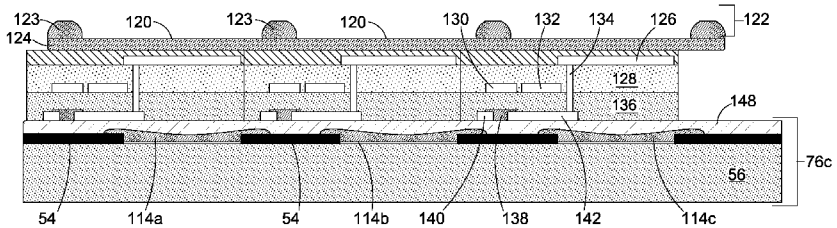


Fig. 3d

(57) **Abstract**: The invention relates to a display device and a method of manufacture thereof. The device comprises a display medium (120) comprising a plurality of pixels; a control component (76c) comprising an array of pixel electrodes (126) controlled by an array of transistors including a plurality of transistors (130, 138, 140, 142) comprising a light-sensitive semiconductor channel (138); and a filter array (78c) comprising an array of relatively transmissive filters (114a, 114b, 114c) interspersed with a plurality of relatively non-transmissive areas (54). The control component (76c) is positioned between said filter array (78c) and said display medium (120). Each relatively transmissive filter (114a, 114b, 114c) is aligned with one of the pixel electrodes (126) and each relatively non-transmissive area (54) is aligned with one of the light-sensitive semiconductor channels (138) whereby said semiconductor channel (138) in each transistor (130, 138, 140, 142) is protected from light exposure.

WO 2015/177539 A1

Display device

FIELD OF THE INVENTION

This invention relates to a display device comprising a transistor having a light-sensitive component.

BACKGROUND TO THE INVENTION

Display devices using switchable display media such as LCDs or LEDs are known in the art. The display medium generally has an active matrix structure, for example LCDs used in high-resolution colour displays (e.g. computer monitors and televisions). A matrix or array of thin-film transistors (TFTs) is used for driving the display medium. Each pixel of the display medium has its own dedicated transistor, which enables each column line to access one pixel. Typically, for amorphous silicon or polycrystalline silicon TFTs, the most commonly used geometry is a bottom gate with top drain and source electrodes.

Organic thin-film transistors (OTFTs) are also known. In OTFTs the channel is made from an organic semiconductor. OTFTs are light sensitive and thus, they must be shielded from light that reaches the OTFT layer.

The present applicant has recognised the need to protect the light sensitive component within the display device.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a display device comprising a display medium comprising a plurality of pixels; a control component comprising an array of pixel electrodes controlled by an array of transistors including a plurality of transistors comprising a light-sensitive semiconductor channel; and a filter array comprising an array of relatively transmissive filters interspersed with a plurality of relatively non-transmissive areas. Each pixel electrode controls a pixel in said display medium. Said control component is positioned between said filter array and said display medium. Each relatively transmissive filter is aligned with one of the pixel

electrodes and each relatively non-transmissive area is aligned with one of the light-sensitive semiconductor channels whereby said semiconductor channel in each transistor is protected from light exposure.

By relatively transmissive and relatively non-transmissive, it is meant that significantly more light passes through each filter than the area. The term "relatively" is thus comparing the relative transmissivity of the filter with that of the interspersed areas. In use, the user views the display medium through both the filter array and the control component. Thus, each relatively transmissive filter (and corresponding pixel electrode) is substantially transparent so as not to obscure a user's view of the associated pixel on the display medium. By contrast, each relatively non-transmissive area is substantially opaque and thus a user cannot view the display medium therethrough. There may be only filters and non-transmissive areas with the non-transmissive areas forming a matrix around the filters. Alternatively, the filter array may comprise other portions which are not used to protect the semi-conductor channel nor are transparent. At least part of the filter array shields other components in the device from light exposure and thus the filter array may be termed a light-shielding component.

The optical density of an opaque (black) material is quantified by its absorbance A which is defined as:

$$A_{\lambda} = log_{10}\left(\frac{I_0}{I}\right)$$

where **I** is the intensity of the light at a specific wavelength **λ**, that has passed through a sample and $\mathbf{I_0}$ is the intensity of light before it enters the sample. Thus, in effect, absorbance is a function of wavelength though it is often quoted as a single figure. For example, an absorbance of 3 will block 99.9% of light giving a maximum contrast ratio of 1000:1. In one example, the relatively non-transmissive areas have an absorbance of greater than about 2 and preferably at least 3 at all wavelengths that impair the performance of the transistor, particularly wavelengths corresponding to the HOMO-LUMO bandgap and higher energies.

The device may be monochrome or colour. In a monochrome embodiment, the filter array may comprise a black matrix that prevents light from reaching the light sensitive channel, i.e. said interspersed areas may form a black matrix around the filters. In a colour embodiment, said filters may be colour filters. Thus, said filter array may further

comprise a plurality of colour filters, e.g. red, green, blue, interspersed with said areas of opaque material. The colour filters may be RGB filters used to provide an RGB LCD. The colour filter patterning may be formed by photolithography or other suitable fabrication processes.

The transistor may be an organic transistor, particularly a thin film transistor. In other words, the semiconductor channel may comprise an organic semiconductor material. Such organic materials are particularly sensitive to light and thus it is important to prevent light exposure to them. In relation to the semiconductor channel, light-sensitive means that one or more characteristics of the channel are changed upon exposure to excessive amounts of light. For example, in this context, the two principle effects of light exposure are a positive threshold voltage (V^{th}) shift and an Increase in 'off-current' (Leakage current seen when the TFT is biased 'Off'). More information on the effect of light exposure can be found for example, in "Light-Exposure Effects on Electrical Characteristics of 6,13-Bis(triisopropylsilylethynyl)Pentacene/CdTe Composite Thin-Film Transistors" by Park et al published in the Japanese Journal of Applied Physics, Vol 52, Number 5 or in "Photoleakage Currents in Organic Thin Film Transistors published in Applied Physics Letters, Vol. 88, 071106 (2006).

The display medium may be an optically switchable medium, e.g. each pixel within the display medium may be switched by the corresponding pixel electrode. For example, the display medium may be a liquid crystal medium or a white light-emissive medium such as white LEDs which form the switchable light source. The device may further comprise a light source, e.g. for a liquid crystal display medium. The light source may be provided on the opposite side of the display medium to the control component. In this case, a user is viewing the display medium through the filter array and the control component and the light source is thus a backlight. Alternatively, the light source may be provided on the opposite side of the filter array to the control component. In this case, a user is viewing the display medium through the filter array, the light source and the control component.

In the arrangement in which the light source is on the opposite side of the filter array to the control component, it will be appreciated that both ambient light on the viewing surface of the device and light from the light source reach the control component through the filter array. Accordingly, the relatively non-transmissive areas of the filter

array protect the light sensitive channel from both ambient light and from light from the light source. However, in the arrangement in which the light source is on the opposite side of the display medium to the control component, the light from the light source reaches the control component from the opposite side of the device to ambient light. In this arrangement, the light sensitive channel also needs to be protected from light from the light source. Each transistor generally comprises a source electrode, a drain electrode, a gate electrode and the semiconductor channel is between said source and drain electrodes. The gate electrode may be aligned with the semiconductor channel. In this way, the filter array and the gate electrode together protect the semiconductor channel from light exposure from two different directions.

Where a light source is required, e.g. for a liquid crystal display and is placed on the opposite side of the display medium to the control component, the light source may be separated from the display medium by one or more layers. None of these layers need to be aligned carefully with any of the other layers. For example, there may be a common electrode layer between the light source and display medium. There may also be a second polarising foil layer to polarise light from the light source before it enters the display medium. There may also be layers comprises a reflector and/or a waveguide depending on the nature of the light source.

The filter array may comprise a flexible plastic substrate. The substrate may be formed of a flexible polymer such as PVC, PET (polyethyleneterephthalate) or PEN (polyethelenemaphthalene). The filter array may comprise a polarizing foil layer. Such a layer protects the transistor from particular polarisations of (external/ambient) light.

Each component (display medium, control component, filter array, light source (where used)) of the device may be flexible to create a fully flexible device.

Said liquid crystal display medium may comprise a pair of alignment layers spaced apart by a plurality of spacers (at least two) with liquid crystal material in spaces between said pair of alignment layers. The liquid crystal material may be injected using any known technique.

Each pixel electrode of the control component may be aligned with a respective transistor in said array of transistors, e.g. each pixel electrode may be connected to a drain electrode of said respective transistor. The pixel electrodes drive the pixels in the display medium. As is well known in the art, a pixel is the smallest controllable element of a picture represented on the screen. Pixels are generally off or on and in this sense the display medium can be considered to be a switchable medium, e.g. switch each pixel on or off. The control component may also be considered to be driving the pixels and thus the control component may be termed a driving component.

According to a second aspect of the present invention, there is provided method of manufacturing a display device such as that described above. The method comprises: forming a filter array comprising an array of relatively transmissive filters and a plurality of relatively non-transmissive areas; forming an array of transistors over said filter array with each transistor comprising a semiconductor channel and wherein said forming step comprises aligning each semiconductor channel with one of said relatively non-transmissive areas in said filter array; forming an array of pixel electrodes over said array of transistors, wherein each said pixel electrode is connected to a respective transistor in said array of transistors; and forming a display medium over said array of pixel electrodes.

As set out above, a user views the display medium through the filter array and the transistor array and thus the device is effectively inverted after manufacture and before use. In this inverted structure, the semiconductor channel risk lights exposure from ambient light and this is avoided by aligning a non-transmissive area in the filter array with the channel. The filter array (or at least the non-transmissive areas thereof) effectively acts as a light-shielding component blocking external light from reaching the semiconductor channel which may be light sensitive as explained above. The key alignment process takes place in the second forming step. Thereafter, no further alignment of the different components is required when building or forming subsequent layers and thus manufacture is simplified.

A planarization layer may be formed on the filter array and the array of transistors may be formed on the planarization layer. In this way, there is no need for the array of transistors to be built up on a separate substrate. The planarization layer enables the

array of transistors (and hence the control component) to be formed directly onto the filter array (which may comprise colour filters as explained above).

Any conventional technique may be used to form the array of transistors and/or the array of pixel electrodes. For example, laser ablation may be used to pattern said source, drain and gate electrodes for each transistor and/or to pattern said pixel electrodes. Alternatively, the electrodes may be formed by depositing and patterning conductive layers through solution processing techniques such as, but not limited to, spin, dip, blade, bar, slot-die, or spray coating, inkjet, gravure, offset or screen printing. Alternatively, vacuum deposition such as evaporation, or sputtering followed by photolithographic patterning or other subtractive patterning techniques may be used. Moreover, the transistors may be any conventional transistors, e.g. top-gate electrodes. For a top-gate electrode, the gate electrode may be aligned with the semiconductor channel. As explained in more detail above, this effectively protects the channel from light exposure from the other direction to the protection provided by the filter array.

Similarly, a broad range of printing techniques may be used to deposit the semiconducting material in the semiconductor channel including, but not limited to, inkjet printing, soft lithographic printing, offset printing, blade coating or dip coating, curtain coating, meniscus coating, spray coating, or extrusion coating. Alternatively, the semiconducting material may be deposited as a thin continuous film and patterned subtractively by techniques such as photolithography or laser ablation.

Similarly, the display medium may be formed using any known technique. For example, the display medium may be a liquid crystal medium which may be formed by forming a first alignment layer; forming a spacer layer comprising a plurality of spacers on said first alignment layer; forming a second alignment layer on said spacer layer whereby said second alignment layer is spaced apart from said first alignment layer; and injecting liquid crystal material into space between said first and said second alignment layers.

As explained above, said user views the display through the filter array and thus there must be transparent areas to view the display. Furthermore, the device may be monochrome or colour. Accordingly, the method may further comprise forming said

filter array by forming a colour filter layer by interspersing a plurality of colour filters interspersed with areas of opaque material which may form a black matrix.

It will be appreciated that the various embodiments described above may be combined and in particular the method may be modified to reflect the detailed features of the device described above.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is diagrammatically illustrated, by way of example, in the accompanying drawings, in which:

Fig. 1a is a schematic cross-sectional view of a prior art LCD structure with a bottom-gate TFT;

Fig. 1b shows a zoomed-in view of part of Fig. 1a;

Fig. 2 is a schematic cross-sectional view showing a prior art LCD structure with a top-gate TFT;

Fig. 3a shows a schematic cross-sectional view of a device according to an embodiment of the invention;

Fig. 3b shows a schematic cross-sectional view of a control component for use in the device of Fig 3a;

Fig. 3c shows a schematic cross-sectional view of an alternative control component for use in the device of Fig 3a;

Figs 3d and 3e show schematic cross-sectional views of the components of Figs 3b and 3c with a filter array;

Fig. 4 shows a flowchart of the method for manufacturing an LCD structure according to Fig. 3a; and

Fig. 5 shows a block diagram of a system comprising an LCD structure according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

Figure 1a illustrates the conventional structure of a bottom-gate based liquid crystal device (LCD). In this known structure, liquid crystal material 20 is driven by an array of bottom-gate thin film transistors (TFT) 62 and is illuminated by a light source 70 located below the TFT array 62 (i.e. the LCD is back-lit by a backlight). The liquid crystal material is sandwiched between two components: a colour filter component 78a and a control component 76a. The two parts are typically manufactured separately and assembled with the liquid crystal material and light source to form the overall device.

The driver component 76a comprises a transparent TFT array substrate 12b (e.g. glass) supporting an array of TFT 62. (Details of the precise fabrication technique are not provided here but are well known in the art.) Each TFT is a bottom gate transistor (i.e. the gate electrode is located below the source and drain electrodes). A top pixel electrode layer 26 is disposed over the TFT array 62. The top pixel electrode layer 26 comprises a plurality of pixel electrodes with each pixel electrode being driven by a transistor in the TFT array to drive the liquid crystal material as required. Storage capacitor 64 is located beneath the TFT array. (Details of the control component and how the pixels are driven/controlled thereby are not provided here but are well known in the art.)

The colour filter component 78a comprises a colour filter substrate 12a. On one side of substrate 12a is disposed a colour filter layer which comprises an array of colour filters 14 interleaved with a black matrix 54. A common electrode layer 16 is provided adjacent the colour filter layer, and a liquid crystal alignment layer 18 is adjacent the common electrode layer. The common electrode layer 16 is an electrically conductive and optically transparent layer, and may be formed from, for example, indium tin oxide (ITO). A backlight panel 74 is provided on the other side of substrate 12a.

The separately manufactured colour filter component 78a and control component 76a are brought together to assemble the device, such that the liquid crystal (LC) alignment layer 18 (of the colour filter component) faces the TFT array 62 (of the control

component). The colour filter component 78a and control component 76a are spaced apart from each other to provide space for a liquid crystal material 20. At least two spacers 22 are provided between the two components to form a spacer layer. The spacer layer is used to maintain the cell gap of the liquid crystal layer. The two components are aligned to a high tolerance such that the black matrix 54 of the colour filter component 78a is aligned over the TFT array 62 to prevent reflections hitting the TFT (as described in more detail below). A sealant 68 seals the edges of the structure to keep the liquid crystal material in position. The liquid crystal material 20 is added to the assembly either just before the sealing of the LC cell (by, for example, a "one drop fill" process) or just after the sealing of the LC cell (by, for example, an "edge fill" process).

Finally, a light source 70 and backlight module 72 are provided below substrate 12b, such that the liquid crystal material 20 is illuminated from below by a "backlight".

Figure 1b is a zoomed-in view of an individual LCD pixel in the conventional bottom-gate LCD structure of Figure 1a. As mentioned above, the LCD is illuminated by a light source (not shown here) located below TFT array 62. The control component 76a comprises a transparent substrate (e.g. glass), onto which is disposed a gate electrode 30 for each TFT in the array. A source electrode 40 and drain electrode 42 for each TFT in the array are disposed spaced apart from each other and above the associated gate electrode 30. A semiconductor material 41 is disposed in a channel between, and at least partially on, the source and drain electrodes. In this conventional bottom-gate structure, the gate electrode 30 shields the semiconductor material 41 in the channel from light exposure from the backlight. As mentioned above, liquid crystal material 20 is disposed above the TFT array 62, and between a pixel electrode layer 26 and a common electrode layer 16. The common electrode layer 16 and the pixel electrode layer 26 are both formed of an electrically conductive and optically transparent material, such as indium tin oxide (ITO).

A user views the LCD of Figures 1a and 1b from above, i.e. through the colour filter layer 14. As indicated in Figure 1b, light from the backlight passes through the optically transparent pixel electrode layer 26 to the liquid crystal material 20, and then through the transparent common electrode layer 16 and colour filter layer 14. The location of each transistor in the TFT array 62 is laterally spaced apart from the location of each

colour filter 14 in the array and each pixel electrode 260 in order for light to illuminate each LCD pixel. If a transistor in the TFT array 62 were located directly beneath a colour filter 14, the electrodes of the TFT would interfere with the user's view of the LCD. Black matrix 54 is provided above the TFT array 62 so that an area of light opaque material (i.e. black material) is arranged above each transistor but not above any of the pixel electrodes. The black material protects each transistor, particularly the semiconductor material in the channel between source and drain electrodes, in the TFT array from external, environmental light exposure from above the TFT stack, and blocks any stray light from the backlight that is reflected off the TFT array (which would degrade image quality). Thus, in this conventional LCD structure, it is crucial that the colour filter component 78a and the control component 76a are aligned precisely during assembly of the LCD structure, in order to ensure that each light opaque area in the black matrix covers a transistor (and only a transistor) in the TFT array 62.

Figure 2 illustrates the conventional structure of a top gate TFT glass-based LCD. In this conventional structure, there is no natural light shield below the TFT array. Again the device comprises two components: a colour filter component 78b and a control component 76b which sandwich the liquid crystal material 20. The two components are typically manufactured separately and then brought together to assemble the LCD architecture.

The control component 76b comprises a transparent TFT array substrate 12b (e.g. glass) supporting the array of TFTs. The structure of each TFT 62 is conventional and comprises a source electrode 40 and drain electrode 42 on the substrate. The source and drain electrodes are disposed spaced laterally apart from each other on the glass substrate 12b. Semiconductor material is disposed in a channel 38 between, and at least partially on, the source and drain electrodes. A gate-insulating layer (i.e. gate dielectric) 36 is disposed on the semiconductor channel 38. A gate electrode 30 and a pixel capacitor 32 are disposed on the gate-insulating layer, such that the gate electrode and pixel capacitor are spaced apart laterally from each other. The gate electrode is aligned with the channel 38 and is above the source and drain electrodes so the TFT is a top gate transistor. A top pixel dielectric layer 28 is disposed over the gate electrode and pixel capacitor. A top pixel electrode 26 is disposed over dielectric layer 28. Via 34, which passes through the dielectric layer 28, electrically connects the top pixel electrode 26 to the drain electrode 42. A liquid crystal (LC) alignment layer 24

is disposed over the pixel electrode 26, such that the alignment layer is electrically connected to the pixel electrode 26. (Details of the precise fabrication technique for such a top gate TFT are not provided here but are well known in the art.)

The colour filter component 78b comprises a colour filter substrate 12a. On one side of substrate 12a is disposed a colour filter layer 14 comprising an array of colour filters interspersed with a black matrix. A common electrode layer 16 is provided over the colour filter layer, and a liquid crystal alignment layer 18 is disposed over the common electrode layer. The common electrode layer 16 is an electrically conductive and optically transparent layer, and may be formed from, for example, indium tin oxide (ITO). A polarising foil 10 is provided on the other side of substrate 12a to polarise and block external light as it enters the LCD device from above (to prevent degradation of image quality).

The separately manufactured colour filter component 78b and control component 76b are brought together to assemble the LCD structure, such that the liquid crystal (LC) alignment layer 18 (of the colour filter component) faces the LC alignment layer 24 (of the control component). The two components 78b and 76b are spaced apart from each other to provide space for a liquid crystal material 20. At least two spacers 22 are provided between the two components to form a spacer layer. The spacer layer is used to maintain the distance or cell gap between LC alignment layers 24 and 18 (i.e. respectively, the back and front of the liquid crystal panel). The two components are aligned to a high tolerance, and a sealant seals the edges of the structure to keep the liquid crystal material in position. The liquid crystal material 20 is added to the assembly in the space provided between the LC alignment layers 24 and 18, either just before the sealing of the LC cell (by, for example, a “one drop fill” process) or just after the sealing of the LC cell (by, for example, an “edge fill” process).

Finally, a light source and backlight module (i.e. control electronics) are provided below TFT array substrate 12b, such that the liquid crystal material 20 is illuminated from below by a “backlight”.

The conventional LCD of Figure 2 is formed in front of a light source to display images, i.e. such that the LCD is illuminated through the back. The light source is necessary to produce a visible image on the LCD panel as the liquid crystal material itself does not

produce light. Backlights illuminate the LCD from the side or back of the display panel, and can be provided by, for example, LEDs. Light from such a backlight (not shown) is guided to the LCD panel via a backlight waveguide 44, and through a polarising layer 10. The polarising layer 10 polarises light from the backlight to block out any undesirable light. Reflector 46, disposed below waveguide 44, is a reflective surface that sends stray light back up to the waveguide 44.

In the arrangement of Figure 2, it is possible for light from the backlight (which is intended to illuminate the liquid crystal material 20) to reach the TFT array. Furthermore, any stray external light that is not blocked by polarising foil 10 may be able to reach the TFT layer through the colour filter glass substrate 12a. As mentioned earlier, the colour filter component 78b includes a black matrix, which is able to block this stray light from reaching each transistor in the TFT array. However, if the conventional TFT was replaced with a light-sensitive OTFT, there is insufficient protection from light exposure from below the OTFT. It is possible to shield a top gate OTFT by providing a metal layer below the OTFT layer (which may be embedded in a planarization layer). Such a metal layer has the sole purpose of shielding the OTFT from light reaching the transistor through a glass substrate. However, such a metal layer (or an equivalent opaque layer) adds an extra layer to the LCD structure, resulting in an increase in the number of processing steps and in the overall manufacturing costs.

Turning now to Figure 3a, this illustrates an embodiment of the present invention. Broadly speaking, Figure 3a illustrates an arrangement in which a top gate, light-sensitive OTFT in an LCD is shielded from light exposure from both above and below the OTFT. This is achieved by inverting (i.e. turning upside-down) the conventional top-gate LCD structure without requiring any extra manufacturing steps. Thus, as indicated, a user views the LCD from the opposite side of the structure when compared to Figure 2. However, the user would not be aware of any change in the structure, and there is no change in image quality by inverting the top-gate structure. As explained in more detail below, the colour filter layer 114 including the black matrix are moved from their conventional position above the TFT array to below the TFT stack 152. Similarly, the light source for the liquid crystal material is moved from below the TFT array to above the TFT array (and thus becomes a top light rather than a back light). Such an

inverted structure requires the TFT array to be processed on top of the colour filter, which is itself an unconventional fabrication technique.

As can be seen from Figure 3a, the inverted structure still comprises the two components which in the known arrangements sandwiched the liquid crystal material 120, namely: a filter array 78c (or light shielding component) and a control component 76c. The terms filter array and light shielding component are used interchangeably throughout the rest of the description. However, here, the control component 76c is sandwiched between the liquid crystal material 120 and the colour filter component 78c, which effectively means that the liquid crystal material 120 is between the light and the control component. Thus, the semiconductor material 138 in the channel between the source and drain electrodes 140, 142 is protected from light exposure from the light source by the gate electrode 130 and from light exposure from ambient light on the side of device which is viewed by a user by the colour filter component 78c.

Figures 3b and 3c show two alternative control components which can be used in the arrangement of Figure 3a. In Figure 3b, each OTFT comprises a source electrode 140 and a drain electrode 142 separated by a channel 138 comprising light sensitive semiconducting material. A gate-insulating layer (i.e. gate dielectric) 136 is disposed on the semiconductor channel 138. A gate electrode 130 and a pixel capacitor 132 are on the gate-insulating layer 136, such that the gate electrode and pixel capacitor are spaced apart from each other. A top pixel dielectric layer 128 is disposed over the gate electrode and pixel capacitor. For each OTFT, a top pixel electrode 126 is disposed over dielectric layer 128. Via 134, which passes through the dielectric layer 128 and the gate-insulating layer 136, electrically connects each top pixel electrode 126 to the corresponding drain electrode 142. Arrow A indicates the area which is transmissive for the control component. It will be appreciated that other pixel architectures are possible, for example four or more metal layers with different layouts could be used.

Figure 3b shows an alternative layout for the control component. Unchanged elements have the same reference numbers as Figure 3a. Like Figure 3a, each OTFT comprises a source electrode 140 separated by a channel 138 comprising light sensitive semiconducting material from a drain electrode 242. However, in this arrangement, in the same layer there is also a second drain electrode 243 separated by a second channel 139 comprising light sensitive semiconducting material from a

Vdd electrode 241. There are also two gate electrodes 230, 231 rather than a gate drain electrode and a pixel capacitor. A via 134 connects the second drain electrode 243 to the pixel electrode 126 and passes through the dielectric layer 128 and the gate insulating layer 136. A second via 234 connects the second gate electrode 231 to the first drain electrode 242 and passes through the gate-insulating layer 136.

The arrangement of Figure 3c could be used with the LCD shown in Figure 3a. However, as illustrated in Figure 3c, the LCD could be replaced with a different display medium, in this case an organic light emitting diode (OLED) stack 224. The stack 224 may be provided within a bank layer. It is common in OLED displays to provide a bank layer to partition each light-emitting element by banks/walls formed from insulating material e.g. a dielectric material. Consequently, the bank layer may be patterned to provide distinct and partitioned OLED stack areas. The arrow indicates the direction of transmission which is through the same general area as indicated in Figure 3b.

In both the arrangements of Figures 3b and 3c, there is a need for an opaque element to shield the light sensitive material in the channels (138, 139) from radiant light. This is achieved as shown in Figures 3d and 3e with a light shielding component 78c and its colour filter layer. The colour filters (red, green, blue) 114a, 114b, 114c and black matrix 54 are formed on a substrate 56. Any appropriate substrate material can be used for substrate 56, such as glass or a polymer film, but preferably a plastic substrate such as PET (polyethyleneterephthalate) or PEN (polyethelenemaphthalene) is used. The colour filters 114a,b,c are patterned directly on the substrate 56, and the planarization layer 148 is disposed directly over the top of the colour filters 114a,b,c. The black matrix 54 is formed from an opaque material and acts as a shield to protect the OTFT from external light from below. For the light shielding component to provide light protection for the transistors, particularly the semiconductor channels, it is necessary to ensure that the array of transistors are aligned with each semiconductor channel above an opaque part, i.e. black part of the matrix 54 and not with the colour filters 114a,b,c.

As shown in Figure 3d, a LC alignment layer 124 is formed on the pixel electrodes. A spacer layer 122 comprising a plurality of spacers 123 is formed on the alignment layer. A second upper alignment layer (not shown) is also formed above the spacer layer 122. Orientation of the liquid crystal molecules is determined by the alignment of

the material at the surfaces of the alignment layers. The space defined by the spacers 122 is filled with a liquid crystal material 120 using a conventional LCD fabrication process. As shown in Figure 3a, the arrangement of Figure 3d may be completed by a light source separated from the liquid crystal medium by a covering component comprising one or more foil layers. Thus, light from the light source is passing through the various layers in the device. Accordingly, it is necessary to protect the light sensitive material in the channel 138 from light in both directions. The light shielding component protects the material from ambient light. Furthermore, as shown in Figure 3d, the gate electrode is aligned with the channel and thus the gate electrode 130 itself protects the channel 138 from light from the light passing through the device.

As shown in Figure 3e, the display can be provided by OLEDs 224 with each OLED being positioned on a pixel electrode 126. In the OLED arrangement, each OLED may be smaller than the pixel electrode on which it is placed and thus the direction and area of the light emission through the layers in the device may be controlled. By contrast, as shown in Figure 3d, the liquid crystal medium may extend beyond the area of the pixel electrode. Accordingly, in the OLED arrangement, it may not be necessary to shield the light sensitive material in the channel in both directions. (Similarly it will be appreciated that the spacer arrangement of the LCD could be arranged so that the liquid crystal medium does not extend beyond the pixel electrode). Each of the gate electrodes 130, 131 is aligned with one of the channels 138,139 and thus if any light does pass through the layers, the light sensitive material in these layers is protected.

Figures 3a to 3e show that the device comprises many layers and the method of manufacturing these layers is summarised in Figure 4. Even though the light shielding component 78c is at the top of the device when viewed by a user, in one embodiment of the invention the light shielding component 78c is manufactured first (Step S100). The light shielding component 78c may be formed by using an optional polarizing foil layer 110 as the bottom-most layer. Such a layer protects the OTFT from below from particular polarisations of (external) light. A colour filter layer 114 comprising a black matrix interleaved with the colour filter array is formed on the polarizing foil layer (where used). The black matrix acts as a further light-shielding layer, protecting the OTFT from any external light that has passed through the polarizing foil 110. The light shielding component 78c therefore assists in shielding the OTFT from ambient light.

The next step is to form an optional planarization layer 148 over the colour filter layer 114 (Step S102).

The control component 76c is manufactured directly on the planarization layer 148 (if used) or on colour filter layer of the light shielding component. Either way, there is no need for the control component to be built up on a separate substrate, thus the conventional OTFT array substrate is removed. Forming the control components comprises two steps, the first step is to form an array of OTFTs (Step S104), followed by forming an array of corresponding pixel electrodes for driving the liquid crystal material. These arrays are built on the planarization layer using standard techniques. As explained in more detail with reference to Figure 4, it is necessary to ensure that the semiconductor channels in the transistors are aligned with the black matrix in the colour filter layer.

For example, the first step in forming the array of top gate transistors may be to dispose a conductive layer on the planarization layer 148 and pattern the layer to form the source and drain electrodes. Each source electrode 140 and drain electrode 142 of each OTFT in the array are disposed directly on the planarization layer (or on the colour filter layer). The conductive layer may comprise a conducting polymer such as PEDOT, or a metallic material, such as gold, copper or silver. The conductive layer may be deposited and patterned through solution processing techniques such as, but not limited to, spin, dip, blade, bar, slot-die, or spray coating, inkjet, gravure, offset or screen printing. Alternatively, vacuum deposition such as evaporation, or sputtering followed by photolithographic patterning or other subtractive patterning techniques, such as laser ablation, may be used. The conductive layer of material may be patterned using laser ablation. The laser ablation may use a single shot of a nano-second laser beam (i.e. having a pulse length of greater than 1ns, 5ns, or 10ns). Preferably, an excimer laser is used to selectively pattern features on the conductive layer. The use of a single laser pulse ensures that essentially all the laser energy is absorbed by the material of the conductive layer, and that the residual laser radiation to which the underlying organic and/or conductive layers are exposed is insufficient to ablate, damage or degrade the latter. This process allows for selective patterning of conductive layers of a device without causing damage to active underlying features.

To avoid damage or ablation of underlying layers during laser ablation of the conductive layers, the thickness of the conductive layer may be below 150-200nm in order to allow ablation in a single shot. Additionally, the thickness may be sufficient such that the optical density of the upper conductive layer is sufficiently high to shield any of the radiation sensitive layers below from the laser light, and to keep the energy density absorbed in any of the lower layers below their respective ablation thresholds.

The intensity of the laser radiation is preferably selected to be above the ablation threshold for the upper layer, but also such that the amount of laser radiation to which an underlying layer, e.g. the planarization layer 147 or the gate dielectric 136, is exposed is below the damage threshold of the underlying layer.

The source and drain electrodes are disposed spaced apart from each other with a channel 138 therebetween. Semiconducting material is disposed in the channel 138 and at least partially on the source and drain electrodes. A broad range of printing techniques may be used to deposit the semiconducting material including, but not limited to, inkjet printing, soft lithographic printing, offset printing, blade coating or dip coating, curtain coating, meniscus coating, spray coating, or extrusion coating. Alternatively, the semiconducting layer may be deposited as a thin continuous film and patterned subtractively by techniques such as photolithography or laser ablation.

A gate-insulating layer (i.e. gate dielectric) 136 is disposed on the semiconductor channel 138. Materials such as polyisobutylene or polyvinylphenol may be used as the dielectric material, but preferably polymethylmethacrylate (PMMA) and polystyrene are used. The dielectric material may be deposited in the form of a continuous layer, by techniques such as, but not limited to, spray or blade coating. Preferably the technique of spray coating is used. Optionally, as described below, more than one dielectric layer may be deposited to form a dielectric stack.

For each OTFT, a gate electrode 130 and a pixel capacitor 132 may be disposed (using one of the above-mentioned laser ablation, solution processing or vacuum deposition techniques) on the gate-insulating layer 136, such that the gate electrode and pixel capacitor are spaced apart from each other. The gate electrode may comprise a thin film of inorganic metal such as gold or copper of a thickness suitable for the desired conductivity.

A top pixel dielectric layer 128 is disposed over the gate electrode and pixel capacitor. For each OTFT, a top pixel electrode 126 is disposed over dielectric layer 128. Via 134, which passes through the dielectric layer 128, electrically connects each top pixel electrode 126 to the corresponding drain electrode 142.

In embodiments, the dielectric layers (e.g. the gate dielectric and dielectric layer 128) are formed from a plurality of dielectric layers rather than a homogeneous layer of dielectric material. This is because use of a dielectric stack facilitates the tailoring of the stack according to the desired characteristics at various levels within the stack. In embodiments, towards the top of the stack or immediately beneath an upper conductive layer (e.g. the conductive layer used to form the gate 130), a relatively absorbing and/or damage resistant dielectric material such as parylene may be used. At one or more lower levels of the stack, a dielectric material may be employed which has better dielectric properties but perhaps a lower damage or ablation threshold, or is less absorbing. For example, one or more lower layers of the stack may be formed of polystyrene and/or PMMA (polymethyl methacrylate). Additionally or alternatively to parylene, an upper layer of the stack may comprise PVP (polyvinyl pyrrolidone). In general, where a dielectric stack is employed, one or more upper layers of the sack may have a higher ablation threshold than one or more lower layers of the stack.

The organic semiconductor material may comprise an organic polymer layer or layers (stack). Preferably, the lower conductive layer is patterned to form the electrodes 140 and 142 before the semiconductor material is disposed over the layer.

As mentioned above, conventional OTFTs are typically fabricated with organic silicon, such as amorphous silicon or polycrystalline silicon. Preferably, the inverted top-gate LCD structure is fabricated using solution-based organic thin film transistors (OTFTs) preferably patterned by techniques such as direct-write printing, laser ablation or photolithography. Further details can be found in the applicant's earlier patent applications, including, in particular, WO 01/47045, WO 2004/070466, WO 01/47043, WO 2006/059162, WO 2006/056808, WO 2006/061658, WO 2006/106365 (which describes a four or five layer pixel architecture) and PCT/GB2006/050265, all hereby incorporated by reference in their entirety. Thus, in embodiments the OTFTs comprise an organic semiconductor material, for example a solution processable conjugated

polymeric or oligomeric material, and in embodiments the LCD structure is adapted to solution deposition, for example comprising solution-processed polymers and vacuum-deposited metals.

While a solution processable semiconducting layer 142 is used to fabricate the LCD, one or more of the conductive layers (i.e. those forming the electrodes of the OTFT) may be formed of an inorganic metal. Preferably, the conductive layers are formed of gold layers.

As an example, the OTFT stack 152 may comprise a gold layer that is evaporated onto planarization layer 148. The thickness of the planarization layer 148 preferably has an absorbance (optical density) that is lower than the absorbance of the gold layer. A 100 mJ cm^{-2} spatially uniform laser pulse is then fired at the gold layer from an excimer laser. This is well above the ablation threshold of the gold layer. Up to the point in time of ablation of the gold layer, early all of the laser energy is absorbed by the gold layer. After the onset of laser ablation in the gold, the plasma and debris particles that exit immediately above the gold-air interface shield the substrate from further damage by reflecting and absorbing the laser beam. The remaining fluence that is able to reach the planarization layer 148 is thus a fraction of the applied fluence, and well below the ablation threshold of the planarization material.

Once the control component with the array of transistors and electrodes is complete, the next step shown in Figure 4 is to form the liquid crystal medium (Step S108). This may be done using any known techniques. For example, a liquid crystal (LC) alignment layer 124 may be disposed over the pixel electrode 126, such that the alignment layer is electrically connected to the pixel electrode 216. A spacer layer (comprising spacers 122) is provided on top of the alignment layer 124, and a covering component 80 is fabricated over the spacers 122. The liquid crystal material may then be injected between the alignment layers to form the liquid crystal medium.

The covering component 80 comprises a liquid crystal alignment layer 118 which is adjacent the liquid crystal material, a common electrode layer 116 adjacent the liquid crystal alignment layer 118 and a polarising foil 110 to polarise and block external light as it enters the LCD device. The covering component 80 also comprises reflector 146 and backlight waveguide 144 for the light source. Thus, returning to Figure 4, the next

step in the manufacturing process is to provide the light source above the liquid crystal medium (Step S110). In this position, the light source could be considered to be a "toplight", since the light source is provided at the end of the manufacturing process such that it is the "top" of the LCD structure. However, before use as shown at step S112, the manufactured device is inverted. Thus, the light source is effectively illuminating the LCD from the back (bottom) of the display, and is not a 'front light' (i.e. a light source to illuminate an LCD that is otherwise viewed in ambient light). As shown in Figures 3b to 3e, gate electrode 130, 230, 231 is arranged to be aligned with the semiconductor channel 138, 139. Thus, the gate electrode acts as a light-shielding layer, protecting the OTFT (in particular the semiconductor channel) from light exposure from the light source.

A skilled person would appreciate that steps S108 and S110 may be replaced by forming other display medium, e.g. OLEDs, on to the pixel array.

In the conventional TFT-LCD, it is necessary to precisely align the upper component which conventionally includes the colour filters and black matrix so that each opaque element in the black matrix is positioned over the corresponding transistor in the TFT array. However in this arrangement, since the colour filter layer 114 including its black matrix is moved to the bottom of the structure, the covering component 80 does not include any layers which require precise alignment relative to the TFT array. Thus, the covering component manufacturing process is simplified.

The concept of the inverted LCD structure applies to display devices which use any transmissive electro-optic mode (e.g. electrowetting).

Figure 5 shows a block diagram of the electronics of an LCD display panel. The device comprises a controller 1002 which includes a microprocessor, for example an ARM™ device, working memory and program memory coupled to one or more display interface integrated circuits 438 for driving the LCD 408. One or more touch interface integrated circuits 1006 interface with the touch electrodes on front window 414 to provide touch data to controller 1002.

The program memory in embodiments stores processor control code to implement functions including an operating system, various types of wireless and wired interface,

document retrieval, storage, annotation (via the touch interface) and export from the device. The stored code also includes code 1003 to implement a document viewer/'printerless printing' function, for example interfacing with corresponding driver code on a 'host' device.

The controller 1002 interfaces with non-volatile memory, for example Flash memory, for storing one or more documents for display and, optionally, other data such as user bookmark locations and the like. Optionally a mechanical user control 1004 may also be provided.

A wireless interface 1010, for example a Bluetooth™ or WiFi interface is provided for interfacing with a consumer electronic device such as a phone 1014a, laptop 1014b or the like. The wireless interface 1010 may comprise a Bluetooth™ RF chip and antenna.

Inductive loop 432 is used to charge the rechargeable battery 430 which has associated circuitry for providing a regulated power supply to the system.

No doubt many other effective alternatives will occur to the skilled person. It will be understood that the invention is not limited to the described embodiments and encompasses modifications apparent to those skilled in the art lying within the spirit and scope of the claims appended hereto.

CLAIMS:

1. A display device comprising:

a display medium comprising a plurality of pixels;

a control component comprising an array of pixel electrodes controlled by an array of transistors including a plurality of transistors comprising a light-sensitive semiconductor channel; and

a filter array comprising an array of relatively transmissive filters interspersed with a plurality of relatively non-transmissive areas;

wherein said control component is positioned between said filter array and said display medium and

wherein each relatively transmissive filter is aligned with one of the pixel electrodes and each relatively non-transmissive area is aligned with one of the light-sensitive semiconductor channels whereby said semiconductor channel in each transistor is protected from light exposure.

2. The device as claimed in claim 1 wherein each relatively transmissive filter is substantially transparent.

3. The device as claimed in claim 1 or claim 2 wherein each relatively non-transmissive area is substantially opaque.

4. The device as claimed in claim 3, wherein each relatively non-transmissive area has an absorbance of greater than about 2, preferably greater than about 3, at all wavelengths that impair the performance of the transistor.

5. The device as claimed in any one of the preceding claims, wherein said relatively non-transmissive areas form a black matrix around the filters.

6. The device as claimed in any one of the preceding claims, wherein said filters are colour filters.

7. The device as claimed in any one of the preceding claims, further comprising a light source for the display medium.

8. The device as claimed in claim 7, wherein each transistor comprises a source electrode, a drain electrode, a gate electrode and the semiconductor channel is between said source and drain electrode wherein the gate electrode is aligned with the semiconductor channel whereby said semiconductor channel in each transistor is protected from light exposure from the light source

9. The device as claimed in any preceding claim wherein said transistor is an organic thin film transistor.

10. The device as claimed in claim 9 wherein said semiconductor channel is formed of an organic semiconductor material.

11. The device as claimed in any preceding claim wherein said display medium is a liquid crystal display medium.

12. The device as claimed in claim 11 wherein said liquid crystal display medium comprises a pair of alignment layers spaced apart by a plurality of spacers with liquid crystal material in spaces between said pair of alignment layers.

13. A method of manufacturing a display device, the method comprising:

forming a filter array comprising an array of relatively transmissive filters and a plurality of relatively non-transmissive areas;

forming an array of transistors over said filter array with each transistor comprising a semiconductor channel and wherein said forming step comprises aligning each semiconductor channel with one of said relatively non-transmissive areas in said filter array;

forming an array of pixel electrodes over said array of top-gate transistors, wherein each said pixel electrode is connected to a respective transistor in said array of transistors; and

forming a display medium over said array of pixel electrodes.

14. The method of claim 13, comprising forming said array of transistors as top-gate transistors comprising source, drain and gate electrodes for each transistor.

15. The method of claim 14, wherein forming said array of transistors comprises aligning each gate electrode in each transistor with a corresponding semiconductor channel.

16. The method of any one of claims 13 to 15 comprising forming said display medium by

forming a first alignment layer;

forming a spacer layer comprising a plurality of spacers on said first alignment layer;

forming a second alignment layer on said spacer layer whereby said second alignment layer is spaced apart from said first alignment layer; and

injecting liquid crystal material into space between said first and said second alignment layers.

17. The method of any one of claims 13 to 16 comprising forming said filter array by forming a plurality of colour filters with a black matrix.

18. The method of any one of claims 13 to 17 comprising forming a planarization layer on said filter array and forming said array of transistors on said planarization layer.

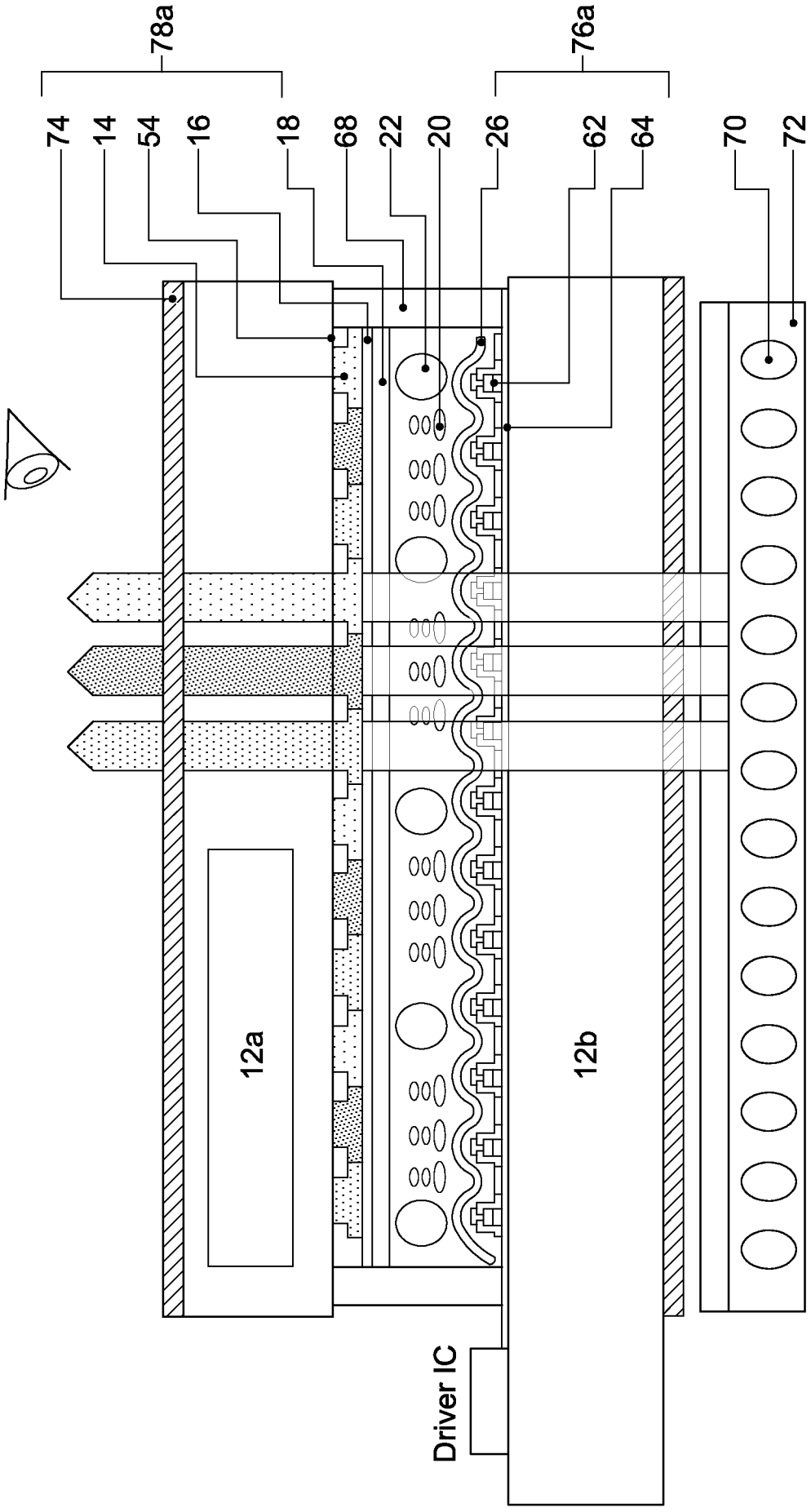


Fig. 1a (prior art)

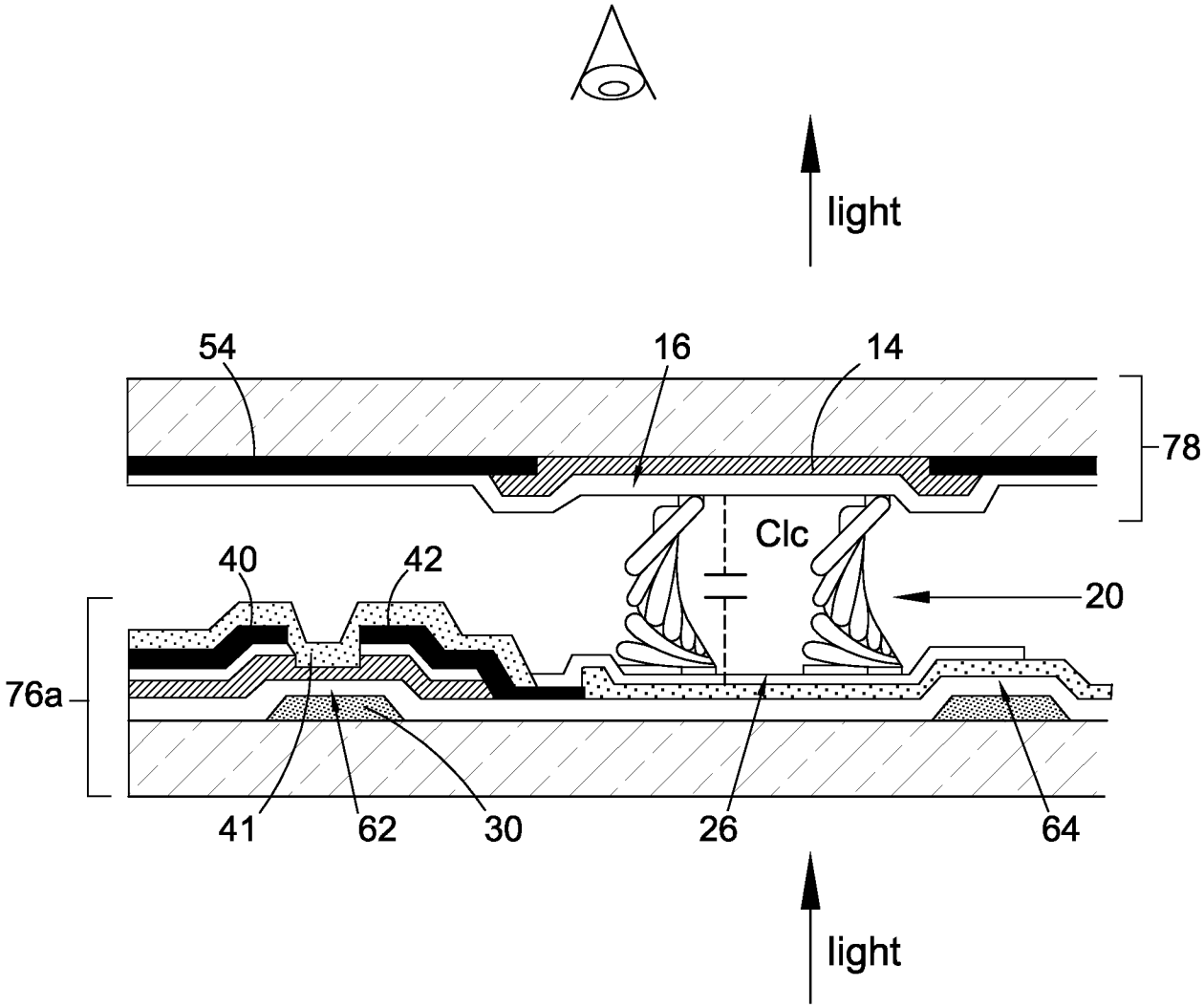


Fig. 1b (prior art)

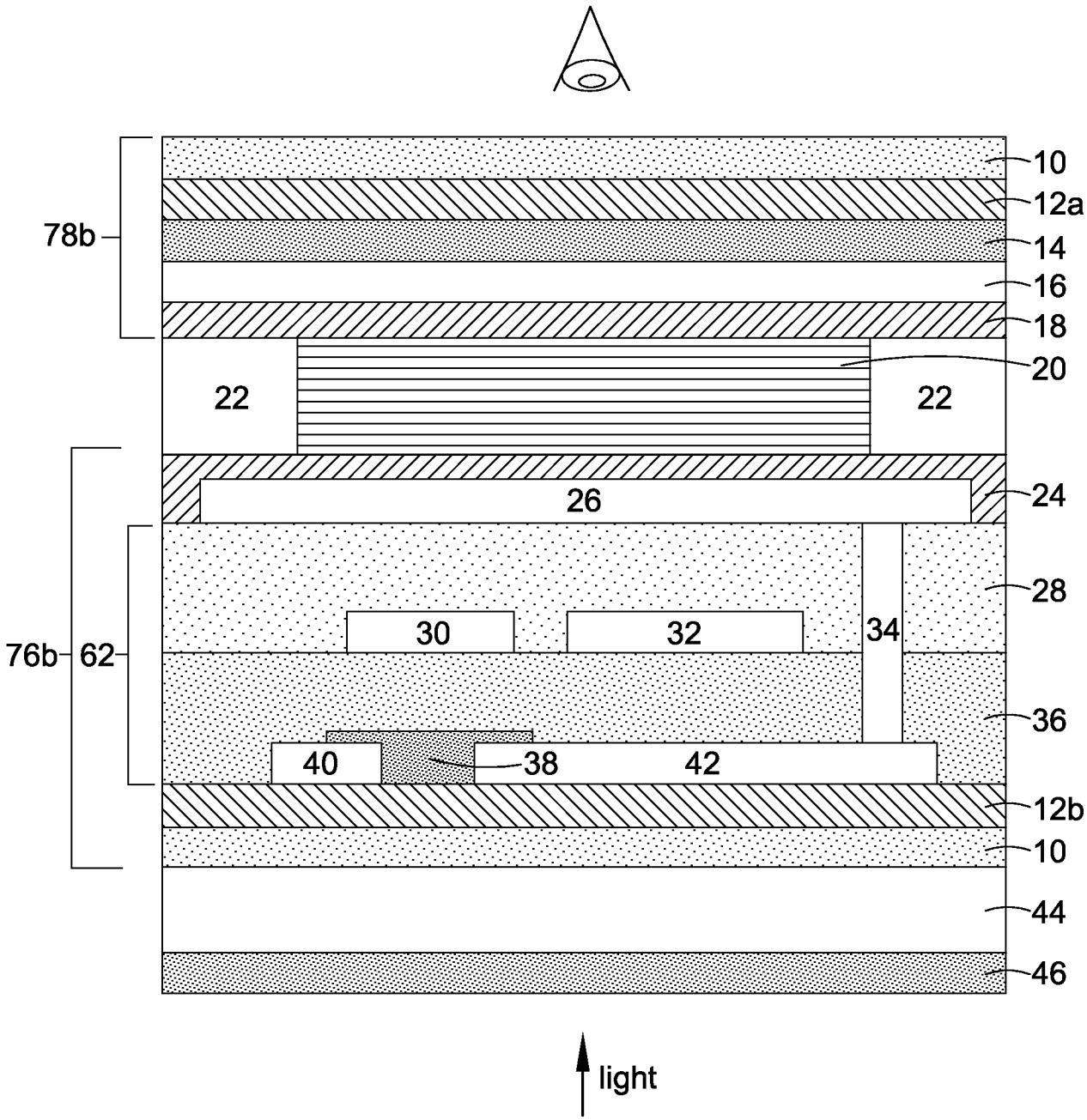


Fig. 2 (prior art)

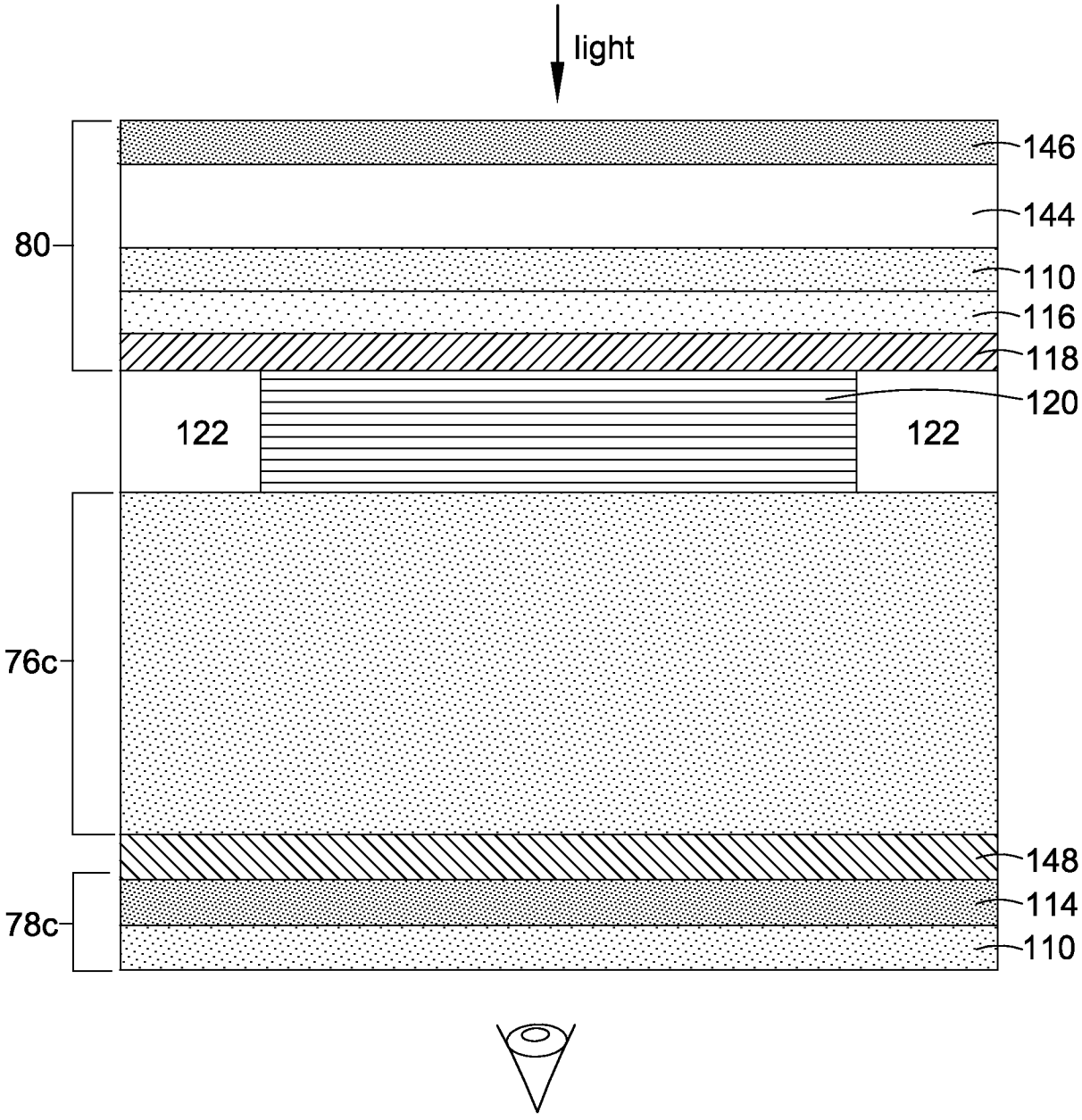


Fig. 3a

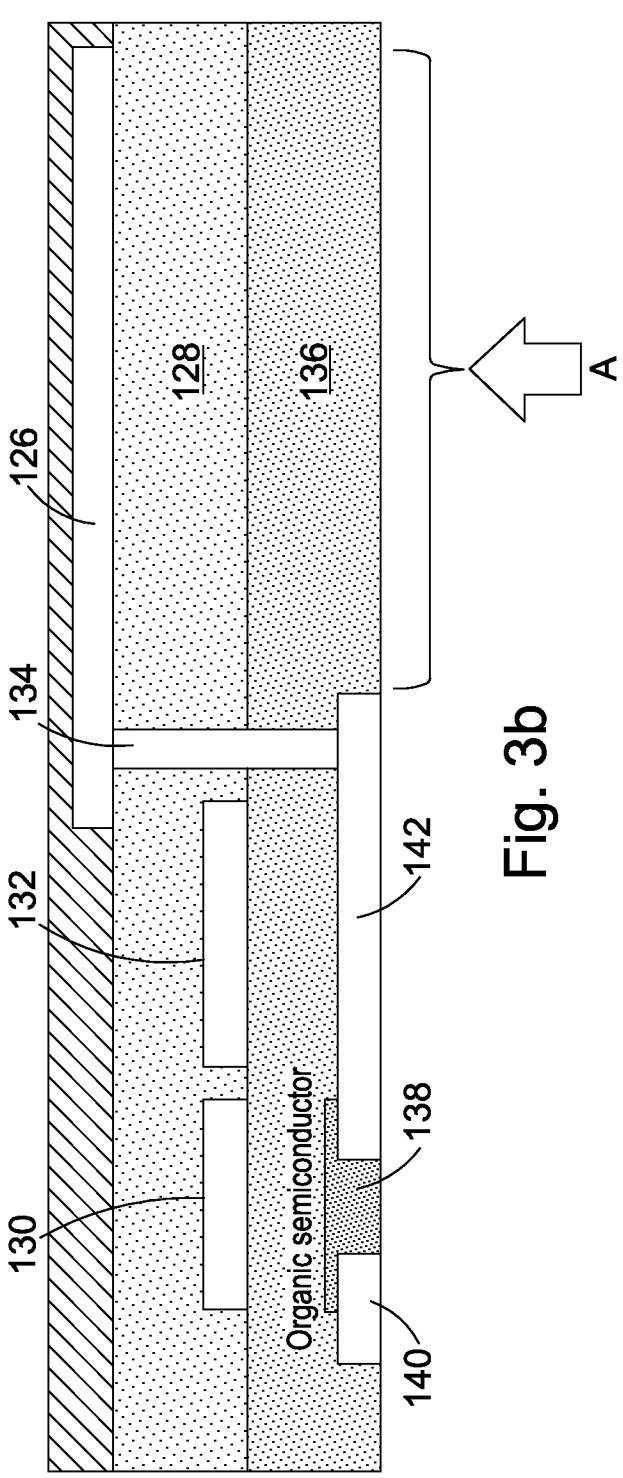

126
134
132
130
128
136
142
138
140
Organic semiconductor
A

Fig. 3b

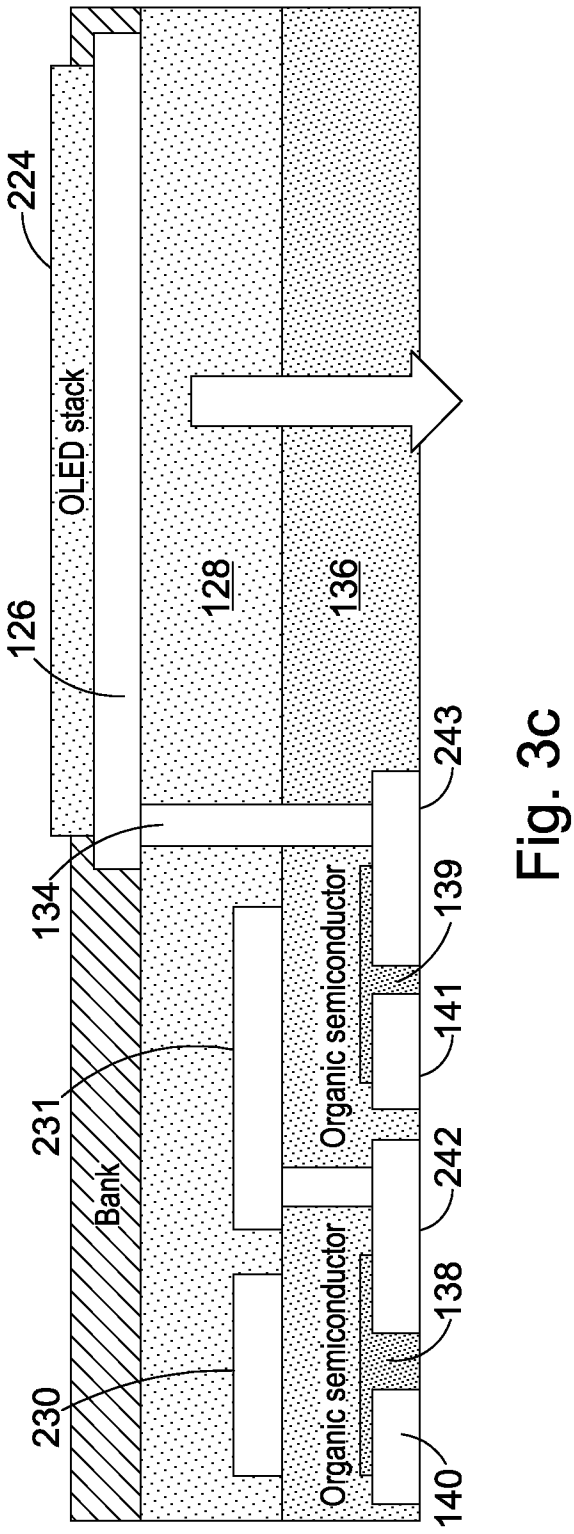

224
OLED stack
126
128
136
134
231
Bank
230
243
139
141
242
138
140
Organic semiconductor
Organic semiconductor

Fig. 3c

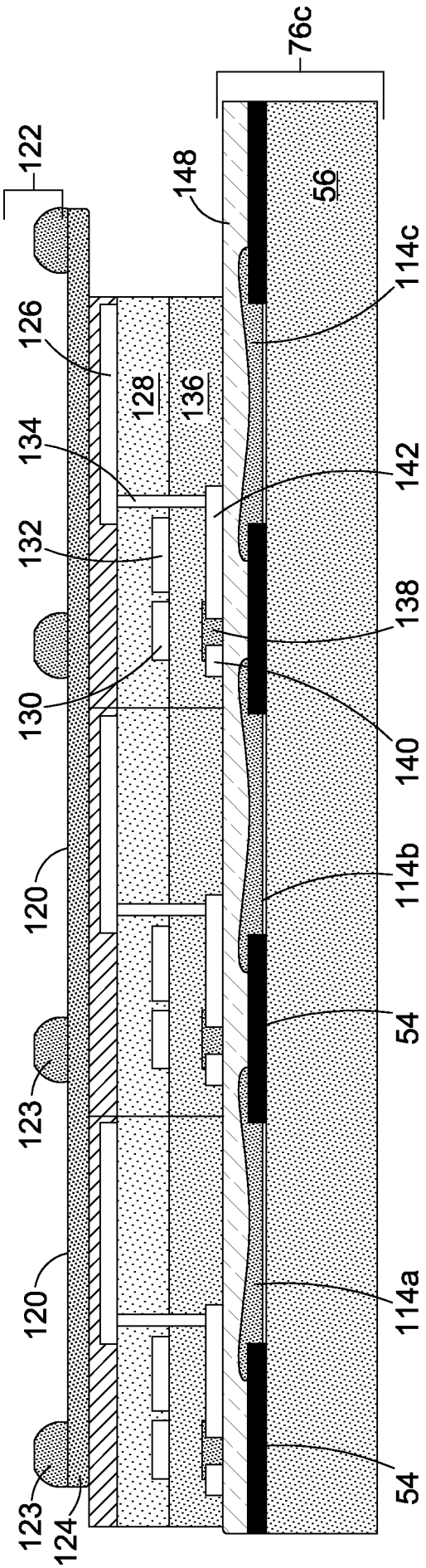
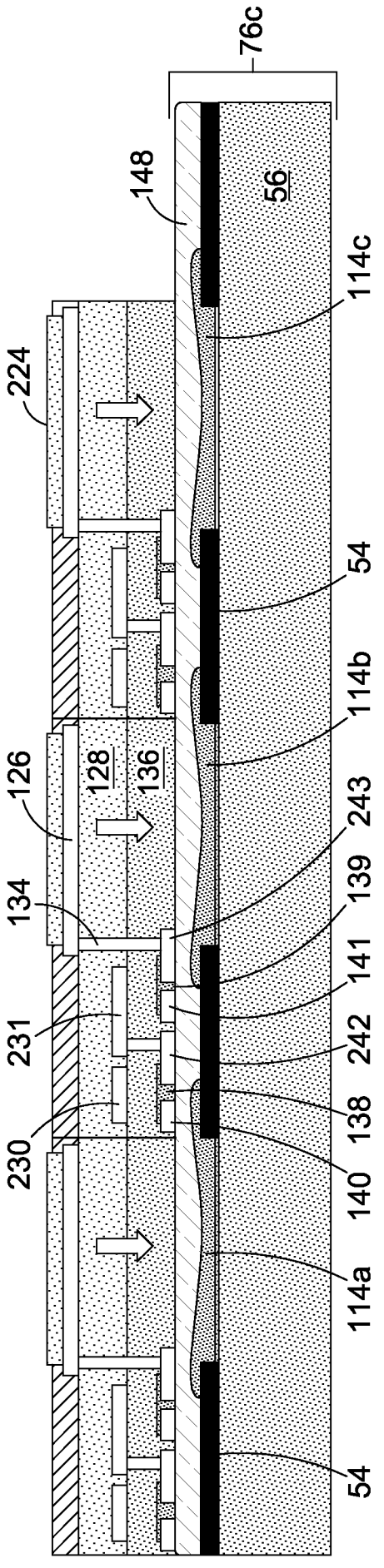

76c
122
148
56
114c
126
128
136
134
142
132
138
130
140
120
114b
54
123
120
114a
54
123
124

Fig. 3d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148
56
114c
224
54
114b
126
128
136
243
134
139
141
231
242
138
230
140
114a
54

Fig. 3e

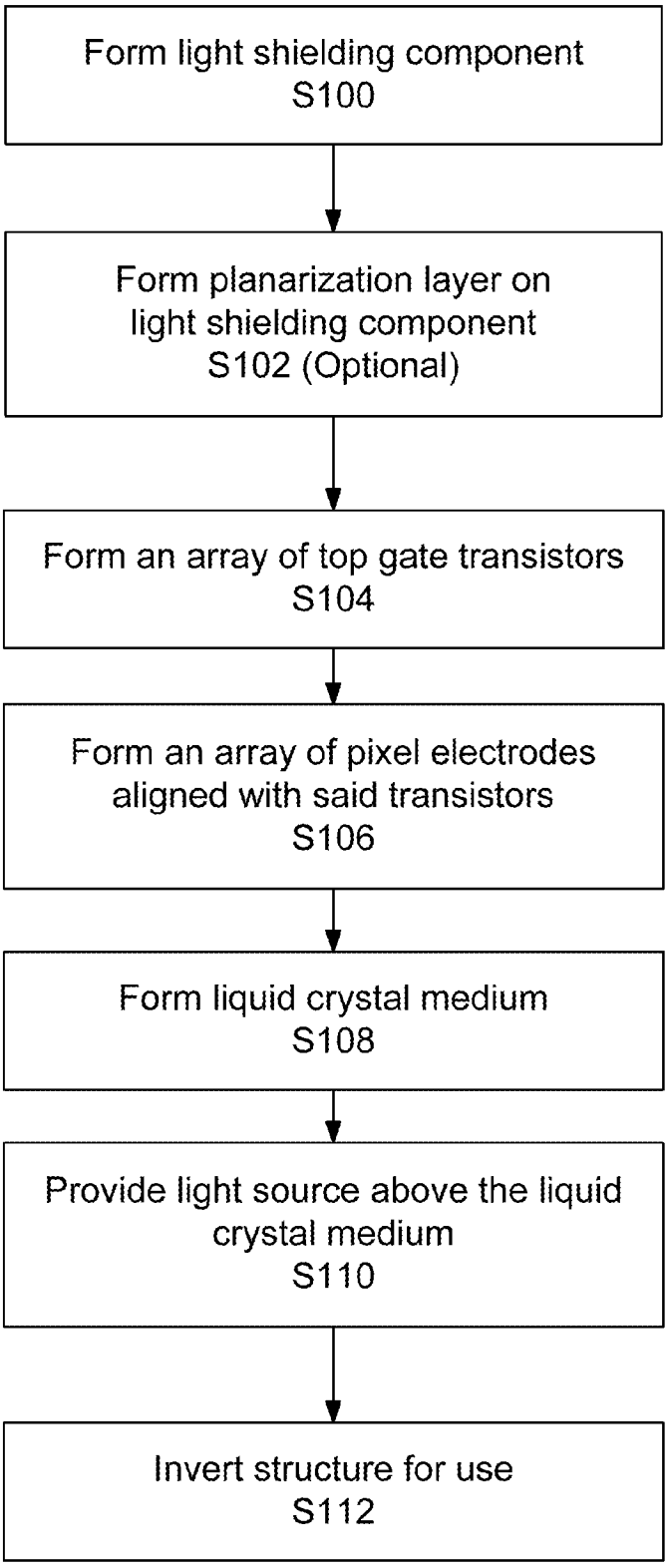
Form light shielding component
S100
Form planarization layer on light shielding component
S102 (Optional)
Form an array of top gate transistors
S104
Form an array of pixel electrodes aligned with said transistors
S106
Form liquid crystal medium
S108
Provide light source above the liquid crystal medium
S110
Invert structure for use
S112

Fig. 4

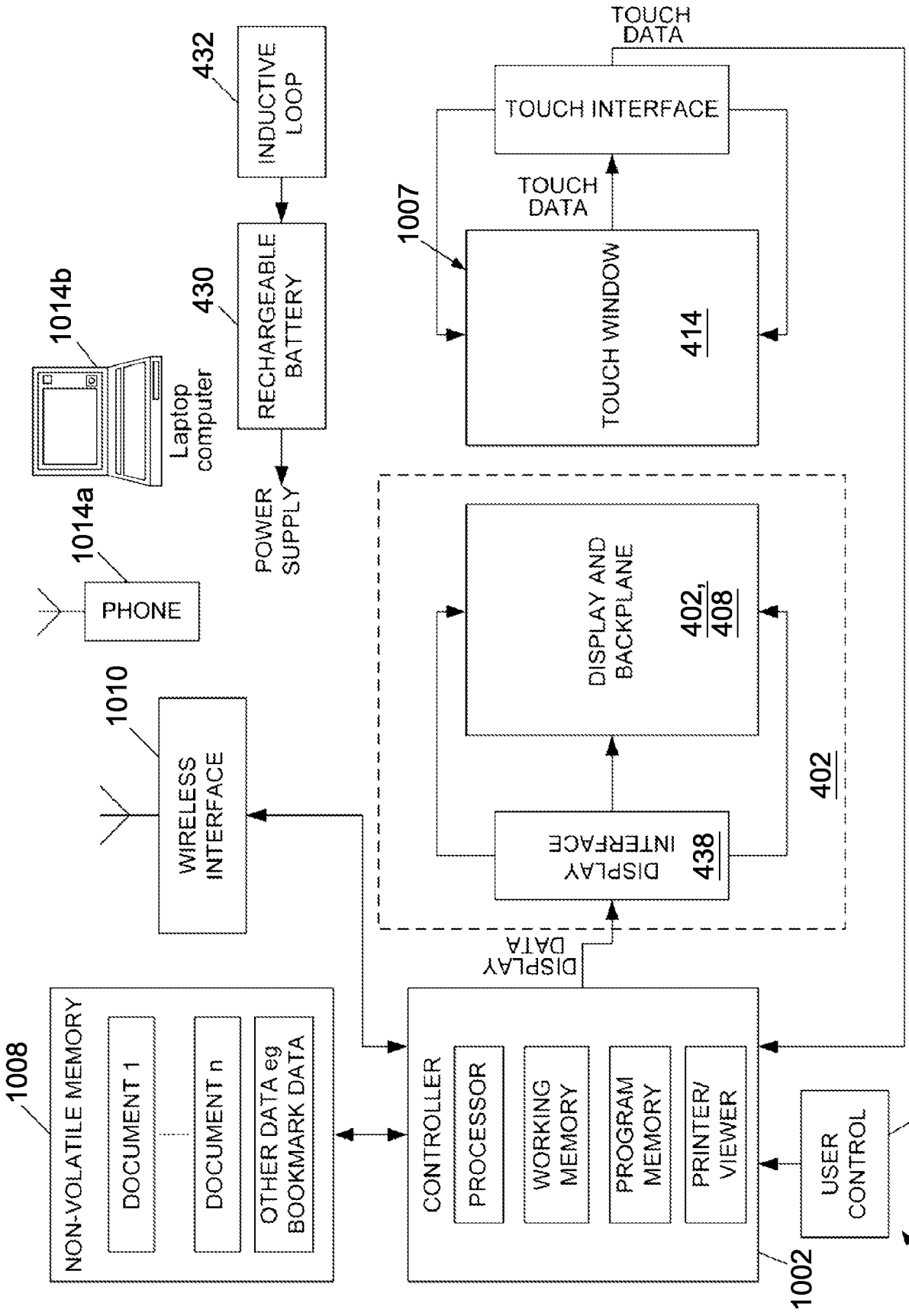
TOUCH DATA
TOUCH INTERFACE
TOUCH DATA
1007
TOUCH WINDOW
414
DISPLAY AND BACKPLANE
402, 408
402
DISPLAY INTERFACE
438
DISPLAY DATA
CONTROLLER
PROCESSOR
WORKING MEMORY
PROGRAM MEMORY
PRINTER/ VIEWER
USER CONTROL
1004
1002
400
NON-VOLATILE MEMORY
DOCUMENT 1
DOCUMENT n
OTHER DATA eg BOOKMARK DATA
1008
WIRELESS INTERFACE
1010
PHONE
1014a
Laptop computer
1014b
POWER SUPPLY
RECHARGEABLE BATTERY
430
INDUCTIVE LOOP
432

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2015/051475

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02F1/1362 G02F1/1335
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/238217 A1 (SHIH MING-HUNG [TW]) 11 October 2007 (2007-10-11) figures 1A-1G paragraph [0003] paragraph [0019] - paragraph [0027]	1-18
X	US 2006/138415 A1 (HUNG MENG-YI [TW] ET AL) 29 June 2006 (2006-06-29) figures 1,2,4a-4I paragraph [0005] paragraph [0025] paragraph [0027] - paragraph [0045]	1-18
X	KR 2004 0050237 A (LG PHILIPS LCD CO LTD) 16 June 2004 (2004-06-16) abstract figures 4a-4f	1-18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 July 2015	24/07/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kentischer, Florian

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2015/051475

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