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(54) **GATE STACK FORMED WITH INTERRUPTED DEPOSITION PROCESSES AND LASER ANNEALING**

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H01L 21/02	(2006.01)

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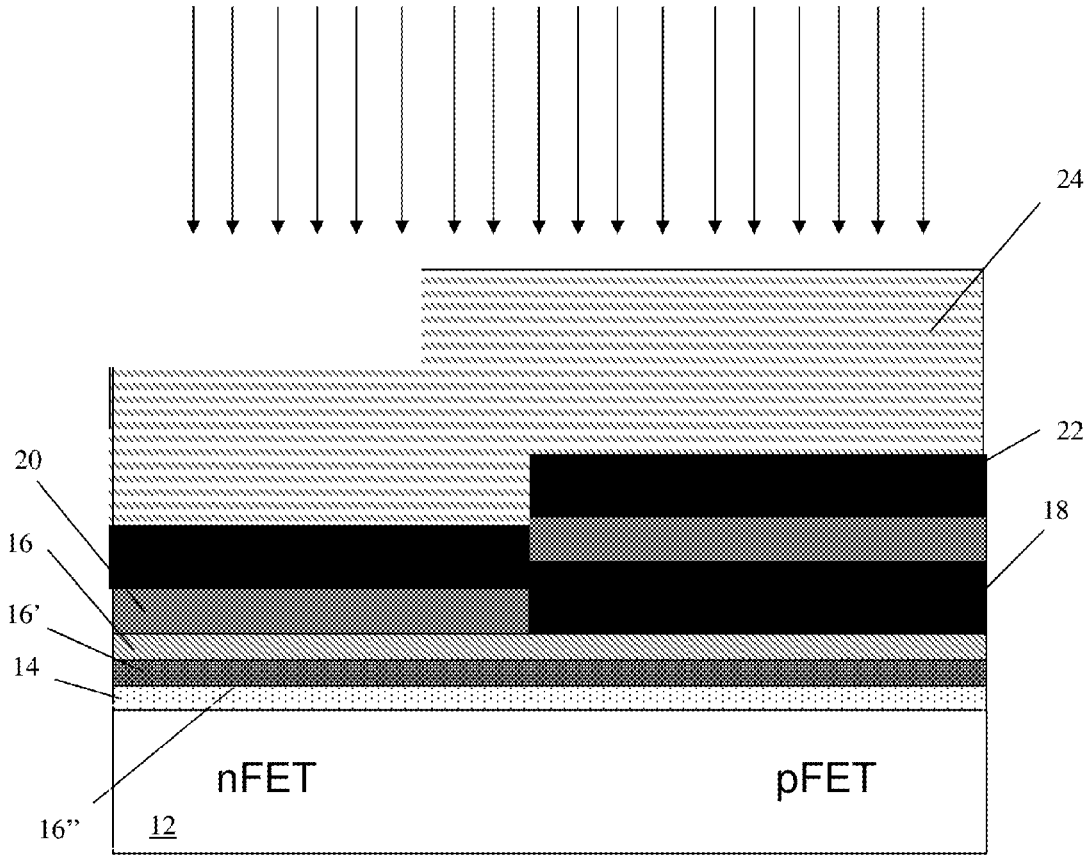
(57) **ABSTRACT**

Semiconductor structures and methods of fabricating the same using interrupted deposition processes and multiple laser anneals are provided. The structure includes a high-k gate stack with a high-k bilayer or nanolaminate where a bottom portion of the bilayer is crystallized while a top portion of the bilayer is amorphous.



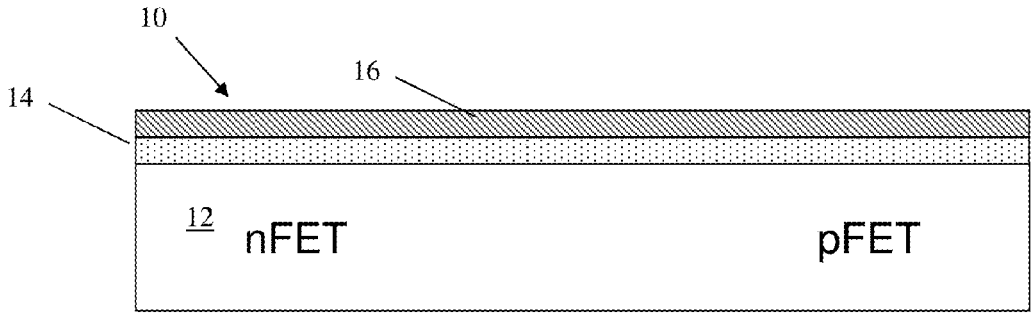


FIG. 1

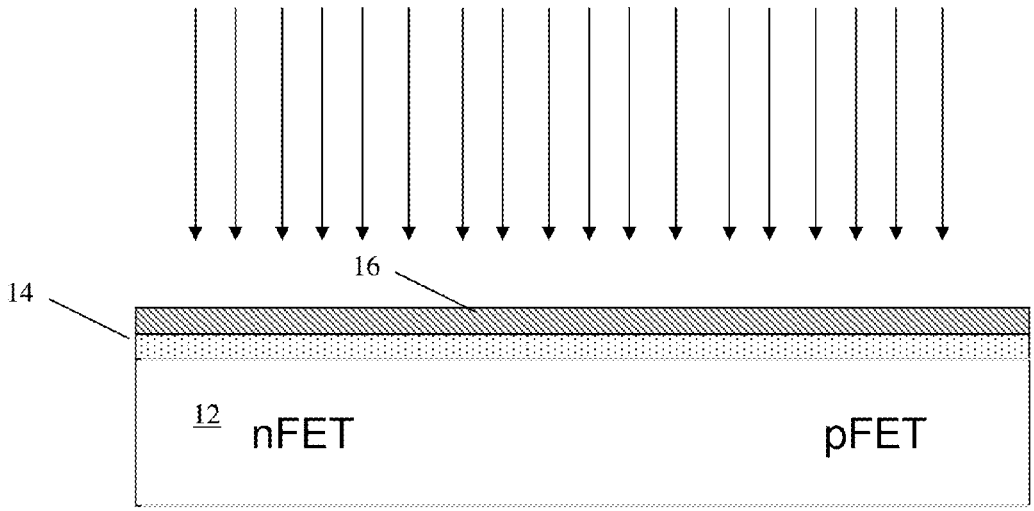


FIG. 2

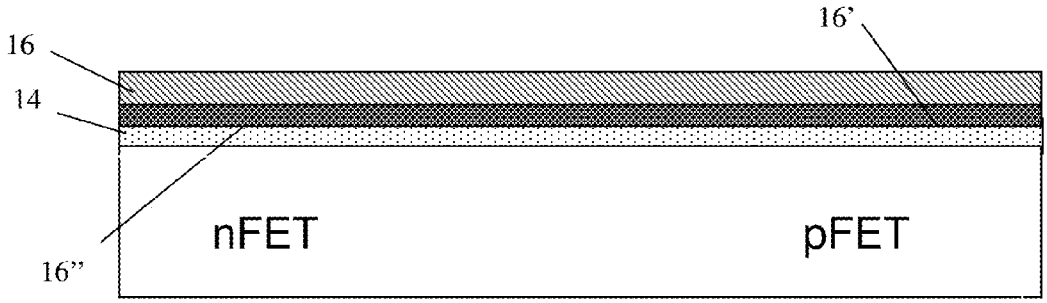


FIG. 3

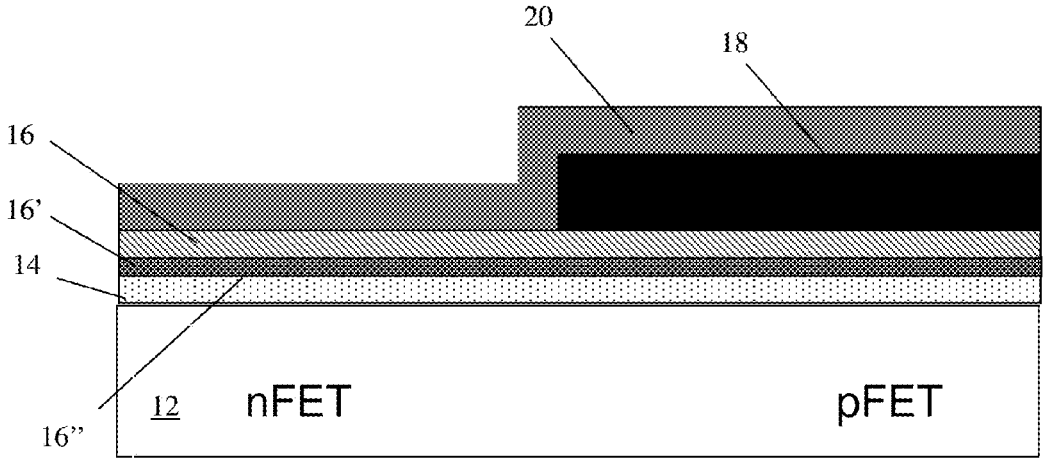


FIG. 4

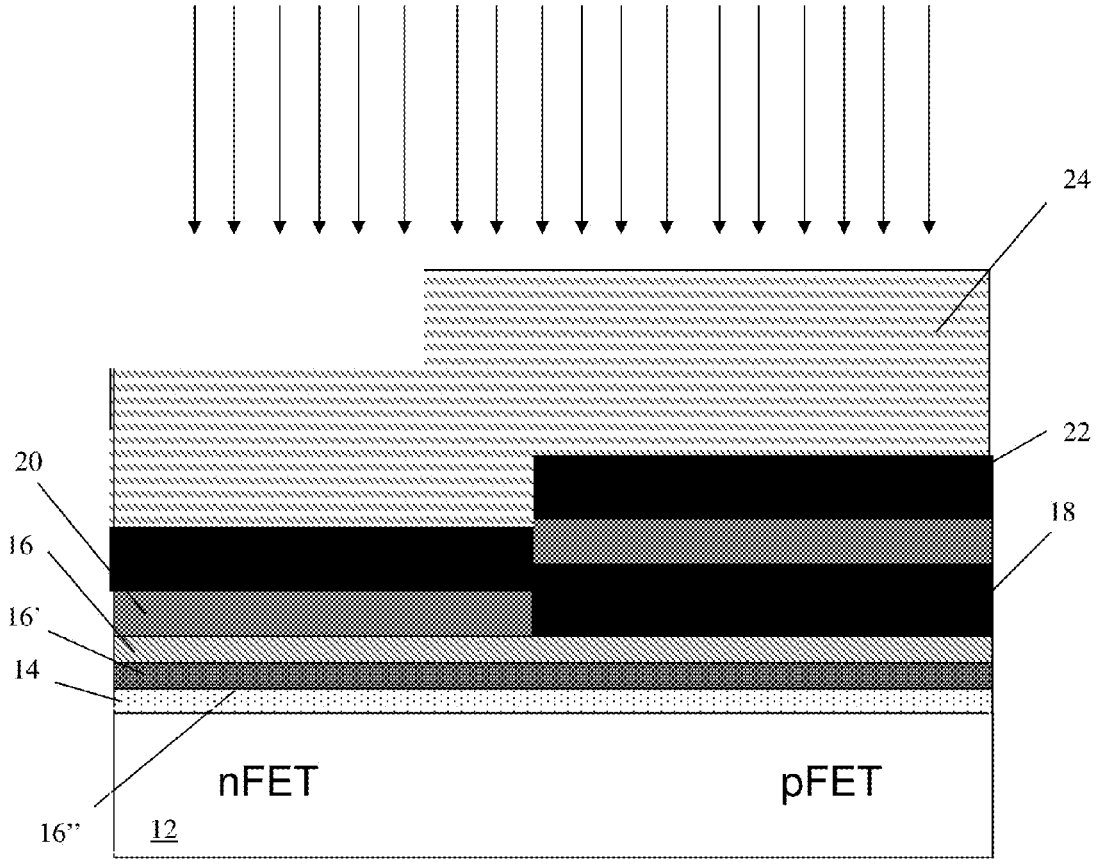


FIG. 5

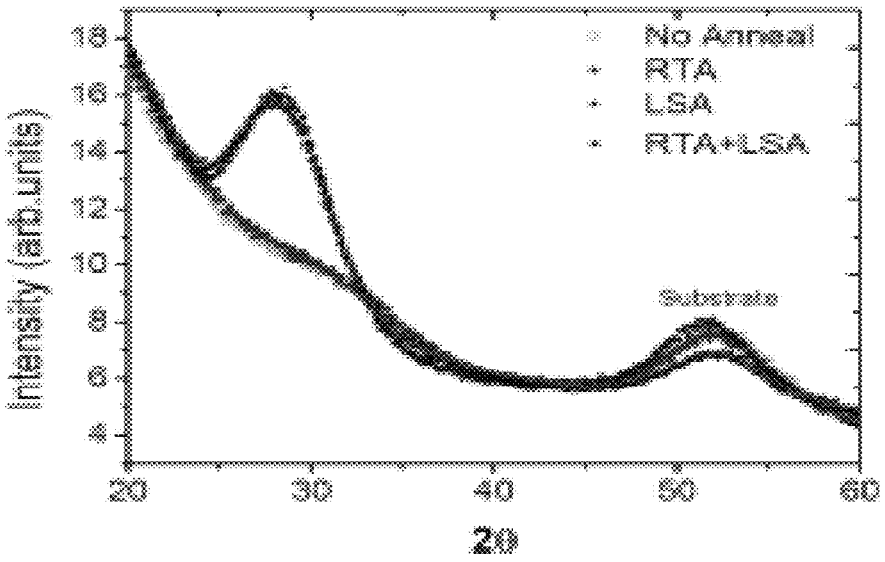

No Anneal
RTA
LSA
RTA+LSA
Substrate
Intensity (arb.units)
2θ
20
30
40
50
60

FIG. 6 (a)

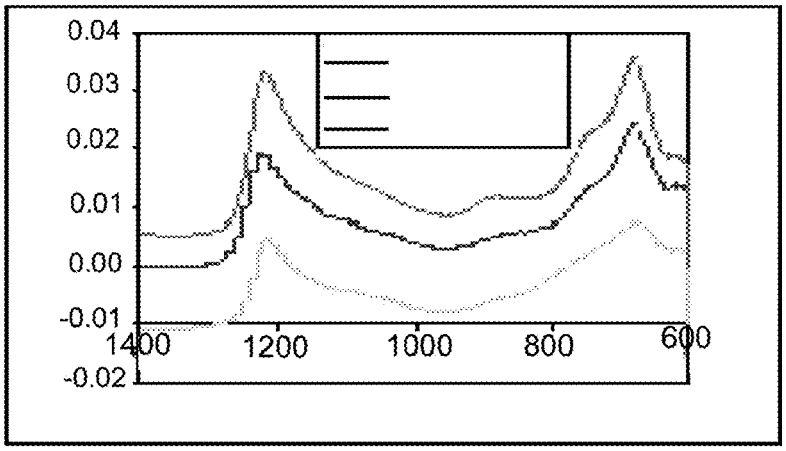

0.04
0.03
0.02
0.01
0.00
-0.01
-0.02
1400
1200
1000
800
600

FIG. 6 (b)

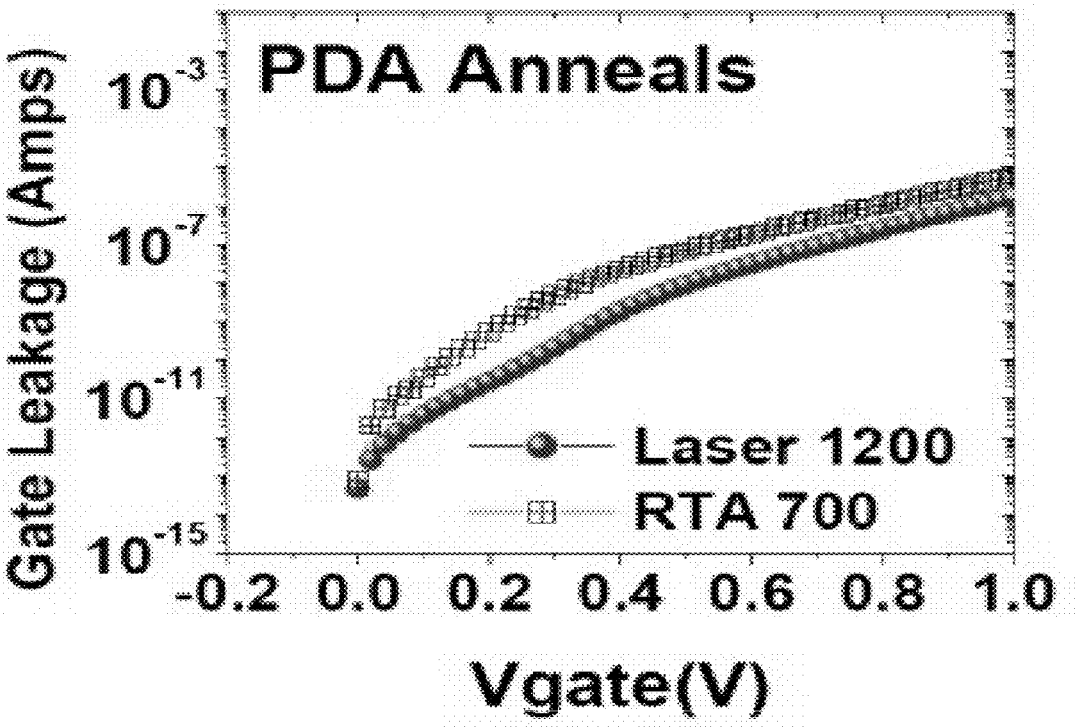

PDA Anneals
Gate Leakage (Amps)
10^-3
10^-7
10^-11
10^-15
-0.2 0.0 0.2 0.4 0.6 0.8 1.0
Vgate(V)
Laser 1200
RTA 700

FIG. 7

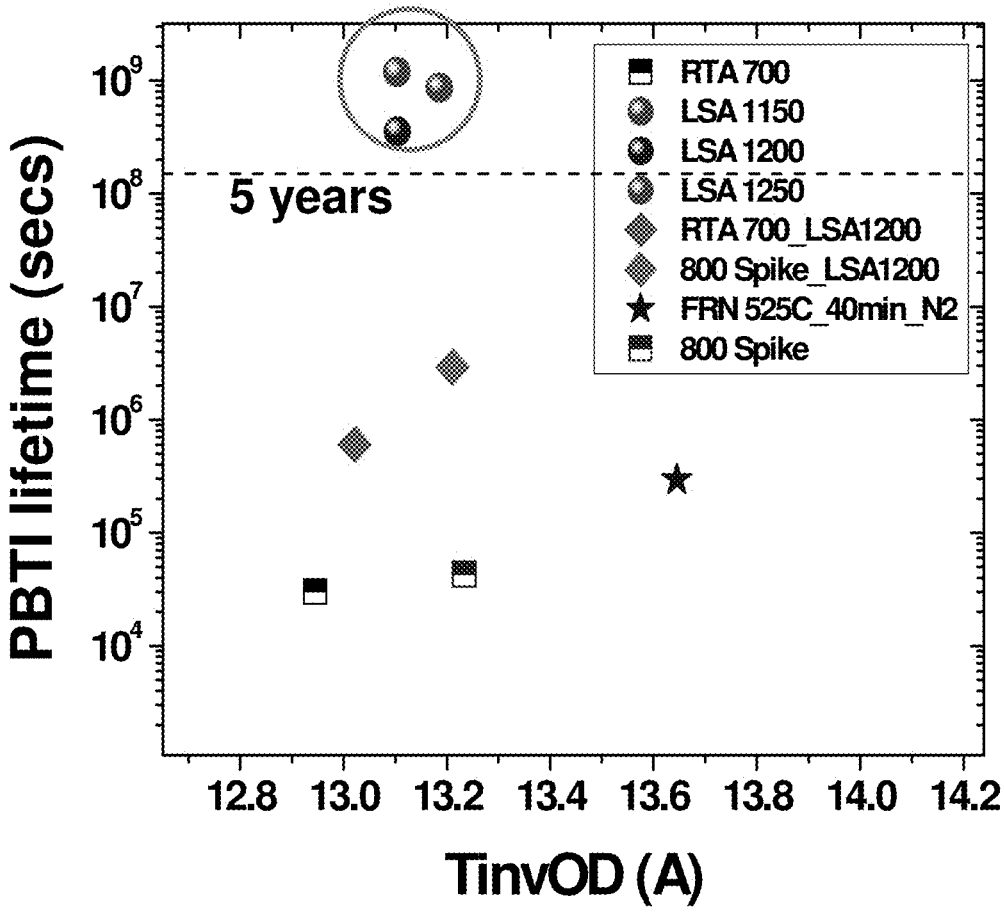

PBTI lifetime (secs)
10^9
10^8
10^7
10^6
10^5
10^4
5 years
RTA 700
LSA 1150
LSA 1200
LSA 1250
RTA 700_LSA1200
800 Spike_LSA1200
FRN 525C_40min_N2
800 Spike
12.8
13.0
13.2
13.4
13.6
13.8
14.0
14.2
TinvOD (A)

FIG. 8

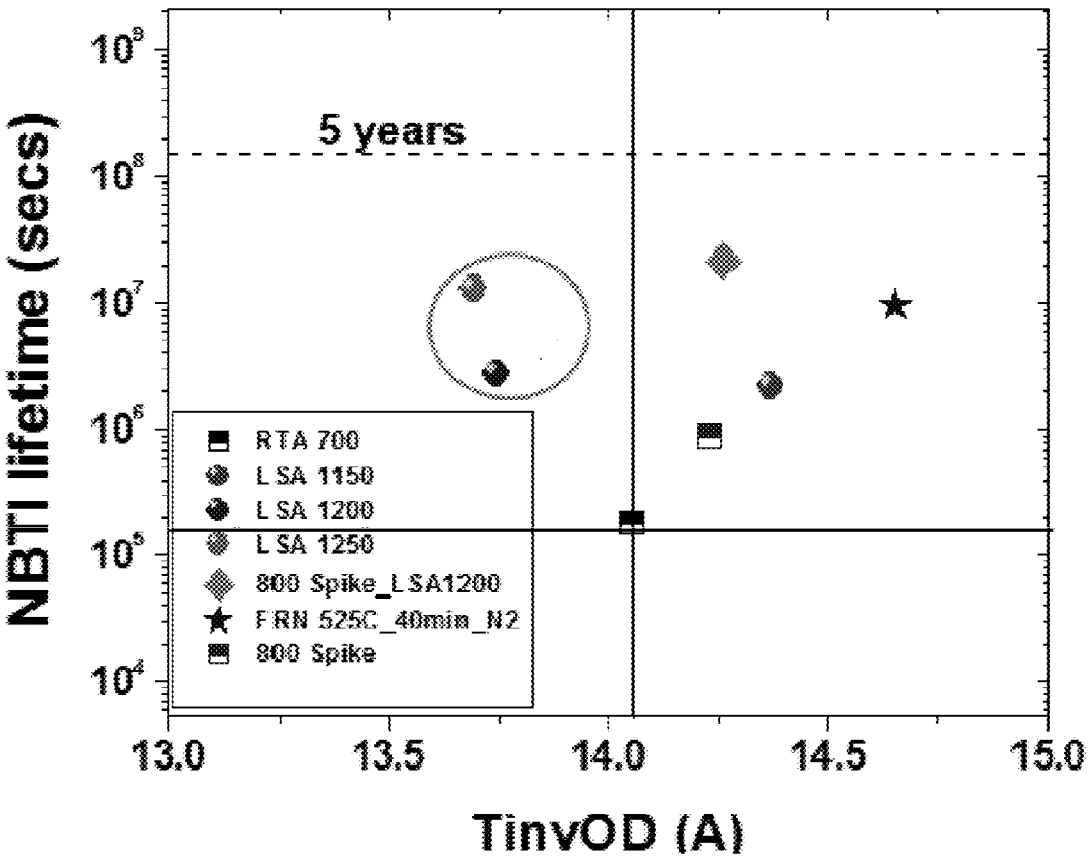
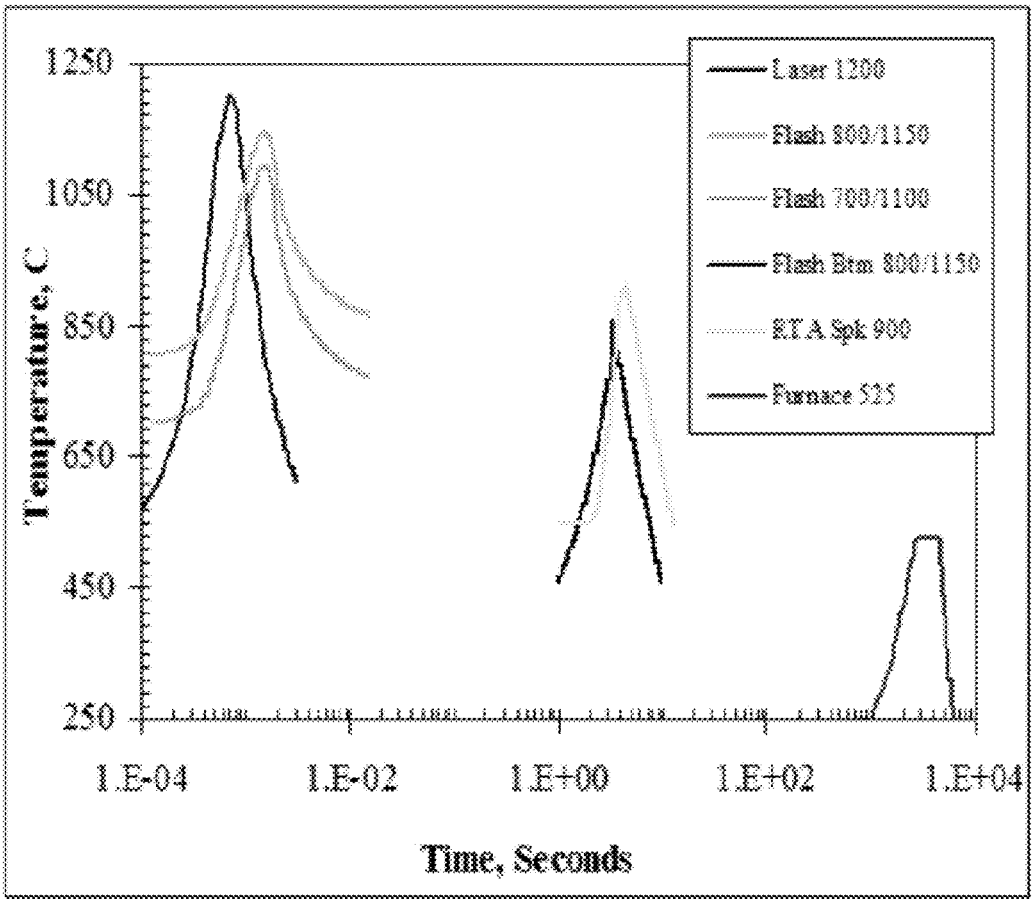

NBTI lifetime (secs)
10^9
10^8
10^7
10^6
10^5
10^4
5 years
RTA 700
LSA 1150
LSA 1200
LSA 1250
800 Spike_LSA1200
FRN 525C_40min_N2
800 Spike
13.0
13.5
14.0
14.5
15.0
TinvOD (A)

FIG. 9



Anneal Type	Base type/ Pre Heat	Temperature	Duration
RTA	Stabilized hold	550C	20-30 Sec
fRTP	RTA component	700-800C	1-2 Sec
LSA	Hot Plate	250C	1-2 min

FIG. 10

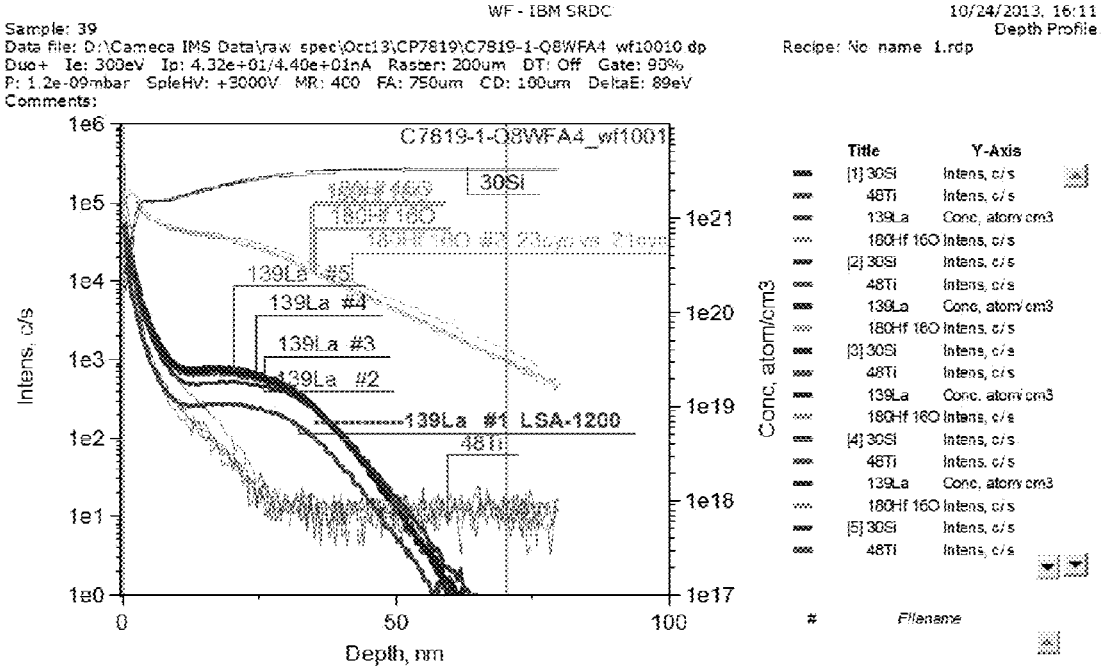

WF - IBM SRDC
10/24/2013, 16:11
Depth Profile
Sample: 39
Data file: D:\Cameca IMS Data\raw spec\Oct13\CP7819\C7819-1-Q8WFA4 wf10010.dp
Recipe: No name 1.rdp
Duo+ Ie: 300eV Ip: 4.32e+01/4.40e+01nA Raster: 200um DT: Off Gate: 95%
P: 1.2e-09mbar SpleHV: +3000V MR: 400 FA: 750um CD: 100um DeltaE: 89eV
Comments:
C7819-1-Q8WFA4_wf1001
30Si
139La #5
139La #4
139La #3
139La #2
139La #1 LSA-1200
48Ti
Intens, c/s
Conc, atom/cm3
Depth, nm
Title
Y-Axis
[1] 30Si Intens, c/s
48Ti Intens, c/s
139La Conc, atom/cm3
180Hf 16O Intens, c/s
[2] 30Si Intens, c/s
48Ti Intens, c/s
139La Conc, atom/cm3
180Hf 16O Intens, c/s
[3] 30Si Intens, c/s
48Ti Intens, c/s
139La Conc, atom/cm3
180Hf 16O Intens, c/s
[4] 30Si Intens, c/s
48Ti Intens, c/s
139La Conc, atom/cm3
180Hf 16O Intens, c/s
[5] 30Si Intens, c/s
48Ti Intens, c/s
Filename

FIG. 11

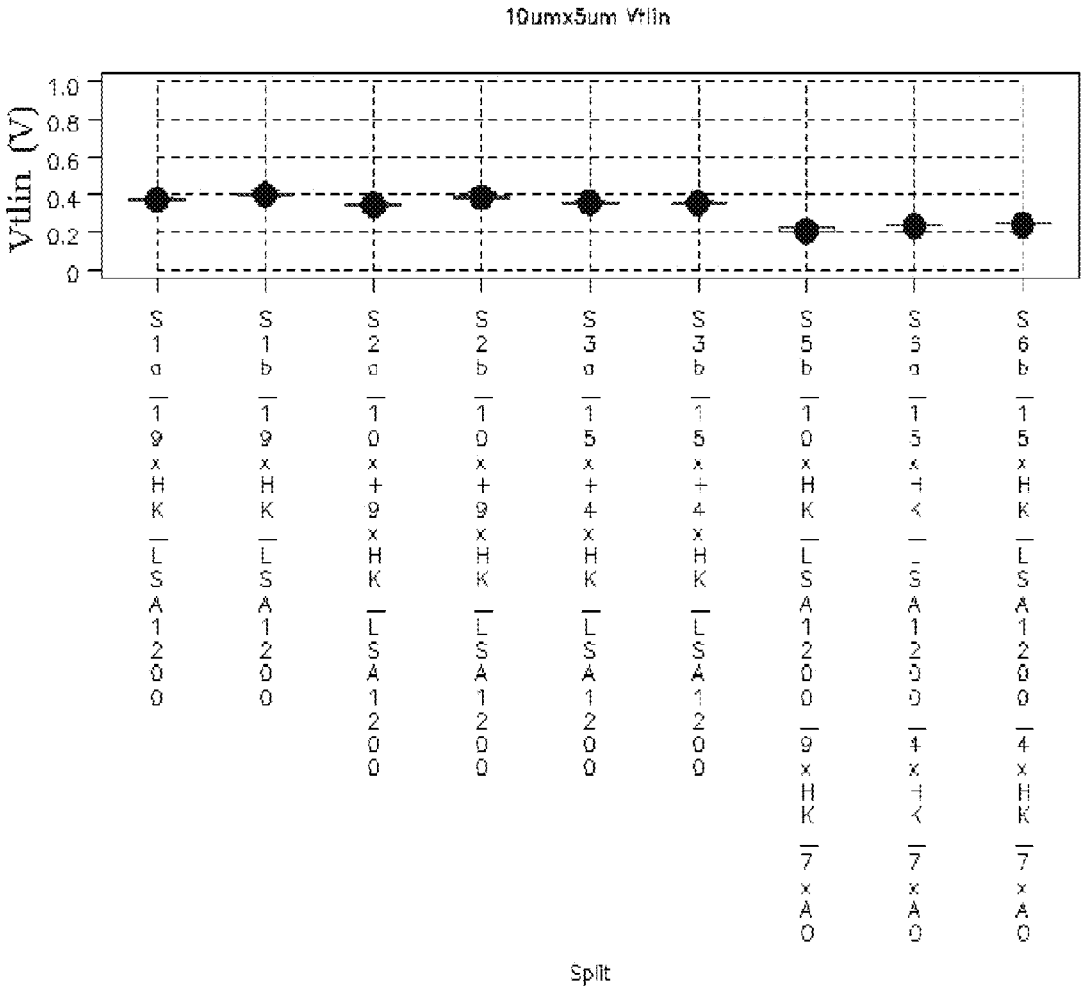

10umx5um Vtlin
Vtlin (V)
1.0
0.8
0.6
0.4
0.2
0
S1a_19xHK_LSA1200
S1b_19xHK_LSA1200
S2a_10x+9xHK_LSA1200
S2b_10x+9xHK_LSA1200
S3a_15x+4xHK_LSA1200
S3b_15x+4xHK_LSA1200
S5b_10xHK_LSA1200_9xHK_7xA0
S5a_15x+4_LSA1200_4x+4_7xA0
S6b_15xHK_LSA1200_4xHK_7xA0
Split

FIG. 12

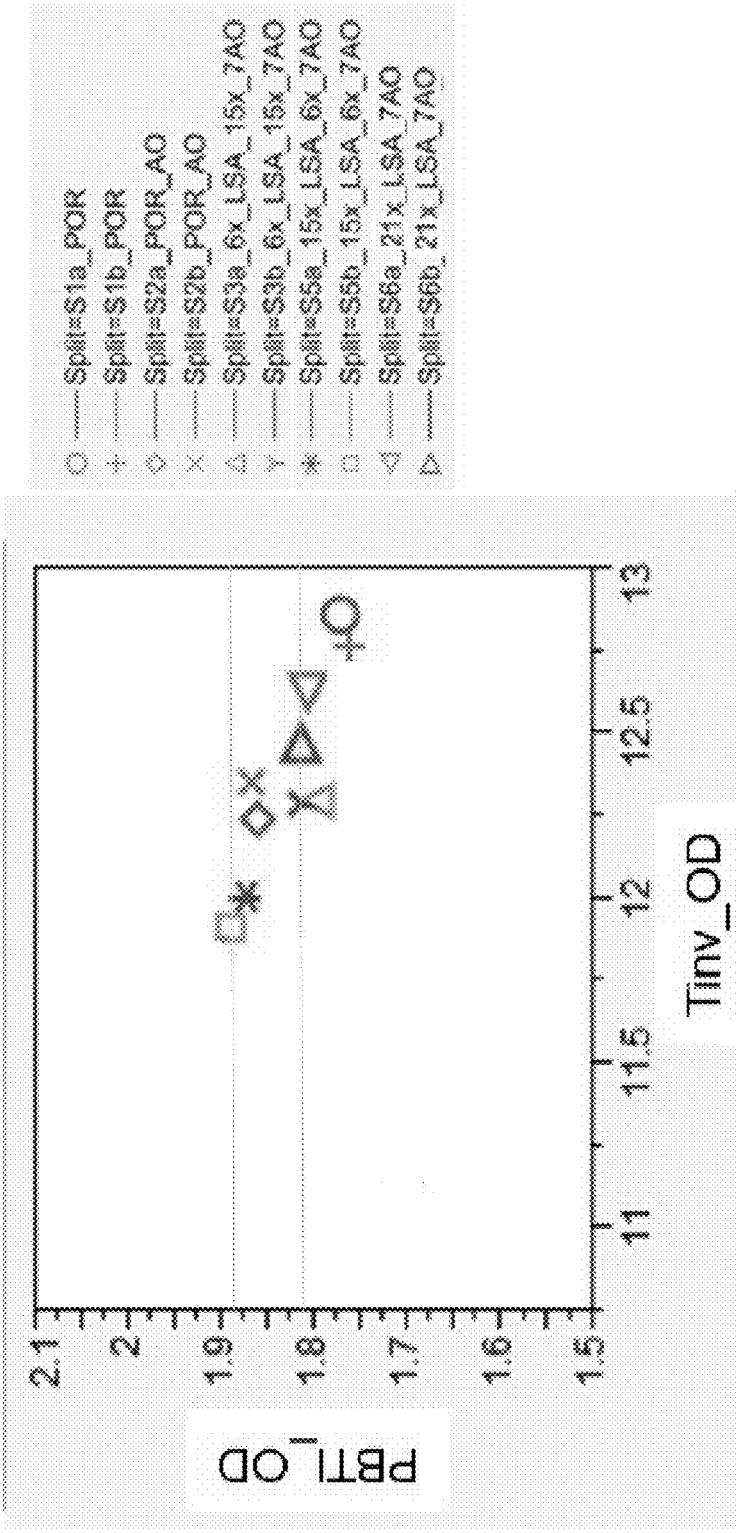

Spill=S1a_POR
Spill=S1b_POR
Spill=S2a_POR_AO
Spill=S2b_POR_AO
Spill=S3a_6x_LSA_15x_7AO
Spill=S3b_6x_LSA_15x_7AO
Spill=S5a_15x_LSA_6x_7AO
Spill=S5b_15x_LSA_6x_7AO
Spill=S6a_21x_LSA_7AO
Spill=S6b_21x_LSA_7AO
PBTI_OD
2.1
2
1.9
1.8
1.7
1.6
1.5
11
11.5
12
12.5
13
Tinv_OD

FIG. 13

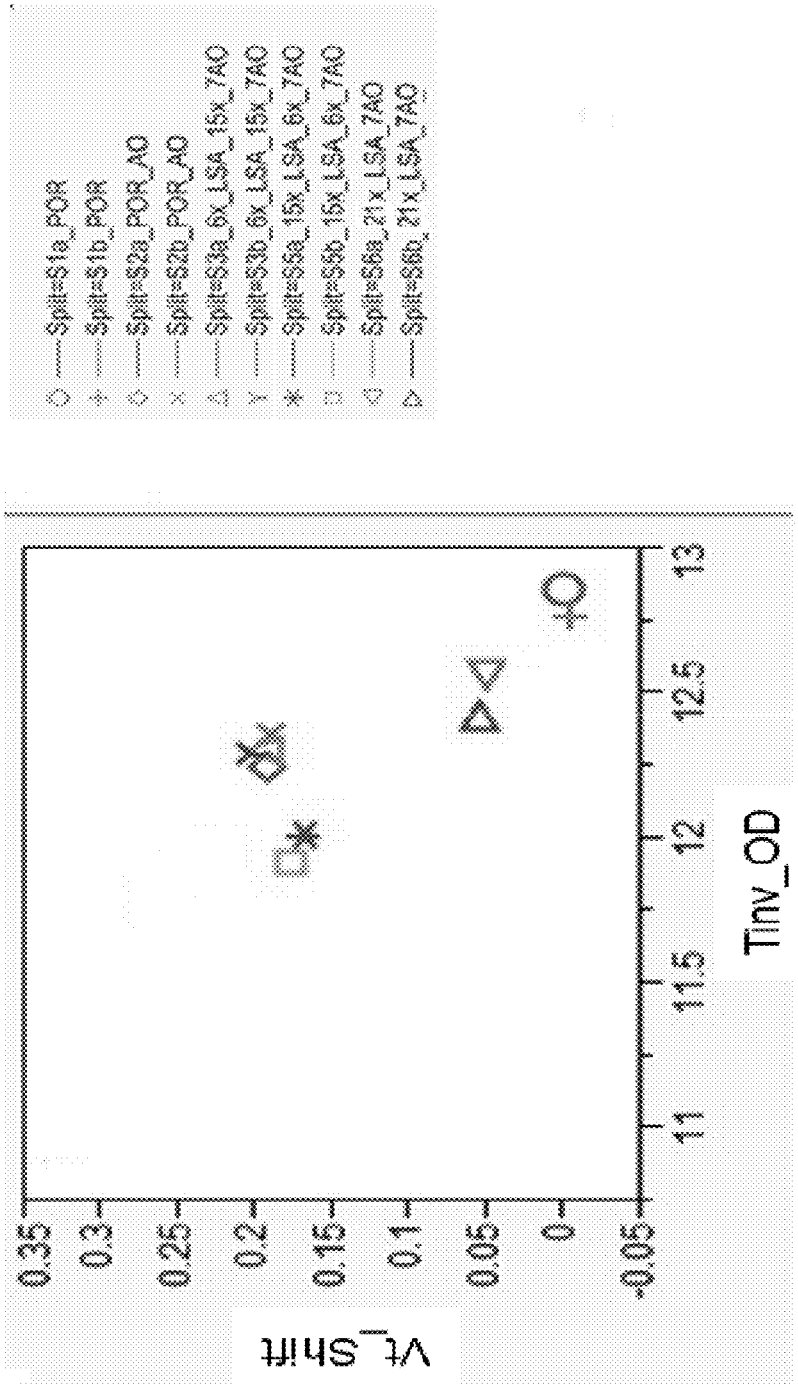

Split=S1a_POR
Split=S1b_POR
Split=S2a_POR_AO
Split=S2b_POR_AO
Split=S3a_6x_LSA_15x_7AO
Split=S3b_6x_LSA_15x_7AO
Split=S5a_15x_LSA_6x_7AO
Split=S5b_15x_LSA_6x_7AO
Split=S6a_21x_LSA_7AO
Split=S6b_21x_LSA_7AO
Vt_Shift
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
-0.05
11
11.5
12
12.5
13
Tinv_OD

FIG. 14

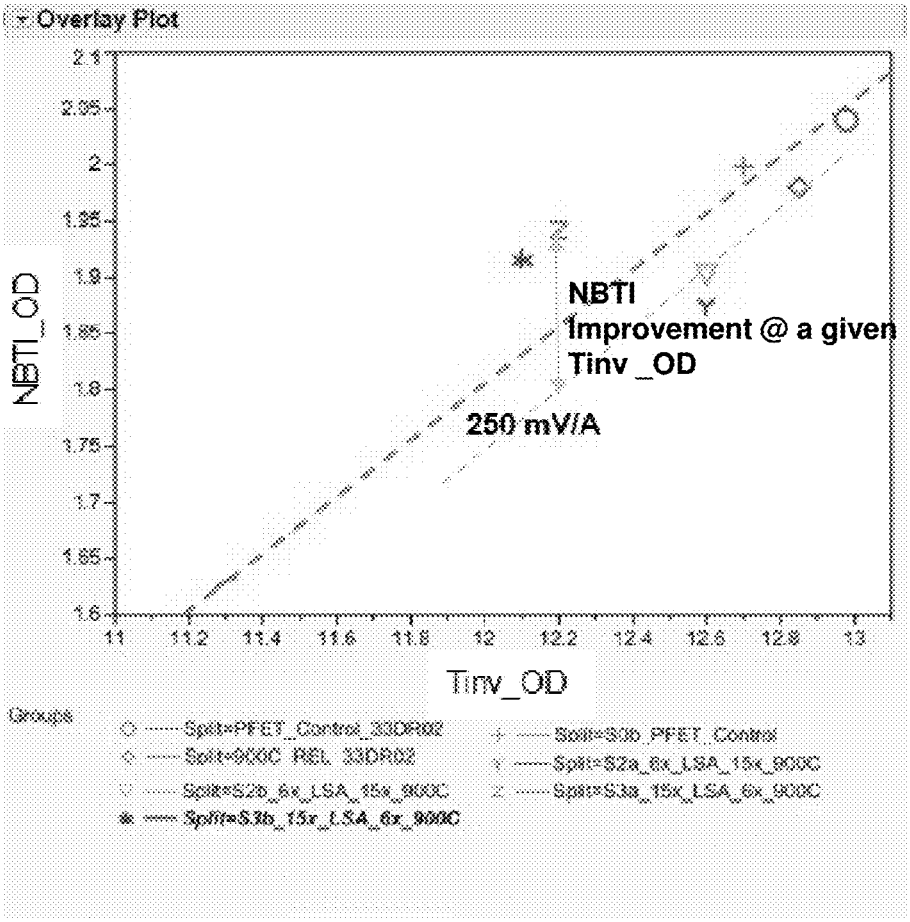

Overlay Plot
NBTI_OD
Tinv_OD
NBTI
Improvement @ a given
Tinv _OD
250 mV/A
Groups
Split=PFET_Control_33DR02
Split=S2b_6x_LSA_15x_900C
Split=S3b_15x_LSA_6x_900C
Split=S3b_PFET_Control
Split=S2a_6x_LSA_15x_900C
Split=S3a_15x_LSA_6x_900C

FIG. 15

GATE STACK FORMED WITH INTERRUPTED DEPOSITION PROCESSES AND LASER ANNEALING

FIELD OF THE INVENTION

[0001] The invention relates to semiconductor structures and, more particularly, to semiconductor structures and methods of fabricating the same using interrupted deposition processes and laser annealing.

BACKGROUND

[0002] In increasing performance of a FET, it is known that gate dielectric reliability vs. Tiny scaling is a major industry trade-off. For example, increasing the thickness of a dielectric material stack increases reliability of the semiconductor device, but this increase in stack thickness will also decrease performance. Conversely, decreasing the thickness of a dielectric material stack can decrease reliability of the semiconductor device, but this decrease in stack thickness will also increase performance.

[0003] Also, as MOSFET devices are scaled down to less than 100 nanometers in gate or channel length, highly doped, shallow source and drain extension regions can be employed to achieve high drive current capability. The dopants are activated by conducting laser annealing or other millisecond-scale (mSec) annealing of the implanted extension regions either prior, during, or after a more conventional, second-scale Rapid Thermal Anneal (RTA).

SUMMARY

[0004] In an aspect of the invention, a structure comprises a high-k gate stack with a high-k bilayer or nanolaminate where a bottom portion of the bilayer is crystallized while a top portion of the bilayer is amorphous.

[0005] In an aspect of the invention, a method comprises a millisecond anneal to crystallize a lower portion of a high-k dielectric material with a top layer of the high-k dielectric material being amorphous, with restriction of a substrate preheat temperature during the millisecond anneal to below 600° C.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is described in the detailed description which follows, in reference to the noted plurality of drawings by way of non-limiting examples of exemplary embodiments of the present invention.

[0007] FIGS. **1-5** show fabrication processes and resultant structures in accordance with aspects of the invention.

[0008] FIG. **6**(*a*) shows a graph of XRD.

[0009] FIG. **6**(*b*) shows a FTIR spectra, comparing a high-k film fabricated using the processes of the invention (laser annealing) and structures fabricated using conventional fabrication processes.

[0010] FIG. **7** shows a graph of gate leakage, comparing a structure fabricated using the processes of the invention (laser annealing) and structures fabricated using conventional fabrication processes (RTA anneals).

[0011] FIG. **8** shows a graph of NFET reliability (PBTI), comparing a gate stack structure fabricated using the processes of the invention (laser annealing) and structures fabricated using conventional fabrication processes (RTA anneals).

[0012] FIG. **9** shows a graph of PFET reliability (NBTI), comparing a gate stack structure fabricated using the processes of the invention (laser annealing) and structures fabricated using conventional fabrication processes (RTA anneals).

[0013] FIG. **10** shows thermal traces of different anneals: Laser, Flash, Flash pre-heat, Spike RTA & Furnace.

[0014] FIG. **11** shows a SIMS profile, with lanthanum (labeled "AO") diffusion comparing a high-k film fabricated using the processes of the invention (laser annealing) and structures fabricated using conventional RTA anneal fabrication processes.

[0015] FIG. **12** shows the Vtlin graph comparing the structures fabricated using the processes of the invention and structures fabricated using conventional fabrication processes.

[0016] FIG. **13** shows a graph of device reliability (e.g., PBTI), comparing a structure fabricated using the processes of the invention and structures fabricated using conventional fabrication processes.

[0017] FIG. **14** shows a graph of device reliability (e.g., NFET Vt shift vs. TinvOD), comparing a structure fabricated using the processes of the invention and structures fabricated using conventional fabrication processes.

[0018] FIG. **15** shows a graph of device reliability (e.g., PFET Reliability: NBTI), comparing a structure fabricated using the processes of the invention and structures fabricated using conventional fabrication processes.

DETAILED DESCRIPTION

[0019] The invention relates to semiconductor structures and, more particularly, to semiconductor structures and methods of fabricating the same using interrupted deposition processes and laser annealing. More specifically, the processes described herein rely on a technique of interrupted atomic layer deposition (ALD) of dielectric material with short-scale (laser) annealing processes. Even more specifically, in embodiments, the processes described herein integrate a high-k dielectric laser annealing with La_2O_3 deposition and diffusion processes allowing for significant improvements of negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) in high-k gate stack structures while providing a wide range of threshold voltage tunability.

[0020] Normally high-k gate oxides are formed by atomic layer deposition (ALD) processes followed by a post deposition (PDA) rapid thermal anneal (RTA) in order to improve the interfacial and bulk properties of the high-k material. The high-k film remains amorphous after RTA PDA conducted at ~700-800° C. The crystallization threshold RTA temperature depends on specific high-k materials used in the stack and is about 800° C.-850° C. for the ultrathin (<3 nm) hafnium oxide layers and is about 400° C.-500° C. for similar zirconium oxide layers, for instance. The threshold crystallization temperature is also high-k thickness dependent being higher for thinner high-k films. An amorphous gate dielectric material is considered to be desirable because the crystallization of high-k layers has multiple detrimental side effects. Crystallization releases excess oxygen atoms from the high-k film causing growth or thickening of the low-k interfacial layer.

[0021] Further, the crystalline high-k material has a higher speed of diffusion for oxygen atoms and oxygen vacancies allowing for their transport from transistor exterior to its

channel region where they affects threshold voltage and uniformity of the interfacial layer. In addition, crystallization of high-k material causes surface roughness and material property variation between crystalline grains, which, in turn, results in non-uniform electrical fields in the channel region adjacent to the dielectric film. This, in turn, significantly degrades device performance. Further, a crystalline high-k film may have an enhanced gate leakage due to the presence of grain boundaries which serve as leakage paths. In general, the crystallization of high-k films in gate stacks is either avoided altogether or postponed until later in the process sequence when high-k layers are sealed mitigating detrimental effects caused by crystallization.

[0022] However, the inventors designed a millisecond Laser Anneal (LA) process for the PDA that crystallizes the high-k film as shown by the appearance of a XRD peak at 28 degrees as shown in FIG. **6**(*a*). The millisecond LSA had a low base substrate temperature of about 250° C., ramp up and ramp down rates in excess of 1e5° C./sec, the peak temperature of 1200° C. and the duration of about 250 microseconds measured at 100° C. lower than the peak temperature. The width of XRD peak in FIG. **6**(*a*) suggests the size of crystallites produced by millisecond LSA to be around 1.5-2 nm. The inventors also noted that the crystallization threshold temperature for the millisecond LSA was about 200-300° C. higher than the crystallization threshold temperature induced by RTA PDA. The high-k film crystallization is further confirmed by FTIR spectroscopy in FIG. **6**(*b*) which shows a mixture of monoclinic and tetragonal phases in crystalline high-k film. The inventors discovered that this LSA PDA treated crystalline high-k film stack leads to lower gate leakage current compared to the amorphous high-k film of same effective electrical thickness, which is completely counterintuitive and unexpected. (See, e.g., FIG. **7**.) Quite surprising to the inventors, this LSA PDA treated crystalline high-k film stack leads to superior gate stack reliability at scaled Tiny, relevant for sub-20 nm planar and FinFET technologies. The improved PBTI lifetimes (for NFETs) and NBTI lifetimes (for PFETs) at scaled Tiny is shown in FIG. **8** and FIG. **9**. This further proves that the NBTI/PBTI lifetimes improve with the ramps rates of the different anneals used for high-k PDA. The ultra short millisecond-scale laser anneal showed best PBTI & NBTI reliability (highest lifetimes) compared to second-scale anneals like RTA and spike RTA and minute-scale furnace anneals. The thermal profiles of these anneals are shown in FIG. **10**. Flash millisecond anneal (also labeled as "fRTP" in FIG. **10**) has an RTA preheat component (labeled as "Flash Btm") as well as a millisecond spike anneal (labeled as "Flash"). The inventors also observed that the presence of high RTA preheat in flash annealing degrades NBTI/PBTI improvements obtained with LA PDA. Accordingly, the millisecond flash anneal can be used as an alternative millisecond PDA if its RTA preheat component is limited to below 600 C.

[0023] Doping the high-k material, on the other hand, provides other advantages such as tuning the effective work function (EWF) and associated threshold voltage of transistors. This, in turn, provides the ability to make multi-work function devices by intentionally varying concentration of high-k dopants. High-k stack doping with metallic elements such as La, Mg is known to be effective in altering or tuning EWF over the range of several hundred millivolts.

[0024] In order to make devices with multiple threshold voltages, Vt, for both logic FETs & SRAM FETs, a capping layer of lanthanum or magnesium containing material such as lanthanum oxide (La2O3), magnesium oxide (MgO) or similar oxides is selectively placed on top of the high-k dielectric film in before the metal gate deposition. These layers provide a source of the doping atoms that will form dipoles within the dielectric and its interfaces. In order to form these dipoles, the atoms are diffused through the dielectric layer and then react with or scavenge oxygen atoms of the dielectric layer. An annealing process is required for diffusing and reacting these atoms to form dipoles. The dipoles formed near the vicinity of semiconducting substrate such as at the high-k/SiOx or substrate/SiOx interfaces lead to a shift in a flatband voltage and an associated shift of threshold voltage Vt. Ability to induce larger flatband shifts is desirable since it enables forming transistors with a plurality of threshold voltages.

[0025] However, integrating the Vt-shift inducing doping technique and the laser-crystallized high-k film results in a much lower Vt shift (~70 mV) than that of the conventional RTA annealed amorphous high-k film gate stack (~200 mV). This reduces the threshold voltage tunability range for multi-Vt transistors. The inventors found that the laser-crystallized high-k film impedes the diffusion of dopant (e.g. La) through the high-k film compared to the case of conventionally annealed amorphous high-k film. To solve this problem, the processes described herein provide an interrupted or bilayer high-k deposition process whose top part is an amorphous high-k film and the bottom part is a crystalline high-k film.

[0026] FIG. **11** shows the SIMS profile of the laser-annealed and conventionally annealed high-k film. The amount of diffused La atoms is summarized in Table 1 and labeled as "SIMS AO". In Table 1, #1 labeled as "LA 1200" in the PDA column has deficient La due to LA induced recrystallization (see FIGS. **6**(*a*) and (*b*)); whereas, #3 has normal La penetration by placing the LA annealing later to avoid high-k crystallization prior to Spike RTA drive-in step (column "Rel. anneal") and #2, #4, and #5 have La penetration similar to #3 while not using any millisecond annealing.

TABLE 1

5-Wafers_thinHiK_LSA_AO_2.xls 13162SD7001.013 FA9991 CP7819 A. Dasgupta

Slot#		Wafer id	IL	HK	PDA	AO	SIMS AO/ cm2	Cap TiN	a-Si cap	Rel. anneal	cap TiN skip	PG patt wets	Late PDA	TF-XRD
24	1	Q8WFA4	POR	21cyc	LSA 1200	7x	1 .0E14	15A MO	POR	970C Spike		ver. C		
25	2	Q7WFD5	POR	23cyc	RTA PDA	7x	1.71E14	15A MO	POR	970C Spike		ver. C		
22	3	NJWFE4	POR	21cyc	skip PDA	7x	1.87E14	15A MO	POR	970C Spike		ver. C	LSA 1200	

TABLE 1-continued

5-Wafers_thinHiK_LSA_AO_2.xls 13162SD7001.013 FA9991 CP7819 A. Dasgupta

Slot#		Wafer id	IL	HK	PDA	AO	SIMS AO/ cm2	Cap TiN	a-Si cap	Rel. anneal	cap TiN skip	PG patt wets	Late PDA	TF-XRD
23	4	1NIWFA2	POR	21cyc	skip PDA	7x	2.08E14	15A MO	POR	970C Spike		ver. C		
10	5	36TSEG6	POR	21cyc	RTA PDA	7x	1.92E14	15A MO	POR	970C Spike		ver. C		

[0027] The structures described herein can be manufactured in a number of ways using a number of different tools. In general, though, the methodologies and tools are used to form structures with dimensions in the micrometer and nanometer scale. The methodologies, i.e., technologies, employed to manufacture the structures described herein have been adopted from integrated circuit (IC) technology. For example, the structures of the present invention are built on wafers and are realized in films of material patterned by photolithographic processes on the top of a wafer. In particular, the fabrication of the structures uses three basic building blocks: (i) deposition of thin films of material on a substrate, (ii) applying a patterned mask on top of the films by photolithographic imaging, and (iii) etching the films selectively to the mask. In accordance with aspects of the present invention, the structure also undergoes two annealing process as represented by the arrows in FIGS. **2** and **5**.

[0028] More specifically, FIG. **1** shows a structure and respective fabrication processes in accordance with aspects of the invention. As shown in FIG. **1**, the structure **10** includes an interfacial layer **14** formed over a substrate **12**. In embodiments, the interfacial layer **14** can be a chemical oxide or oxynitride, deposited to a thickness of about 6 Å to 7 Å; although other thicknesses are contemplated herein, e.g., about 9 Å to 10 Å. The substrate **12** can include an nFET side and a pFET side, as an example. The substrate **12** can be any suitable semiconductor material including, but not limited to, Si, SiGe, SiGeC, SiC, Ge alloys, GaAs, InAs, InP, and other III/V or II/VI compound semiconductors. The semiconductor material of substrate **12** is lightly doped having doping polarity opposite to the FET type, e.g. a lightly doped n-type or p-type semiconducting material for pFET and nFET, respectively.

[0029] While the substrate **12** is drawn as a horizontal slab, it is equally representative of various three-dimensional transistors where the substrate **12** may be oriented differently and/or may have a different shape. Such three-dimensional, non-planar transistors include finFETs, surround-gate FETs, multiple-gate FETs, nano-wire or nano-sheet FETs, vertical FETs, and others. The substrate **12** can further include sidewall isolation structures and doped source and drain structures and metallic contacts that are not shown. The sequential order of making various useful elements that may exits in the substrate **12** can also be different. For instance, the source drain structures and isolation features can be formed prior to making interfacial layer **14**. This approach is known as the replacement gate sequence.

[0030] In FIG. **1**, a thin layer of dielectric material **16** is formed on the interfacial layer **14**. In embodiments, the dielectric material **16** can be a high-k dielectric material such as hafnium based material (e.g., HfO_2) or zirconium based material (ZrO_2), as non-limiting examples of a high-k dielectric material. The dielectric material **16** can be formed using chemical vapor deposition (CVD) processes or an atomic layer deposition (ALD) processes over several cycles, e.g., 6 cycles to 25 cycles, resulting in a thickness of about 20 Å or less (noting that a single cycle results in a deposition thickness of about 0.75 Å).

[0031] There is a minimum number of cycles needed to make the film continuous because the film nucleates as islands and then, as the number of cycles increases, the islands coalesce forming a continuous layer. There is also a minimum number cycles needed to make the film uniform, a point at which the islands completely merge forming a uniform layer. With the continuous need to scale down gate dielectrics, the CVD/ALD deposition processes as well as the properties of the interfacial layer **14** are optimized to make a highly-uniform ultra-thin gate dielectric film with the lowest number of cycles. An optimized process runs at 1-4 cycles above the point where the film becomes completely uniform. 5-8 cycles are typically needed to make the film continuos. For instance, a state-of-the-art deposition process runs about 21 cycles yielding a highly uniform high-k layer of about 16 Å to 16.5 Å in thickness. The point at which thickness uniformity of the film degrades is about 17 cycles or about 13 Å to 13.5 Å in thickness. The point at which the film becomes discontinuous is about 5-8 cycles or about 3.5 Å to 6 Å in thickness.

[0032] In accordance with the invention, as shown in FIG. **2**, the deposition process of the high-k dielectric material **16** is interrupted (e.g., stopped between 6 to 15 cycles) to perform a laser anneal process. In one more specifically contemplated embodiment, the deposition process of the high-k dielectric material **16** is interrupted after the high-k film becomes continuos. In another specifically contemplated embodiment, the deposition process of the high-k dielectric material **16** is interrupted prior to the high-k film becomes fully uniform. That is, the interruption occurs between 6 cycles to 15 ALD cycles of depositing dielectric material **16** and a laser anneal is performed. More specifically, after the interruption of the ALD deposition of the dielectric material **16**, the structure undergoes laser anneal on the order of about 100 to 3000 microseconds measured at 100° C. below temperature peak value at a peak temperature range of about 1000° C. to 1250° C. Preferred substrate base temperature is from the room temperature to about 500° C. with 150° C. to 300° C. being preferred. Preferred range of heat up and cool down rates is from about 1e4 to about 1e6° C./sec. In alternate embodiments, the anneal process can be a flash anneal with similar peak temperatures and durations. For the flash anneal, a low preheat temperature of below 550° C. is highly desirable.

[0033] As described above and shown in FIG. **6**, the laser anneal process forms a crystalline high-k dielectric material resulting in a micro-crystallized layer **16'** on top of the interfacial layer **14**. The annealing process is followed by a second sequence of more cycles of high-k dielectric material **16**. Thus, a bi-layer high-k dielectric stack, consisting of an

amorphous high-k dielectric material **16** on top of crystalline high-k dielectric material **16'** is formed. The electrical properties of the gate stack are governed by this bi-layer high-k dielectric stack (**16**, **16'**) and the interface **16"** between the crystalline high-k film **16'** and the interfacial layer **14**. In embodiments, the dielectric material **16** can be high-k dielectric material such as a hafnium based material (e.g., HfO_2) or a zirconium based material (ZrO_2), as non-limiting examples of a high-k dielectric material. In embodiments, the high-k dielectric material **16** can be formed using chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process over several cycles, e.g., 6 cycles to 15 cycles, depending on a number of cycles used to form the high-k dielectric material **16'**.

[0034] In one more specifically contemplated embodiment, the crystalline dielectric material **16'** can be formed using ALD processes of 15 cycles (when the dielectric material **16** is formed in 6 cycles). In another more specifically contemplated embodiment, the crystalline dielectric material **16'** can be formed using ALD processes over 11 cycles (when the dielectric material **16** is formed in 10 cycles). In embodiments, the total thickness of both the dielectric materials **16**, **16"** should be about 16 Å to 16.5 Å, e.g., on the order of 19 to 21 cycles total. In other embodiments, the total thickness of both the dielectric materials **16**, **16"** is selected to form a highly-uniform ultra-thin high-k layer.

[0035] In FIG. **4**, a blocking material **18** is deposited on the high-k dielectric material **16**. In embodiments, the blocking material **18** can be, e.g., TiN, or a composite sandwich of TiN/oxide/TiN deposited to a thickness of about 35 Å to 50 Å on both the nFET side and the pFET side of the structure. It should be understood by those of skill in the art that other thicknesses are also contemplated by the present invention. The blocking material **18** can be deposited using a CVD or ALD process.

[0036] Still referring to FIG. **4**, the blocking material **18** can be removed from the nFET side of the preselected devices to expose an upper surface of the high-k dielectric material **16**. In embodiments, the blocking material **18** is removed using conventional lithography and etching processes. For example, a photoresist can be formed on blocking material **18** (not shown) which is then exposed to energy (light) through a mask to form a pattern. A reactive ion etching (RIE) is performed through the resist pattern to remove the blocking material **18** over the nFET side of the device, exposing a surface of the high-k dielectric material **16**. Following reactive ion etching, the resist material is removed using an oxygen free resist ashing process.

[0037] Following the patterning, lanthanum oxide film (La_2O_3) **20** is deposited on the blocking material **18** and the exposed surface of the high-k dielectric material **16**, on the nFET side of the preselected devices. In embodiments, a magnesium based material or other materials which form dipoles that shift Vt can be used in the processes described herein. In embodiments, the film **20** can be formed by ALD processes. In more specific embodiments, the La_2O_3 film **20** is deposited in 7 cycles of the ALD process.

[0038] In FIG. **5**, a capping layer **22** is formed over the film **20**. In embodiments, the capping layer **22** is TiN, formed by a CVD or ALD process. In embodiments, the optional capping layer **22** will prevent the film **16** from crystallizing during subsequent annealing processes. Moreover, the optional capping layer **22** can protect the film **20** from interacting with the ambient of the subsequent annealing process during the subsequent annealing process.

[0039] An optional a-Si capping layer **24** is formed on the capping layer **22**. In embodiments, the a-Si capping layer **24** can be deposited to a thickness of about 15 Å to about 20 Å using CVD processes. The a-Si capping layer **24** will prevent interaction between the capping layer **22** or capping layer **18** and the ambient of the subsequent annealing process. In this way, the a-Si capping layer **24** can prevent oxidation of the TiN films.

[0040] Still referring to FIG. **5**, the structure undergoes an additional annealing process. More specifically, the annealing process includes a anneal, e.g., a triangular-shaped anneal with a ramp-up and ramp down rates of about 100° C./s and a duration of about two seconds at about 50° C. below the peak temperature. The peak temperature of such the anneal is from about 900° C. to about 1050° C. and the peak temperature of the laser anneal from about 1200° C. to about 1300° C. In embodiments, the annealing process will drive the lanthanum into the nFET side of the selected devices, e.g., toward the substrate **12**, through the bilayer high-k dielectric material **16**, **16'** and toward the interface **16"** between the HfOx and SiOx **14** and the interface between substrate interfacial layer **14** and the substrate **12**, to form dipoles which shift the Vt for the nFET transistor; whereas, the blocking material **18** over the pFET area and unselected nFETs will prevent such diffusion of the lanthanum into this pFET transistors and unselected nFETs. In one more specifically contemplated embodiments, the anneal process parameters are selected to prevent crystallization of material **16** while enabling the drive-in process for La atoms and a reaction to form La-based dipole. This selection is afforded by the presence of capping layers **22**, **24** that have an effect of shifting crystallization threshold for material **16** toward higher temperatures.

[0041] Advantageously and unexpectedly, the laser crystallizing anneal conducted while interrupting high-k deposition cycles improves gate leakage, negative-bias temperature instability (NBTI) and positive bias temperature instability (PBTI) of the gate stack; whereas, La_2O_3 attains lower nFET Vt and hence provides the ability to use multiple Vt nFET transistors while providing improved Tiny scaling and improved PBTI. In this way, it is possible to integrate La_2O_3 with the high-k dielectric crystallizing millisecond anneals to obtain the synergistic benefits of both processes.

[0042] FIG. **12** shows a Vtlin graph comparing the structures fabricated using the processes of the invention and structures fabricated using conventional fabrication processes. The x-axis of the graph represents several different structures, with the last three structures, e.g., labeled S**5***b*, S**6***a* and S**6***b*, implementing embodiments of the invention. The y-axis is Vtlin.

[0043] More specifically, the structures labeled S**1***a*, S**1***b*, S**2***a*, S**2***b*, S**3***a* and S**3***b* include the following conventional process parameters, respectively:

[0044] (i) 19 deposition cycles of high-k dielectric with a laser anneal (labeled LSA) at 1200° C.;

[0045] (ii) 19 deposition cycles of high-k dielectric with a laser anneal (labeled LSA) at 1200° C.;

[0046] (iii) 10 deposition cycles+9 deposition cycles of high-k dielectric with a laser anneal (labeled LSA) at 1200° C.;

[0047] (iv) 10 deposition cycles+9 deposition cycles of high-k dielectric with a laser anneal (labeled LSA) at 1200° C.;

[0048] (v) 15 deposition cycles+4 deposition cycles of high-k dielectric with a laser anneal (labeled LSA) at 1200° C.; and

[0049] (vi) 15 deposition cycles+4 deposition cycles of high-k dielectric with a laser anneal (labeled LSA) at 1200° C.

[0050] The fabrication processes for the structures labeled S5*b*, S6*a* and S6*b* include the following process parameters, respectively:

[0051] (i) 10 deposition cycles of high-k dielectric, followed by a laser anneal (labeled LSA) at 1200° C.+9 deposition cycles of high-k dielectric, a laser anneal (labeled LSA) at 1200° C. and 7 cycles of La_2O_3;

[0052] (ii) 15 deposition cycles of high-k dielectric, followed by a laser anneal (labeled LSA) at 1200° C.+4 deposition cycles of high-k dielectric, and 7 cycles of La_2O_3; and

[0053] (iii) 15 deposition cycles of high-k dielectric, followed by a laser anneal (labeled LSA) at 1200° C.+4 deposition cycles of high-k dielectric, and 7 cycles of La_2O_3.

[0054] As shown in FIG. **12**, the processes labeled S1*a*, S1*b*, S2*a*, S2*b*, S3*a* and S3*b* show a Vtlin (in volts) of about 0.4 V, e.g., Vtlin of approximately 0.37-0.4 V. In comparison, the structures fabricated in accordance with processes of the present invention, e.g., labeled S5*b*, S6*a* and S6*b*, show a Vtlin of about 0.2 V. Accordingly, the inventors observed a significant Vtlin shift of the order of approximately 200 mV for an nFET device for the inventive method fully recovering La-induced threshold shift.

[0055] FIG. **13** shows a graph of NFET device reliability (e.g., PBTI), comparing a structure fabricated using the processes of the invention and structures fabricated using conventional fabrication processes. The y-axis shows PBTI and the x-axis shows Tiny. The structure labeled POR are processes of records, compared to the remaining processes which are provided in accordance with aspects of the invention. Clearly there is a significant improvement of the PBTI performance of the structures which implement embodiments of the invention, particularly S5*a* and S5*b*. So, for example, by implementing the processes of the present invention PBTI_OD (corrected for effective work function or EWF) is ~70-75 mV higher (better reliability) and at a lower Tiny (hence better transistor performance). Accordingly, it is shown that it is possible to combine additional PBTI benefits afforded by the crystallizing laser anneal with the La-based threshold voltage shift.

[0056] FIG. **14** shows a graph of NFET Vt shift vs. TinvOD, comparing a structure fabricated using the processes of the invention and structures fabricated using conventional fabrication processes such as non-crystallizing RTA anneals in the absence of La-containing material. As shown in FIG. **14**, using the processes described herein, e.g., Split HK=HK1/LSA PDA_1200° C./HK_2, it is possible to diffuse La to form dipoles at the SiOx/HfO_2 and SiOx/substrate interfaces and hence achieve Tiny scaling (e.g., hence better performance) and EWF reduction (for Multi WF devices). Also, using the processes described herein, it is possible to integrate the benefits of millisecond-scale crystallizing post deposition anneals (improved NBTI, PBTI, gate leakage) with La-induced work function shifts and Tiny electrical scaling.

[0057] FIG. **15** shows a graph of pFET reliability, NBTI), comparing a structure fabricated using the processes of the invention and structures fabricated using conventional fabrication processes. For example, a split labeled S3*a* and S3*b* with 900° C. RTA drive-in anneal is shown to provide significantly better NBTI than the NBTI-Tinv trendline. Thus, the bilayer high-k dielectric and related gate stack formed using the inventive processes improves PFET reliability (NBTI) at a scaled Tiny even at a reduced drive-in temperature preventing additional high crystallization and allowing for improved transistor performance.

[0058] Accordingly, by using processes of the present invention, the following was observed: improved gate leakage at lower work function of the metal gate stack, lower Tiny, improved gate stack reliability (PBTI, NBTI) and breakdown voltage (VBD), thus showing significant performance and reliability gains on both FinFET and planar devices.

[0059] Accordingly, a synergistic effect in improvement of device performance with the integration processes described herein. For example, the inventors observed Vtlin shift of the order of approximately 200 mV for an nFET device as shown in FIG. **12** (last three cells, S5*b* & S6*a* & S6*b*), comparable to a device formed using conventional fabrication processes, e.g., using only a single drive-in RTA process for driving La from a capping layer of La_2O_3 film through amorphous high-k film.

[0060] The method(s) as described above is used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[0061] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

What is claimed:

1. A method of fabricating a semiconductor structure, the method comprising performing a millisecond anneal to crystallize a lower portion of a high-k dielectric material with a top layer of the high-k dielectric material being

amorphous, with restriction of a substrate preheat temperature during the millisecond anneal to below a predefined temperature.

2. The method of claim **1**, wherein the millisecond anneal is a millisecond laser anneal.

3. The method of claim **1**, wherein the millisecond anneal is from 100 to 3000 microseconds measured at 100° C. below temperature peak value at a peak temperature range of from 1000° C. to 1250° C.

4. The method of claim **1**, further comprising depositing the high-k dielectric material in an interrupted atomic layer deposition (ALD) process with the millisecond anneal to crystallize the high-k dielectric material being performed during an interrupted cycle of the deposition of the high-k dielectric material.

5. The method of claim **4**, further comprising diffusing La or Mg atoms into the high-k dielectric bi-layer.

6. The method of claim **5**, further comprising creating multiple nFET transistors.

7. The method of claim **6**, wherein the La or Mg is provided over select transistors, diffusing La/Mg atoms through the high-k dielectric bi-layer.

8. The method of claim **1**, wherein the crystallizing of the lower portion of the high-k dielectric material is below 2 nm.

9. The method of claim **1**, wherein a thickness of the crystallized lower portion of the high-k dielectric material is less than 12 Å.

10. The method of claim **9**, wherein the high-k dielectric material contains La or Mg atoms.

11. The method of claim **10**, wherein an amount of atoms of the La or Mg atoms is larger than 1.5e14 atoms/cm^2.

12. The method of claim **9**, further comprising forming multiple nFET transistors where at least one of the nFET transistors has the La or Mg atoms.

13. The method of claim **9**, wherein the La or Mg atoms will form dipoles by binding with oxygen.

14. A method of fabricating a semiconductor structure, comprising:

forming an interfacial layer on a substrate;

forming a lower portion of a high-k dielectric bilayer on the interfacial layer;

performing a millisecond anneal to crystallize the lower portion of the high-k dielectric bilayer;

forming an upper portion of the high-k dielectric bilayer on the crystallized lower portion.

15. The method of claim **14**, wherein:

the forming the lower portion comprises performing a first number of deposition cycles of a high-k dielectric material; and

the forming the upper portion comprises performing a second number of deposition cycles of the high-k dielectric material after the millisecond anneal.

16. The method of claim **14**, further comprising restricting a substrate preheat temperature during the millisecond anneal to below a predefined temperature.

17. The method of claim **14**, wherein the millisecond anneal is a millisecond laser anneal.

18. The method of claim **14**, wherein the millisecond anneal is from 100 to 3000 microseconds measured at 100° C. below temperature peak value at a peak temperature range of from 1000° C. to 1250° C.

19. The method of claim **14**, further comprising diffusing La or Mg atoms into the high-k dielectric bi-layer.

20. The method of claim **14**, wherein:

the lower portion of the high-k dielectric bilayer is crystalline; and

the upper portion of the high-k dielectric bilayer is amorphous.

* * * * *