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(54) **NON-PLANAR SEMICONDUCTOR DEVICE WITH ASPECT RATIO TRAPPING**

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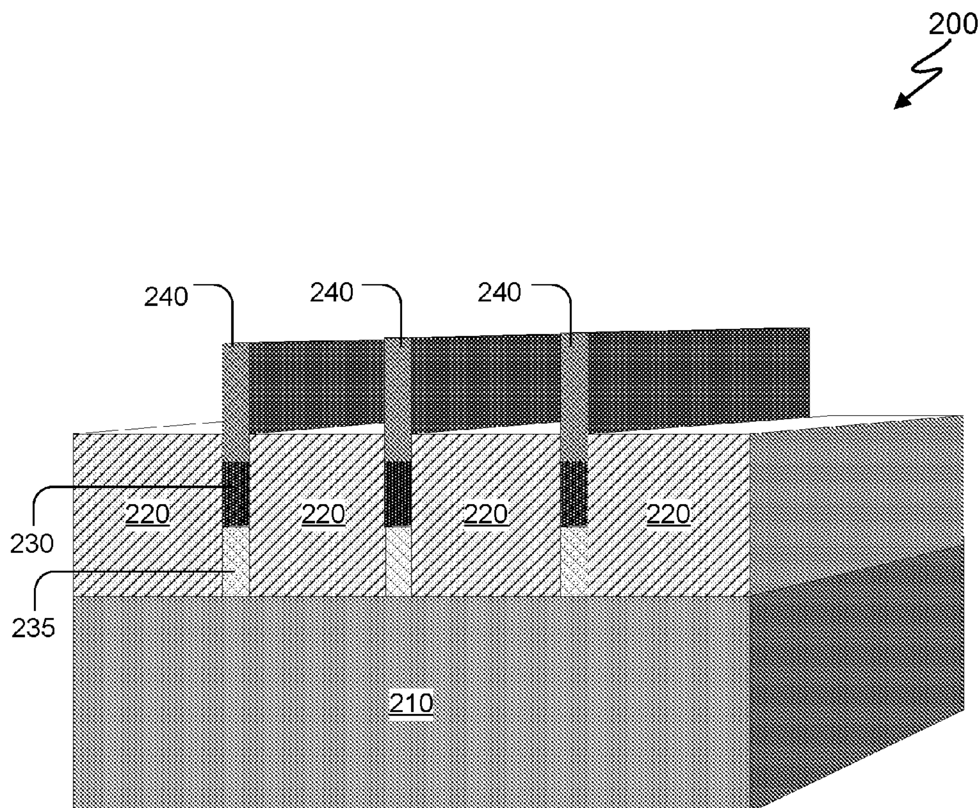
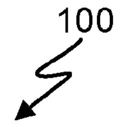
(57) **ABSTRACT**

As disclosed herein, a semiconductor device with aspect ratio trapping including, a bulk substrate, a plurality of isolation pillars formed on the bulk substrate, wherein one or more gaps are formed between the isolation pillars, an oxide layer formed by epitaxy on the bulk substrate, between the isolation pillars, wherein the oxide layer partially fills the gaps between the isolation pillars, one or more fins formed over the oxide layer between the isolation pillars, such that the one or more fins fill the gaps between the isolation pillars, wherein the oxide layer electrically isolates the one or more fins from the bulk substrate. The size of the gaps between the isolation pillars is selected to statistically eliminate defects caused by a lattice mismatch between the bulk substrate and the oxide layer. The semiconductor device may also contain an aspect-ratio trapping layer between the bulk substrate and oxide layer.





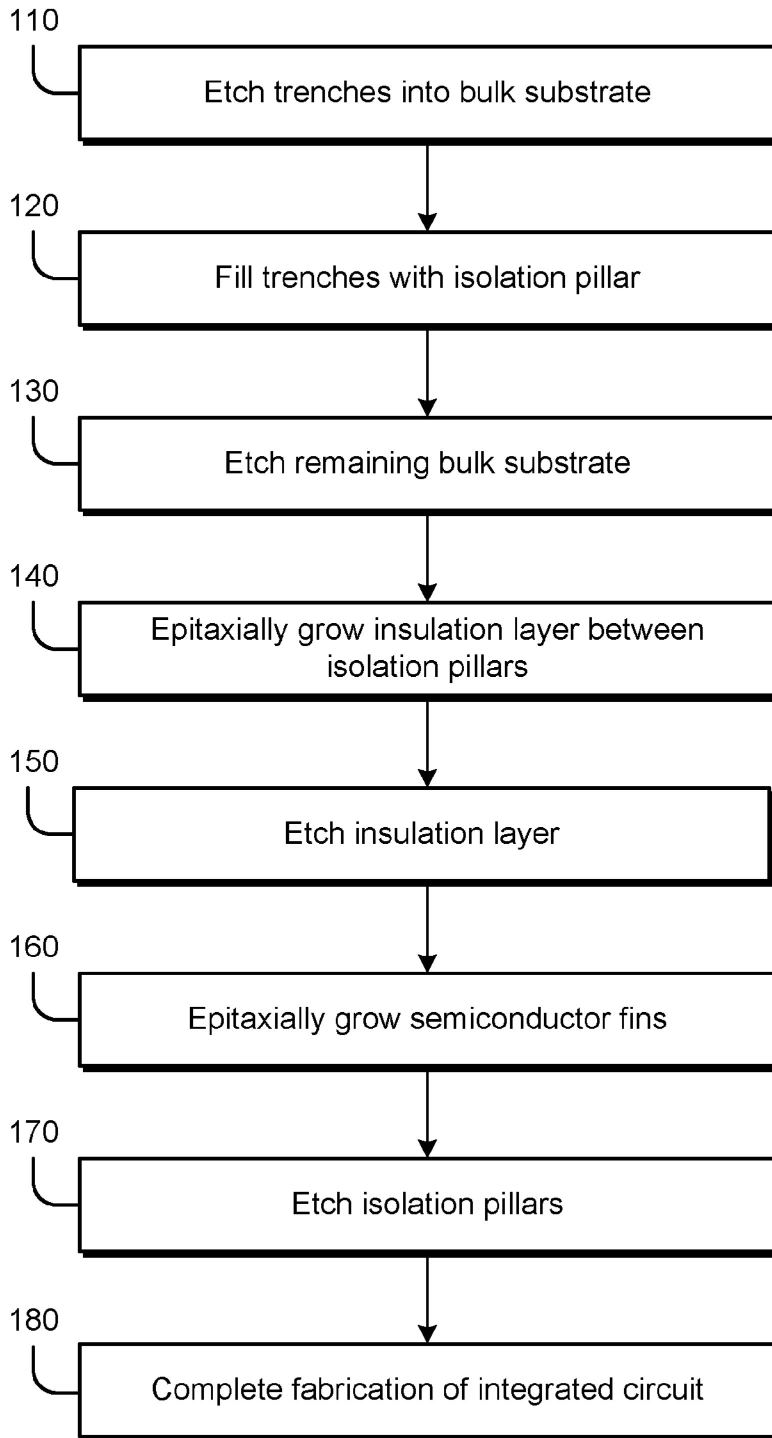


FIG. 1

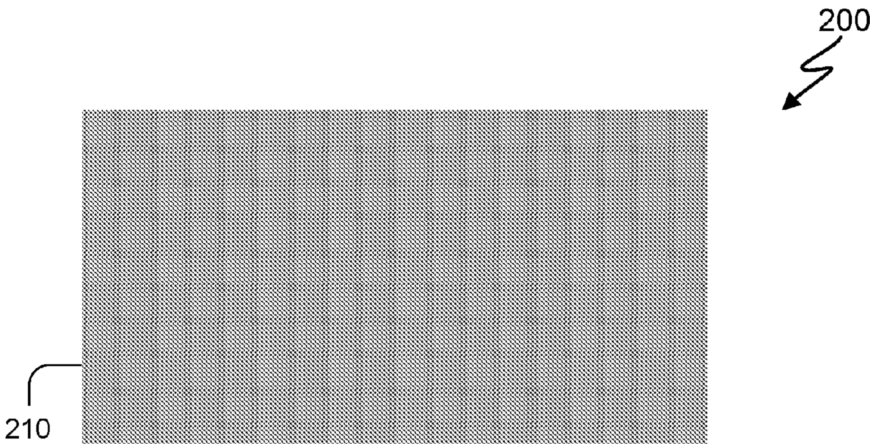


FIG. 2A

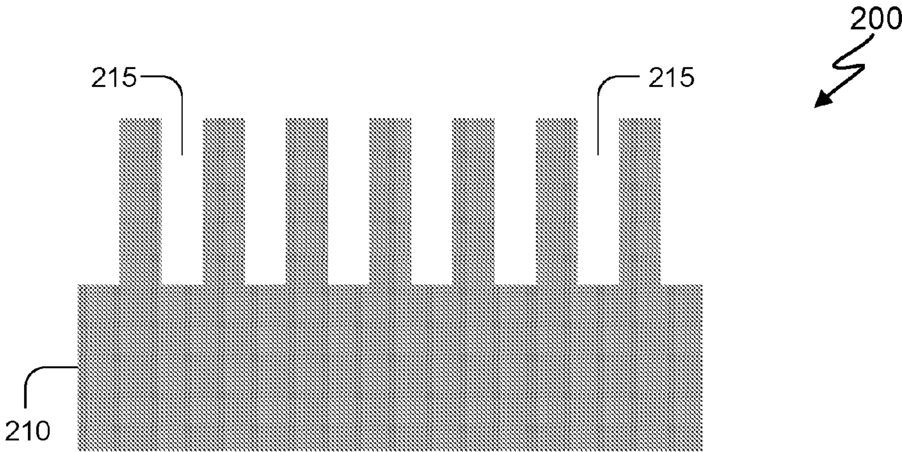


FIG. 2B

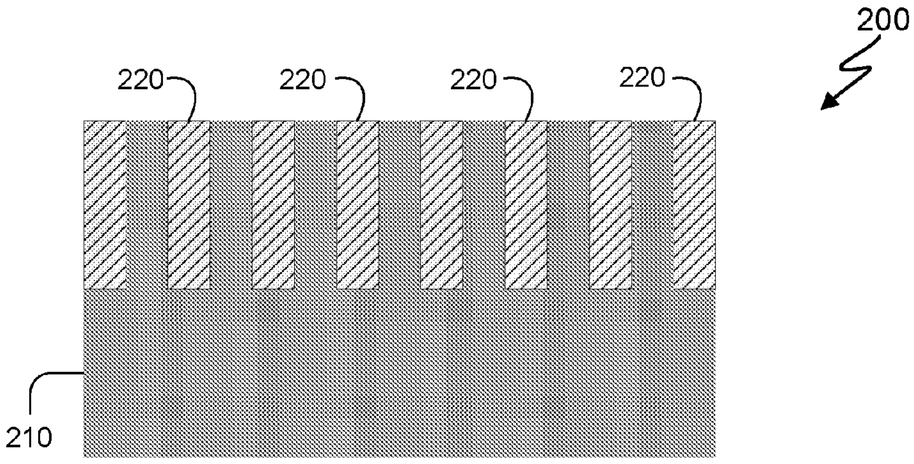


FIG. 2C

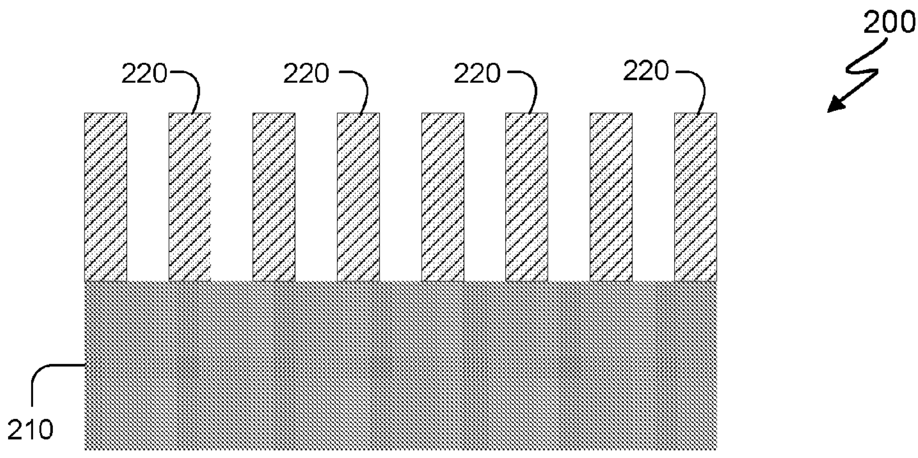


FIG. 2D

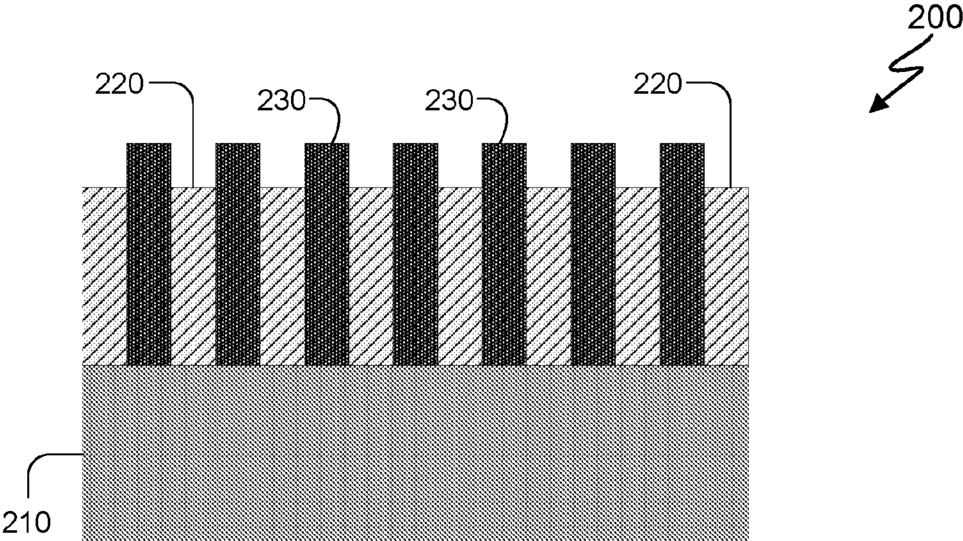


FIG. 2E

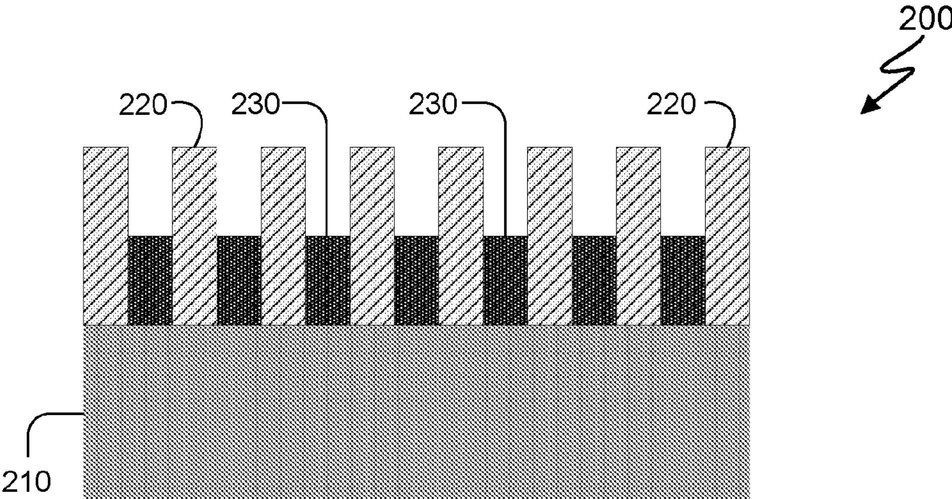


FIG. 2F

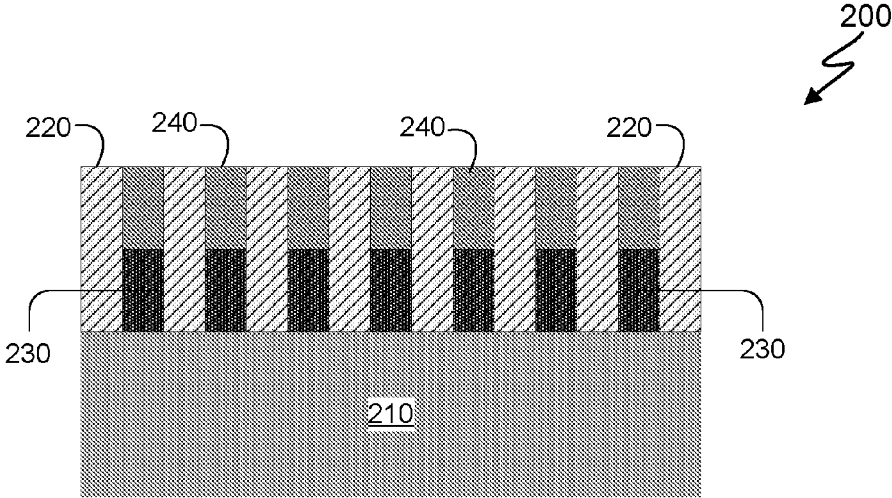


FIG. 2G

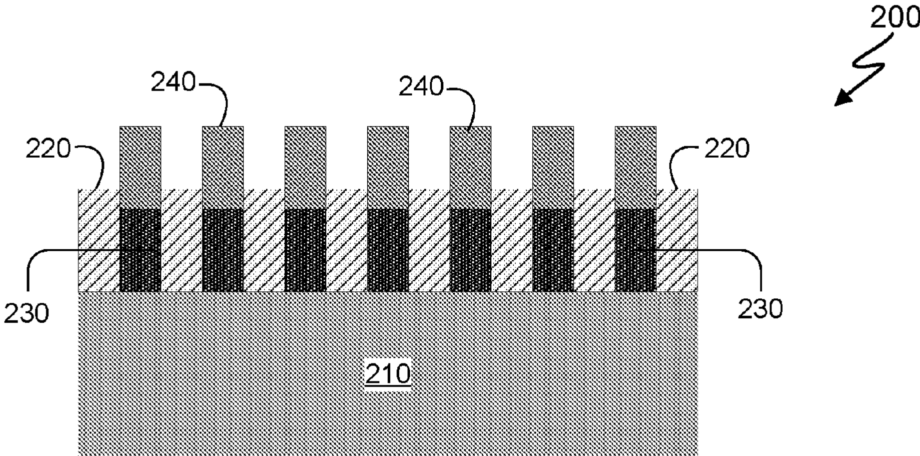


FIG. 2H

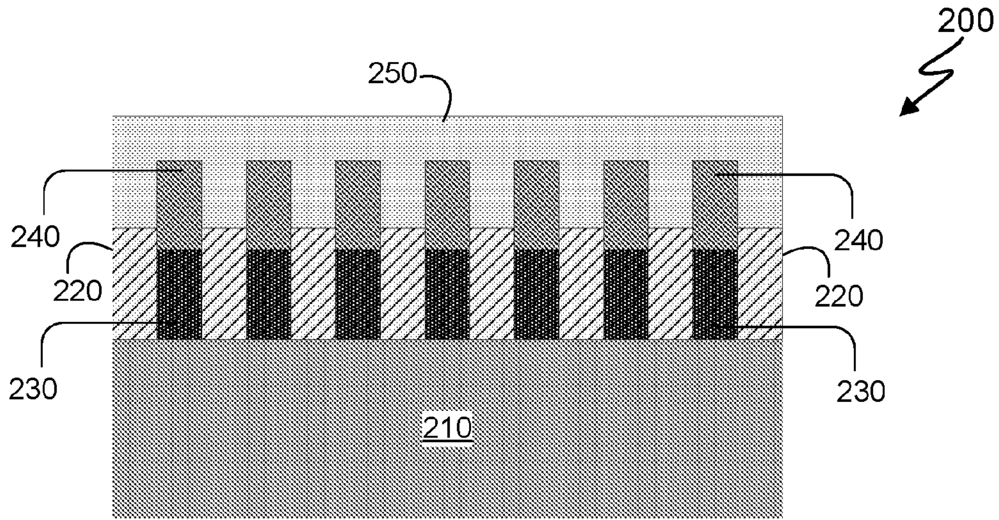


FIG. 2I

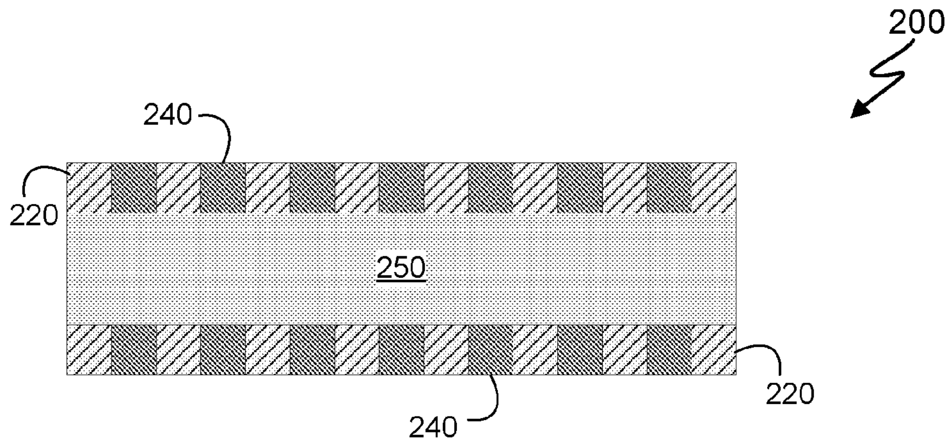


FIG. 2J

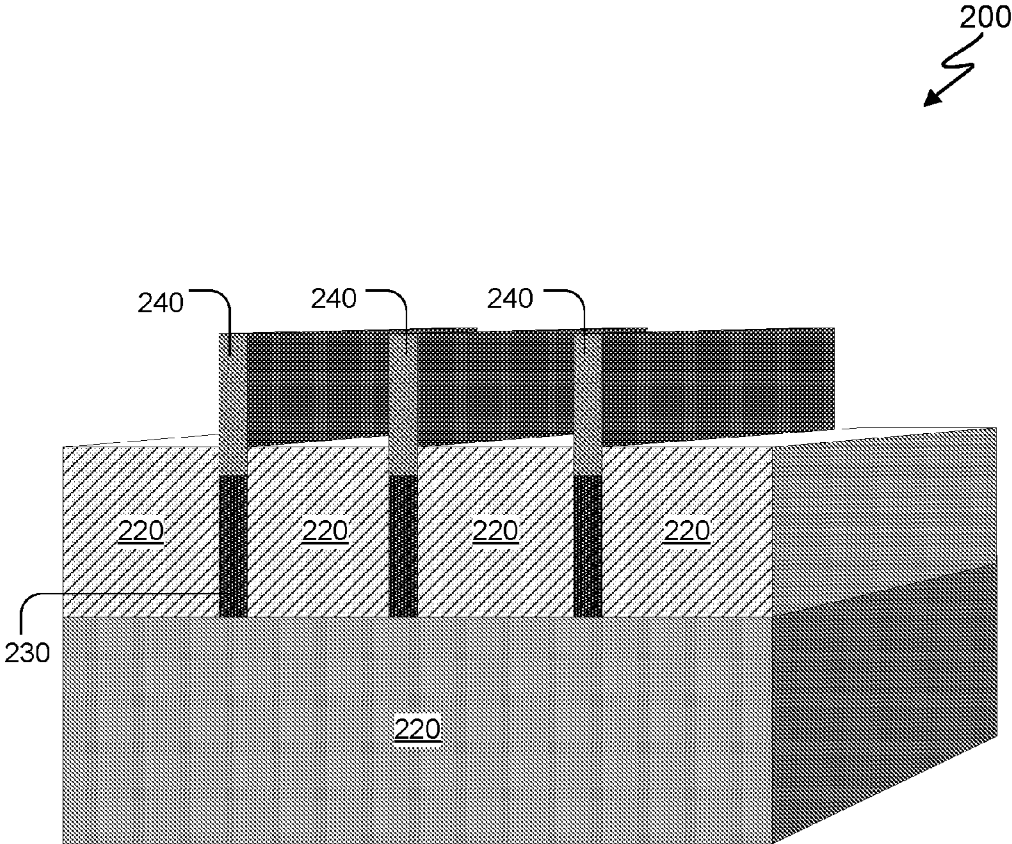


FIG. 3

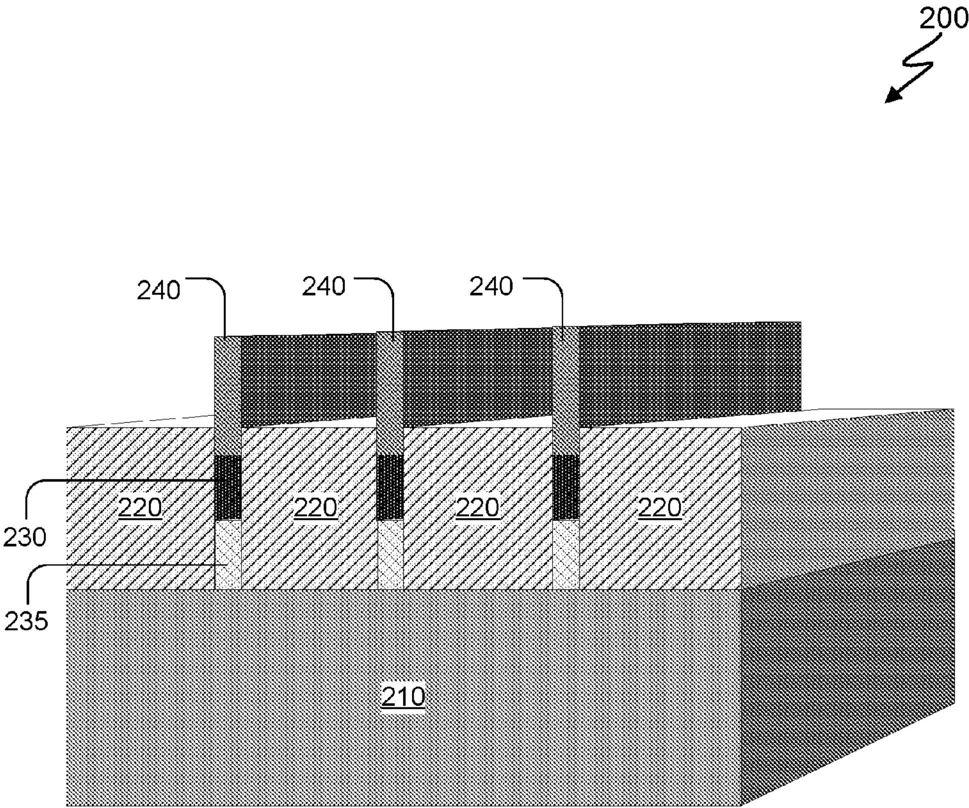


FIG. 4

NON-PLANAR SEMICONDUCTOR DEVICE WITH ASPECT RATIO TRAPPING

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to the field of semiconductor devices, and more particularly to non-planar semiconductor devices.

[0002] As electronic components become smaller, control over electron flow across an integrated circuit is diminished. The current complimentary metal-oxide semiconductor (CMOS) technology roadmap calls for the size of integrated circuit components to be cut in half every two years. To maintain this roadmap, non-planar architectures have been developed including the use of trigates and finFETs. While new CMOS architectures have proven to be efficient, challenges still exist in integrating 3-dimensional elements onto an integrated circuit chip.

SUMMARY

[0003] As disclosed herein, a semiconductor device with aspect ratio trapping includes, a bulk substrate, a plurality of isolation pillars formed on the bulk substrate, wherein one or more gaps are formed between the isolation pillars, an oxide layer formed by epitaxy on the bulk substrate, between the isolation pillars, wherein the oxide layer partially fills the gaps between the isolation pillars, one or more fins formed over the oxide layer between the isolation pillars, such that the one or more fins fill the gaps between the isolation pillars and wherein the oxide layer electrically isolates the one or more fins from the bulk substrate. The size of the gaps between the isolation pillars is selected to statistically eliminate defects caused by a lattice mismatch between the bulk substrate and the oxide layer. The semiconductor device may also contain an aspect-ratio trapping layer between the bulk substrate and oxide layer. A method of fabricating the same is also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. **1** is a flowchart depicting one embodiment of a non-planar semiconductor device fabrication method;

[0005] FIGS. **2***a-j* depict a cross-section of one embodiment of a non-planar semiconductor device throughout the fabrication method of FIG. **1**;

[0006] FIG. **3** is a prospective view depicting one embodiment of a non-planar semiconductor device made through the fabrication method of FIG. **1**; and

[0007] FIG. **4** is a prospective view depicting an alternative embodiment of a non-planar semiconductor device.

DETAILED DESCRIPTION

[0008] As integrated circuit (IC) components decrease in size, new technologies must be developed to ensure component requirements are maintained. One issue that has become prevalent in IC component design, is voltage leakage across transistors. To minimize the leakage, non-planar devices—such as trigates or finFETs—can be implemented. By minimizing the lattice mismatch of the materials in such devices, defects can be reduced; resulting in minimized voltage leakage.

[0009] FIG. **1** is a flowchart depicting one embodiment of a non-planar semiconductor device fabrication method **100**. As depicted, the non-planar semiconductor device fabrication method **100** includes etching (**110**) trenches into a bulk substrate, filling (**120**) the trenches with an insulator material creating isolation pillars, etching (**130**) the bulk substrate remaining between the isolation pillars, growing (**140**) an engineered lattice epitaxial oxide layer between the isolation pillars, etching (**150**) the oxide layer to a point below the isolation pillars, epitaxially growing (**160**) semiconductor fins on top of oxide layer, and etching (**170**) the isolation pillars, revealing the upper portion of the semiconductor fins. Creating a non-planar semiconductor using the non-planar semiconductor device fabrication method **100** decreases leakage across the circuit.

[0010] The depicted method may be used to form transistors onto a bulk substrate, for use in an integrated circuit. The non-planar semiconductor device fabrication method **100** begins by etching (**110**) trenches into a bulk substrate. The etching may be executed by several existing material etching processes, including reactive-ion etching.

[0011] Next, by filling (**120**) the trenches with an insulator material, multiple fins can be created on the same substrate. The insulator material in the trenches may include SiO_2. The SiO_2 may act as an isolation pillar between fins on the non-planar semiconductor.

[0012] Gaps between the isolation pillars may be formed by etching (**130**) the bulk substrate that remains between the isolation pillars. The base of the fin is formed by growing (**140**) an engineered lattice epitaxial oxide layer between the isolation pillars. The oxide layer may prevent voltage leakage through the bulk substrate. The height of the oxide layer is controlled by etching (**150**) the oxide layer to a point below the top of the isolation pillars.

[0013] The source/drain of the non-planar semiconductor is created by epitaxially growing (**160**) semiconductor fins on the oxide layer, between the isolation pillars. Finally, by etching (**170**) the isolation pillars, the upper portion of the fin is exposed. The method may continuing (**180**) with a standard CMOS process flow, including implementing a gate over the semiconductor fins.

[0014] The method as described above may be used in the fabrication of integrated circuit chips.

[0015] FIGS. **2***a-j* depict a cross-section of one embodiment of a non-planar semiconductor device throughout the non-planar semiconductor device fabrication method **100**. The depicted embodiment of the non-planar semiconductor device **200** include bulk substrate **210**, trenches **215**, isolation pillars **220**, lattice engineered epitaxial oxide **230**, fins **240**, gate **250**, and bottom aspect-ratio-trapped (ART) semiconductor **235**. The depicted sequence shows the fabrication of a non-planar semiconductor device using aspect ratio trapping.

[0016] In the depicted embodiment, as shown in FIG. **2***a*, the fabrication process begins with a bulk substrate **210**. In the depicted embodiment, the bulk substrate **210** is comprised of silicon; however, bulk substrate **210** can also be comprised of Ge, InP, or other similar materials. The thickness of bulk substrate **210** can vary from about 0.5-1.5 mm.

[0017] As shown in FIG. **2***b*, trenches **215** can be etched into the bulk substrate **210** using a reactive ion etching process. A hard mask is placed over portions of the bulk substrate **210**, which shield the covered portion from the etching process. The hard mask may be made of nitrides, oxides, oxinitrides, or a combination of these materials. The masks may be placed such that the trenches **215** are 5 nm to 40 nm in width. The depth of the trench **215** is adjusted by controlling the contact time of the etch materials on the bulk substrate **210**. In one embodiment, the depth of the trench **215** is between 50

nm and 200 nm. Due to natural variances in etching speed, the depth of each trench **215** may vary by several nanometers.

[0018] In one embodiment, as shown in FIG. **2***c*, the trenches **215** may be filled with an insulating material including SiO_2. The use of the insulation material is to create shallow trench isolation. The insulation material may prevent electrical current leakage between adjacent semiconductor device components; therefore, the insulating material will act as an isolation pillar **220** between fins **240** in the finFET device **200**. The insulating material may be deposited using plasma enhanced chemical vapor deposition, low-temperature chemical vapor deposition, high-temperature chemical vapor deposition, flowable oxide or other similar deposition methods.

[0019] The hard masks placed over bulk substrate **210** may be removed using processes known to those skilled in the art. The bulk substrate **210** may then be etched, using a reactive ion or wet etch process, to create gaps between each of the isolation pillars **220**. The etching process is selective, such that the isolation pillars **220** are not adversely affected by the process. The depth of the bulk substrate **210** etch may be adjusted by controlling the contact time of the etch materials on the bulk substrate **210**. Due to natural variances in etching speed, the height of gaps may vary by several nanometers. One embodiment of the selective etch is shown in FIG. **2***d*; while the height of each isolation pillar and each gap is uniform in the depicted figure, there is no requirement that the depth of the trenches **215** or gaps be precisely uniform.

[0020] The width and depth of the gaps are selected to statistically eliminate defects in the oxide layer **230**—or ART layer **235** as described below—caused by lattice mismatch between the bulk substrate **210** and oxide layer **230**. The statistical analysis determines the aspect ratio of the gaps that will result in the least amount of defects in the oxide layer **230**. Defects in the oxide layer **230** can allow voltage leakage into the bulk substrate **210**. By minimizing the number of defects in oxide layer **230**, the voltage leakage across the non-planar semiconductor device **200** can be minimized.

[0021] Next, as shown in FIG. **2***e*, an oxide layer **230** is formed above the bulk substrate **210** between the isolation pillars **220**. The oxide layer **230** may be a lattice engineered epitaxial oxide. The oxide layer **230** may been engineered such that minimal lattice mismatch occurs in the epitaxial growth due to the aspect ratio of the gap, decreasing the number of defects created during epitaxial growth. The greatest number of defects may occur where the bulk substrate **210** and oxide layer **230** meet; i.e. the defects that do occur during the epitaxial growth of the oxide layer **230** will be trapped towards the bottom, nearest the bulk substrate **210**. Trapping the defects at the bottom of the oxide layer **230** further decreases voltage leakage across non-planar semiconductor device **200**. The oxide layer **230** may be made of a material such as $La_{1-x}Y_xO_y$; for example, in one embodiment the chemical formula for the oxide layer **230** is $(La_{1-x}Y_x)_2O_3$. However, the oxide layer **230** may be made of several rare-earth oxides including Y_2O_3, Pr_2O_3, or CeO_2.

[0022] The oxide layer **230** may undergo chemical mechanical polishing (CMP), to smooth the upper portion of the layer and minimize height differentials between sections of the layer. The CMP process may be followed by etching the oxide layer **230**. In one embodiment, as shown in FIG. **2***f*, the oxide layer **230** is etched such that the height of the isolation pillars **220** is greater than the height of the oxide layer **230**. A wet or dry etching process may be used, and is time controlled.

[0023] In another embodiment, a semiconductor layer **235** is grown on the bulk substrate **210** prior to the growth of the oxide layer **230**. The semiconductor layer may be grown through epitaxy and may be made of SiGe, Ge, or any other III-V materials. A finFET device **200** containing semiconductor layer **235** is depicted in FIG. **4**. In an embodiment containing the semiconductor layer **235**, the semiconductor layer **235** would undergo a CMP process and an etching process. The process may then continue as described, with the growth of the oxide layer **230**.

[0024] Next, a fin **240** may be formed on the oxide layer **230**, as shown in FIG. **2***g*. The fins **240** may be made of Ge, strained-Si, or other III-V materials. The fins may be grown epitaxially from the oxide layer **230**, to form a fully crystalline structure.

[0025] The isolation pillars **220** may be etched, as shown in FIG. **2***h*, to reveal the upper portion of the fin **240**. The isolation pillar **220** can be below, in-line, or above the top of oxide layer **230**; however, for best results, the etch should not reach the defects in the oxide layer **230**.

[0026] Lastly, once the fins **240** are created, the process can continue with standard CMOS flow. A gate **250** can be created using either a gate first or gate last method. A front view of the finFET device **200** including a gate is depicted in FIG. **2***i*; whereas, a top view of the finFET device **200** with a gate is depicted in FIG. **2***j*.

[0027] FIG. **3** depicts a perspective view of the non-planar semiconductor device **200**. Additionally, a second embodiment of the non-planar semiconductor device **200**, containing the semiconductor layer **235**, is depicted in FIG. **4**. As discussed above, a gate may be added to the non-planar semiconductor device **200** after the non-planar semiconductor device fabrication method **100** is completed.

[0028] In certain embodiments, the method as described above is used in the fabrication of integrated circuit chips. The fabrication steps described above may be included on a semiconductor substrate consisting of many devices and one or more wiring levels to form an integrated circuit chip.

[0029] The resulting integrated circuit chip(s) can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip may be mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case, the chip may be then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[0030] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” and/or “comprising,” when used in this specification, specify the

presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0031] It should be noted that this description is not intended to limit the invention. On the contrary, the embodiments presented are intended to cover some of the alternatives, modifications, and equivalents, which are included in the spirit and scope of the invention as defined by the appended claims. Further, in the detailed description of the disclosed embodiments, numerous specific details are set forth in order to provide a comprehensive understanding of the claimed invention. However, one skilled in the art would understand that various embodiments may be practiced without such specific details.

[0032] Although the features and elements of the embodiments disclosed herein are described in particular combinations, each feature or element can be used alone without the other features and elements of the embodiments, or in various combinations with or without other features and elements. This written description uses examples of the subject matter disclosed to enable any person skilled in the art to practice the same, including making and using any devices or systems and performing any incorporated methods. The patentable scope of the subject matter is defined by the claims, and may include other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims.

What is claimed is:

1. A method for fabricating a non-planar semiconductor device with aspect ratio trapping, the method comprising:
- etching trenches into a bulk substrate;
- filling the trenches with a material forming a plurality of isolation pillars;
- etching the bulk substrate forming one or more gaps between the isolation pillars;
- epitaxially growing an oxide layer on the bulk substrate in the one or more gaps, wherein the oxide layer comprises a $La_{1-x}Y_xO_y$ material, wherein x is greater than 0, wherein the oxide layer comprises a gradient of defects, and wherein the gradient of defects is concentrated at an interface of the bulk substrate and the oxide layer;
- etching the oxide layer forming one or more cavities between the isolation pillars;
- epitaxially growing one or more semiconductor fins on the oxide layer in the one or more cavities; and
- etching the isolation pillars such that an upper portion of the one or more semiconductor fins is exposed.

2. The method claim **1**, wherein the bulk substrate comprises silicon.

3. The method of claim **1**, wherein the isolation pillars comprise SiO_2.

4. The method of claim **1**, wherein the fin is comprised of Ge or strained-Si.

5. The method of claim **1**, wherein the size of the gaps between the isolation pillars is selected to statistically eliminate defects caused by a lattice mismatch between the bulk substrate and the oxide layer.

6. A method for fabricating a non-planar semiconductor device with aspect ratio trapping, the method comprising:
- etching trenches into a bulk substrate;
- filling the trenches with a material forming a plurality of isolation pillars;
- etching the bulk substrate forming one or more gaps between the isolation pillars;
- epitaxially growing an aspect-ratio trapping (ART) layer on the bulk substrate in the one or more gaps;
- etching the ART layer forming one or more cavities between the isolation pillars;
- epitaxially growing an oxide layer on the ART layer in the one or more cavities between the isolation pillars, wherein the oxide layer comprises a $La_{1-x}Y_xO_y$ material, wherein x is greater than 0, wherein the oxide layer comprises a gradient of defects, and wherein the gradient of defects is concentrated at an interface of the bulk substrate and the oxide layer;
- etching the oxide layer forming one or more spaces between the isolation pillars;
- epitaxially growing one or more semiconductor fins on the oxide layer in the one or more spaces; and
- etching the isolation pillars such that an upper portion of the one or more semiconductor fins is exposed.

7. The method of claim **6**, wherein the bulk substrate comprises silicon.

8. The method of claim **6**, wherein the isolation pillars comprise SiO_2.

9. The method of claim **6**, wherein the ART layer is comprised of a III-V material.

10. The method of claim **6**, wherein the fin is comprised of Ge or strained-Si.

11. The method of claim **6**, wherein the size of the gaps between the isolation pillars is selected to statistically eliminate defects caused by a lattice mismatch between the bulk substrate and the ART layer.

* * * * *