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(54) **SEMICONDUCTOR MEMORY DEVICE**

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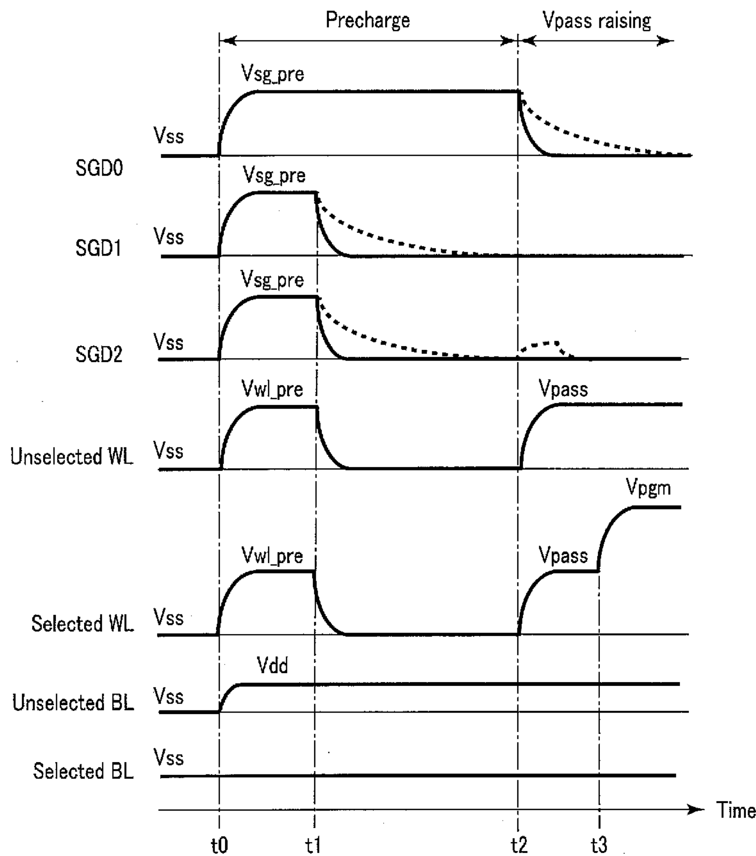
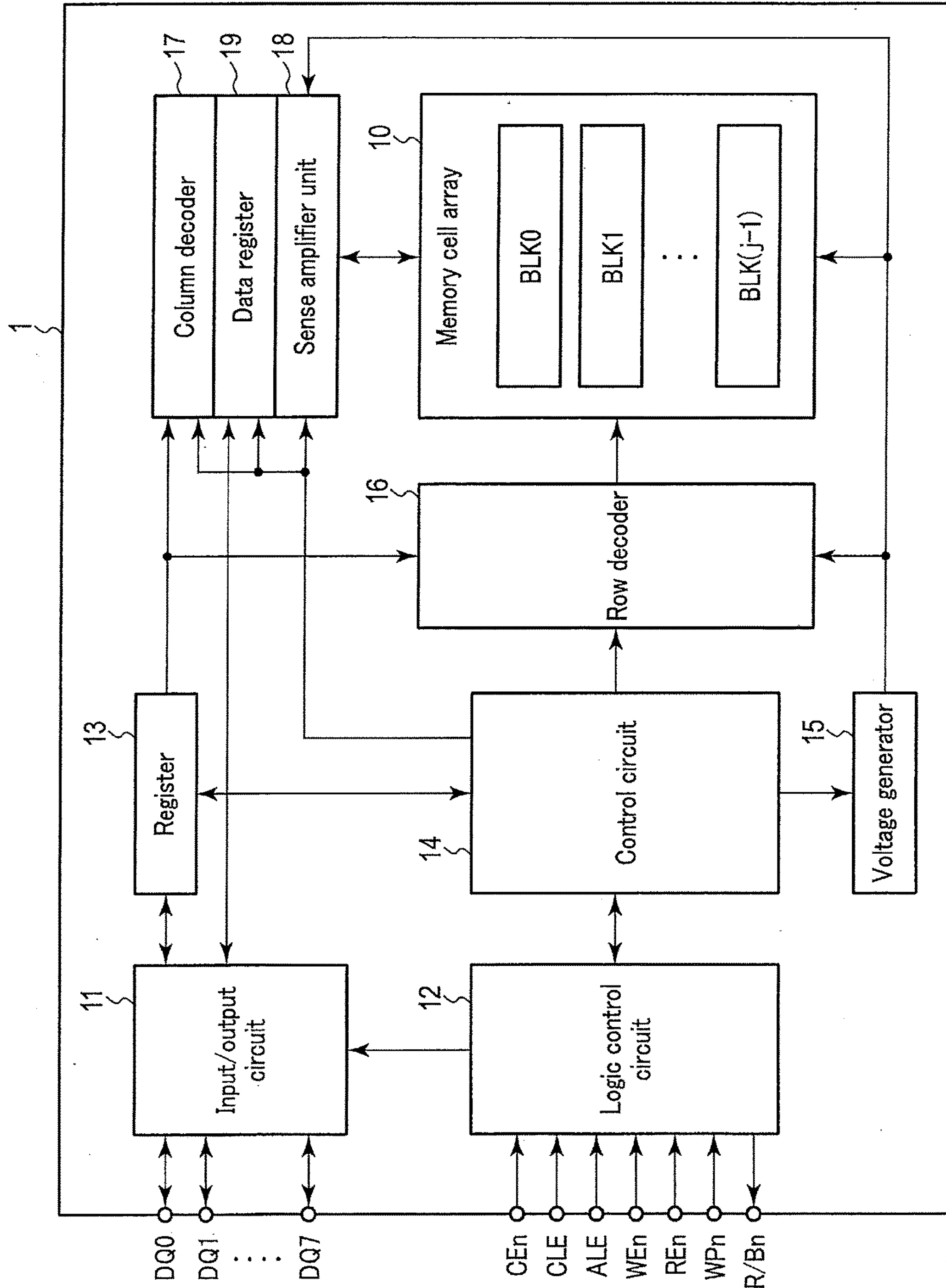
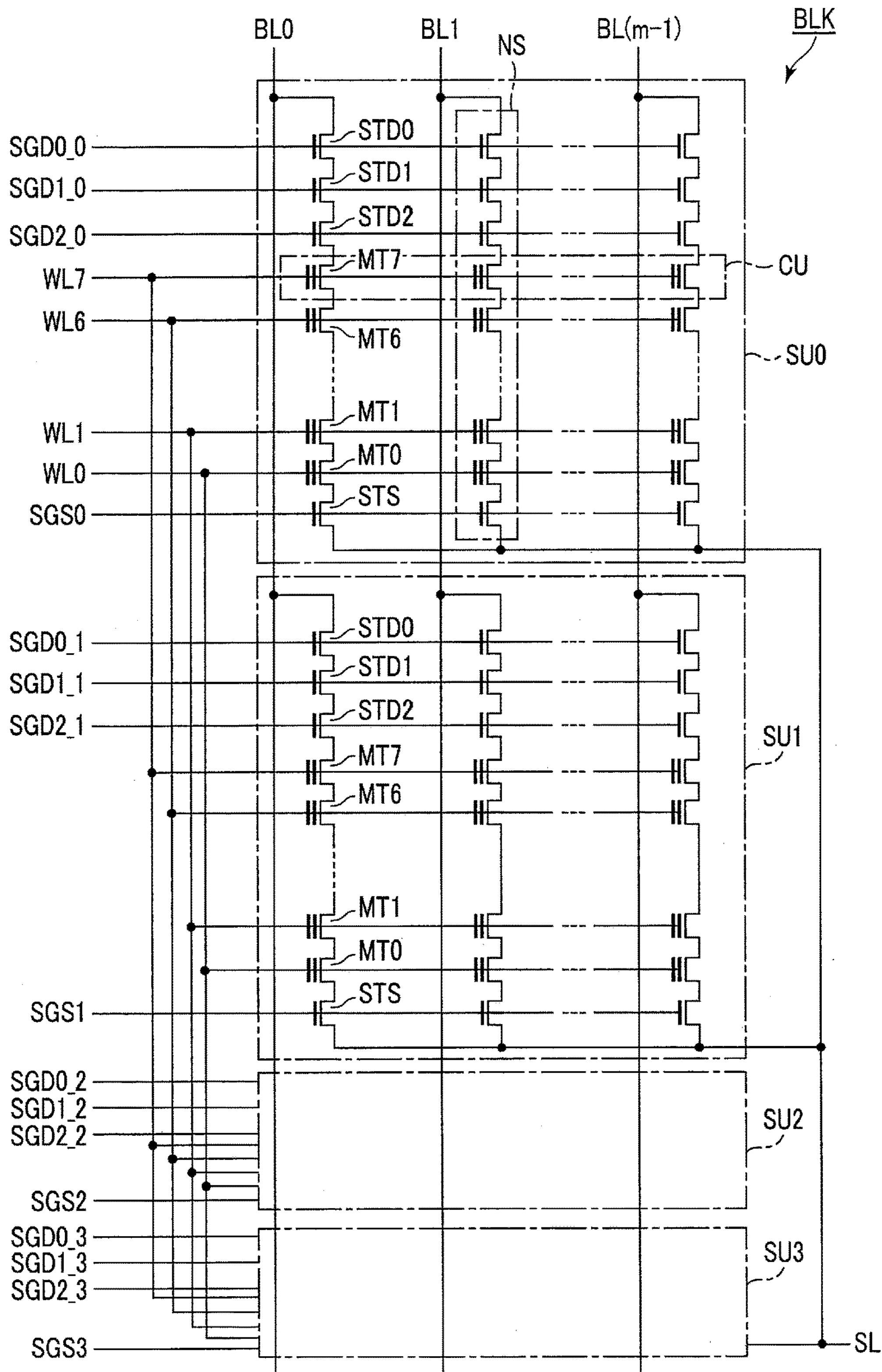
(57) **ABSTRACT**

According to one embodiment, a semiconductor memory device includes: a memory string including first and second select transistors and memory cell transistors; a bit line connected to the first select transistor; word lines which are connected to gates of the memory cell transistors, respectively; first and second select gate lines which are connected to gates of the first and second select transistors, respectively; a first contact plug connected to the first select gate line; a first wiring layer provided on the first contact plug; a second contact plug connected to the second select gate line; a second wiring layer provided on the second contact plug; and a row decoder connected to the first and second wiring layers. The row decoder applies different voltages to the first select gate line and the second select gate line.





F I G. 1



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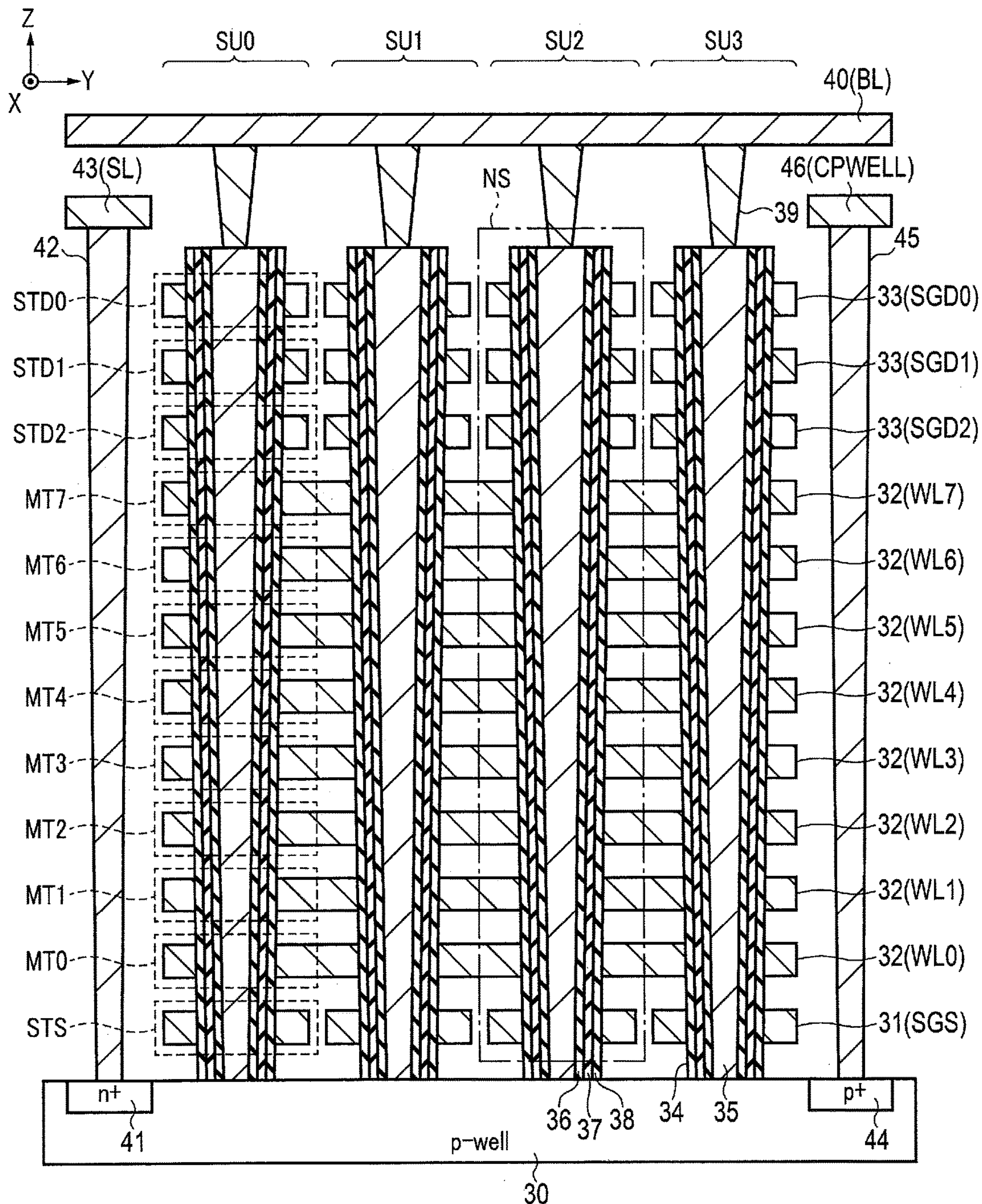

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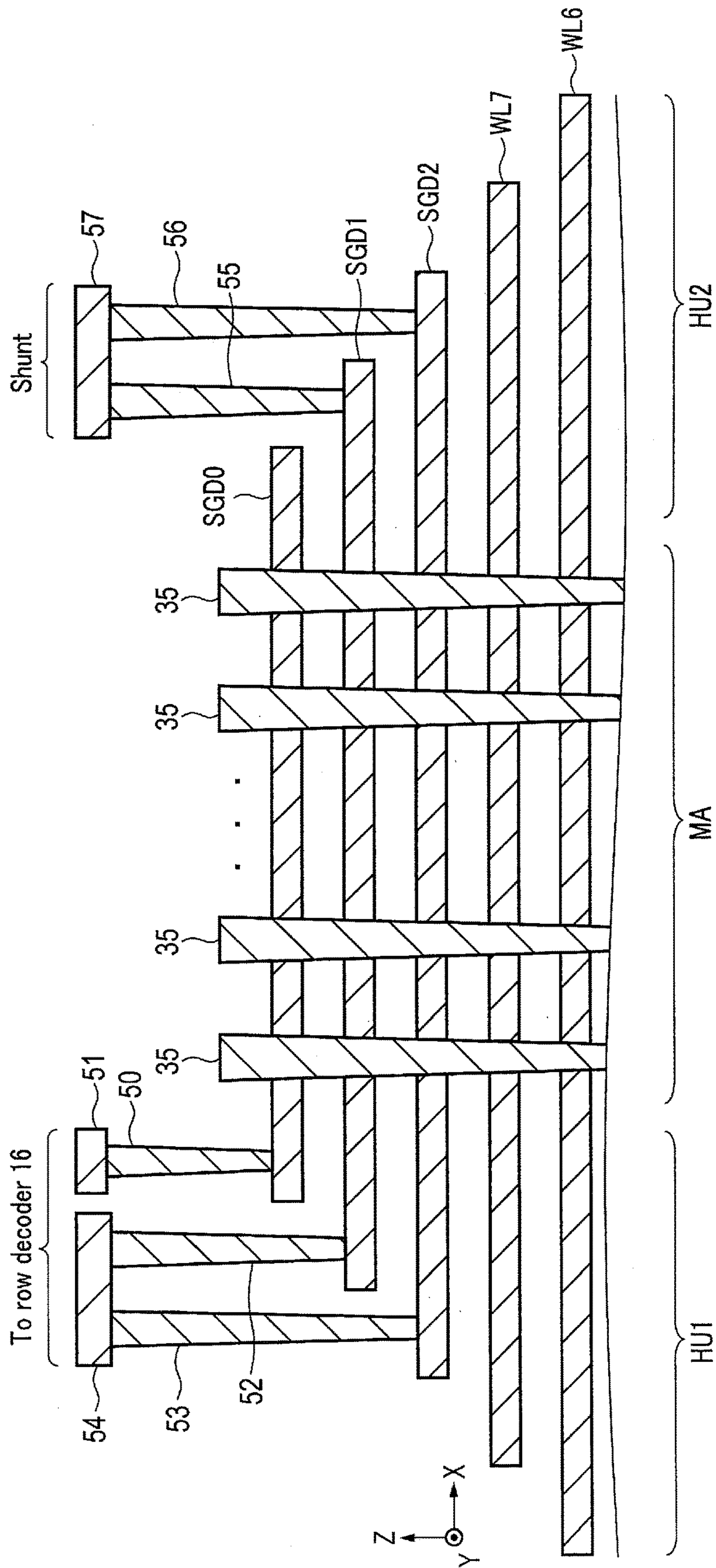

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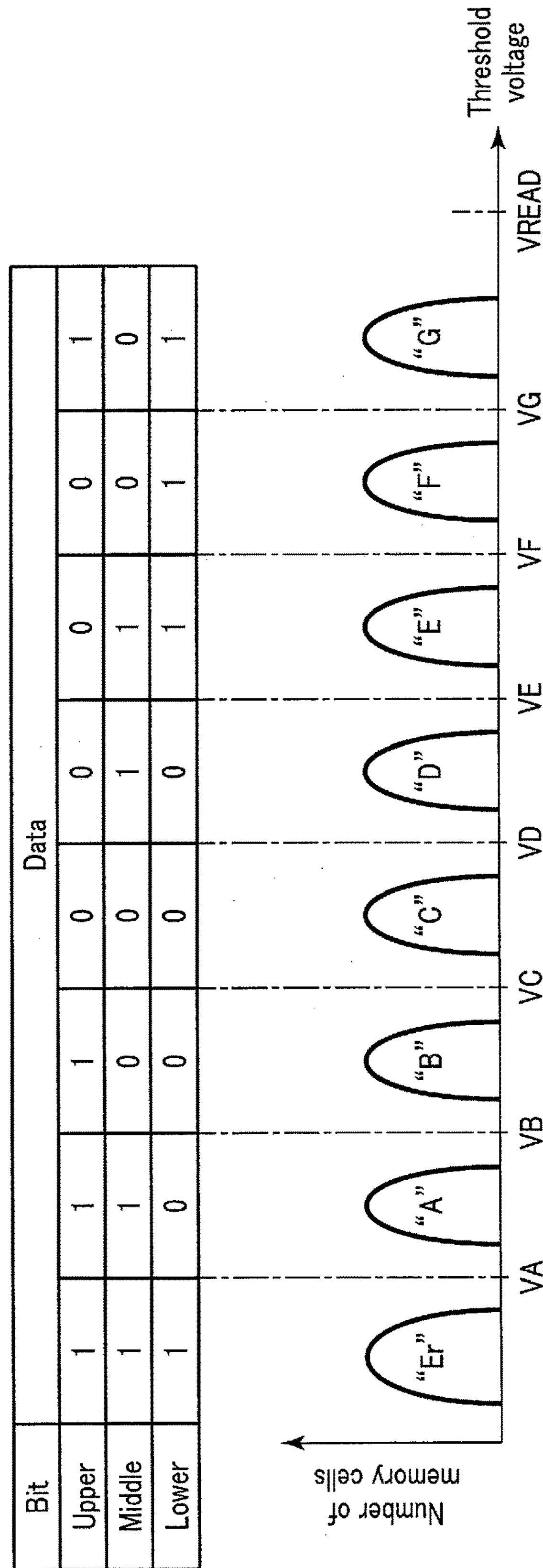
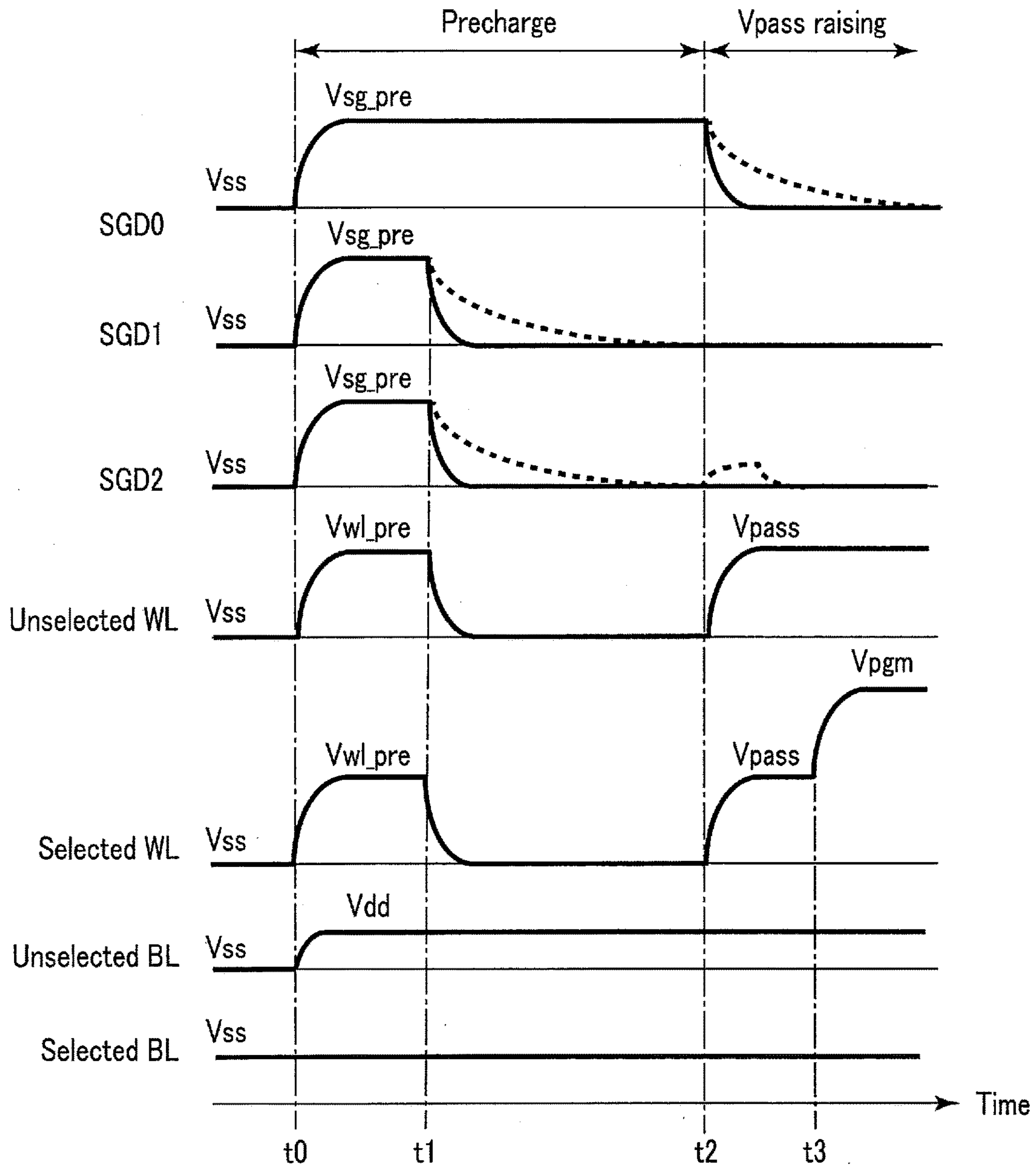


Bit	Data							
Upper	1	1	1	0	0	0	0	1
Middle	1	1	0	0	1	1	0	0
Lower	1	0	0	0	0	1	1	1

F I G. 5



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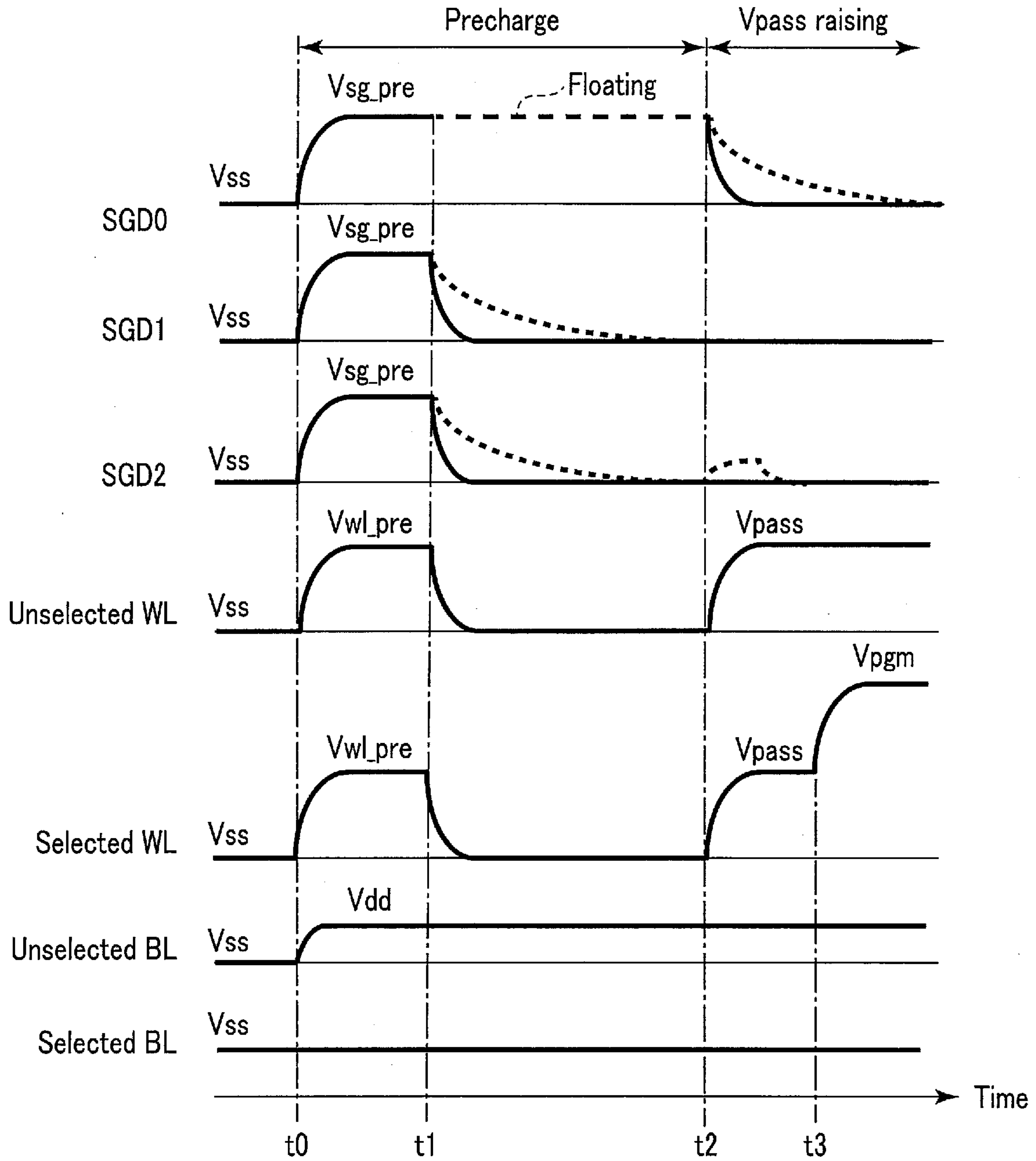

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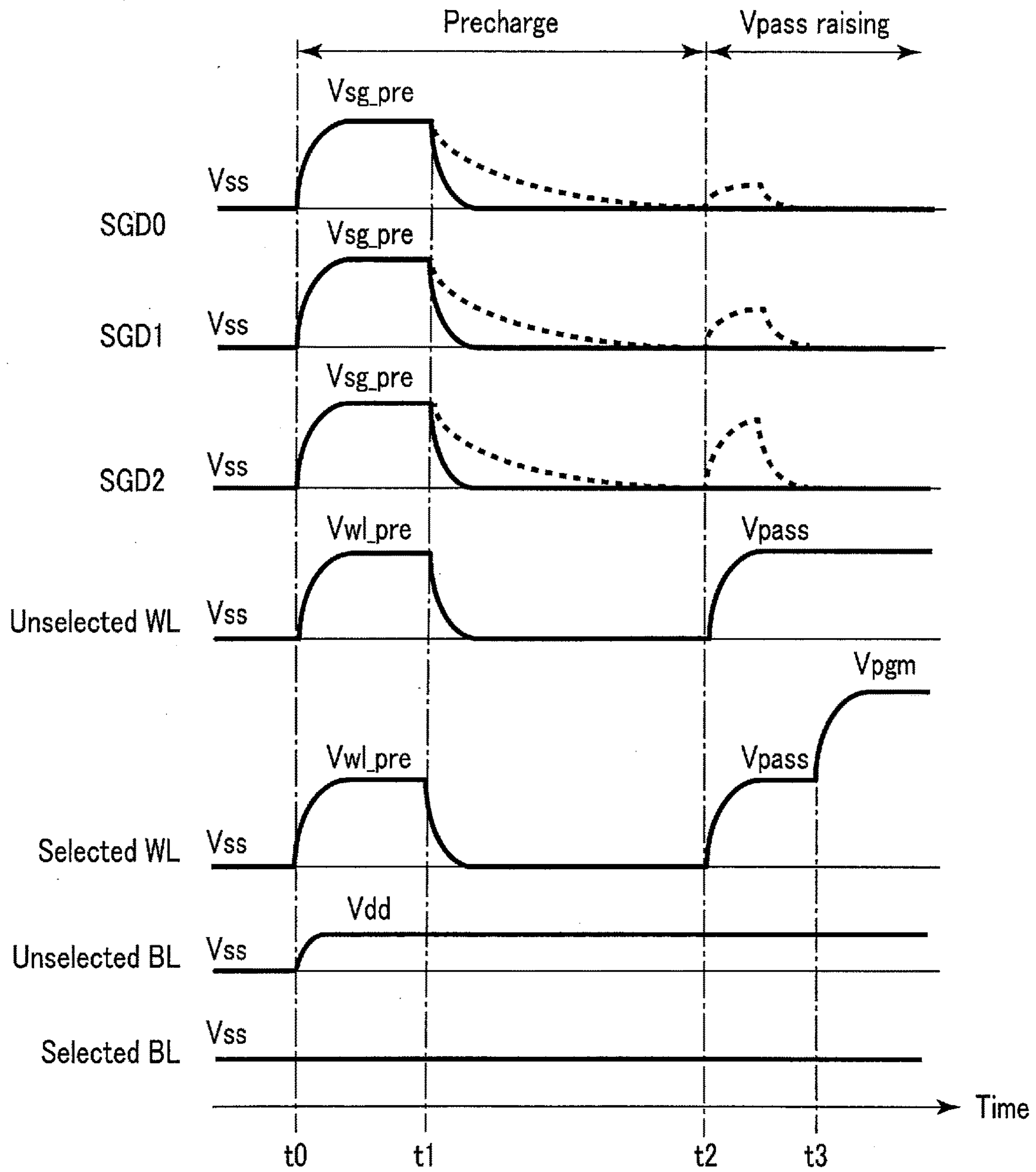

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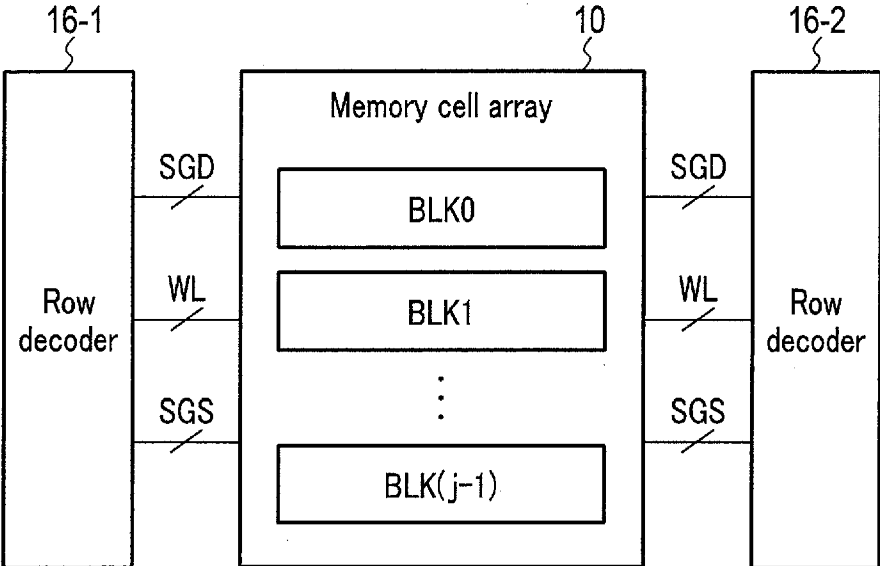


F I G. 9

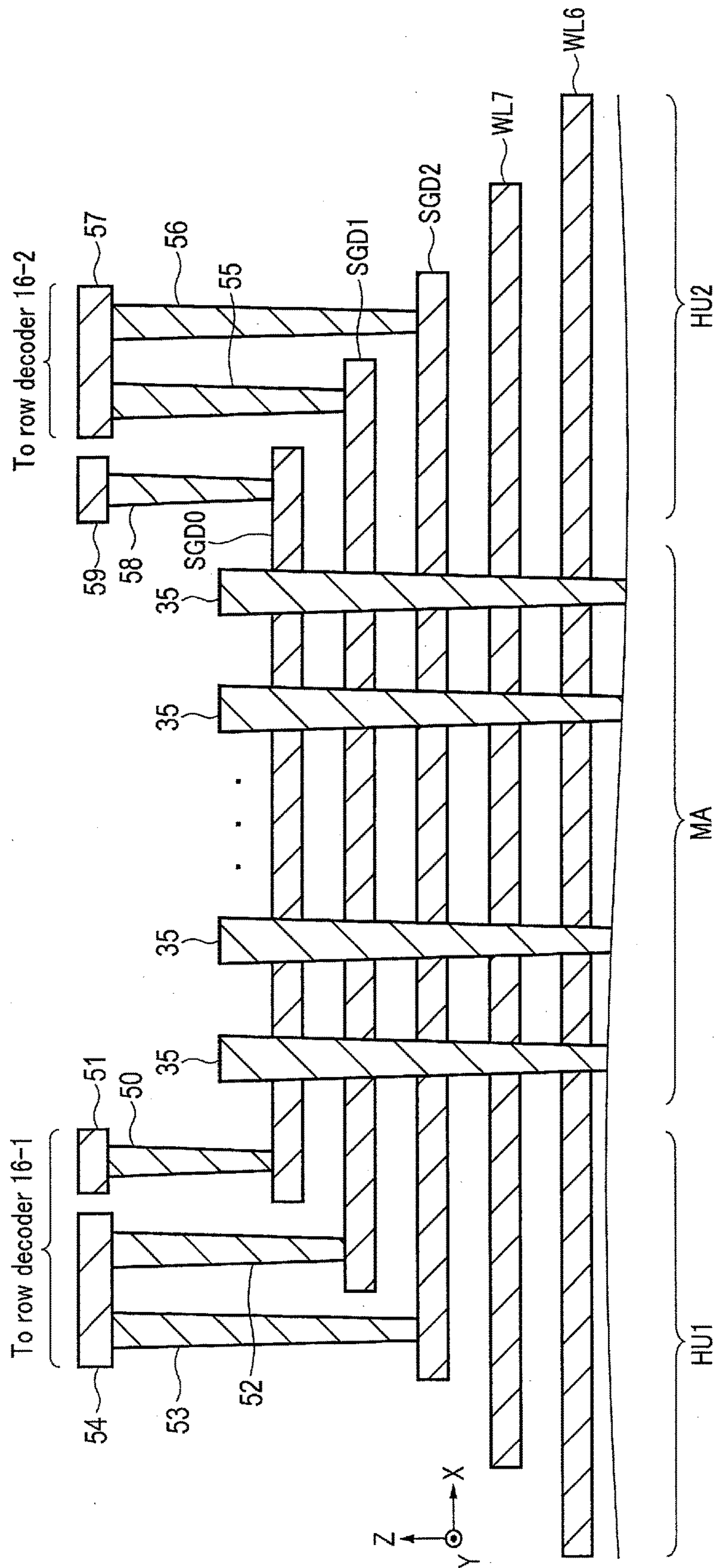
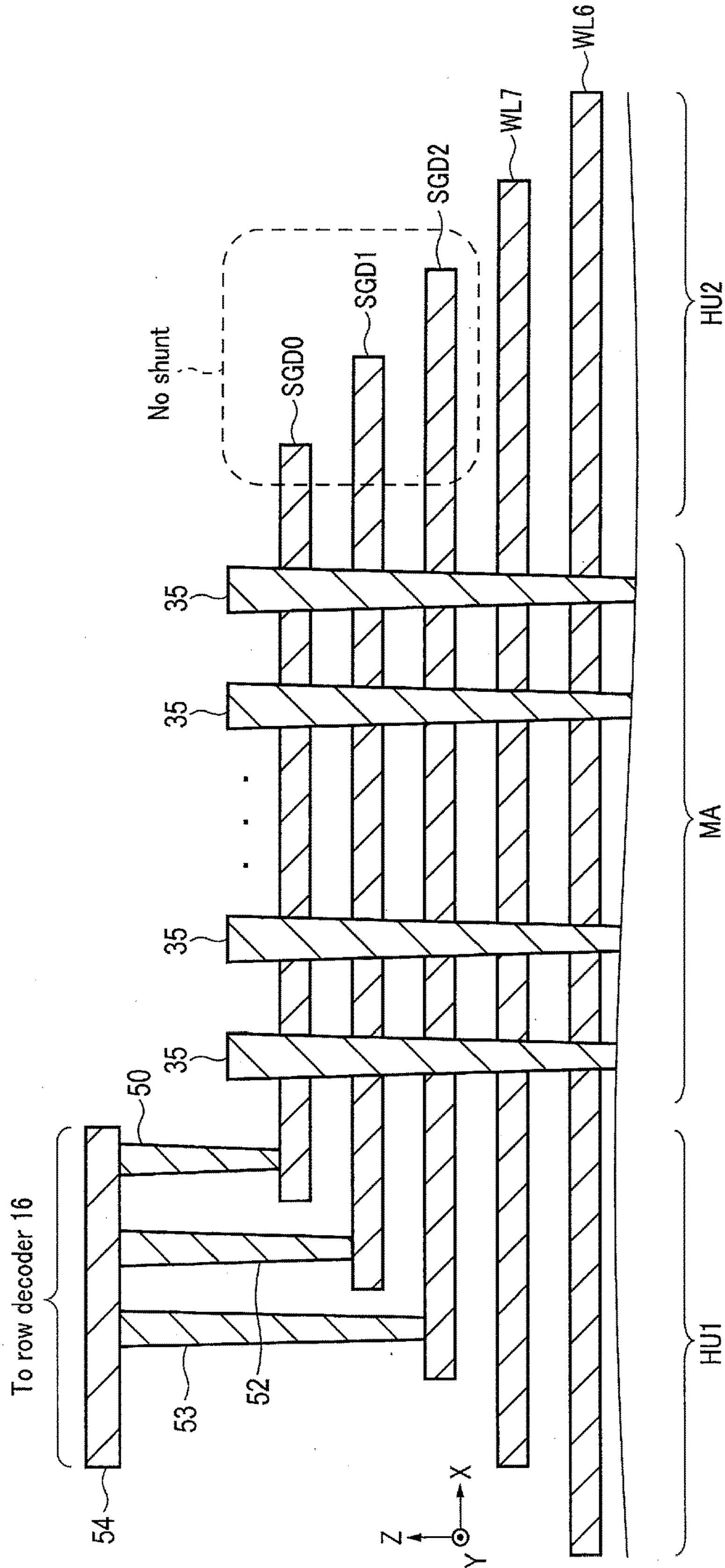


FIG. 10



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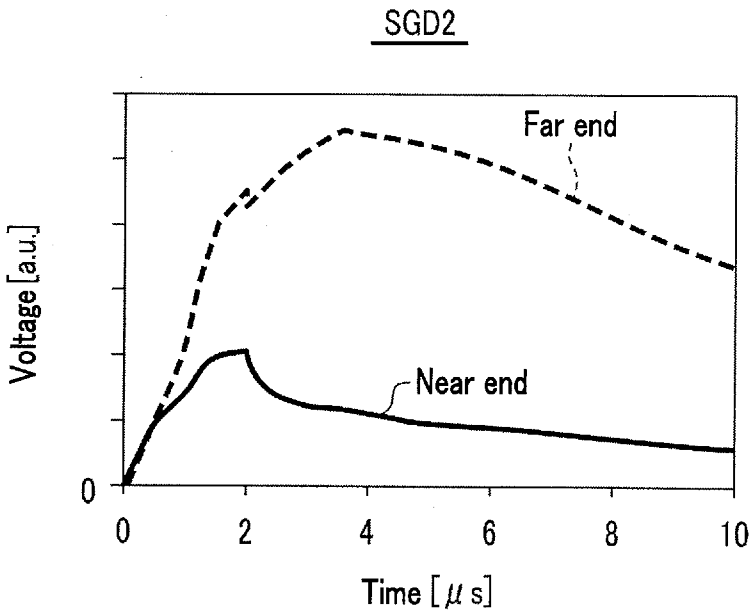

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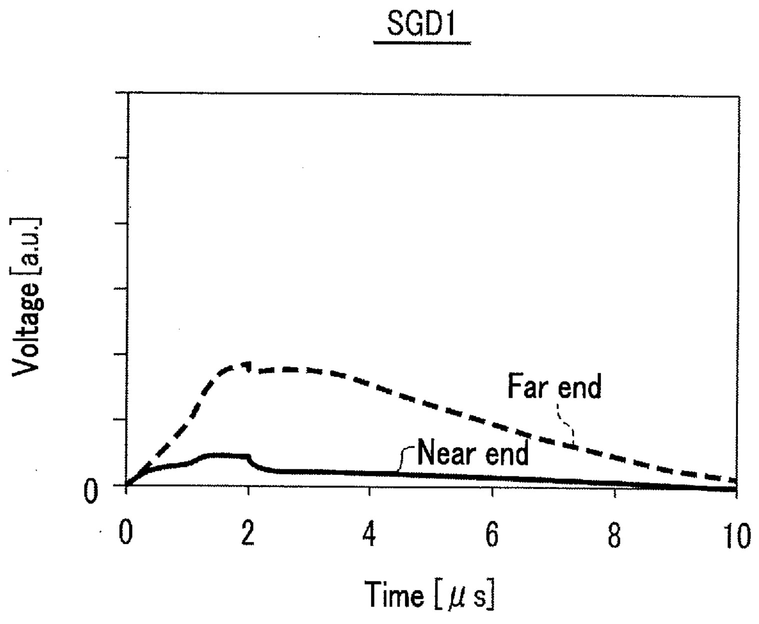


F I G. 13

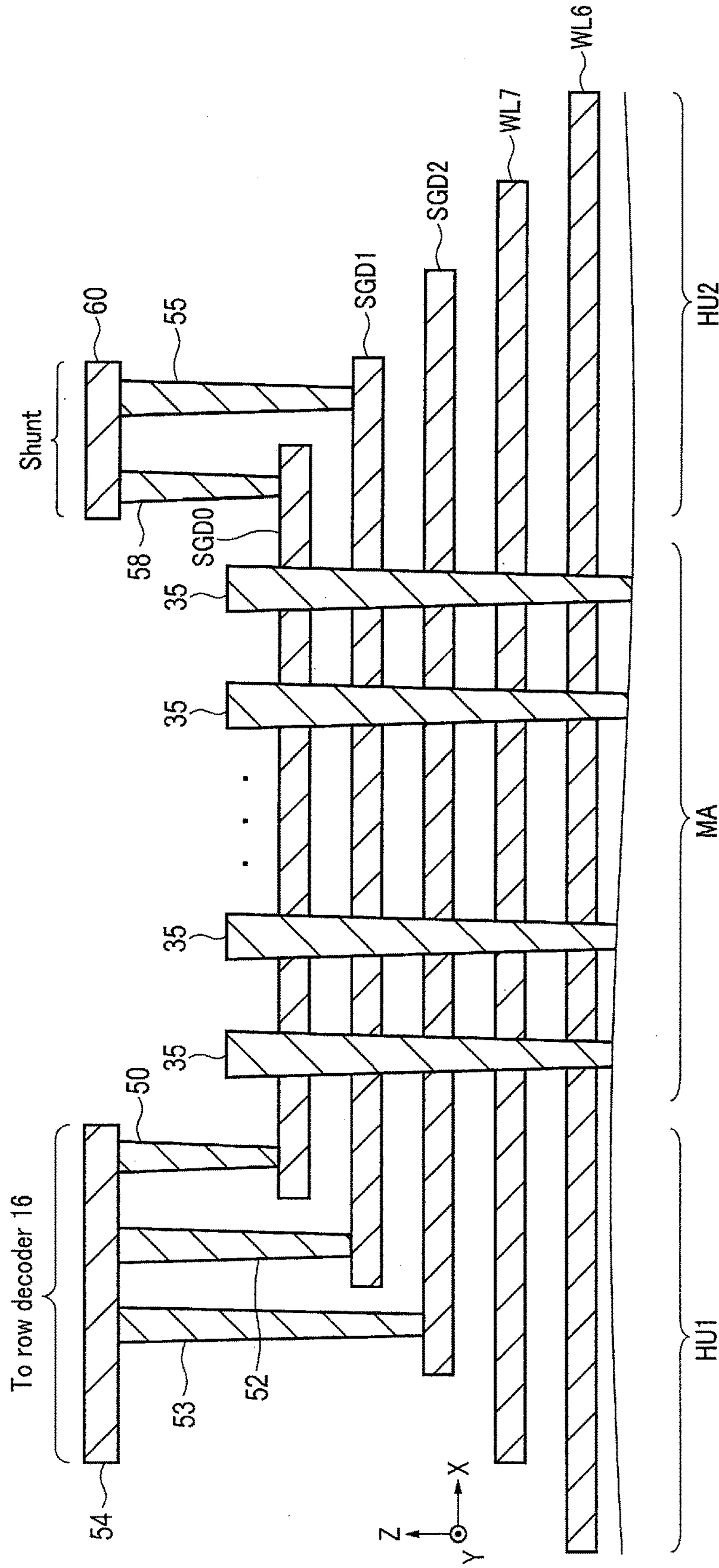
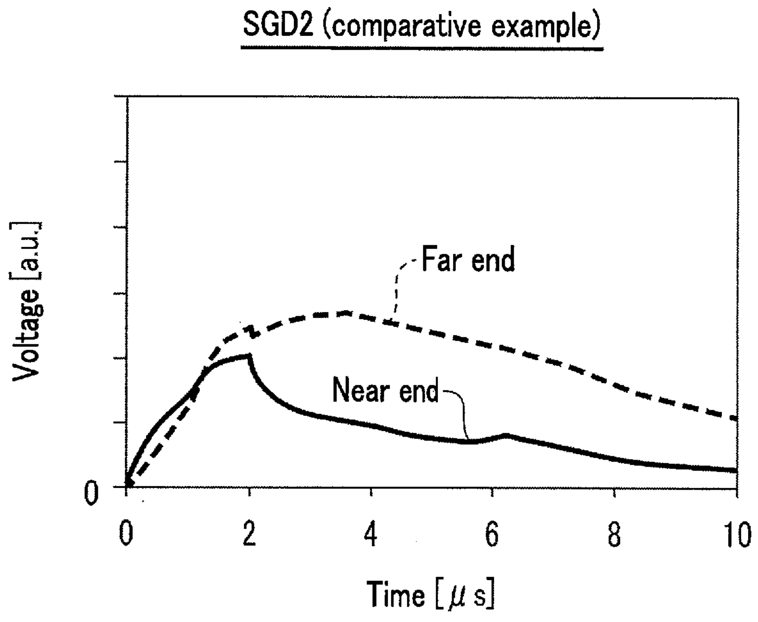


FIG. 14



F I G. 15

SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2017-178814, filed Sep. 19, 2017, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a semiconductor memory device.

BACKGROUND

[0003] A NAND flash memory is known as a kind of semiconductor memory device. A NAND flash memory comprising three-dimensionally stacked memory cell transistors is also known.

[0004] A NAND flash memory comprises NAND strings, and each of the NAND strings comprises memory cell transistors and a select transistor that are serially connected. A word line is connected to a gate of the memory cell transistor, and a select gate line is connected to a gate of the select transistor. When resistance of the select gate line is high, potential of the select gate line floats up due to capacitive coupling with a word line adjacent to the select gate line, during a potential variation of the adjacent word line. Thus, the select transistor can not be normally cut off, and a leak current is generated from a channel of a boosted NAND string. As a result, erroneous writing occurs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** is a block diagram of a NAND flash memory according to a first embodiment;

[0006] FIG. **2** is a circuit diagram of one block BLK included in a memory cell array;

[0007] FIG. **3** is a sectional view of a partial area of the block BLK;

[0008] FIG. **4** is a sectional view of hookup areas according to a first embodiment;

[0009] FIG. **5** is a schematic diagram showing one example of distributions of threshold voltages of a memory cell transistor;

[0010] FIG. **6** is a timing chart illustrating a write operation of the NAND flash memory according to the first embodiment;

[0011] FIG. **7** is a timing chart illustrating a write operation of the NAND flash memory according to a modification of the first embodiment;

[0012] FIG. **8** is a timing chart illustrating a write operation according to a comparative example;

[0013] FIG. **9** is a block diagram illustrating configurations of two row decoders according to a second embodiment;

[0014] FIG. **10** is a sectional view of the hookup areas according to the second embodiment;

[0015] FIG. **11** is a sectional view of the hookup areas according to a third embodiment;

[0016] FIG. **12** is a graph illustrating voltage waveforms of a select gate line SGD**2** according to the third embodiment;

[0017] FIG. **13** is a graph illustrating voltage waveforms of a select gate line SGD**1** according to the third embodiment;

[0018] FIG. **14** is a sectional view of the hookup areas according to a modification of the third embodiment; and

[0019] FIG. **15** is a graph illustrating voltage waveforms of the select gate line SGD**2** according to a comparative example.

DETAILED DESCRIPTION

[0020] In general, according to one embodiment, there is provided a semiconductor memory device comprising:

[0021] a memory string including first and second select transistors and memory cell transistors which are serially connected in this order;

[0022] a bit line connected to the first select transistor;

[0023] word lines which are connected to gates of the memory cell transistors, respectively, and which are stacked via insulating layers;

[0024] first and second select gate lines which are connected to gates of the first and second select transistors, respectively, and which are stacked on the word lines via insulating layers;

[0025] a first contact plug connected to the first select gate line;

[0026] a first wiring layer provided on the first contact plug;

[0027] a second contact plug connected to the second select gate line;

[0028] a second wiring layer provided on the second contact plug; and

[0029] a row decoder connected to the first and second wiring layers,

[0030] wherein the row decoder is configured to be capable of applying different voltages to the first select gate line and the second select gate line.

[0031] Embodiments will now be described with reference to the accompanying drawings. Several embodiments shown below merely exemplify devices and methods that embody the technical concepts of the present invention, and the shapes, structures, layouts, and the like of the components do not limit the technical concepts of the present invention. Each functional block can be obtained as one of hardware and software or a combination of these. It is not necessary for each functional block to be distinguished as in examples below. For example, some functions may be executed by a functional block different from a functional block shown by way of example. Moreover, a functional block shown by way of example may be divided into smaller functional sub-blocks. Note that in the following explanation, the same reference numerals denote elements having the same functions and configurations, and a duplicated explanation will be made only when necessary.

[1] First Embodiment

[1-1] Configuration of Semiconductor Memory Device

[0032] FIG. **1** is a block diagram of a semiconductor memory device **1** according to the first embodiment. The semiconductor memory device **1** comprises a NAND flash memory. The NAND flash memory **1** comprises a memory cell array **10**, an input/output circuit **11**, a logic control

circuit **12**, a register **13**, a control circuit **14**, a voltage generator **15**, a row decoder **16**, a column decoder **17**, a sense amplifier unit **18**, and a data register (data cache) **19**.

[0033] The memory cell array **10** comprises j blocks BLK**0** to BLK(j−1). j is an integer of **1** or more. Each of the blocks BLK comprises memory cell transistors. The memory cell transistor comprises an electrically rewritable memory cell. In the memory cell array **10**, bit lines, word lines, source lines, and others are provided to control a voltage to be applied to the memory cell transistor. A specific configuration of the block BLK will be described later.

[0034] The input/output circuit **11** and the logic control circuit **12** are connected to a host device (memory controller) via a NAND bus. The input/output circuit **11** transmits and receives signals DQ (e.g. DQ**0** to DQ**7**) to and from the memory controller via the NAND bus.

[0035] The logic control circuit **12** receives external control signals (e.g., a chip enable signal CEn, a command latch enable signal CLE, a address latch enable signal ALE, a write enable signal WEn, a read enable signal REn, and a write protect signal WPn) from the memory controller via the NAND bus. "n" added to a signal name indicates an active row. The logic control circuit **12** also transmits a ready/busy signal R/Bn to the memory controller via the NAND bus.

[0036] The signal CEn enables selection of the NAND flash memory **1**. The signal CLE enables a command transmitted as the signal DQ to be latched in a command register. The signal ALE enables an address transmitted as the signal DQ to be latched in an address register. The signal WEn enables writing. The signal REn enables reading. The signal WPn inhibits writing and erasing. The signal R/Bn indicates whether the NAND flash memory **1** is in a ready state (a state of being ready to accept an external instruction) or in a busy state (a state of being unready to accept an external instruction). The memory controller can know a state of the NAND flash memory **1** by receiving the signal R/Bn.

[0037] The register **13** comprises a command register, an address register, a status register, and others. The command register temporarily holds a command. The address register temporarily holds an address. The status register temporarily holds data necessary to operate the NAND flash memory **1**. The register **13** comprises, for example, an SRAM.

[0038] The control circuit **14** receives a command from the register **13**, and takes overall control of the NAND flash memory **1** in accordance with a sequence based on this command.

[0039] The voltage generator **15** receives a power supply voltage from the outside of the NAND flash memory **1**, and uses this power supply voltage to generate voltages necessary for a write operation, a read operation, and an erase operation. The voltage generator **15** supplies the generated voltages to the memory cell array **10**, the row decoder **16**, the sense amplifier unit **18**, and the like.

[0040] Receiving a row address from the register **13**, the row decoder **16** decodes this row address. On the basis of the decoded row address, the row decoder **16** performs an operation of selecting a word line. The row decoder **16** then transfers, to the selected block BLK, the voltages necessary for the write operation, the read operation, and the erase operation.

[0041] Receiving a column address from the register **13**, the column decoder **17** decodes this column address. On the basis of the decoded column address, the column decoder **17** selects one bit line.

[0042] The sense amplifier unit **18** detects and amplifies data read to the bit line from the memory cell transistor, during data reading. Further, the sense amplifier unit **18** transfers write data to the bit line, during data writing. The sense amplifier unit **18** comprises sense amplifiers connected to the bit lines, respectively.

[0043] The data register **19** temporarily holds data transferred from the sense amplifier unit **18**, and serially transfers the data to the input/output circuit **11**, during data reading. Further, the data register **19** temporarily holds data serially transferred from the input/output circuit **11**, and transfers the data to the sense amplifier unit **18**, during data writing. The data register **19** comprises an SRAM or the like.

[0044] [1-1-1] Configuration of Block BLK

[0045] FIG. **2** is a circuit diagram of one block BLK included in the memory cell array **10**. Each of the blocks BLK comprises string units SU. In FIG. **2**, four string units SU**0** to SU**3** are shown by way of example. Any number of string units SU to be included in one block BLK can be set.

[0046] Each of the string units SU comprises NAND strings (memory strings) NS. Any number of NAND strings NS to be included in one string unit SU can be set.

[0047] Each of the NAND strings NS comprises memory cell transistors MT, three drain-side select transistors STD, and a source-side select transistor ST. In the present embodiment, the select transistor STD included in one NAND string NS comprises three select transistors STD**0** to STD**2**. In the following explanation, the select transistors STD**0** to STD**2** are denoted as a select transistor STD unless otherwise needed to be distinguished in particular, and an explanation of the select transistor STD is common to the select transistors STD**0** to STD**2**.

[0048] Although one select transistor STS is only shown in FIG. **2** for simplicity, the NAND string NS may comprise more than one select transistor STS. In addition, although the NAND string NS comprises eight memory cell transistors MT (MT**0** to MT**7**) for simplicity in a configuration example shown in FIG. **2**, any number of memory cell transistors MT to be provided in the NAND string NS can be set.

[0049] The memory cell transistors MT are serially connected between a source of the select transistor STD**2** and a drain of the select transistor STS. The memory cell transistor MT comprises a control gate electrode and a charge storage layer, and stores data in a volatile manner. The memory cell transistor MT is capable of storing 1 bit or 2 or more bits of data.

[0050] In the string unit SU**0**, gates of the select transistors STD**0** are connected in common to a select gate line SGD**0_0**, gates of the select transistors STD**1** are connected in common to a select gate line SGD**1_0**, gates of the select transistors STD**2** are connected in common to a select gate line SGD**2_0**. Branch numbers attached to the select gate lines SGD**0** to SGD**2** signify numbers of the corresponding string units SU. Likewise, select gate lines SGD**0_1** to SGD**2_1**, SGD**0_2** to SGD**2_2**, and SGD**0_3** to SGD**2_3** are connected to the string units SU**1** to SU**3**, respectively.

[0051] Gates of select transistors STS included in the string unit SU**0** are connected in common to a select gate line SGS**0**, and likewise, select gate lines SGS**1** to SGS**3** are

connected to the string units SU**1** to SU**3**, respectively. Gates of select transistors STS in each block BLK may be connected to a common select gate line SGS.

[0052] Control gates of the memory cell transistors MT**0** to MT**7** in each block BLK are connected to word lines WL**0** to WL**7**, respectively.

[0053] Drains of the select transistors STD**0** of the NAND strings NS in the same column among the NAND strings NS arranged in each block BLK in matrix form are connected in common to one of bit lines BL**0** to BL(m−1). "m" is an integer of **1** or more. Further, each bit line BL connects, in common, one NAND string NS in each string unit SU between the blocks BLK. Sources of the select transistors STS included in each block BLK are connected in common to a source line SL. The source line SL connects, in common, the NAND strings NS between the blocks, for example.

[0054] Data in the memory cell transistors MT in each block BLK are, for example, collectively erased. Data are collectively read from and written into the memory cell transistors MT connected in common to one word line WL provided in one string unit SU. A set of the memory cell transistors MT having the word line WL in common in one string unit SU is referred to as a cell unit CU. A group of 1-bit data stored in each of the memory cell transistors MT included in the cell unit CU is referred to as a page. That is, a write operation and a read operation for the cell unit CU are performed with the page as a unit.

[0055] Note that the NAND string NS may comprise a dummy cell transistor. Specifically, for example, two dummy cell transistors DT**0** and DT**1** are serially connected between the select transistor STS and the memory cell transistor MT**0**. For example, two dummy cell transistors DT**2** and DT**3** are serially connected between the memory cell transistor MT**7** and the select transistor STD**2**. Dummy word lines DWL**0** to DWL**3** are connected to gates of the dummy cell transistors DT**0** to DT**3**, respectively. The structure of the dummy cell transistor is the same as that of the memory cell transistor. The dummy cell transistor is not intended to store data, and has a function of easing disturbance to which the memory cell transistor and the select transistor are subjected during a write operation or an erase operation.

[0056] [1-1-2] Stacked Structure of Block BLK

[0057] FIG. **3** is a sectional view of a partial area of the block BLK. An X-direction is a direction in which the select gate line extends, a Y-direction crossing the X-direction in a horizontal plane is a direction in which the bit line extends, a Z-direction is a stacking direction.

[0058] The NAND strings NS are provided on a p-type well area **30**. That is, a wiring layer **31** functioning as the select gate line SGS, an eight-layer wiring layer **32** functioning as the word lines WL**0** to WL**7**, and a three-layer wiring layer **33** functioning as the select gate lines SGD**0** to SGD**2** are sequentially stacked on the well area **30**. Unshown insulating layers are provided between the stacked wiring layers.

[0059] A memory hole **34** reaches the well area **30** through the wiring layers **31**, **32**, and **33**. A pillar-shaped semiconductor layer **35** is provided in the memory hole **34**. A gate insulating film **36**, a charge storage layer (insulating film) **37**, and a block insulating film **38** are provided in this order on a side surface of the semiconductor layer **35**. These constitute the memory cell transistor MT, and the select transistors STD and STS. The semiconductor layer **35** functions as a current path of the NAND string NS, and serves as an area where a channel of each transistor is formed. An upper end of the semiconductor layer **35** is connected, via a contact plug **39**, to a metal wiring layer **40** functioning as the bit line BL.

[0060] An n^+-type impurity diffusion layer **41** is provided in a surface area of the well area **30**. A contact plug **42** is provided on the diffusion layer **41**, and is connected to a metal wiring layer **43** functioning as the source line SL. Further, a p^+-type impurity diffusion layer **44** is provided in a surface area of the well area **30**. A contact plug **45** is provided on the diffusion layer **44**, and is connected to a metal wiring layer **46** functioning as a well wiring line CPWELL. The well wiring line CPWELL is a wiring line intended to apply a voltage to the semiconductor layer **35** via the well area **30**.

[0061] More than one configuration described above are arrayed in a depth direction (X-direction) of the sheet of FIG. **3**, and a group of NAND strings NS arranged in the depth direction constitutes the string unit SU.

[0062] [1-1-3] Configuration of Hookup Area

[0063] Next, a configuration of a hookup area is described. The hookup area is an area used to connect the select gate line SGS, the word lines WL, and the select gate lines SGD**0** to SGD**2** that are stacked to the decoder and the like.

[0064] FIG. **4** is a sectional view of hookup areas HU**1** and HU**2**. FIG. **4** is a sectional view taken along the X-direction. FIG. **4** mainly shows upper parts of the semiconductor layers (semiconductor pillars) **35**. In FIG. **4**, the gate insulating film **36**, the charge storage layer **37**, and the block insulating film **38** provided on the side surface of the semiconductor layer **35** are not shown.

[0065] The memory cell array **10** comprises a memory area MA where the semiconductor pillars **35** in which the memory cell transistors MT are formed are arranged, and the hookup areas HU**1** and HU**2** disposed on the X-direction side of the memory area MA. For example, the row decoder **16** is disposed on the hookup area HU**1** side.

[0066] In the hookup area HU**1**, the select gate line SGS, the word lines WL, and the select gate lines SGD**0** to SGD**2** that are stacked are formed in a stair-like manner. Likewise, in the hookup area HU**2**, the select gate line SGS, the word lines WL, and the select gate lines SGD**0** to SGD**2** that are stacked are formed in a stair-like manner.

[0067] In the hookup area HU**1**, a contact plug **50** is provided on the select gate line SGD**0**, and a wiring layer **51** is provided on the contact plug **50**. In the hookup area HU**1**, a contact plug **52** is provided on the select gate line SGD**1**, and a wiring layer **54** is provided on the contact plug **52**. In the hookup area HU**1**, a contact plug **53** is provided on the select gate line SGD**2**, and the wiring layer **54** is provided on the contact plug **53**. That is, the select gate line SGD**1** and the select gate line SGD**2** are electrically connected to each other. The wiring layer **51** and the wiring layer **54** are connected to the row decoder **16**.

[0068] In the hookup area HU**2**, a contact plug **55** is provided on the select gate line SGD**1**, and a shunt wiring layer **57** is provided on the contact plug **55**. In the hookup area HU**2**, a contact plug **56** is provided on the select gate line SGD**2**, and the shunt wiring layer **57** is provided on the contact plug **56**. That is, in the hookup area HU**2** on a side far from the row decoder **16**, the select gate line SGD**1** and the select gate line SGD**2** are electrically connected to each other by the shunt wiring layer **57**.

[0069] Thus, in the present embodiment, the select gate line SGD**0** disposed on the bit line BL side is electrically isolated from the select gate lines SGD**1** and SGD**2**. That is, the select gate line SGD**0** and the select gate line SGD**1** (or SGD**2**) permit independent voltage control.

[0070] [1-1-4] Threshold Distributions of Memory Cell Transistor

[0071] Next, distributions of threshold voltages that can be taken by the memory cell transistor MT are described. FIG. **5** is a schematic diagram showing one example of distributions of threshold voltages of the memory cell transistor MT. The memory cell transistor MT is capable of storing 2 or more bits of data. In the present embodiment, the case where the memory cell transistor MT stores 3 bits of data, that is, a triple level cell (TLC) scheme is described by way of example.

[0072] The 3-bit data are defined by an upper bit, a middle bit, and a lower bit. When the memory cell transistor MT stores 3 bits, the memory cell transistor MT has one of eight threshold voltages. The eight threshold voltages are referred to as "Er", "A", "B", "C", "D", "E", "F", and "G" levels in ascending order. The memory cell transistors MT belonging to each of the "Er", "A", "B", "C", "D", "E", "F", and "G" levels form distributions.

[0073] For example, "111" data, "110" data, "100" data, "000" data, "010" data, "011" data, "001" data, and "101" data are allocated to the threshold distributions of the "Er", "A", "B", "C", "D", "E", "F", and "G" levels, respectively. Any allocation of the data to the threshold distributions can be set.

[0074] To identify the data stored in the memory cell transistor MT to be read from, the level to which the threshold voltage of this memory cell transistor MT belongs is determined. Read voltages VA, VB, VC, VD, VE, VF, and VG are used to determine the level.

[0075] The "Er" level corresponds to, for example, an erase state of data. In addition, the threshold voltage of the memory cell transistor MT included in the "Er" level is lower than the voltage VA, and has, for example, a negative value.

[0076] The "A" level to the "G" level correspond to a state where the charge storage layer is charged and data are thus written in the memory cell transistor MT, and the threshold voltage of the memory cell transistor MT included in each distribution has, for example, a positive value. The threshold voltage included in the "A" level is higher than the read voltage VA, and less than or equal to the read voltage VB. The threshold voltage included in the "B" level is higher than the read voltage VB, and less than or equal to the read voltage VC. The threshold voltage included in the "C" level is higher than the read voltage VC, and less than or equal to the read voltage VD. The threshold voltage included in the "D" level is higher than the read voltage VD, and less than or equal to the read voltage VE. The threshold voltage included in the "E" level is higher than the read voltage VE, and less than or equal to the read voltage VF. The threshold voltage included in the "F" level is higher than the read voltage VF, and less than or equal to the read voltage VG. The threshold voltage included in the "G" level is higher than the read voltage VG, and less than or equal to a voltage VREAD. The voltage VREAD is a voltage which is applied to the word line WL connected to the memory cell transistor MT of the cell unit CU untargeted for reading, and higher than the threshold voltage of the memory cell transistor MT at any level. That is, the memory cell transistor MT in which the voltage VREAD is applied to a control gate comes into an on-state regardless of data to be held therein.

[0077] As described above, each memory cell transistor MT can take eight kinds of states by having one of the distributions of the eight threshold voltages. Moreover, data are written and read on a page unit in one cell unit CU. When the memory cell transistor MT stores 3-bit data, the lower bit, the middle bit, and the upper bit are allocated to three pages in one cell unit CU, respectively. Pages collectively written or read for the lower bit, the middle bit, and the upper bit are referred to as a lower page, a middle page, and an upper page, respectively.

[1-2] Operation

[0078] Next, an operation of the NAND flash memory **1** having the above configuration is described. FIG. **6** is a timing chart illustrating a write operation of the NAND flash memory **1** according to the first embodiment. FIG. **6** shows voltage waveforms regarding the unselected select gate lines SGD.

[0079] The write operation includes a precharge operation and a Vpass raising operation. The precharge operation is an operation in which a channel is precharged to a predetermined voltage. Specifically, in the precharge operation, a write inhibit voltage is transferred to an unselected NAND string. The Vpass raising operation is an operation in which all the word lines WL are raised to a voltage Vpass before an operation of applying a program voltage Vpgm to a selected word line. The voltage Vpass is a voltage which brings the memory cell transistor MT into an on-state regardless of the threshold voltage of the memory cell transistor MT. The voltage Vpgm and the voltage Vpass are in a relation of Vpgm>Vpass.

[0080] At a time t**0**, the row decoder **16** applies a voltage Vsg_pre to the select gate lines SGD**0** to SGD**2**. The voltage Vsg_pre is a voltage which brings the select transistors STD**0** to STD**2** into an on-state. Accordingly, the select transistors STD**0** to STD**2** turn on. At the time t**0**, the row decoder **16** applies a voltage Vwl_pre to all the word lines WL. The voltage Vwl_pre is a voltage which brings the memory cell transistor MT into an on-state regardless of the threshold voltage of the memory cell transistor MT. Alternatively, the voltage Vwl_pre may be a voltage which brings, into an on-state, the drain-side memory cell transistor MT in which no data are written. The voltage Vwl_pre has a relation of Vwl_preVpass. Accordingly, all the memory cell transistors MT in the block BLK turn on.

[0081] At the time t**0**, the sense amplifier unit **18** applies a ground voltage Vss (0 V) to the selected bit line BL, and applies a voltage for write inhibition (e.g. a power supply voltage Vdd) to the unselected bit line BL. A select transistor SGS is in an off-state. As a result, the power supply voltage Vdd is transferred to the channel in the NAND string connected to the unselected bit line BL. On the other hand, the ground voltage Vss is transferred to the channel in the NAND string connected to the selected bit line BL.

[0082] At a time t**1**, the row decoder **16** applies the voltage Vsg_pre to the select gate line SGD**0**, and applies the ground voltage Vss to the select gate lines SGD**1** and SGD**2**. Accordingly, the select transistor STD**0** maintains the on-state, and the select transistors STD**1** and STD**2** turn off. At the time t**1**, the row decoder **16** applies the ground voltage Vss to all the word lines WL.

[0083] Note that broken lines in FIG. **6** indicate a voltage at an end of the select gate line SGD on a side far from the row decoder **16**. At the end of the select gate line SGD on the side far from the row decoder **16**, dropping of the voltage of the select gate line SGD is slower due to resistance of the select gate line SGD and the like.

[0084] At a time t**2**, the row decoder **16** applies the ground voltage Vss to the select gate line SGD**0**. At the time t**2**, the row decoder **16** applies the voltage Vpass to all the word lines WL. Accordingly, all the memory cell transistors MT in the block BLK turn on. In an unselected NAND string, the voltage of the channel is boosted.

[0085] In the present embodiment, the voltage of the select gate line SGD is dropped at a raising timing of the voltage of the word line WL. This makes it possible to inhibit the voltages of the select gate lines SGD**1** and SGD**2** from rising due to capacitive coupling between the select gate line SGD**2** and the word line WL adjacent to the select gate line SGD**2**. That is, cut-off characteristics of the select transistors STD**0** to STD**2** can be improved. Therefore, in an unselected NAND string, generation of a leak current from a boosted channel can be inhibited.

[0086] Thereafter, the program voltage Vpgm is applied to the selected word line WL, and the voltage Vpass is kept applied to the unselected word line WL. Note that a voltage Vsg is applied to the selected select gate lines SGD (SGD**0** to SGD**2**). The voltage Vsg is a voltage lower than the voltage Vsg_pre, and is a voltage that turns on the select transistor STD to which the ground voltage Vss is applied but cuts off the select transistor STD to which the power supply voltage Vdd is applied. Accordingly, in a selected NAND string, a potential difference between the selected word line WL and the channel increases, and an electron is injected to the charge storage layer of the selected memory cell transistor MT. On the other hand, in an unselected NAND string, a potential difference between the selected word line WL and the channel does not increase, and the threshold voltage of the memory cell transistor MT is maintained.

[1-3] Modification

[0087] Next, a write operation according to a modification of the first embodiment is described. FIG. **7** is a timing chart illustrating a write operation of the NAND flash memory **1** according to the modification of the first embodiment.

[0088] At a time t**1**, the row decoder **16** brings the select gate line SGD**0** into a floating state. Accordingly, the select gate line SGD**0** is kept substantially at the voltage Vsg_pre.

[0089] At a time t**2**, the row decoder **16** applies the ground voltage Vss to the select gate line SGD**0**. This makes it possible to inhibit the voltages of the select gate lines SGD**1** and SGD**2** from rising.

[0090] In the modification, there is no need to prepare an additional power supply during a period t**1** to t**2**. This makes it possible to simplify a power-supply-related circuit configuration, and makes voltage control of the select gate line SGD**0** easier.

[1-4] Comparative Example

[0091] Next, a comparative example is described. FIG. **8** is a timing chart illustrating a write operation according to the comparative example. In the comparative example, voltage control of the select gate lines SGD**0** to SGD**2** is the same. For example, the select gate lines SGD**0** to SGD**2** are electrically connected to one another.

[0092] At a time t**1**, the ground voltage Vss is applied to the select gate lines SGD**0** to SGD**2**.

[0093] At a time t**2**, the voltage Vpass is applied to all the word lines WL. At this point, the voltage of the select gate line SGD**2** rises (floats up) due to capacitive coupling between the select gate line SGD**2** and the word line WL adjacent to the select gate line SGD**2**. The voltage of the select gate line SGD**1** also rises due to capacitive coupling between the select gate line SGD**2** and the select gate line SGD**1**. Likewise, the voltage of the select gate line SGD**0** also rises due to capacitive coupling between the select gate line SGD**1** and the select gate line SGD**0**. In particular, as indicated by broken lines in FIG. **8**, the voltage of the select gate line SGD**2** considerably rises at the end of the select gate line SGD**2** on the side far from the row decoder **16**.

[0094] In this case, cutting-off of the select transistors STD**1** and STD**2** weakens, and leak currents are generated from the select transistors STD**1** and STD**2**. Thus, in an unselected NAND string, a boosted channel voltage decreases, and erroneous writing can occur.

[1-5] Advantageous Effects of First Embodiment

[0095] As described above in detail, in the first embodiment, for example, three select transistors STD**0** to STD**2** are serially connected between the bit line BL and the word line WL. The select gate lines SGD**0** to SGD**2** are connected to the gates of the select transistors STD**0** to STD**2**, respectively. The select gate line SGD**0** and the select gate line SGD**1** (and SGD**2**) permit independent voltage control, and the row decoder **16** can apply different voltages to the select gate line SGD**0** and the select gate line SGD**1** (and SGD**2**). In addition, the row decoder **16** drops the voltage of the select gate line SGD**0** at a raising timing of the voltages of the word lines WL.

[0096] Therefore, according to the first embodiment, it is possible to inhibit the voltages of the select gate lines SGD**1** and SGD**2** from rising (floating up) due to capacitive coupling with the adjacent word line WL. Thus, the cut-off characteristics of the select transistors STD**0** to STD**2** can be improved, so that generation of a leak current from a boosted channel in an unselected NAND string can be inhibited. This makes it possible to inhibit erroneous writing in an unselected NAND string, and thus improve reliability of the NAND flash memory **1**.

[2] Second Embodiment

[0097] FIG. **9** is a block diagram illustrating configurations of two row decoders **16-1** and **16-2** according to a second embodiment. Configurations other than the row decoders **16-1** and **16-2** are the same as those in the first embodiment.

[0098] The NAND flash memory **1** comprises the two row decoders **16-1** and **16-2**. The row decoders **16-1** and **16-2** are disposed on both sides of the memory cell array **10**. The row decoders **16-1** and **16-2** are connected to the select gate lines SGD, the word lines WL, and the select gate lines SGS, respectively. The row decoders **16-1** and **16-2** execute the same voltage control.

[0099] FIG. **10** is a sectional view of hookup areas HU**1** and HU**2**. The row decoder **16-1** is disposed on the hookup area HU**1** side, and the row decoder **16-2** is disposed on the hookup area HU**2** side.

[0100] In the hookup area HU**1**, the wiring layer **51** and the wiring layer **54** are connected to the row decoder **16-1**.

[0101] In the hookup area HU**2**, a contact plug **58** is provided on the select gate line SGD**0**, and a wiring layer **59** is provided on the contact plug **58**. The wiring layer **57** and the wiring layer **59** are connected to the row decoder **16-2**.

[0102] In the second embodiment, voltages of the select gate lines SGD, the word lines WL, and the select gate lines SGS can be controlled from both sides of the memory cell array **10**. A write operation according to the second embodiment is the same as the write operation according to the first embodiment. The second embodiment is particularly advantageous when the resistance of the select gate line SGD is higher and when the size of the memory cell array is larger. Other advantageous effects are similar to those according to the first embodiment.

[3] Third Embodiment

[3-1] Configuration of Memory Cell Array 10

[0103] FIG. **11** is a sectional view of the hookup areas HU**1** and HU**2** according to the third embodiment.

[0104] In the hookup area HU**1**, the contact plug **50** is provided on the select gate line SGD**0**, the contact plug **52** is provided on the select gate line SGD**1**, and the contact plug **53** is provided on the select gate line SGD**2**. The wiring layer **54** is provided on the contact plugs **50**, **52**, and **53**. That is, in the hookup area HU**1**, the select gate lines SGD**0** to SGD**2** are electrically connected to one another by the wiring layer **54**. The wiring layer **54** is connected to the row decoder **16**. The row decoder **16** executes the same voltage control over the select gate lines SGD**0** to SGD**2**.

[0105] In the hookup area HU**2** on the side far from the row decoder **16**, the select gate lines SGD**0** to SGD**2** are electrically isolated from one another, that is, are not shunted to one another.

[3-2] Operation

[0106] Next, a write operation of the NAND flash memory **1** having the above configuration is described. A basic operation is the same as that in FIG. **6**. In a precharge operation included in the write operation, the row decoder **16** applies the voltage Vsg_pre to the select gate lines SGD**0** to SGD**2**, and precharges the channel of the NAND string. The row decoder **16** then applies the ground voltage Vss to the select gate lines SGD**0** to SGD**2**. That is, the select gate lines SGD**0** to SGD**2** undergo the same voltage control as the select gate lines SGD**1** and SGD**2** in FIG. **6**.

[0107] Further, in a Vpass raising operation (at a time t**2** in FIG. **6**), the row decoder **16** applies the voltage Vpass to all the word lines WL. Accordingly, in an unselected NAND string, the voltage of the channel is boosted.

[0108] FIG. **12** is a graph illustrating voltage waveforms of the select gate line SGD**2** closest to the word line WL. FIG. **13** is a graph illustrating voltage waveforms of the select gate line SGD**1** adjacent to the select gate line SGD**2**. A vertical axis in FIG. **12** indicates the voltage (any unit: a.u.) of the select gate line SGD**2**, and a horizontal axis in FIG. **12** indicates time (μs). The end of the select gate line SGD**2** on the side far from the row decoder **16** is referred to as a "far end", and the end of the select gate line SGD**2** on the side near the row decoder **16** is referred to as a "near end". A time zero in FIG. **12** corresponds to a timing of raising the word line WL to Vpass. FIG. **13** is also a graph similar to that in FIG. **12**.

[0109] As shown in FIG. **12**, the select gate line SGD**2** is considerably affected by capacitive coupling with the adjacent word line WL. At the far end of the select gate line SGD**2** in particular, the voltage of the select gate line SGD**2** significantly rises.

[0110] Herein, the select gate lines SGD**0** to SGD**2** are not shunted at the near ends thereof. Therefore, as shown in FIG. **13**, at the near end of the select gate line SGD**1**, rising of the voltage of the select gate line SGD**1** can be inhibited. Moreover, the select gate line SGD**0** is farther from the word line WL, so that rising of the voltage of the select gate line SGD**0** can be further inhibited.

[0111] In the present embodiment, the cut-off characteristics of the select transistor STD**2** closest to the word line WL deteriorate. However, the cut-off characteristics of the select transistors STD**0** and STD**1** can be improved. As a result, leak currents can be inhibited in the select transistors STD**0** to STD**2** as a whole.

[3-3] Modification

[0112] Next, a modification of the third embodiment is described. FIG. **14** is a sectional view of the hookup areas HU**1** and HU**2** according to a modification of the third embodiment.

[0113] In the hookup area HU**2**, the contact plug **58** is provided on the select gate line SGD**0**, and the contact plug **55** is provided on the select gate line SGD**1**. A shunt wiring layer **60** is provided on the contact plugs **55** and **58**. That is, in the hookup area HU**2**, the select gate line SGD**0** and the select gate line SGD**1** are electrically connected to each other by the shunt wiring layer **60**.

[0114] In the modification as well, rising of the voltages of the select gate lined SGD**0** and SGD**1** can be inhibited. As a result, leak currents can be inhibited in the select transistors STD**0** to STD**2** as a whole.

[3-4] Comparative example

[0115] Next, a comparative example is described. FIG. **15** is a graph illustrating voltage waveforms of the select gate line SGD**2** according to the comparative example. In the comparative example, the select gate lines SGD**0** to SGD**2** are shunted at the near ends thereof.

[0116] As shown in FIG. **15**, the voltage of the select gate line SGD**2** rises at the timing of raising the word lines WL to the voltage Vpass. Moreover, because the select gate lines SGD**0** to SGD**2** are shunted, the select gate lined SGD**0** and SGD**1** have substantially the same voltage waveform as the select gate line SGD**2**. Therefore, in the comparative example, leak currents are higher in the select transistors STD**0** to STD**2** as a whole.

[3-5] Advantageous Effects of Third Embodiment

[0117] As described above in detail, in the third embodiment, for example, three select transistors STD**0** to STD**2** are serially connected between the bit line BL and the word line WL. The select gate lines SGD**0** to SGD**2** are connected to the gates of the select transistors STD**0** to STD**2**, respec-

tively. The select gate lines SGD**0** to SGD**2** are connected to the row decoder **16** at a first end. Moreover, the select gate lines SGD**0** to SGD**2** are electrically isolated from one another at a second end (an end on the hookup area HU**2** side) opposite to the first end (an end on the hookup area HU**1** side) across the NAND strings NS. In addition, the row decoder **16** applies the same voltage to the select gate lines SGD**0** to SGD**2**.

[0118] Therefore, according to the third embodiment, it is possible to inhibit the voltages of the select gate lines SGD**0** and SGD**1** located apart from the word line WL from rising when the word line WL rises to the voltage Vpass. Thus, the cut-off characteristics of the select transistors STD**0** and STD**1** can be improved. This makes it possible to inhibit erroneous writing in an unselected NAND string, and thus improve reliability of the NAND flash memory **1**.

[0119] Note that in each of the embodiments described above, the memory cell array **10** comprises three select gate lines SGD**0** to SGD**2**. However, without being limited thereto, the memory cell array **10** may comprise two select gate lines SGD**0** and SGD**1**, and the select gate lines SGD**0** and SGD**1** may be under independent voltage control. Alternatively, four or more select gate lines SGD may be provided.

[0120] Although a MONOS film is used for the memory cell in the examples described above in the embodiments, the memory cell is not limited thereto. For example, a floating gate type memory cell may be used.

[0121] In the present specification, “connection” means electric connection, and for example, intervention of an additional element between two connected elements is not excluded.

[0122] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit.

1. A semiconductor memory device comprising:
a memory string including first and second select transistors and memory cell transistors which are serially connected in this order;
a bit line connected to the first select transistor;
word lines which are connected to gates of the memory cell transistors, respectively, and which are stacked via insulating layers;
first and second select gate lines which are connected to gates of the first and second select transistors, respectively, and which are stacked on the word lines via insulating layers;
a first contact plug connected to the first select gate line;
a first wiring layer provided on the first contact plug;
a second contact plug connected to the second select gate line;
a second wiring layer provided on the second contact plug; and
a row decoder connected to the first and second wiring layers,
wherein the row decoder is configured to be capable of applying different voltages to the first select gate line and the second select gate line.

2. The device according to claim **1**, wherein
the row decoder drops a voltage of the first select gate line at a raising timing of voltages of the word lines.

3. The device according to claim **1**, wherein
at a first time, the row decoder applies a first voltage to the first and second select gate lines, and applies a second voltage to the word lines,
at a second time, the row decoder applies a ground voltage to the second select gate line and the word lines, and
at a third time, the row decoder applies the ground voltage to the first select gate line, and applies a third voltage to the word lines.

4. The device according to claim **3**, wherein
at a fourth time, the row decoder applies a write voltage higher than the third voltage to a selected word line.

5. The device according to claim **1**, further comprising:
a third select transistor connected between the second select transistor and the memory cell transistors; and
a third select gate line which is connected to a gate of the third select transistor and which is provided between the word lines and the second select gate line via an insulating layer,
wherein the row decoder applies the same voltage as that of the second select gate line to the third select gate line.

6. The device according to claim **5**, wherein
at a first time, the row decoder applies a first voltage to the first to third select gate lines, and applies a second voltage to the word lines,
at a second time, the row decoder applies a ground voltage to the second and third select gate lines and the word lines, and
at a third time, the row decoder applies the ground voltage to the first select gate line, and applies a third voltage to the word lines.

7. The device according to claim **6**, wherein
at a fourth time, the row decoder applies a write voltage higher than the third voltage to a selected word line.

8. The device according to claim **5**, further comprising:
a third contact plug connected to the second select gate line;
a fourth contact plug connected to the third select gate line; and
a third wiring layer provided on the third contact plug and the fourth contact plug.

9. A semiconductor memory device comprising:
a memory string including first and second select transistors and memory cell transistors which are serially connected in this order;
a bit line connected to the first select transistor;
word lines which are connected to gates of the memory cell transistors, respectively, and which are stacked via insulating layers;
first and second select gate lines which are connected to gates of the first and second select transistors, respectively, and which are stacked on the word lines via insulating layers;
a first contact plug connected to the first select gate line;
a second contact plug connected to the second select gate line;

a first wiring layer provided on the first and second contact plugs; and
a row decoder connected to the first wiring layer,
wherein the row decoder applies the same voltage to the first and second select gate lines, and
the first and second select gate lines are electrically isolated from one another at a second end opposite, across the memory string, to a first end on a side where the row decoder is disposed.

10. The device according to claim **9**, further comprising:
a third select transistor connected between the second select transistor and the word lines;
a third select gate line which is connected to a gate of the third select transistor and which is provided between the word lines and the second select gate line via an insulating layer; and
a third contact plug connected to the third select gate line and the first wiring layer,
wherein the row decoder applies the same voltage to the first to third select gate lines, and
the first to third select gate lines are electrically isolated from one another at the second end.

11. The device according to claim **9**, further comprising:
a third select transistor connected between the second select transistor and the word lines;
a third select gate line which is connected to a gate of the third select transistor and which is provided between the word lines and the second select gate line via an insulating layer;
a third contact plug connected to the first end of the third select gate line and the first wiring layer,
a fourth contact plug connected to the second end of the first select gate line;
a fifth contact plug connected to the second end of the second select gate line; and
a second wiring layer provided on the fourth and fifth contact plugs,
wherein the row decoder applies the same voltage to the first to third select gate lines.

12. The device according to claim **9**, wherein
at a first time, the row decoder applies a first voltage to the first and second select gate lines, and applies a second voltage to the word lines,
at a second time, the row decoder applies a ground voltage to the first and second select gate lines and the word lines, and
at a third time, the row decoder applies a third voltage to the word lines.

13. The device according to claim **12**, wherein
at a fourth time, the row decoder applies a write voltage higher than the third voltage to a selected word line.

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