(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 May 2013 (10.05.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/066584 A1

(51) International Patent Classification:
G11C 11/34 (2006.01)

(21) International Application Number:
PCT/US2012/059623

(22) International Filing Date:
10 October 2012 (10.10.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/286,933 1 November 2011 (01.11.2011) US

(71) Applicant: **SILICON STORAGE TECHNOLOGY, INC.** [US/US]; 450 Holger Way, San Jose, CA 95134 (US).

(72) Inventors; and
(71) Applicants *(for US only)*: **MARKOV, Viktor** [US/US]; 1075 Valencia Avenue, Apt. 8, Sunnyvale, CA 94086 (US). **YOO, Jong-Won** [KR/US]; 22466 Rancho Ventura Street, Cupertino, CA 95014 (US). **NGUYEN, Hung, Quoc** [US/US]; 3272 Winding Vista Common, Fremont, CA 94539 (US). **KOTOV, Alexander** [US/US]; 1235 Wildwood Avenue, Apt. 87, Sunnyvale, CA 94089 (US).

(74) Agent: **LIMBACH, Alan, A.**; Dla Piper LLP US, 2000 University Avenue, East Palo Alto, CA 94303 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) **Title**: A METHOD OF PROGRAMMING A SPLIT GATE NON-VOLATILE FLOATING GATE MEMORY CELL HAVING A SEPARATE ERASE GATE

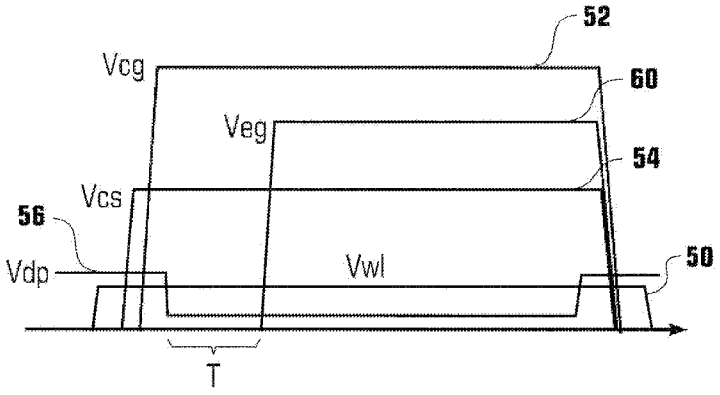

FIG. 2

(57) **Abstract**: During the programming of a non-volatile memory cell, a voltage pulse is applied to an erase gate of the cell a delay time after voltage pulses are applied to the other elements of the cell. The erase gate voltage pulse ends at substantialy the same time as the other voltage pulses end.

WO 2013/066584 A1

A METHOD OF PROGRAMMING A SPLIT GATE NON-VOLATILE FLOATING GATE MEMORY CELL HAVING A SEPARATE ERASE GATE

TECHNICAL FIELD

[0001] The present invention relates to a method of programming a non-volatile memory cell having a floating gate and more particularly to a method of programming a split gate non-volatile memory cell having a separate erase gate.

BACKGROUND OF THE INVENTION

[0002] Non-volatile memory cells having a floating gate for the storage of charges thereon are well known in the art. Referring to Figure 1 there is shown a cross-sectional view of a non-volatile memory cell 10 of the prior art. The memory cell 10 comprises a single crystalline substrate 12, of a first conductivity type, such as P type. At or near a surface of the substrate 12 is a first region 14 of a second conductivity type, such as N type. Spaced apart from the first region 14 is a second region 16 also of the second conductivity type. Between the first region 14 and the second region 16 is a channel region 18. A word line 20, made of polysilicon is positioned over a first portion of the channel region 18. The word line 20 is spaced apart from the channel region 18 by an insulating layer 22, such as silicon (di)oxide. Immediately adjacent to and spaced apart from the word line 20 is a floating gate 24, which is also made of polysilicon, and is positioned over another portion of the channel region 18. The floating gate 24 is separated from the channel region 18 by another insulating layer 30, typically also of silicon (di)oxide. A coupling gate 26, also made of polysilicon is positioned over the floating gate 24 and is insulated therefrom by another insulating layer 32. On another side of the floating gate 24, and spaced apart therefrom, is an erase gate 28, also made of polysilicon. The erase gate 28 is positioned over the second region 16 and is insulated therefrom. The erase gate 28 is adjacent to and spaced apart from the coupling gate 26. The erase gate 28 can have a slight overhang over the floating gate 24. In the operation of the memory cell 10, charge stored on the

floating gate 24 controls the flow of current between the first region 14 and the second region 16. Where the floating gate 24 is negatively charged thereon, the memory cell is programmed. Where the floating gate 24 is positively charged thereon, the memory cell is erased. The memory cell 10 is fully disclosed in USP 7,868,375 whose disclosure is incorporated herein in its entirety by reference.

[0003] The memory cell 10 operates as follows. During the programming operation, when electrons are injected to the floating gate 24 through hot-electron injection with the portion of the channel 18 under the floating gate 24 in inversion, a first positive voltage in the shape of a pulse is applied to the word line 20 causing the portion of the channel region 18 under the word line 20 to be conductive. A second positive voltage, also in the shape of a pulse, is applied to the coupling gate 26, to utilize high coupling ratio between coupling gate 26 and floating gate 24 to maximize the voltage coupling to the floating gate 24. A third positive voltage, also in the shape of a pulse, is applied to the erase gate 28, to utilize coupling ratio between erase gate 28 and floating gate 24 to maximize the voltage coupling to the floating gate 24. A voltage differential, also in the shape of a pulse, is applied between the first region 14 and the second region 16, to provide generation of hot electrons in the channel 18. All of the first positive voltage, second positive voltage, third positive voltage and the voltage differential are applied substantially at the same time, and terminate substantially at the same time. During programming operation the potential on the floating gate 24 monotonically reduces from a highest value at the beginning of programming operation to a lowest value at the end of programming operation.

[0004] During the erase operation, when electrons are removed from the floating gate 24, a high positive voltage is applied to the erase gate 28. A negative voltage or ground voltage can be applied to the coupling gate 26 and/or the word line 20. Electrons are transferred from the floating gate 24 to the erase gate 28 by Fowler-Nordheim tunneling through the insulating layer between the floating gate 24 and

the erase gate 28. In particular, the floating gate 24 may be formed with a sharp tip facing the erase gate 28, thereby facilitating said tunneling of electrons.

[0005] During the read operation, a first positive voltage is applied to the word line 20 to turn on the portion of the channel region 18 beneath the word line 20. A second positive voltage is applied to the coupling gate 26. A voltage differential is applied to the first region 14 and the second region 16. If the floating gate 24 were programmed, i.e. the floating gate 24 stores electrons, then the second positive voltage applied to the coupling gate 26 is not able to overcome the negative electrons stored on the floating gate 24 and the portion of the channel region 18 beneath the floating gate 24 remains non-conductive. Thus, no current or a negligibly small amount of current would flow between the first region 14 and the second region 16. However, if the floating gate 24 were not programmed, i.e. the floating gate 24 remains neutral or positively charged, then the second positive voltage applied to the coupling gate 26 is able to cause the portion of the channel region 18 beneath the floating gate 24 to be conductive. Thus, a current would flow between the first region 14 and the second region 16.

[0006] As is well known, memory cells 10 are typically formed in an array, having a plurality of rows and columns of memory cells 10, on a semiconductor wafer. One of the uses for an array of floating gate non-volatile memory cells is as a smart card. However, in such application, the array of non-volatile memory cells must have high program/erase endurance. In the prior art, during programming a high voltage has been applied to the coupling gate 26 and erase gate 28 in order to induce sufficient potential on the floating gate 24 to cause hot electrons to be injected from the channel region 18 to the floating gate 24. However, the maximum potential induced on the floating gate 24 at the beginning of programming operation can cause relatively fast degradation of the insulating layer 30 between the floating gate 24 and the channel region 18 as well as the interface between the channel region 18 and the insulating layer 30. The degradation of

these areas is a major factor which affects program/erase endurance of a memory cell.

[0007] The prior art also discloses applying a ramped voltage to the coupling gate 26 of a memory cell having a word line gate 20 and a coupling gate 26 (but without an erase gate) during programming to increase the endurance of the memory cell. See "Method For Endurance Optimization of The HIMOS Flash Memory Cell" by Yao et al, IEEE 43rd Annual International Reliability Physics Symposium, San Jose, 2005, pp. 662-663.

[0008] The memory cell 10 does not require a high voltage to be applied to the second region 16 to cause programming, which enables high program/erase endurance. Nevertheless, the prior art method of programming has not been optimized for high program/erase endurance. Hence, one object of the present invention is to optimize the parameters for programming the memory cell of the type shown in Figure 1 so that endurance is further increased.

SUMMARY OF THE INVENTION

[0009] The present invention is a method of programming a non-volatile memory cell of the type with a single crystalline substrate of a first conductivity type and having a top surface. A first region of a second conductivity type is in the substrate along the top surface. A second region of the second conductivity type is in the substrate along the top surface, spaced apart from the first region, with a channel region between the first region and the second region. A word line gate is positioned over a first portion of the channel region, spaced apart from the channel region by a first insulating layer. A floating gate is positioned over another portion of the channel region, adjacent to and separated from the word line gate. The floating gate is separated from the channel region by a second insulating layer. A coupling gate is positioned over the floating gate and is insulated therefrom by a

third insulating layer. An erase gate is positioned adjacent to the floating gate and is on a side opposite to the word line gate. The erase gate is positioned over the second region and is insulated therefrom. In the programming method a first positive voltage is applied to the word line gate to turn on the portion of the channel region beneath the word line gate. A voltage differential is applied between the first region and the second region, substantially at the same time as the first positive voltage, to provide generation of hot electrons in the channel. A second positive voltage is applied to the coupling gate, substantially at the same time as the first positive voltage, to provide hot electron injection from the channel to the floating gate. A third positive voltage is applied to the erase gate gate. The third positive voltage is applied after a period of delay after the start of the first and second positive voltages and voltage differential between the first region and the second region, to reduce the maximum potential of the floating gate during programming operation and, therefore, to improve program/erase endurance of the memory cell.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a cross-sectional view of a non-volatile memory cell of the prior art with a floating gate for the storage of charges thereon to which the programming method of the present invention is applicable.

[0011] Figure 2 are graphs showing the various waveforms for the voltages used in programming the memory cell of Figure 1 in the method of the present invention.

[0012] Figure 3 are graphs showing the voltage potential on the floating gate as a result of the prior art method wherein the voltage pulses to the erase gate and the control gate are applied substantially simultaneously, and as a result of the present method when they are not applied simultaneously.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0013] Referring to Figure 2 there is shown a graph of the various waveforms, used in the method of the present invention to program the memory cell 10 shown in Figure 1. In the method of the present invention, a first positive voltage, substantially of a pulse form shape 50 is applied to the word line gate 20. The pulse applied to the word line gate 20 is identified as the pulse Vwl in Figure 2. A second positive voltage, substantially of a pulse form shape 52 is applied to the coupling gate 26. The pulse applied to the coupling gate 26 is identified as the pulse Vcg in Figure 2. The pulse Vwl and Vcg are applied substantially at the same time, and end substantially at the same time. A voltage differential comprising of a voltage Vcs 54 which is applied to the second region 16 and a voltage Vdp 56 which is applied to the first region 14 are also substantially of pulse shape form and are also applied substantially at the same time as the pulses Vwl and Vcg. A third positive voltage, substantially of a pulse form shape 60 is applied to the erase gate 28. The pulse applied to the erase gate 28 is identified as the pulse Veg in Figure 2. The pulse Veg is applied after a period of delay T after the start of the pulses Vwl and Vcg, but with the pulse Veg terminating substantially at the same time as the pulses Vwl and Vcg.

[0014] In the method of programming of the present invention, a first positive voltage is applied to the word line gate to turn on the portion of the channel region beneath the word line gate. A voltage differential is applied between the first region and the second region, substantially at the same time as the first positive voltage, to provide generation of hot electrons in the channel. A second positive voltage is applied to the coupling gate, substantially at the same time as the first positive voltage, to induce high potential to floating gate and, therefore, to cause hot electrons to be injected to the floating gate from the channel region. A third positive voltage is applied to the erase gate, to provide additional voltage to attract electrons to be injected to the floating gate. A third positive voltage is applied after

a period of delay from the application of the first positive voltage, the second positive voltage and the voltage differential between the first region and the second region, to improve program/erase endurance of the memory cell.

[0015] In the prior art when the pulse Vcg, the pulse Vwl, and the pulse Veg are all applied substantially at the same time, the voltage experience by the floating gate 24 is at the highest peak, and the insulating layer 30 between the floating gate 24 and the channel region 18 is stressed at the maximum. This reduces the endurance of the memory cell 10.

[0016] In the present invention, by delaying the application of the Veg, the maximum floating gate potential during the programming operation is reduced, thereby reducing degradation of the insulating layer 30 between the floating gate 24 and the channel region 18 as well as the interface between the channel region 18 and the insulating layer 30 and, therefore, increasing the endurance of the memory cell 10.

[0017] Referring to Figure 3 there is a shown a graph 80 of the voltage on the floating gate 24 as a result of the voltage pulses to the erase gate 28 and the control gate 26 being applied substantially simultaneously, as in the method of the prior art, as well as a graph 82 of the voltage on the floating gate 24 as a result of the voltage pulses to the erase gate 28 being applied after a period of delay from the voltage applied to the control gate 26. Because of the delay in the application in the voltage to the erase gate 28 occurring after a period of delay T, the peak voltage Vfg2 as in the method of the invention is lower than the peak voltage Vfg1 as in the method of the prior art. As a result, degradation of the insulating layer 30 between the floating gate 24 and the channel region 18 as well as the interface between the channel region 18 and the insulating layer 30 is reduced.

What Is Claimed Is

1. A method of programming a non-volatile memory cell having a single crystalline substrate of a first conductivity type and having a top surface, with a first region of a second conductivity type in said substrate along the top surface, and a second region of the second conductivity type, in said substrate along the top surface, spaced apart from the first region, with a channel region between the first region and the second region; a word line gate is positioned over a first portion of the channel region, spaced apart from the channel region by a first insulating layer; a floating gate is positioned over another portion of the channel region, adjacent to and separated from the word line gate, wherein the floating gate is separated from the channel region by a second insulating layer; a coupling gate is positioned over the floating gate and insulated therefrom by a third insulating layer; and an erase gate is positioned adjacent to the floating gate and on a side opposite to the word line gate; said erase gate positioned over the second region and is insulated therefrom; said method comprising:

applying a first positive voltage to the word line gate to turn on the portion of the channel region beneath the word line gate;

applying a voltage differential between the first region and the second region;

applying a second positive voltage to the coupling gate, substantially at the same time as the first positive voltage, to cause hot electrons to be injected to the floating gate from the channel region;

applying a third positive voltage to the erase gate after a period of delay after the start of the first and second positive voltages and a voltage differential between the first region and the second region, to cause electrons to be injected to the floating gate.

2. The method of claim 1 wherein said first, second and third positive voltages terminate at substantially the same time.

3. The method of claim 1 wherein said voltage differential between the first region and the second region is applied at substantially the same time as the first and second positive voltages.

4. The method of claim 1 wherein each of said first, second and third voltages is a pulse shaped signal, and wherein said third voltage is a delayed pulse signal.

5. The method of claim 4 wherein said first, second and third positive voltages terminate at substantially the same time.

6. The method of claim 1 whereby the period of delay is long enough to reduce the maximum potential on the floating gate during the programming operation.

7. The method of claim 1 wherein said erase gate has an overhang over the floating gate.

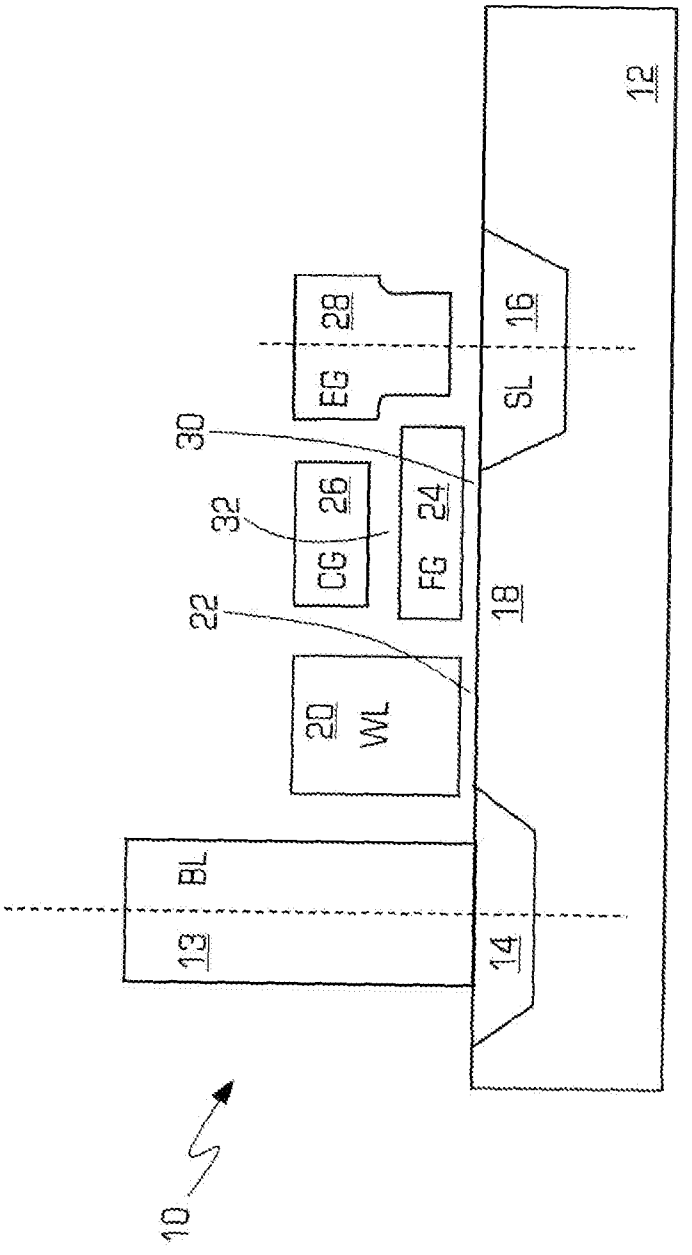

FIG. 1 (PRIOR ART)

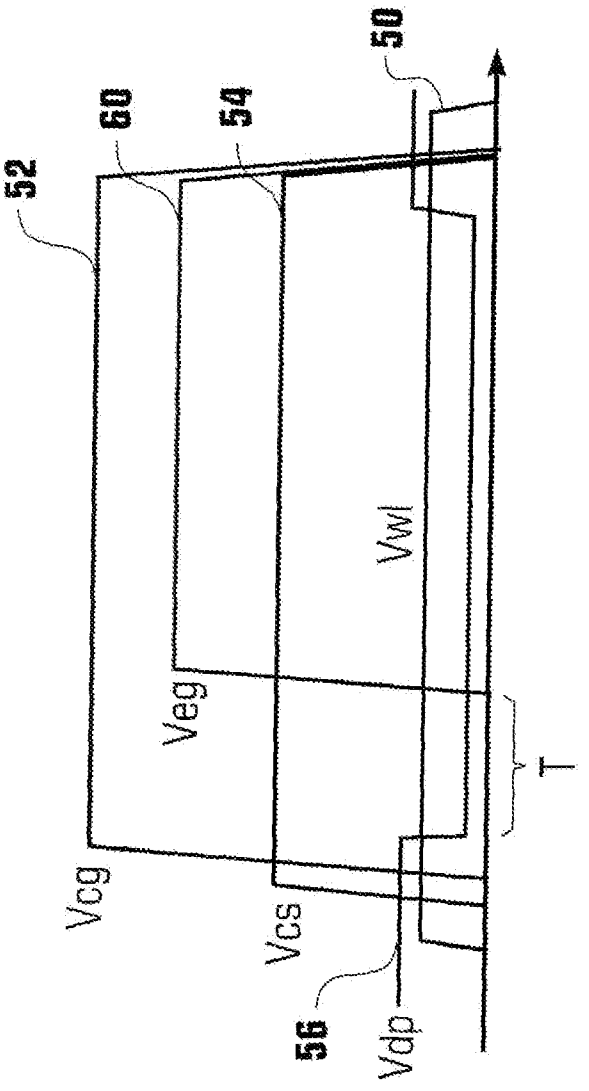

FIG. 2

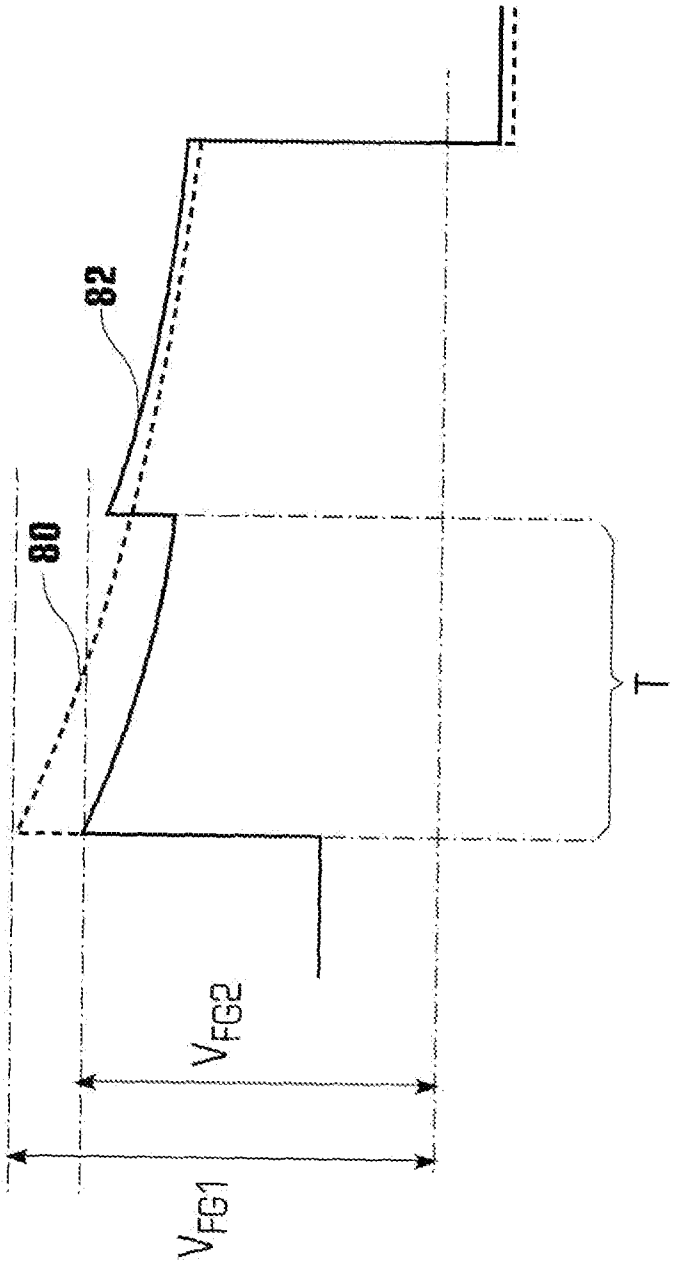

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/59623

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G11C 11/34 (2012.01)
USPC - 365/185.05
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 365/185.05

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 365/185.01; 365/185.18 (text search - see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase(All); PubWEST(USPT,PGPB,EPAB,JPAB); Google
Search Terms: split gate, non volatile, memory, erase gate, delay, timing, floating gate, pulse, program, word line, bit line, coupling gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7,868,375 B2 (LIU et al.) 11 January 2011 (11.01.2011), entire document especially Figs 1A, 1B; col 2, lns 31-59; col 9, lns 44-66	1-7
Y	US 2003/0218920 A1 (HARARI) 27 November 2003 (27.11.2003), entire document especially col 2, lns 20-30; col 3, lns 32-34; col 24, lns 4-27	1-7
Y	US 2007/0291545 A1 (MOKLESI) 20 December 2007 (20.12.2007), entire document especially Fig 11; para [0071]	1-7
A	US 6,747,310 B2 (FAN et al.) 08 June 2004 (08.06.2004), entire document	1-7
A	US 2008/0291737 A1 (MOON et al.) 27 November 2008 (27.11.2008), entire document	1-7

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2012 (25.11.2012)	10 DEC 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)