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(54) **VERIFICATION APPARATUS AND VERIFICATION METHOD FOR TOUCH DISPLAY PANEL**

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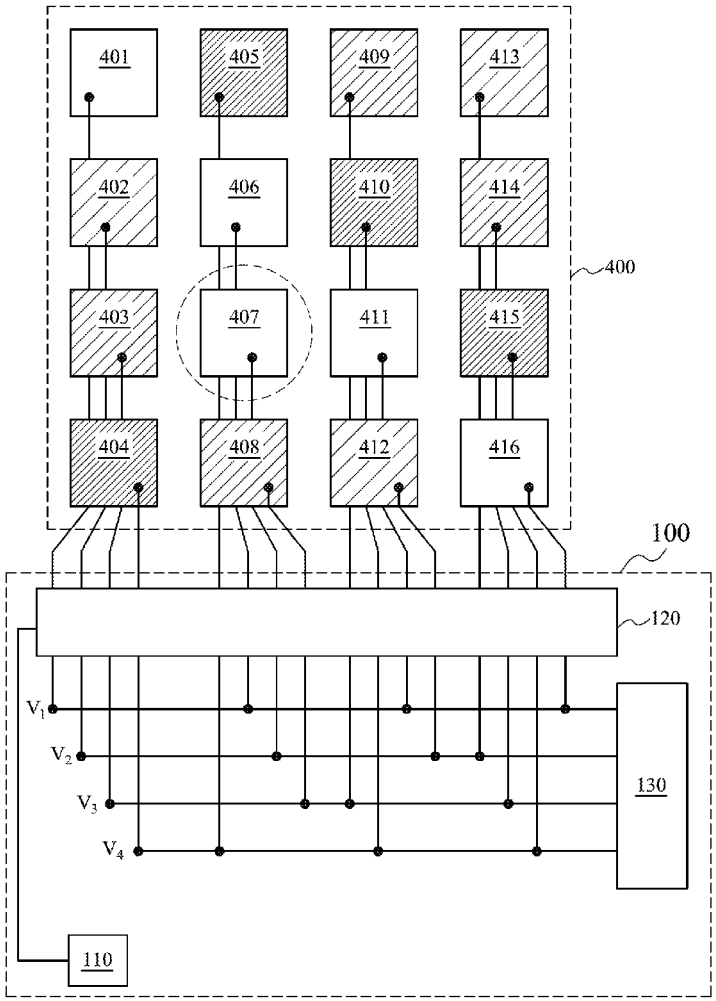
CPC ***G06F 3/0418*** (2013.01)

(57) **ABSTRACT**

A verification apparatus and a verification method are provided in this disclosure. The verification apparatus is suitable for touch display panel which comprises multiple partitions. The verification apparatus includes signal generating circuit and verification switch circuit. The signal generating circuit is configured to generate verification voltage. The verification switch circuit comprises multiple switch units which is separately coupled to the partitions and the signal generating circuit, and is configured to deliver verification voltage simultaneously to a least two of multiple partitions.



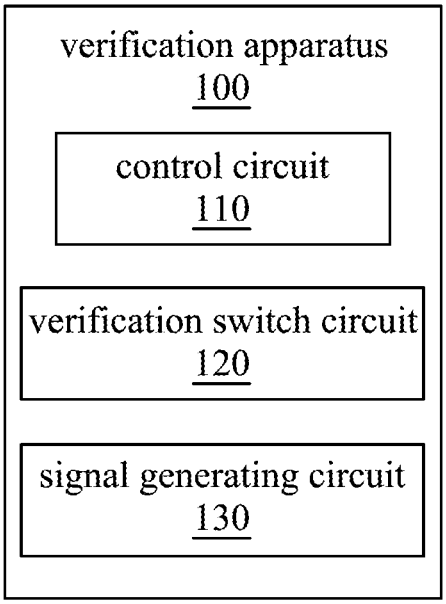
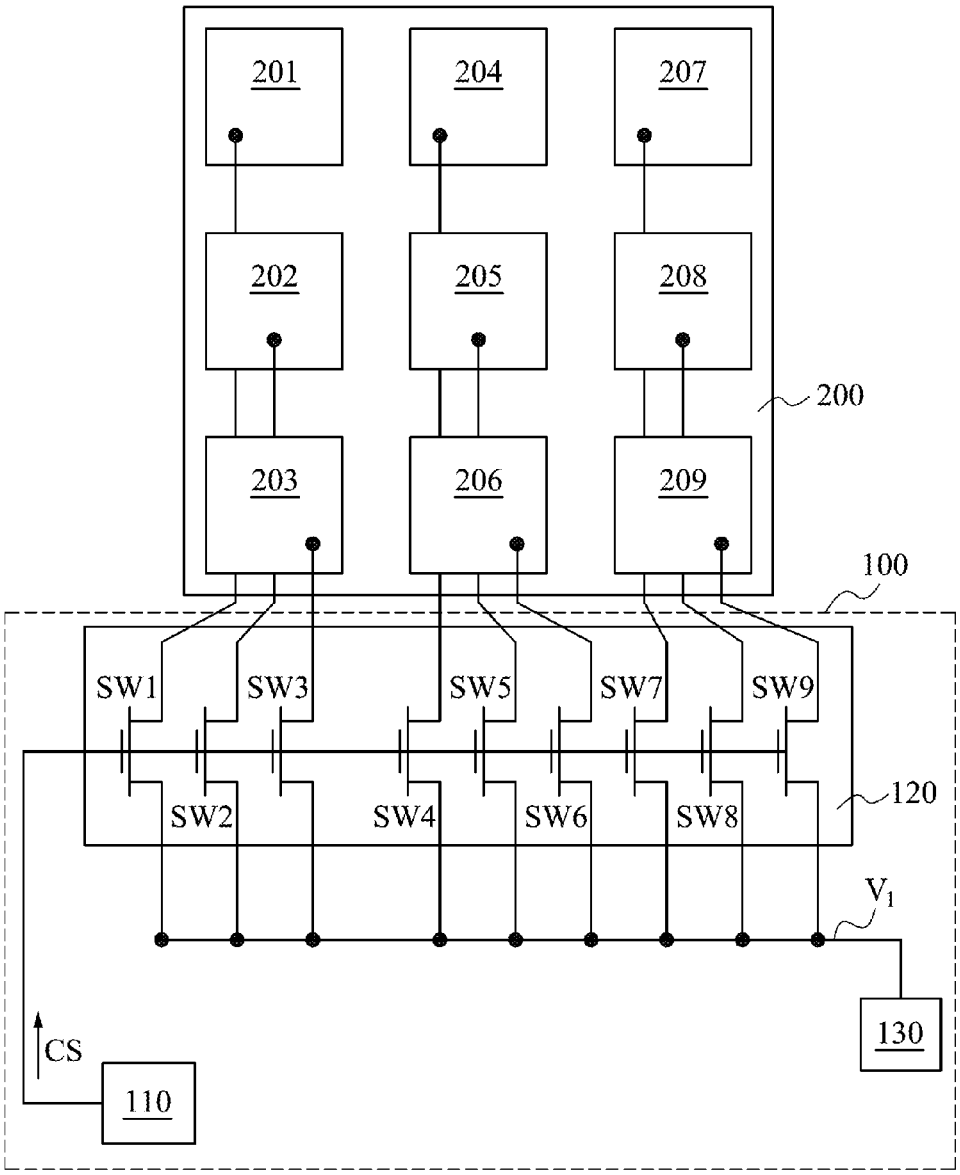

verification apparatus
100
control circuit
110
verification switch circuit
120
signal generating circuit
130

Fig. 1


201
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209
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SW4
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SW8
120
V_1
CS
110
130

Fig. 2

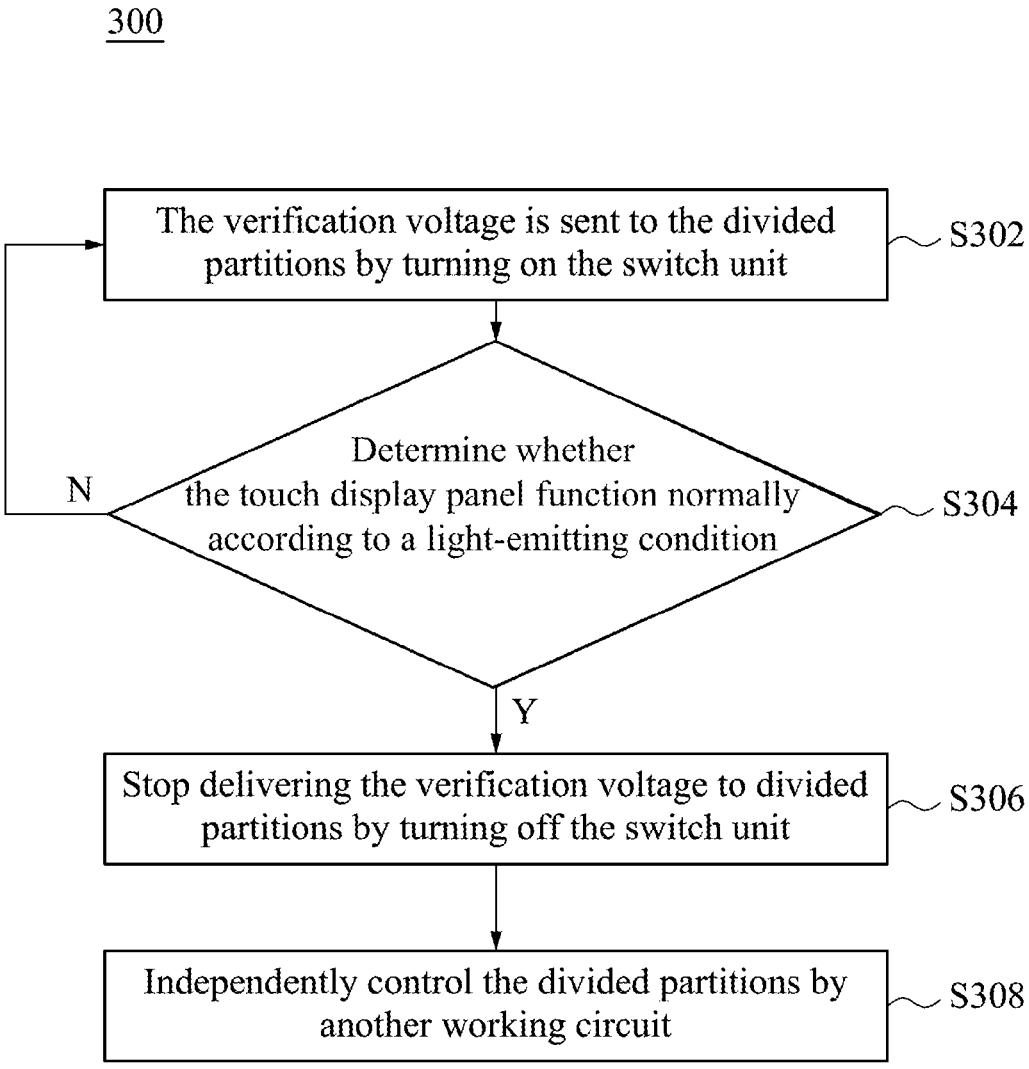

300
The verification voltage is sent to the divided partitions by turning on the switch unit
S302
Determine whether the touch display panel function normally according to a light-emitting condition
S304
N
Y
Stop delivering the verification voltage to divided partitions by turning off the switch unit
S306
Independently control the divided partitions by another working circuit
S308

Fig. 3A

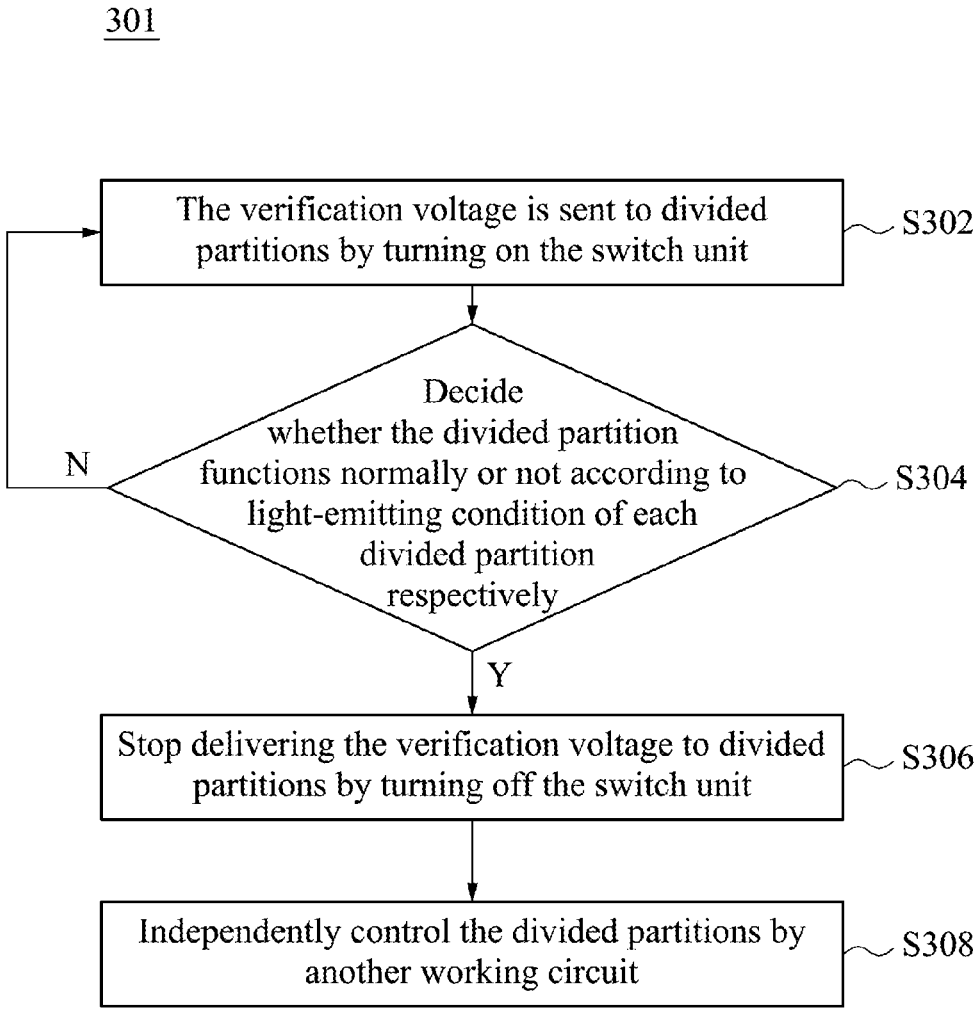

301
The verification voltage is sent to divided partitions by turning on the switch unit
S302
Decide whether the divided partition functions normally or not according to light-emitting condition of each divided partition respectively
S304
N
Y
Stop delivering the verification voltage to divided partitions by turning off the switch unit
S306
Independently control the divided partitions by another working circuit
S308

Fig. 3B

302

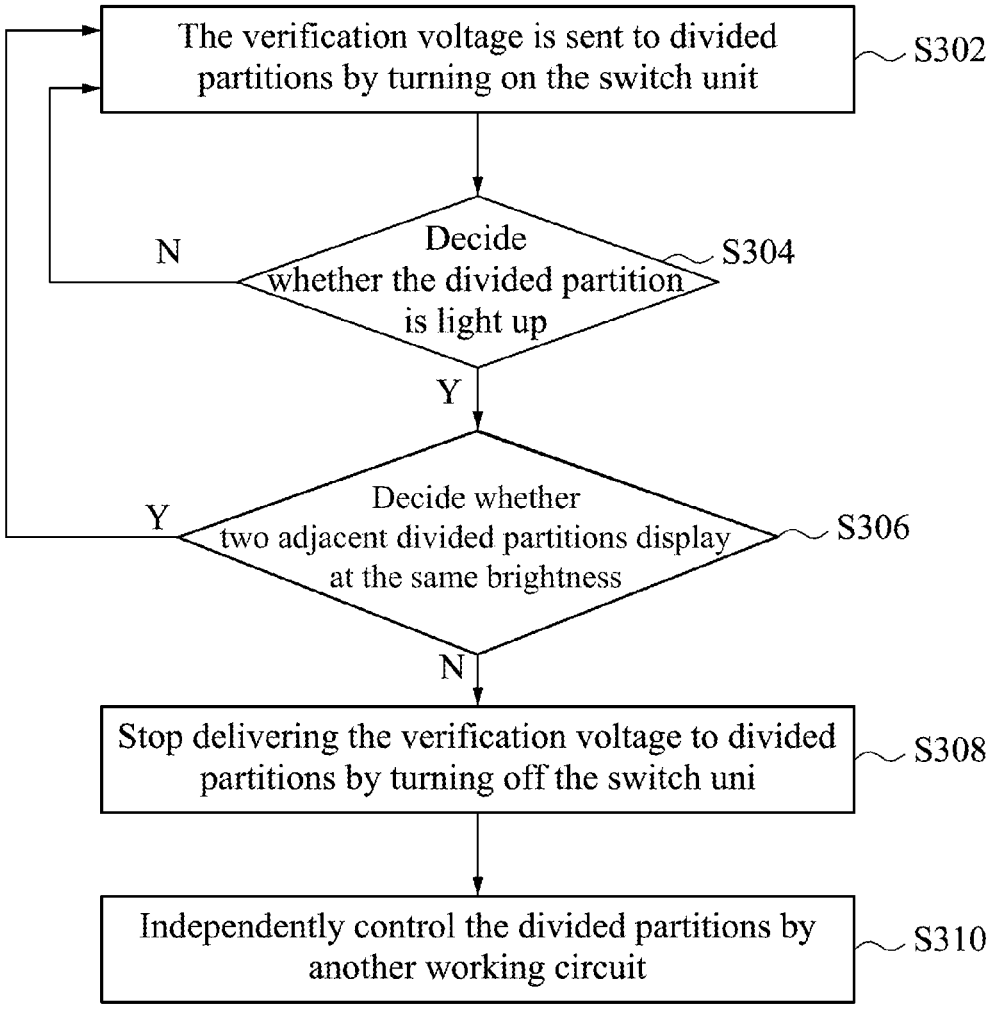
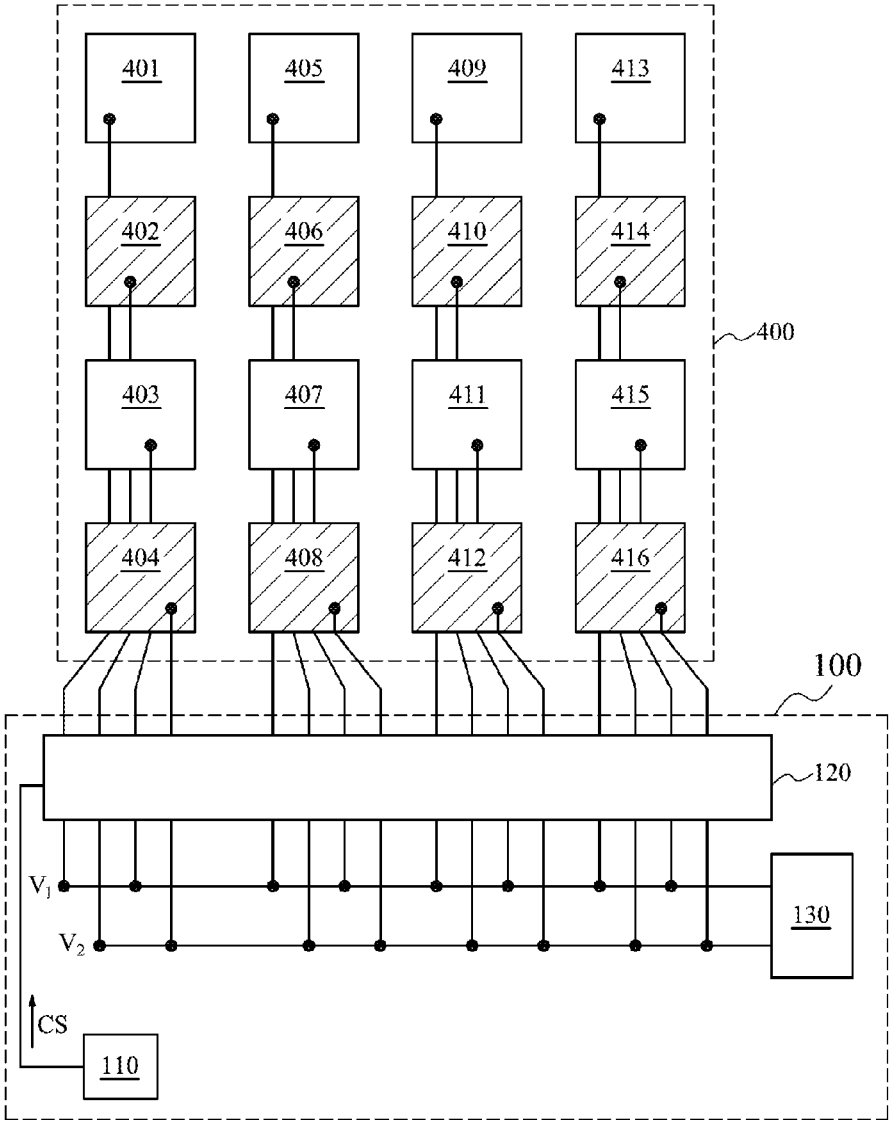

The verification voltage is sent to divided partitions by turning on the switch unit
S302
Decide whether the divided partition is light up
S304
N
Y
Decide whether two adjacent divided partitions display at the same brightness
S306
Y
N
Stop delivering the verification voltage to divided partitions by turning off the switch uni
S308
Independently control the divided partitions by another working circuit
S310

Fig. 3C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CS
110

Fig. 4A

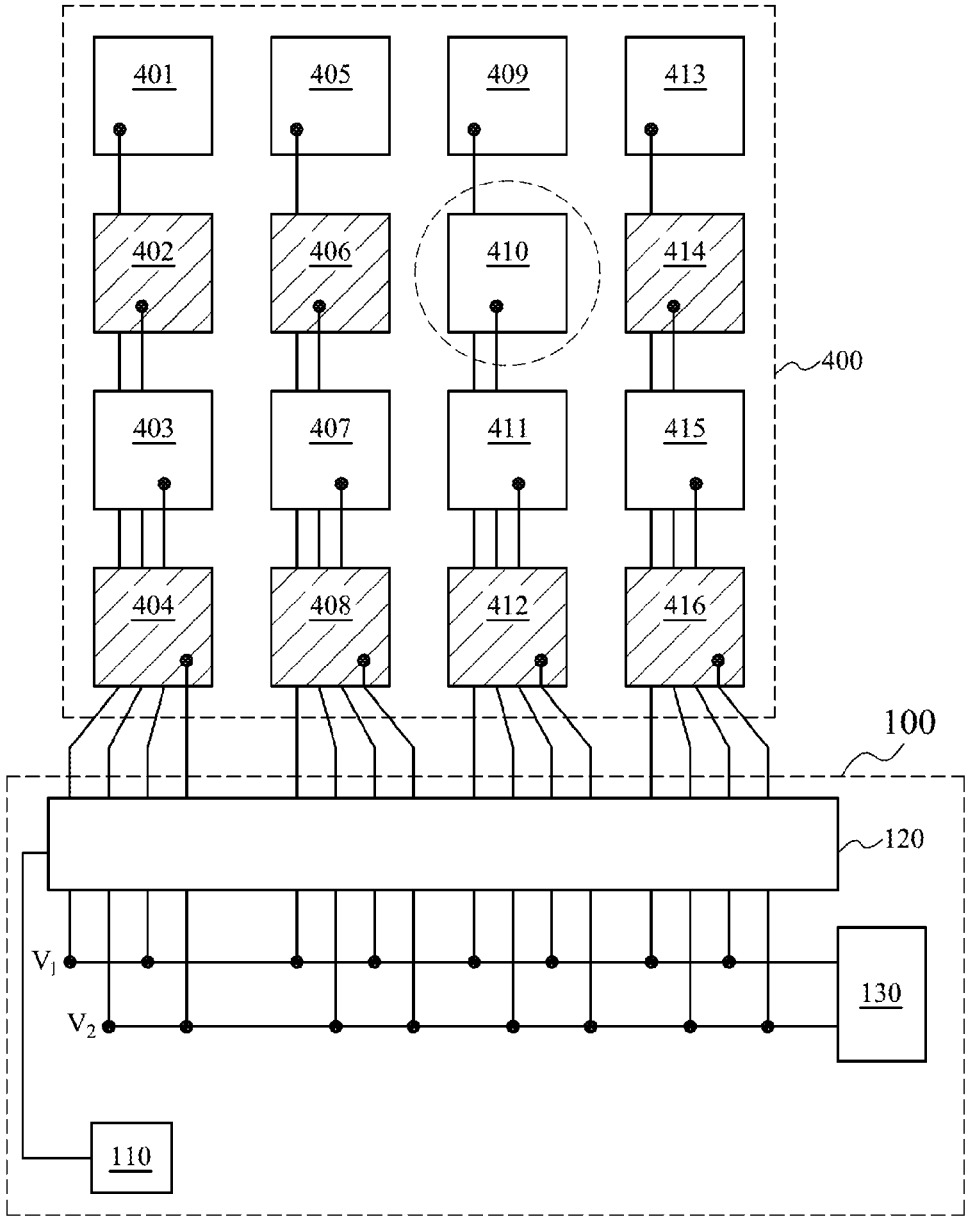
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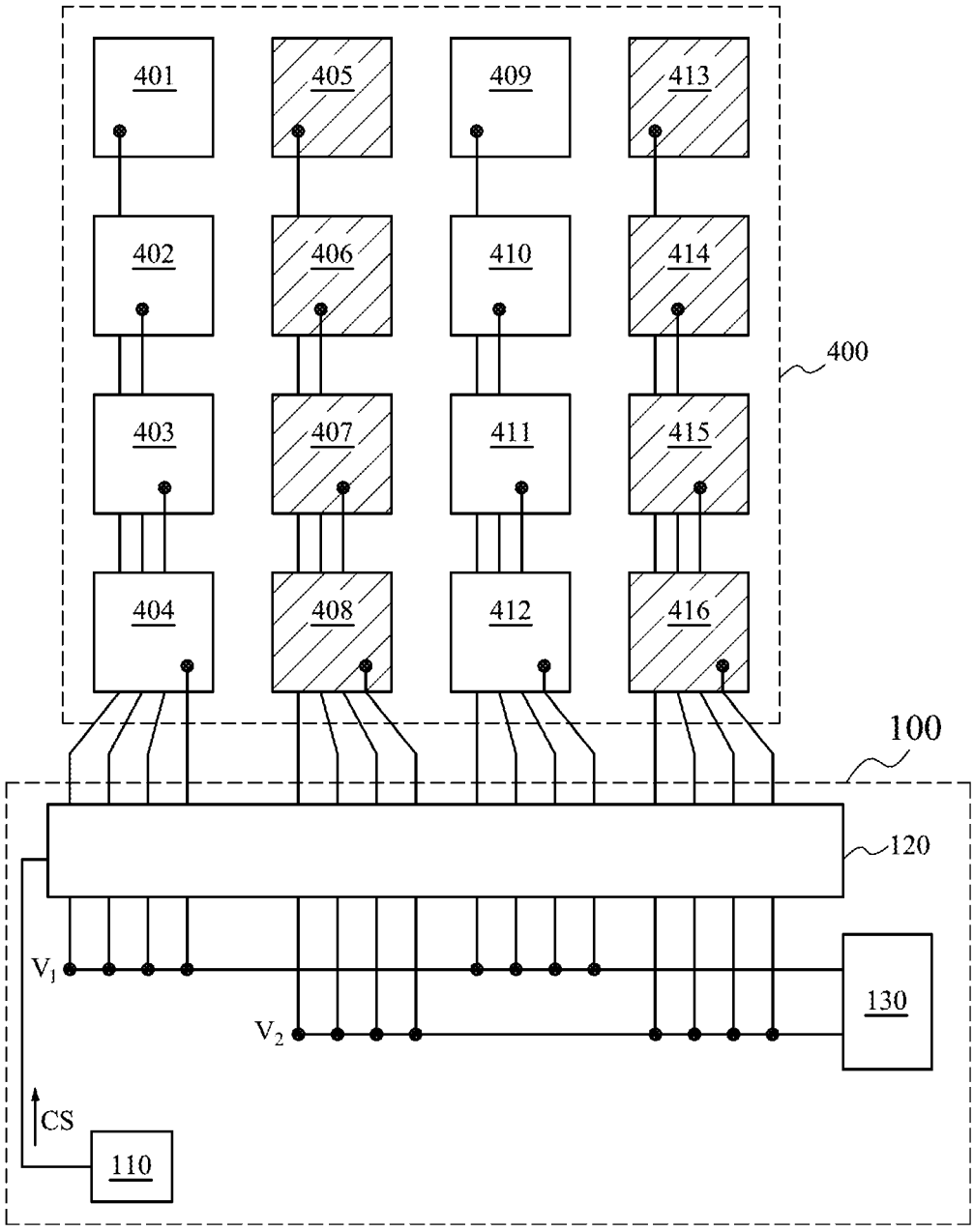
Fig. 4B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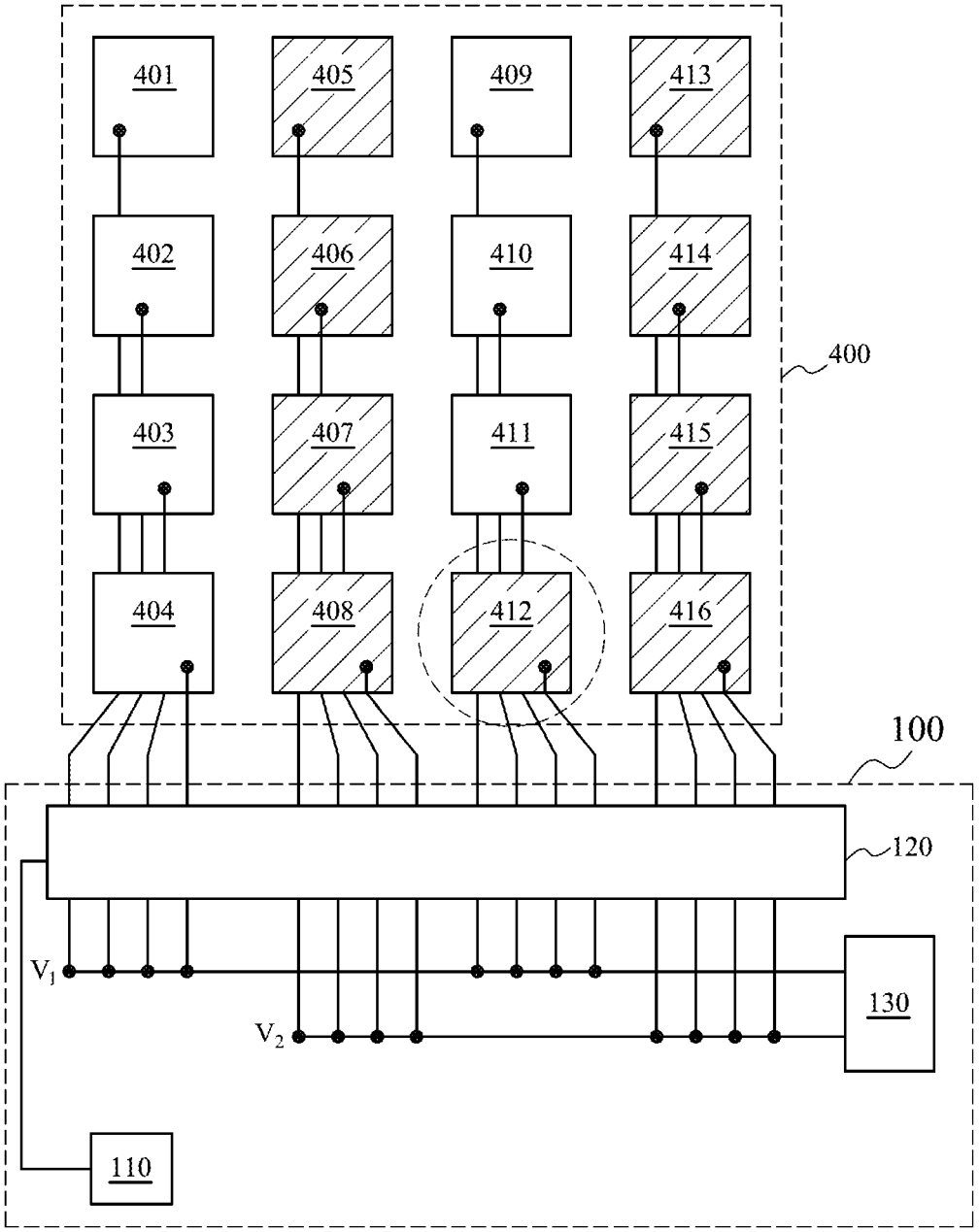
V_2
CS
110

Fig. 5A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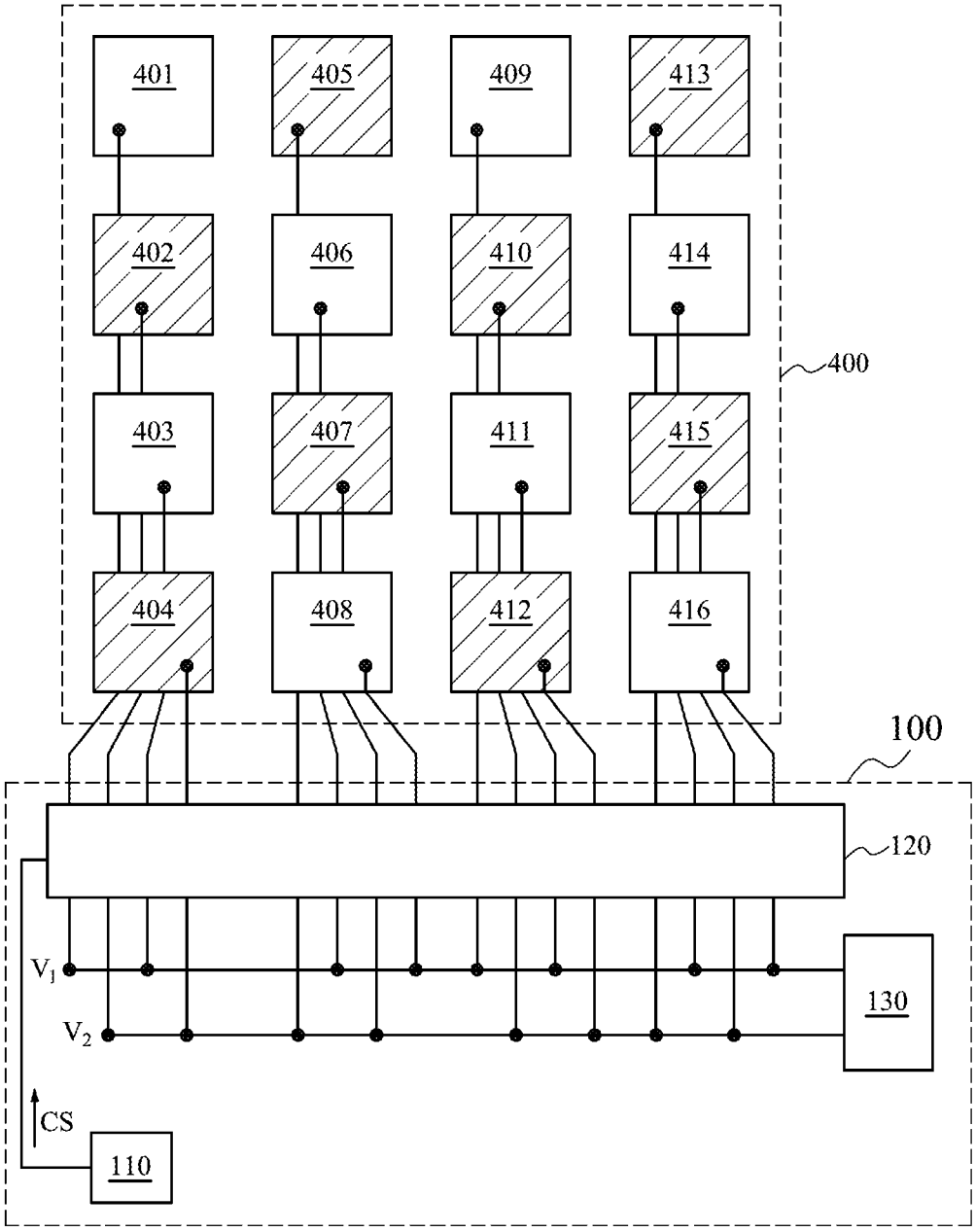
110

Fig. 5B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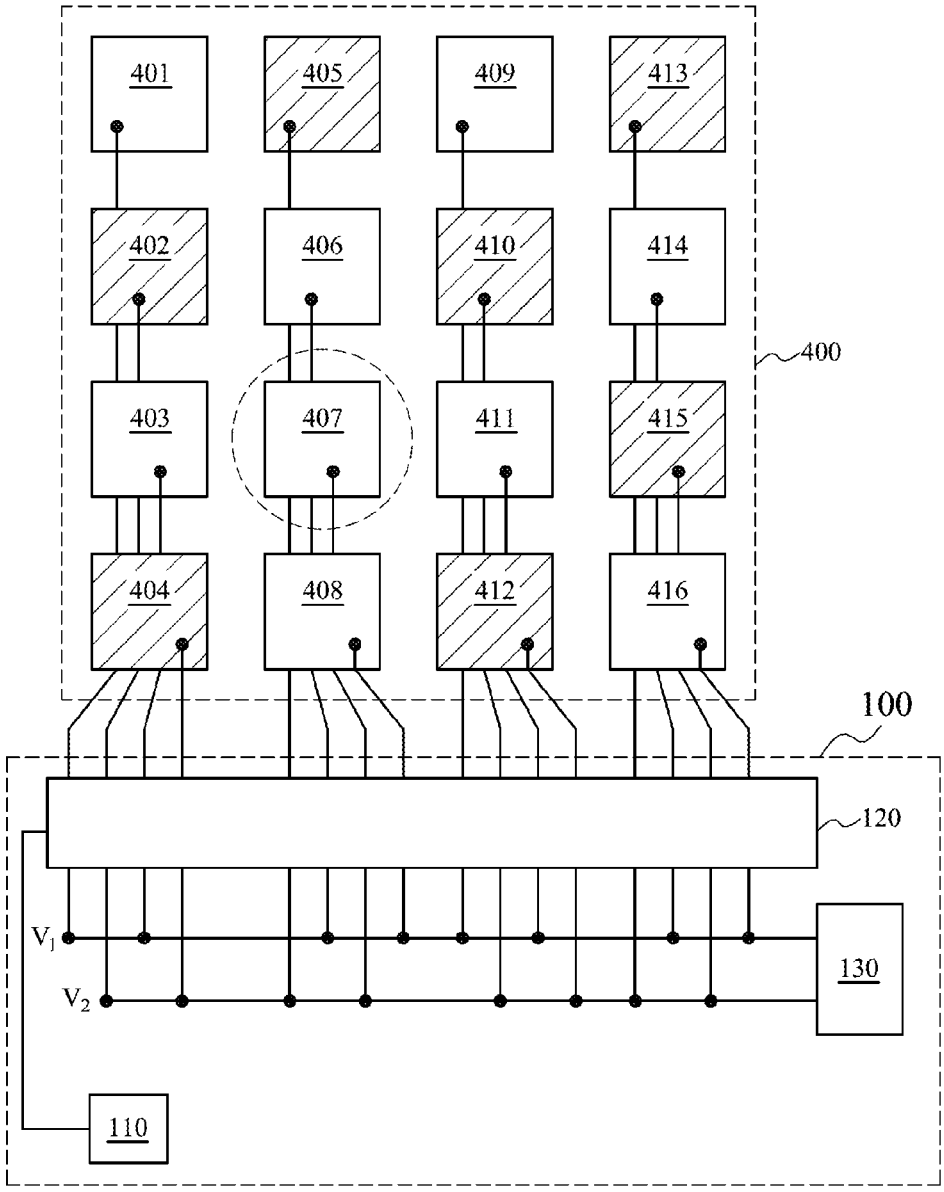
V_1
V_2
130
CS
110

Fig. 6A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V_1
V_2
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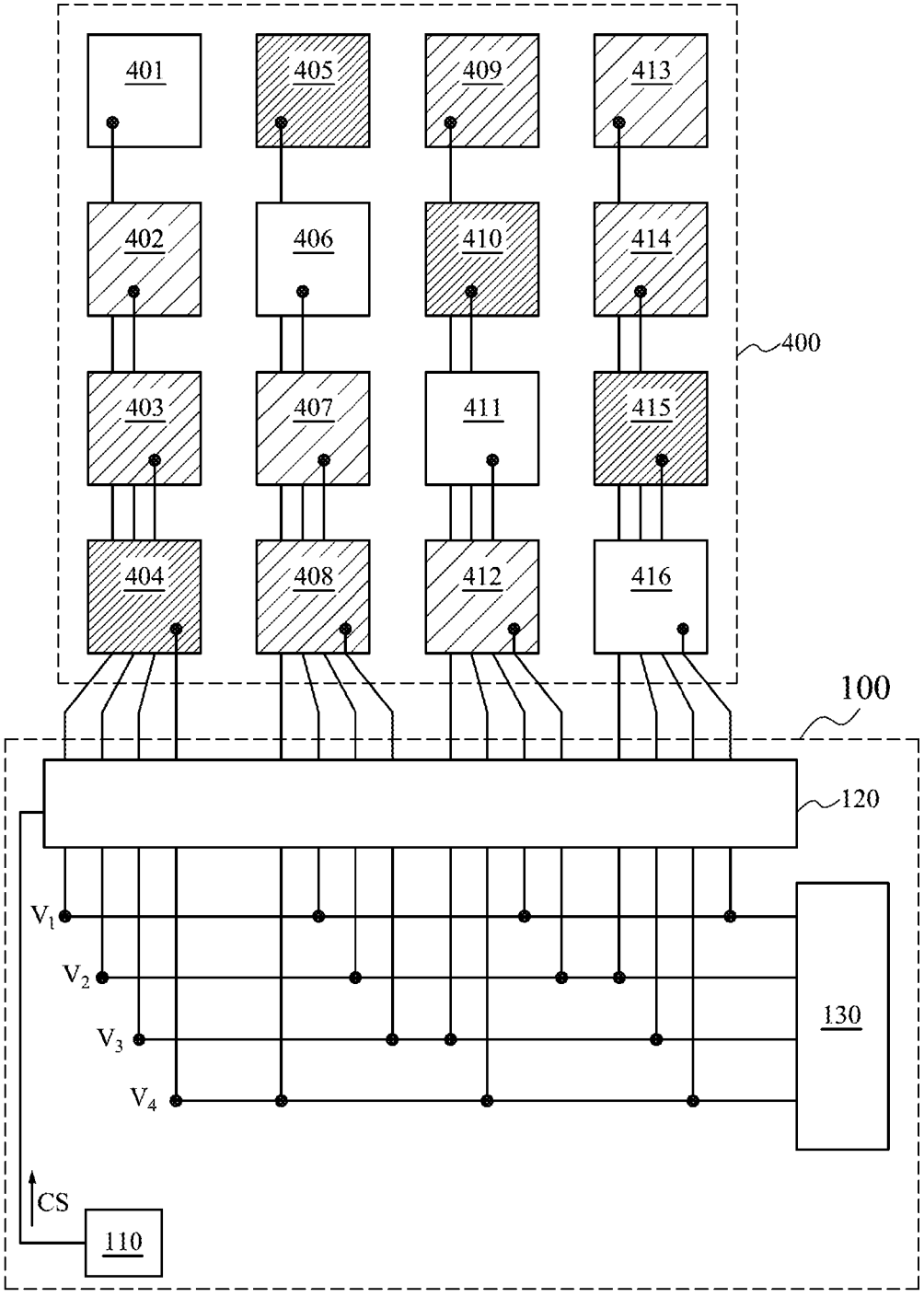
110

Fig. 6B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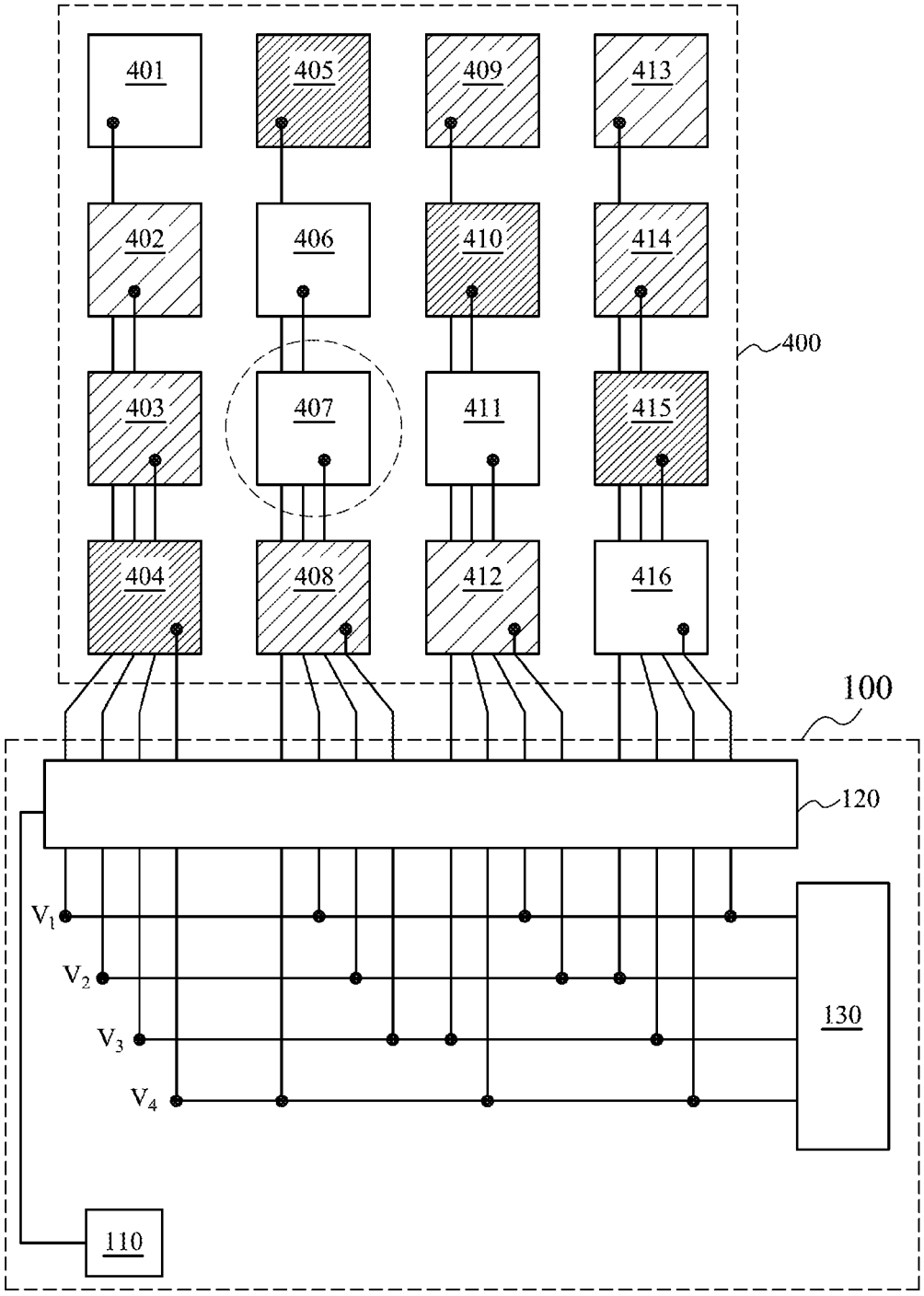
V_1
V_2
V_3
V_4
130
CS
110

Fig. 7A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100
120
V_1
V_2
V_3
V_4
130
110

Fig. 7B

VERIFICATION APPARATUS AND VERIFICATION METHOD FOR TOUCH DISPLAY PANEL

[0001] This application claims priority to Chinese Application Serial Number 201610004021.X, filed Jan. 4, 2016, the disclosures of which are incorporated herein by reference in their entireties.

BACKGROUND

[0002] Field of Invention

[0003] The present disclosure relates to a verification apparatus and a verification method. More particularly, the present disclosure relates to a verification apparatus and a verification method for verifying qualities of touch display panels.

[0004] Description of Related Art

[0005] In a general process of manufacturing a display panel, one verification procedure is required to light up the display panel, so as to check the equality of the display panel. Currently, a usual verification approach for display panel includes connecting a common mode voltage signal (Vcom) to testing probes of the display panel and utilizing the Vcom signal to light up the display panel. However, aforesaid verification approach is not suitable for latest models of touch display panels.

SUMMARY

[0006] The disclosure provides a verification apparatus and a verification method for verification of touch display panels.

[0007] It is to be understood that both the foregoing general description and the following detailed description are by examples, and are intended to provide further explanation of the disclosure as claimed.

[0008] According to an embodiment of this disclosure, a verification apparatus suitable for touch display panel is proposed. The touch display panel includes multiple divided partitions. The verification apparatus includes signal generating circuit and verification switch circuit. The signal generating circuit is used to generate verification voltage. The verification switch circuit is used to simultaneously send the verification voltage to at least two of the multiple divided partitions, and includes multiple switch units which are coupled to divided partitions and signal generating circuit.

[0009] A verification method suitable for touch display panel is proposed according to another embodiment of this disclosure. The verification method includes simultaneously sending verification voltage to at least two of multiple divided partitions, light-emitting separately at least two divided partitions according to verification voltage, and judging whether the divided partition functions normally according to the light-emitting condition of the divided partition.

[0010] With the verification apparatus, verifications toward touch display panel can be conducted to light up the divided partitions, and to find whether adjacent divided partitions are short-connected or not.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The disclosure can be more fully understood by reading the following detailed description of the embodiment, with reference made to the accompanying drawings as follows:

[0012] FIG. **1** is a block diagram of a verification apparatus according to one embodiment of the disclosure;

[0013] FIG. **2** is a schematic diagram of a verification apparatus according to one embodiment of the disclosure;

[0014] FIG. **3**A is a flow chart of a verification method according to one embodiment of the disclosure;

[0015] FIG. **3**B is a flow chart of a verification method according to another embodiment of the disclosure;

[0016] FIG. **3**C is a flow chart of a verification method according to still another embodiment of the disclosure;

[0017] FIG. **4**A to FIG. **7**A and FIG. **4**B to FIG. **7**B are diagrams of verification apparatus according to different embodiments of the disclosure.

DETAILED DESCRIPTION

[0018] The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0019] Reference is made to FIG. **1**, which is a block diagram of a verification apparatus **100** suitable for touch display panel according to one embodiment of the disclosure. The verification apparatus **100** includes control circuit **110**, verification switch circuit **120**, and signal generating circuit **130**. The verification switch circuit **120** includes switch units (not shown in the figure). The signal generating circuit **130** is configured to generate verification voltage. The control circuit **110** is configured to adjust switch units for triggering the verification switch circuit **120**. The verification switch circuit **120** is triggered to send a verification voltage to divided partitions of touch display panel.

[0020] Reference is made to FIG. **2**, which is a schematic chart of a verification apparatus **100** suitable for touch display panel **200** according to one embodiment of the disclosure. The touch display panel **200** includes divided partitions **201**~**209**, which are separated from each others by non-conductive gaps. That is, the divided partitions **201**~**209** are not directly electrically connected to each others. The above mentioned divided partitions **201**~**209** serve as an explanatory example, and the disclosure is not limited to the divided partitions **201**~**209** shown in FIG. **2**. In other embodiments, the touch display panel **200** may include more or less divided partitions.

[0021] Each of the divided partitions **201**~**209** are different parts of the touch display panel **200**. In practices, various driving signals are required to control touch function and display function on a large-scale panel. Controlling the whole large-scale panel with one singular driving circuit leads to higher costs for implementing the powerful driving circuit, and also causes difference between response times on different rows/columns of pixels. In practical applica-

tions, the touch display panel **200** is often separated into multiple smaller divided partitions **201**~**209**, such that each divided partitions **201**~**209** will be easier to drive and control. Every single divided partitions **201**~**209** is connected to corresponding control circuit (not shown in the figure).

[0022] Each switch unit SW**1**~SW**9** in the verification switch circuit **120** is respectively connected to one corresponding divided partition. As shown in FIG. **2**, the verification switch circuit **120** includes the switch units SW**1**~SW**9**. The switch unit SW**1** is connected to divided partition **201**. The switch unit SW**2** is connected to divided partition **202**. Likewise, the switch units SW**3**~SW**9** are connected to divided partitions **203**~**209** respectively.

[0023] On the other hand, the switch units SW**1**~SW**9** of the verification switch circuit **120** are coupled to the signal generating circuit **130** on the other side. According to the control signal CS from the control circuit **110**, the verification switch circuit **120** sends verification voltage V**1** to the divided partitions **201**~**209**. Switch units SW**1**~SW**9** are manipulated according to the logic level of control signal CS.

[0024] Reference is made to FIG. **3**A, which is a flow chart illustrating a verification method **300** suitable for touch display panel **200** according to one embodiment of the disclosure. In step S**302**, the control signal CS generated by the control circuit **110** is adjusted to high-logic level. The switch units SW**1**~SW**9** in the verification switch circuit **120** is turned on and the verification voltage is sent from the signal generating circuit **130** to every divided partitions of touch display panel **200**. Based on the structure shown in FIG. **1**, when the control signal CS generated by the control circuit **110** is provided at high-logic level, the switch units SW**1**~SW**9** are turned on. The verification voltage V**1** generated by the signal generating circuit **130** is send through the switch units SW**1**~SW**9** to the divided partitions **201**~**209** divided partitions **201**~**209** receive the detection voltage V**1** correctly. If the divided partitions **201**~**209** receive the detection voltage V**1** correctly, the divided partitions **201**~**209** will be driven and lit up by the detection voltage V**1**. In aforesaid example, the verification voltage V**1** serves as driving voltage or source voltage for every divided partitions **201**~**209**.

[0025] Step S**304**, as shown in FIG. **1**, is performed to determine whether the touch display panel **200** is able to function normally according to a light-emitting condition of the touch display panel **200**. If the light-emitting condition indicates that touch display panel **200** is able to function normally, the method **300** performs step S**306** for adjusting the control signal CS generated by the control circuit **110** to low-logic level, such that the verification apparatus **100** will stop sending the verification voltage V**1** to the divided partition **201**~**209** of touch display panel **200**. The verification ends now and the divided partitions **201**~**209** will be controlled by another working circuit in the following step S**308**.

[0026] For instance, aforesaid working circuit includes a gate driving circuit (for displaying function), a data driving circuit, and a touch sensing circuit (for touch-sensing function). The gate driving circuit is configured to control transistor switches in divided partitions of the panel. When the transistor switches is on, data driving circuit sends the data that control gray scale and brightness to pixel capacitors in divided partitions of the panel. As mentioned above, since the control signal CS has been adjusted to low-logic level, the switch units SW**1**~SW**9** are turned off, and the verification apparatus **100** stop sending the verification voltage V**1** to touch display panel **200**, so as to terminates the verification. The verification apparatus **100** is separated from the whole touch display panel, and the verification apparatus **100** will no longer conduct any verification to the touch display panel **200**. The signal wirings connected to each divided partition will be used to send signals required by the working circuit, such as the gate driving circuit, the data driving circuit, and/or the touch sensing circuit.

[0027] Reference is made to FIG. **3**B for another instance. FIG. **3** is a flow chart of a verification method **301** suitable for the touch display panel **200** according to one embodiment of the disclosure. Comparing to the step S**304** of verification method **300** shown in FIG. **3**A, the verification method **301** shown in FIG. **3**B gives a further example about how to decide whether the touch display panel **200** is able to function normally or not. In the embodiment shown in FIG. **3**B, step S**304** determines whether the divided partitions **201**~**209** is able to function normally according to light emitting conditions of each divided partitions **201**~**209**. For example, step S**304** is configured to decide whether the divided partitions **201**~**209** are lit or not. If the divided partitions **201**~**209** are lit up, then the divided partitions **201**~**209** are regarded as functioning normally. If the divided partitions **201**~**209** are not lit, then the divided partitions **201**~**209** regards to be mal-functioned.

[0028] After the function is confirmed to be normal, in step S**306**, the control signal CS generated by the control circuit **110** is adjusted to low-logic level. Meanwhile, the switch units SW**1**~SW**9** in the verification switch circuit **120** is turned off, and the signal generating circuit **130** stop sending the verification voltage V**1** to the divided partitions **201**~**209** of the touch display panel **200**.

[0029] In other words, at the moment there is no signal transmission between the verification apparatus **100** and the divided partitions **201**~**209** of the touch display panel **200**. In the following step S**308**, the working circuit (not shown in the figure) will replace the verification apparatus **100**. The working circuit controls the divided partitions **201**~**209** of the touch display panel **200**. For example, the input and output interface of the working circuit can be connected to signal circuits of the divided partitions **201**~**209**.

[0030] In some embodiments, after the verification is finished, the signal wirings of each divided partitions **201**~**209** remain electrical connected to the verification apparatus **100**, but the switch units SW**1**~SW**9** in the verification switch circuit **120** will be turned off. Therefore, the signal generating circuit **130** will not affect the signal wirings of each divided partitions **201**~**209**. In some other embodiments, after the verification is finished, the electrical connections between the verification apparatus **100** and the signal circuits of each divided partitions **201**~**209** are removed/interrupted by laser cutting.

[0031] Reference is made to FIG. **3**C, which is a flow chart of a verification method **302** suitable for touch display panel according to still another embodiment of the disclosure. Comparing the verification method **302** shown in FIG. **3**C and the verification method **301** shown in FIG. **3**B, the flow of decision in the verification method **302** based on the light-emitting condition of divided partitions includes step S**304** and S**306**. Step S**304** is executed for deciding whether

the divided partition is lit. Step S306 is further executed for deciding whether two adjacent divided partitions display at the same brightness.

[0032] In the embodiment shown in FIG. **2**, the same verification voltage V1 is provided to two adjacent divided partitions. Even if the two adjacent divided partitions are lit, it still cannot be confirmed whether two adjacent divided partitions are short-connected or not.

[0033] To detect whether adjacent divided partitions or the signal wirings thereof are short-connected, different verification voltages are provided to the two adjacent divided partitions in some embodiments. If two adjacent divided partitions receive different verification voltages and display at different brightness, the two adjacent divided partitions are regarded as functioning normally. Two adjacent divided partitions suppose to receive different verification voltages by default and display at different brightness. However, when the divided partitions are short-connected, the divided partitions will receives the same verification voltage and display at the same brightness.

[0034] For instance, reference is made to FIG. **4**A to FIG. **7**A and FIG. **4**B to FIG. **7**B, which are diagrams of verification apparatus **100** suitable for touch display panel **200** according to different embodiments of the disclosure.

[0035] As shown in FIG. **4**A, a touch display panel **400** includes divided partitions **401~416**. Divided partitions **401**, **403**, **405**, **407**, **409**, **411**, **413**, **415** are arranged on odd rows of the touch display panel **400**, and divided partitions **402**, **404**, **406**, **408**, **410**, **412**, **414**, **416** are arranged on even rows of the **400**.

[0036] When the signal generating circuit **130** simultaneously sends the verification voltages V1 and V2 respectively to the divided partitions on the odd and even rows. The brightness of the divided partitions on the odd rows are the same, and the brightness of the divided partitions on the even rows are also the same but different from that of the odd rows.

[0037] In this situation, there is no short circuit between two vertical-adjacent divided partitions of the touch display panel **400**. Step S308 is executed to adjust the control signal CS generated by the control circuit **110** to low-logic level to turn off the switch units in the verification switch circuit **120**, then the verification voltages V1 and V2 will not be sent to the divided partitions **401~416** of the touch display panel **400**. Another circuit (that is, the working circuit) takes over the control of the divided partitions in step S310. However, in another situation as shown in FIG. **4**B, the divided partition **410** on the even row displays at the same brightness with the divided partitions **409** and **411** on the odd rows. It can be observed that there is a short circuit between divided partition **410** and divided partition **409** or **411**, and in this situation, the flow will return to step S302 to send the verification voltages V1 and V2 again to confirm the function of the touch display panel.

[0038] The above embodiment can be used to confirm whether there is a short circuit between the up and down adjacent divided partitions. Nonetheless, by this method, whether there is a short circuit between divided partitions in odd and even rows or between left and right adjacent divided partitions cannot be validated.

[0039] In another embodiment, as shown in FIG. **5**A, a touch display panel **400** includes divided partitions **401~416**. Divided partitions **401**, **402**, **403**, **404**, **409**, **410**, **411**, **412** are arranged on odd columns of the touch display panel **400**, and divided partitions **405**, **406**, **407**, **408**, **413**, **414**, **415**, **416** are arranged on even columns of the **400**.

[0040] When the signal generating circuit **130** simultaneously send the verification voltages V1 and V2 respectively to the divided partitions on the odd and even columns. The brightness of the divided partitions on the odd columns are the same, and the brightness of the divided partitions on the even columns are also the same but different from that of the odd columns.

[0041] In this situation the left and right adjacent divided partitions of the touch display panel **400** have no short circuit. However, in another situation as shown in FIG. **5**B, the divided partition **412** on the even column displays at the same brightness with the divided partitions **408** and **416** on the odd columns. It can be observed that there is a short circuit between divided partition **412** and divided partition **408** or **416**.

[0042] The above embodiment can be used to confirm whether there is a short circuit between the left and right adjacent divided partitions. Nonetheless, by this method, whether there is a short circuit between divided partitions in odd and even columns or between up and down adjacent divided partitions cannot be validated.

[0043] In still another embodiment, as shown in FIG. **6**A, a touch display panel **400** includes divided partitions **401~416**. Divided partitions **401**, **402**, **403**, **404**, **409**, **410**, **411**, **412** are arranged on odd columns of the touch display panel **400**, and divided partitions **405**, **406**, **407**, **408**, **413**, **414**, **415**, **416** are arranged on even columns of the **400**.

[0044] Comparing to FIG. **5**A and FIG. **5**B, in the embodiment shown in FIG. **6**A, the signal generating circuit **130** alternately sends the verification voltages to every two adjacent divided partitions on the odd columns via the circuit switch units in the verification switch circuit **120**. The so-called alternately sends the verification voltages to every two adjacent divided partitions indicates that, as shown in FIG. **6**A, for the divided partitions **401~404** in odd column, send verification voltages V1 and V2 to adjacent divided partitions **401** and **402**, and simultaneously send verification voltages V1 and V2 to adjacent divided partitions **403** and **404**. Namely, for the divided partitions **405~408** in even column, send verification voltages V2 and V1 to adjacent divided partitions **405** and **406**, and simultaneously send verification voltages V2 and V1 to adjacent divided partitions **407** and **408**.

[0045] At this moment any arbitrary adjacent divided partitions in odd and even columns receive different verification voltage. For example, the divided partition **401** on the odd column and the divided partition **405** on the even column receive verification voltages V1 and V2 respectively. The divided partition **402** on the odd column and the divided partition **406** on the even column receive verification voltages V2 and V1 respectively.

[0046] By the same method, alternately send the verification voltages V1 and V2 to the divided partitions **409~412** on the odd column, and alternately send the verification voltages V2 and V1 to the divided partitions **413~415** on the even column.

[0047] In this situation, as shown in FIG. **6**A, the brightness of an arbitrary divided partition on the odd or even column is different from its neighbors in four directions. If this is true, it can be confirmed that there is no short circuit between the divided partition and its neighbors in four directions.

[0048] For instance, the brightness of the divided partition **407** on the even column is different from the brightness of the divided partition **406** (i.e., the partition adjacent to the divided partition **407** on the top side) and the brightness of the divided partition **408** (i.e., the partition adjacent to the divided partition **407** on the bottom side). Moreover, the brightness of the divided partition **407** is different from the brightness of the divided partition **403** (i.e., the partition adjacent to the divided partition **407** on the left side) and the divided partition **411** (i.e., the partition adjacent to the divided partition **407** on the right side). Then there is no short circuit between the divided partition **407** and the divided partitions **406/408/403/411** in the neighborhood along four directions.

[0049] For another instance, the brightness of the divided partition **410** on the even column is different from the brightness of the upside/downside adjacent divided partitions **409** and **411**. Moreover, the brightness of the divided partition **410** is different from the brightness of the leftside/rightside adjacent divided partitions **406** and **414**. Then there is no short circuit between the divided partition **410** and the neighboring divided partitions **409**, **411**, **406**, and **414** in four directions.

[0050] In another situation, as shown in FIG. **6**B, the brightness of the divided partition **407** on even column is the same as the divided partitions **403** and **411** on odd column and the divided partitions **406** and **408** on even column. It can be judged that there is a short circuit between the divided partition **407** and one of the divided partitions **403**, **406**, **408**, and **411**. Comparing to the embodiments shown in FIG. **4**A to FIG. **4**B and FIG. **5**A to FIG. **5**B above, whether there is a short circuit between an arbitrary divided partition and the neighbors in four directions can be verified simultaneously in this embodiment.

[0051] When it is confirmed that the touch display panel functions normally and there is no short circuit, as mentioned above, in step S**306**, the control signal CS generated by the control circuit **110** is adjusted to low-logic level (such as 0). At this moment, the switch units in the verification switch circuit **120** is turned off, and the sending of verification voltages from the signal generating circuit **130** to the divided partitions **401**~**416** of the touch display panel **400** is stopped. In the following step S**208**, another circuit (which is the working circuit) will replace the verification apparatus **100**, and control the divided partitions **401**~**416** of the touch display panel **400** separately. The mechanism of how the working circuit controls touch display panel is the same as it is mentioned previously.

[0052] Comparing to the verification voltage V**1** and V**2** shown in FIG. **6**A, there are extra verification voltages V**3** and V**4** sent in the embodiment shown in FIG. **7**A. The signal generating circuit **130** sends verification voltages V**1**, V**2**, V**3**, and V**4** via the circuit switch units in the verification switch circuit **120** to four adjacent divided partitions on the odd column. That is, send the verification voltage V**1**, V**2**, V**3**, and V**4** to divided partitions **401**, **402**, **403**, and **404**. Also, send the verification voltage V**4**, V**1**, V**2**, and V**3** to divided partitions **405**, **406**, **407**, and **408**. In the same manner, send the verification voltage V**3**, V**4**, V**1**, and V**2** to divided partitions **409**, **410**, **411**, and **412**. Likewise, send the verification voltage V**2**, V**3**, V**4**, and V**1** to divided partitions **413**, **414**, **415**, and **416**.

[0053] Comparing to FIG. **6**A, as shown in FIG. **7**A, the same part is that the brightness of an arbitrary divided partition on the odd or even rows is different from the brightness of the neighbors in the four directions. But the unlike part is that when there is a short circuit in any arbitrary divided partition, the location of the short circuit can be found more clearly.

[0054] For example, as shown in FIG. **7**B, when the divided partition **407**, **406**, and **411** display at the same brightness, it can be concluded that there is a short circuit between the divided partition **407** and the divided partition **406** or **411**. Possibilities in other directions can be excluded.

[0055] The abovementioned locations of short circuits shown in FIG. **4**B to FIG. **7**B only serve as examples for explanation. Practically, short circuits can be found at any arbitrary divided partition on the touch display panel.

[0056] Based on the abovementioned contents and embodiments, this disclosure provides a verification apparatus. By using the verification apparatus, light-emitting verification and short circuit verification for the divided partitions of the touch display panel can be conducted.

[0057] Although the present disclosure has been described in considerable detail with reference to certain embodiments thereof, other embodiments are possible. Therefore, the spirit and scope of the appended claims should not be limited to the description of the embodiments contained herein.

[0058] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present disclosure without departing from the scope or spirit of the disclosure. In view of the foregoing, it is intended that the present disclosure cover modifications and variations of this disclosure provided they fall within the scope of the following claims.

What is claimed is:

1. A verification apparatus, suitable for a touch display panel comprising a plurality of divided partitions, the verification apparatus comprising:

a signal generating circuit configured to generate a first verification voltage; and

a verification switch circuit comprising a plurality of switch units, the switch units being coupled between the divided partitions and the signal generating circuit, the verification switch circuit being configured to send the first verification voltage simultaneously to at least two of the divided partitions.

2. The verification apparatus of claim **1**, further comprising:

a control circuit configured to generate a control signal for switching the switch units, wherein the switch units are turned on to send the first verification voltage simultaneously to at least two of the divided partitions in response to the control signal with logic-high level, the switch units are turned off and stopped from sending the first verification voltage in response to the control signal with logic-low level.

3. The verification apparatus of claim **1**, wherein the signal generating circuit further generates a second verification voltage, the divided partitions are arranged on odd columns or even columns, the switch units simultaneously send the first verification voltage to the divided partitions on the odd columns, the switch units simultaneously send the second verification voltage to the divided partitions on the even columns.

4. The verification apparatus of claim **1**, wherein the signal generating circuit further generates a second verification voltage, the divided partitions are arranged on odd

rows or even rows, the switch units simultaneously send the first verification voltage to the divided partitions on the odd rows, the switch units simultaneously send the second verification voltage to the divided partitions on the even rows.

5. The verification apparatus of claim **1**, wherein the signal generating circuit further generates a second verification voltage, the divided partitions are arranged on odd columns or even columns, the switch units alternatively send the first verification voltage and the second verification voltage to every two adjacent divided partitions on the odd columns, the switch units alternatively send the second verification voltage and the first verification voltage to every two adjacent divided partitions on the even columns.

6. A verification method, suitable for a verification apparatus, the verification apparatus is configured to detect a touch display panel comprising a plurality of divided partitions, the verification method comprising:

the verification apparatus simultaneously sends a first verification voltage to at least two of the divided partitions; and

the first verification voltage provided by the verification apparatus separately light at least two of the divided partitions, wherein the light-emitting condition of the at least two of the divided partitions is configured to decide whether the at least two of the divided partitions function normally.

7. The verification method of claim **6**, further comprising:

in response to any one of the at least two of the divided partitions is lit, the verification apparatus decides that the lit divided partition functions normally; and

in response to any one of the at least two of the divided partitions is not lit, the verification apparatus decides that the not lit divided partition does not function normally.

8. The verification method of claim **7**, wherein the at least two divided partitions comprises a first divided partition and a second divided partition adjacent to each other, the verification apparatus separately sends the first verification voltage and the second verification voltage to the first divided partition and the second divided partition, the verification apparatus decides that there is a short circuit between the first divided partition and the second divided partition when the brightness of the first divided partition and the second divided partition are the same.

9. The verification method of claim **7**, wherein the divided partitions comprise a plurality of divided partitions on odd columns and a plurality of divided partitions on even columns, the verification method further comprising:

the verification apparatus sends the first verification voltage to the divided partitions on odd columns, and simultaneously sends a second verification voltage to the divided partitions on even columns.

10. The verification method of claim **7**, wherein the verification apparatus generates a second verification voltage, the divided partitions comprise a plurality of divided partitions on odd columns and a plurality of divided partitions on even columns, the verification apparatus alternately sends the first verification voltage and the second verification voltage to every adjacent two of the divided partitions on odd columns, the verification apparatus alternately sends the second verification voltage and the first verification voltage to every adjacent two of the divided partitions on even columns.

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