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(54) **DIGITAL PHASE LOCKED LOOP FREQUENCY ESTIMATION**

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(57) **ABSTRACT**

A Digital Phase Locked Loop (DPLL), including a Time-to-Digital Converter (TDC) configured generate quantized phase values of a Voltage Controlled Oscillator (VCO) signal; and a frequency estimation circuit configured to receive the quantized phase values, determine wraparound phase of the quantized phase values, and least-squares estimate a frequency based on the quantized phase values and the wraparound phase.

100
Communication Device

110
Digital Baseband Processor

112
DPLL

120
RF Front End

122
DPLL

130 Antenna

Figure 1

100
Communication Device

110
Digital Baseband Processor

112
DPLL

120
RF Front End

122
DPLL

130 Antenna

Figure 2

200
DPLL

Reference Frequency Oscillator

ref. signal

210
Time-to-Digital Converter (TDC)

220
Frequency Estimation Circuit

230
VCO

Figure 3

Figure 4

400

Setting a constant tuning voltage of a Voltage Controlled Oscillator (VCO) using an open control loop — 410

Least-squares estimating a frequency based on quantized phase values and a wraparound phase of a VCO signal — 420

Determining a tuning voltage offset of the VCO based on the estimated frequency — 430

Updating the tuning voltage of the VCO to compensate for the tuning voltage offset — 440

Resetting loop filter memories of the VCO — 450

Dynamically updating the tuning voltage of the VCO using a closed control loop — 460

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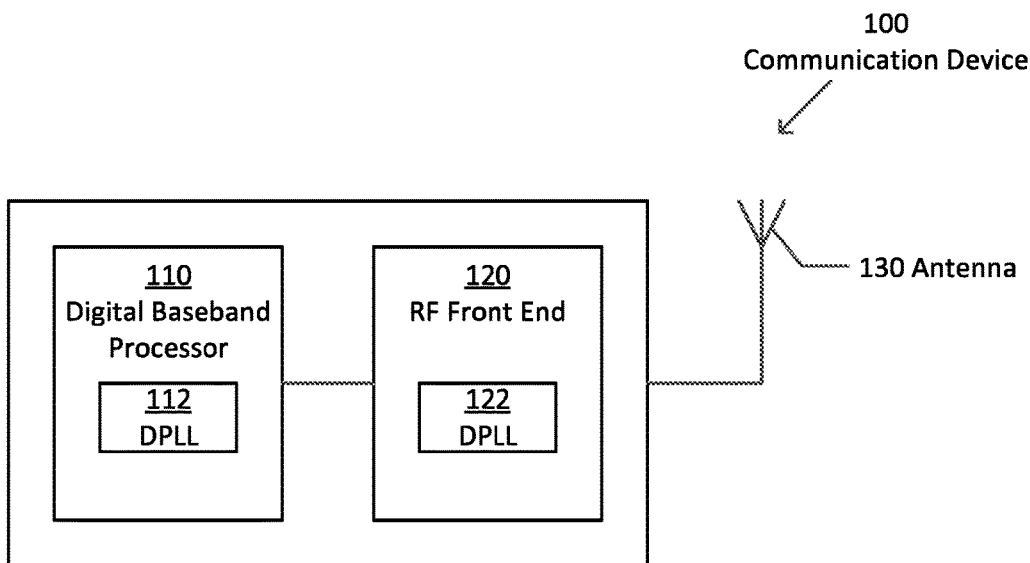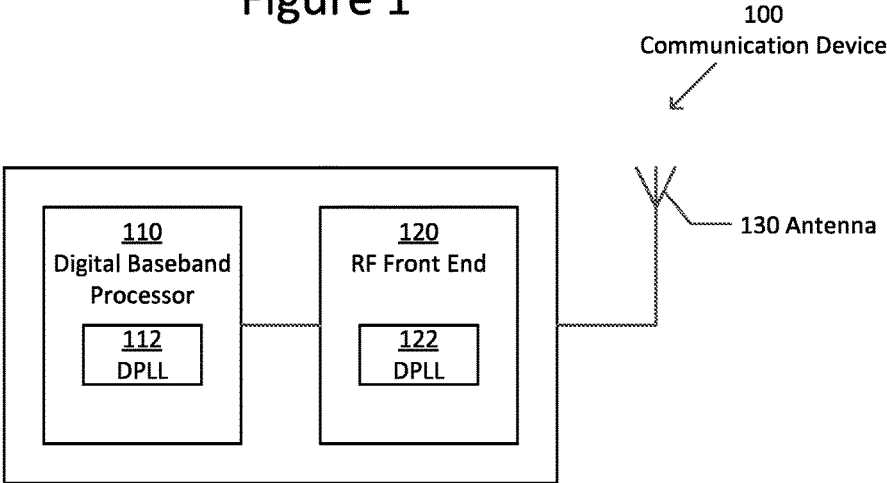
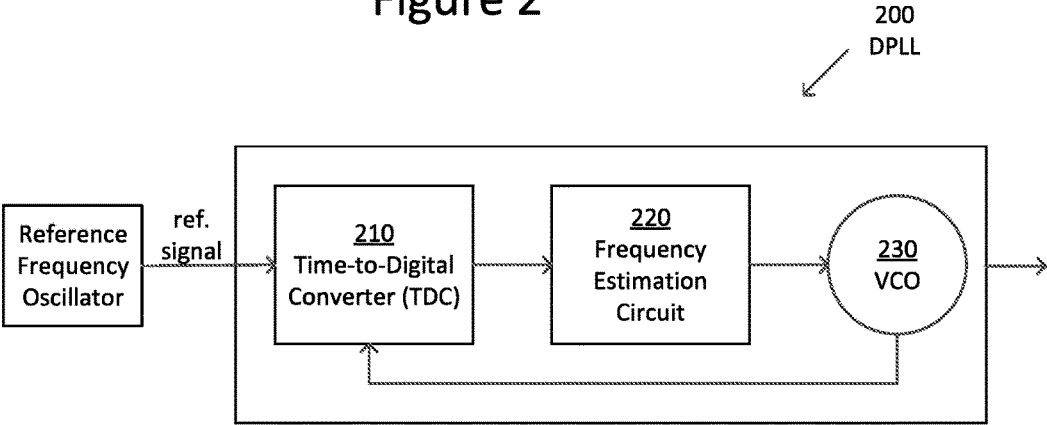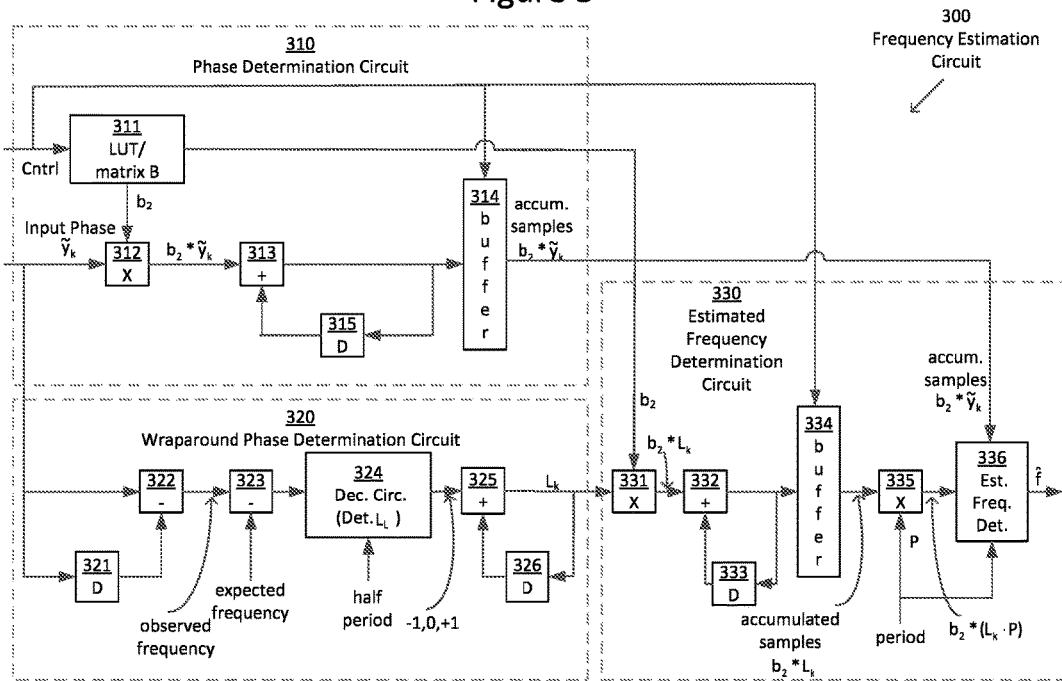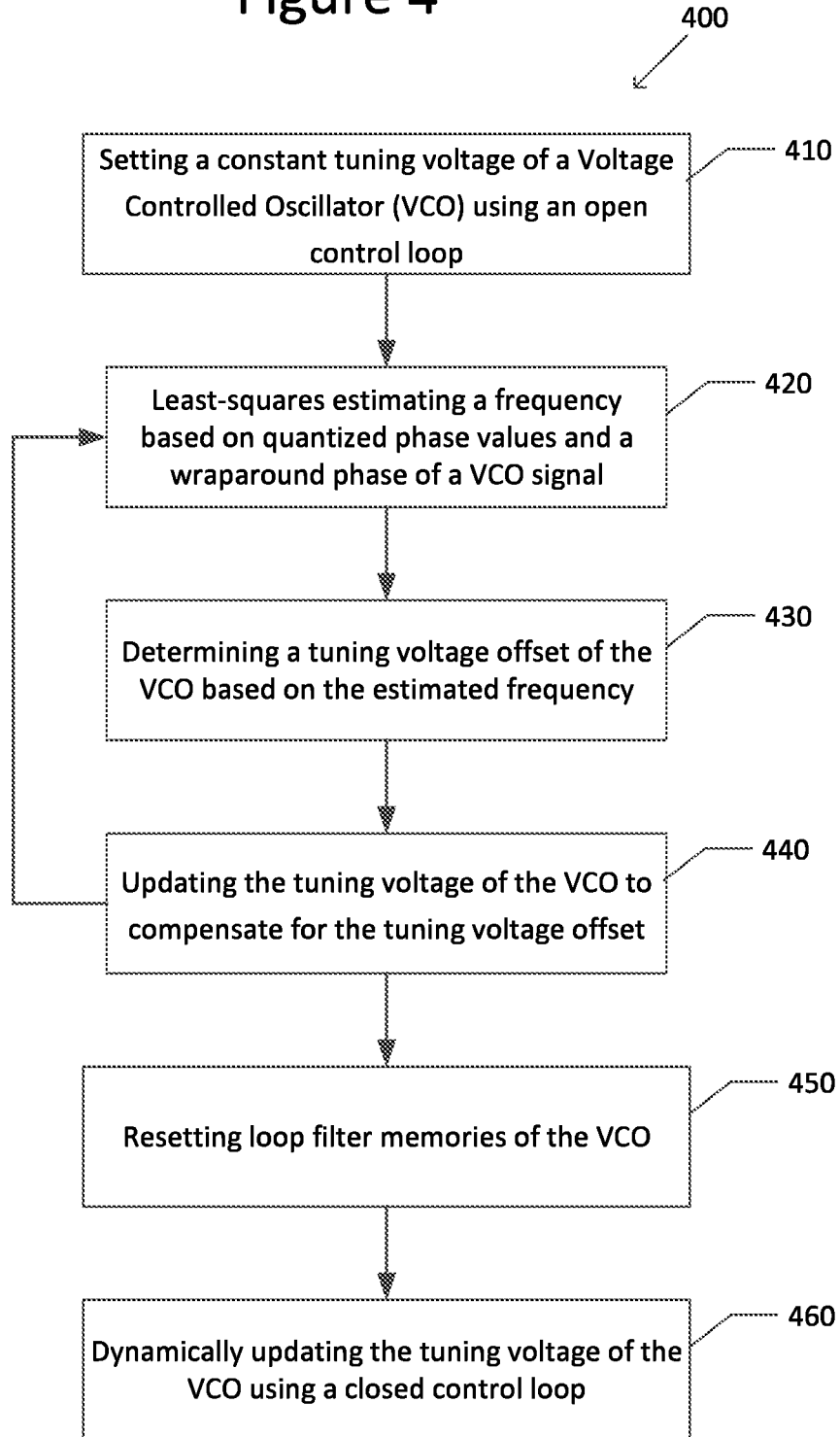## DIGITAL PHASE LOCKED LOOP FREQUENCY ESTIMATION

TECHNICAL FIELD

[0001]   The present disclosure relates to frequency estimation in a Digital Phase Locked Loop (DPLL).

BACKGROUND

[0002]   Digital Phase Locked Loops (DPLLs) provide a low-power, small-area solution relative to analog PLLs. In a DPLL, a phase offset between a Voltage Controlled Oscillator (VCO) and a reference clock is measured by a Time-to-Digital Convertor (TDC). The measured phase is then compared with a required phase, and the result is used to correct the VCO frequency. Even though the DPLL is a phase-locked loop, knowing the frequency would be useful for many functions, such as fast PLL locking and band calibration.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003]   FIG. 1 illustrates a communication device comprising an exemplary DPLL in accordance with an exemplary aspect of the disclosure.

[0004]   FIG. 2 illustrates a DPLL in accordance with an exemplary aspect of the disclosure.

[0005]   FIG. 3 illustrates a frequency estimation circuit in accordance with an exemplary aspect of the disclosure.

[0006]   FIG. 4 illustrates a flowchart 400 of an exemplary method of DPLL fast locking using the frequency estimation circuit of FIG. 3.

DESCRIPTION OF THE ASPECTS

[0007]   The present disclosure is directed to a faster frequency estimation in a Digital Phase Locked Loop (DPLL). The digital domain of the PLL allows implementation of Least-Square (LS) estimation for maximum accuracy based on a minimum number of samples. More specifically, a frequency estimation circuit configured to receive quantized phase values of a Voltage Controlled Oscillator (VCO) signal, determine wraparound phase of the quantized phase values, and least-squares estimate a frequency based on the quantized phase values and the wraparound phase.

[0008]   FIG. 1 illustrates a communication device 100 comprising an exemplary DPLL in accordance with an aspect of the disclosure. The communication device 100 may comprise, for example, a tablet computer, a netbook, a notebook computer, a laptop computer, mobile phone, a cellular phone, a smartphone, a personal digital assistant, a multimedia playback device, a digital music player, a digital video player, a navigational device, a digital camera, or the like.

[0009]   The communication device 100 comprises a digital baseband processor 110, a Radio Frequency (RF) front end 120, and an antenna 130, among other elements not shown. The digital baseband processor 110 may comprise an exemplary DPLL 112. Similarly, the RF front end 120 may comprise an exemplary DPLL 122. The RF front end 120 is coupled between the digital baseband processor 110 and the antenna 130.

[0010]   FIG. 2 illustrates a DPLL 200 in accordance with an exemplary aspect of the disclosure.

[0011]   The DPLL 200 may be configured to generate an output signal whose phase is related to the phase of the input signal. A particular application of this, for example, is with regard to tuning to different carrier frequencies during communication between communication devices 100.

[0012]   The DPLL 200 comprises a Time-to-Digital Converter (TDC) 210, a frequency estimation circuit 220, and a Voltage Controlled Oscillator (VCO) 230.

[0013]   The TDC 210 is configured to measure time intervals of a signal of the VCO 230 and generate quantized phase values. In a closed-loop control scenario, the TDC 210 is configured to receive a reference signal from a reference frequency oscillator and a feedback signal from the VCO 230; the TDC 210 measure a times difference between the reference signal and the feedback signal.

[0014]   The frequency estimation circuit 220 is configured to receive the quantized phase values from the TDC 210. The quantized phase values have a modulo nature, that is, wraparound phase.

[0015]   The TDC 210 samples the phase of the VCO signal every clock cycle of a reference frequency oscillator. For any reference frequency (e.g., 80 MHz), if the VCO frequency is an integer multiplication of it (e.g., 8 GHz=100*80 MHz),—at every sample this is a constant phase; so the VCO signal frequency is 100 times the reference frequency. On the other hand, if the frequency of the VCO signal is a fraction (e.g., 8.008 GHz=100.1*80 MHz), than for each successive sample there is a phase increase of 10%. This phase increase of 10% can be translated into an estimated frequency offset. The frequency estimation circuit 220 measures the phase ramp, that is, how much the phase changes, and determines the VCO frequency based on this phase ramp. If the phase is linear line, the only difference in phase is that it wraps around every cycle (i.e., 2π).

[0016]   The frequency estimation circuit 220 is further configured to determine the wraparound phase of the quantized phase values, and then least-squares estimate a frequency based on the quantized phase values and the wraparound phase. The frequency estimation is performed in an open loop. The frequency is a slope of the quantized phase values, or samples, and thus least-squares estimation can be applied to the quantized phase values to determine the frequency.

[0017]   Again, the TDC 210 is configured to measure the VCO phase. The units of the measured phase are not radians. The units are relative to a period, and a period is defined as the TDC value which matches a full cycle (2π).

[0018]   A constant frequency corresponds with a linear-phase in accordance with:

$$\varphi_k = \varphi_0 + f \cdot k, \qquad \text{(Equation 1)}$$

where φ_k is a phase at sample k in radians, φ_0 is an unknown starting phase in radians, f is the frequency to be estimated, and k is an index of the sample. The phase is measured in radian due to the characteristics of the TDC 210.

[0019]   As mentioned above, the phase is observed in units relative to a period of the VCO signal. Equation 1, which is in radians, may be converted to periods, as represented as:

$$\theta_k = \theta_0 + f \cdot P \cdot k, \qquad \text{(Equation 2)}$$

where θ_k is a phase at quantized phase value (sample) k, θ_0 is an unknown starting phase, and P is a threshold proportional to a period of the VCO signal. A period P represents 2π, that is, a full cycle. The difference between Equation 1 (with φ_k) and Equation 2 (with θ_k), respectively, is the units.

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[0020] When noise ε_k is added, the observed phase at sample k, without modulo (i.e., wraparound phase), is:

$$y_k := \theta_0 + f \cdot P \cdot k + \varepsilon_k, \text{ for } k=1 \ldots N. \qquad \text{(Equation 3)}$$

[0021] Due to a limited dynamic range of the TDC **210**, the phase ramp has modulo, that is, wraparound phase. This is because the TDC **210** can only measure the phase between 0 and 2π (a period). The observed phase $\tilde{y}_k$ at sample k with modulo or wraparound phase of the VCO **230** is observed as follows:

$$\tilde{y}_k := \text{mod}(\theta_0 + f \cdot P \cdot k + \varepsilon_k, P), \text{ for } k=1 \ldots N. \qquad \text{(Equation 4)}$$

[0022] As mentioned above, the frequency f is the slope of the phase. If the noise is Gaussian and independent and identically distributed, there is a known Least-Squares(LS)/ Maximum Likelihood solution for determining the estimated frequency $\hat{f}$:

$$\hat{f}_{LS} := \underbrace{[A^T \cdot A]^{-1} \cdot A^T}_{B} \cdot y, \qquad \text{(Equation 5)}$$

$$\text{where } A := \begin{bmatrix} 1 & 1 \\ \vdots & \vdots \\ 1 & N \end{bmatrix}, \, y := \begin{bmatrix} y_1 \\ \vdots \\ y_N \end{bmatrix},$$

A^T is the transverse of matrix A, and B is a predefined matrix. B in the equation is defined by what is above it, that is, $[A^T \cdot A]^{-1} \cdot A^T$. A is predefined, and thus B is known.

[0023] The second term of the 2×1 vector B·y is the estimated frequency y. For implementation purposes, only the second term of the predefined matrix B is used, and can be stored in a memory (e.g., ROM); this is a 1×N vector. The multiplication is performed term-by-term, meaning that there is no need to buffer each of the samples/quantized values; only an accumulated value needs to be stored after each sample.

[0024] Described above is the classic solution, but it does not take into consideration modulo/wraparound phase. Due to wraparound phase, the actual observed phase with modulo is:

$$\tilde{y}_k := \text{mod}(\theta_0 + f \cdot P \cdot k + \varepsilon_k, P). \qquad \text{(Equation 6)}$$

[0025] Equation 6 may alternatively be written as:

$$\tilde{y}_k := \theta_0 + f \cdot P \cdot k + \varepsilon_k - L_k \cdot P, \qquad \text{(Equation 7)}$$

where L is a number of wraparounds. It is easy to detect the wraparounds with accuracy by comparing a difference between a currently observed quantized phase value φ_k and a previous quantized phase value φ_{k-1} with an expected frequency f_{exp}. Counting these occurrences produces L as follows:

$$L_l = \begin{cases} -1, & (\varphi_k - \varphi_{k-1}) - f_{exp} & < -P/2 \\ 0, & \text{else} \\ 1, & (\varphi_k - \varphi_{k-1}) - f_{exp} & > P/2 \end{cases}, \, L = \sum_{l=1}^{L} L_l. \qquad \text{(Equation 8)}$$

[0026] The phase y_k can be broken into two parts:

$$y_k = \tilde{y}_k + L_k \cdot P, \qquad \text{(Equation 9)}$$

where y_k is the observed phase without modulo/wraparound phase, $\tilde{y}_k$ is the observed phase with modulo/wraparound phase, and $L_k \cdot P$ is the modulo wraparound phase. Once wraparound-counter L is determined, and period P is known, then the phase without the modulo/wraparound phase can be determined; then the classic solution for $\hat{f}_{LS}$ described above can be used.

[0027] Thus, the estimated frequency $\hat{f}$, which eliminates the modulo/wraparound phase, is:

$$\hat{f} = b_2 * y_k = b_2 * \tilde{y}_k + b_2 * (L_k \cdot P), \qquad \text{(Equation 10)}$$

where b_2 is a second column of the matrix B. Matrix B has two vectors, one vector b_1 to estimate the initial phase, and the other vector b_2 to estimate the phase ramp, which is the frequency. This calculation can be done on a sample-by-sample basis without a need to store each of the samples; only an accumulated value needs to be stored after each sample. Also, the multiplication of the second term by period P can be done at the end of the calculations. In such a case where period P needs to be estimated, this estimation can be done in parallel to the calculations. Only a coarse initial estimation of period P is needed for calculating a number of wraparounds L, as described above.

[0028] FIG. **3** illustrates an exemplary frequency estimation circuit **300** to implement the frequency estimation described above. This frequency estimation circuit **300** is an example of the frequency estimation circuit **220** of FIG. **2**.

[0029] The frequency estimation circuit **300** comprises a phase determination circuit **310**, a wraparound phase determination circuit **320**, and an estimated frequency determination circuit **330**.

[0030] The phase determination circuit **310** is configured to determine an accumulation of the quantized phase values/ samples $b_2 * \tilde{y}_k$ including the wraparound phase. The phase determination circuit **310** comprises a Look-Up-Table (LUT) or matrix B **311**, a multiplier **312**, an accumulator **313**, an accumulated samples buffer **314**, and a delay **315**.

[0031] The multiplier **312** is configured to multiply the observed input phase $\tilde{y}_k$ by a second vector b_2 of matrix B, and output the product $b_2 * \tilde{y}_k$, which is the phase ramp or frequency, which includes modulo or wraparound phase. Regarding the notation, the "*" symbol is a multiplication operation of a vector by a vector on a sample-by-sample basis.

[0032] The accumulator **313** and the delay **315** are configured to perform cumulative-summation of the output values $b_2 * \tilde{y}_k$. The accumulated total is then stored in buffer **314**; this result is the first portion of Equation 10 above. As previously mentioned, it is not necessary to store individuals ones of the samples, only the accumulated result.

[0033] The wraparound phase determination circuit **320** is configured to determine the wraparound phase of the quantized phase values. The wraparound phase determination circuit **320** comprises a delay **321**, a derivative **322**, a subtractor **323**, decision circuit **324**, an accumulator **325**, and a delay **326**.

[0034] The derivative **322** is configured to determine a derivative of the observed input phase $\tilde{y}_k$ using the current observed phase and a previously observed input phase $\tilde{y}_{k-1}$ received from the delay **321**, to determine the ramp of the input phase $\tilde{y}_k$. In other words, the derivative **322** is configured to determine the observed frequency ($\varphi_k - \varphi_{k-1}$, as in Equation 8 above).

[0035] The subtractor **323** is configured to subtract an expected frequency from the observed frequency received from the derivative **322**, as in Equation 8 discussed above, and output a result to the decision circuit **324**.

[0036] The decision circuit 324 is configured to compare the result from the subtractor 323 with a half period P/2, as in Equation 8 discussed above. If the subtractor 323 result is less than –P/2, then the current value of the wraparound L_l is –1. On the other hand, if the subtractor 323 result is greater than P/2, then the current value of the wraparound L_l is 1. Otherwise, there is no wraparound in either the positive or negative direction, and the current value of L_l is 0. The value of the period P here does not need to be accurate, and may instead be estimated roughly.

[0037] The accumulator 325 and the delay 326 are configured to perform cumulative-summation of the wraparound values L_l for each of the samples, and output the accumulated wraparound values L_k.

[0038] The estimated frequency determination circuit 330 is configured to determine the estimated frequency by removing the wraparound phase L_k from the quantized phase values $b_2 * \tilde{y}_k$. The estimated frequency determination circuit 330 comprises a multiplier 331, an accumulator 332, a delay 333, an accumulated wraparound values buffer 334, a multiplier 335, and an estimated frequency determiner 336.

[0039] The multiplier 331 is configured to multiply the accumulated wraparound values L_k of quantized phase value k by the second vector b_2 of matrix B, and output result $b_2 * L_k$.

[0040] The accumulator 332 and the delay 333 are configured to perform cumulative-summation of the output values $b_2 * L_k$, and then store the accumulated total in the accumulated wraparound values buffer 334. The delay 333 configured to merely provide the accumulator 332 with time to perform its functions.

[0041] The multiplier 335 is configured to multiple the accumulated wraparound values $b_2 * L_k$ by the period P and output the result; this result is the second portion of Equation 10 above $b_2 * (L_k \cdot P)$. The period P may be estimated in parallel to the calculations of the quantized phase values, and then used with the multiplier 335. The value of P used with the determination circuit 324 earlier in the process is not need to be accurate, and thus a rough estimate was sufficient. For this multiplication by multiplier 335, the value of the period P may be more accurately estimated.

[0042] Finally, the estimated frequency determiner 336 is configured to combine the multiplier 335 output $b_2 * (L_k \cdot P)$ with the accumulated samples output $b_2 * \tilde{y}_k$ from sample buffer 314, as in Equation 10 above, to determine an estimated frequency $\hat{f}$ which has the modulo/wraparound taken into consideration. The estimated frequency determiner 336 is also configured to translate the units of the estimated frequency $\hat{f}$ as necessary.

[0043] FIG. 4 illustrates a flowchart 400 of a method of DPLL fast locking using the frequency estimation circuit 300 of FIG. 3.

[0044] In Step 410, a constant tuning voltage, V-tune, of a VCO 230 is set using an open control loop. An open control loop is when there is no feedback control loop with an error to correct an offset of the tuning voltage V-tune.

[0045] In Step 420, a frequency is least-squares estimated based on quantized phase values and a wraparound phase of a VCO signal, as described above with respect to FIG. 3. This is an open loop.

[0046] In Step 430, an offset of the tuning voltage V-tune is determined using an estimated gain K of the VCO.

[0047] In Step 440, the tuning voltage, V-tune, is updated.

[0048] Steps 420-440 may be repeated any number of times as suitable for the intended purpose. For example, if the VCO gain estimation is inaccurate, it will cause an inaccurate V-tune correction-step. With each loop step, the residual error will decrease exponentially.

[0049] In Step 450, loop filter memories (not shown) of the VCO are reset.

[0050] In Step 460, the control loop is closed. More specifically, the tuning voltage value K-VCO of the VCO is dynamically updated using a closed control loop with error feedback.

[0051] Using multiple iterations, where K>1, is useful in a case of a VCO gain (K-VCO) mismatch. Error in the estimated VCO gain results in a frequency error that is proportional to the tuning voltage value V-tune step size. Using multiple iterations results in a final frequency error proportional to the last tuning voltage value V-tune correction step-size, which, in the last iteration, should be small.

[0052] The frequency estimation of this disclosure has many advantages over previous solutions. For example, previous analog counters count a number of VCO/DCO cycles in a predefined time window, but with limited quantization and a long time for high accuracy. Digital phase derivative averaging is simpler, but requires twice as many samples to reach the same accuracy.

[0053] The fast frequency estimation in accordance with the present disclosure allows for fast DPLL locking. This faster DPLL locking is important for processes such as band switching and channel scanning, thereby allowing more time for initial calibrations.

[0054] A previous solution for fast loop locking is gear-shifting, which involves locking in a closed loop while changing the loop bandwidth. This approach is limited by a loop delay, so there is slower convergence. Also, changing the filter on-the-run is sub-optimal due to un-updated internal memories.

[0055] The term "circuit" shall be understood to be circuit (s), processor(s), logic, or a combination thereof. For example, a circuit can include an analog circuit, a digital circuit, state machine logic, other structural electronic hardware, or a combination thereof. In one or more of the exemplary aspects described herein, a circuit can include memory that stores data and/or instructions. The memory can be any well-known volatile and/or non-volatile memory, including, for example, Read Only Memory (ROM), Random Access Memory (RAM), flash memory, a magnetic storage media, an optical disc, erasable programmable read only memory (EPROM), and Programmable Read Only Memory (PROM). The memory can be non-removable, removable, or a combination of both.

[0056] The following examples pertain to further embodiments.

[0057] Example 1 is a Digital Phase Locked Loop (DPLL), comprising: a Time-to-Digital Converter (TDC) configured generate quantized phase values of a Voltage Controlled Oscillator (VCO) signal; and a frequency estimation circuit configured to receive the quantized phase values, determine wraparound phase of the quantized phase values, and least-squares estimate a frequency based on the quantized phase values and the wraparound phase.

[0058] In Example 2, the subject matter of Example 1, wherein the frequency estimation circuit comprises: a phase determination circuit configured to determine an accumulation of the quantized phase values with the wraparound phase.

[0059] In Example 3, the subject matter of Example 1, wherein the frequency estimation circuit comprises: a wraparound phase determination circuit configured to determine the wraparound phase of the quantized phase values.

[0060] In Example 4, the subject matter of Example 3, wherein the wraparound phase determination circuit comprises a decision circuit configured to determine the wraparound phase by comparing a difference between a current quantized phase value and a previous quantized phase value with an expected frequency.

[0061] In Example 5, the subject matter of Example 4, wherein the decision circuit determines wraparound phase in accordance with the following:

$$L_l = \begin{cases} -1, & (\varphi_k - \varphi_{k-1}) - f_{exp} & < -P/2 \\ 0, & \text{else} \\ 1, & (\varphi_k - \varphi_{k-1}) - f_{exp} & > P/2 \end{cases}, \quad L = \sum_{l=1}^{L} L_l,$$

where L is an accumulated number of phase wraparounds, φ_k is the current quantized phase value, φ_{k-1}, is the previous quantized phase value, f_{exp} is the expected frequency, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

[0062] In Example 6, the subject matter of Example 5, further comprising: an estimated frequency determination circuit configured to determine the estimated frequency by removing the wraparound phase from the quantized phase values.

[0063] In Example 7, the subject matter of Example 5, wherein a value of the period used in the wraparound phase determination is an estimate of the period of the VCO signal.

[0064] In Example 8, the subject matter of Example 1, wherein the estimated frequency is represented as follows: $\hat{f}=b_2{}^*y_k=b_2{}^*\tilde{y}_k+b_2{}^*(L_k\cdot P)$, where $\hat{f}$ is the estimated frequency, b_2 is a predetermined matrix, * is a multiplication operation of a vector by a vector, y_k is a quantized phase value without wraparound phase, $\tilde{y}_k$ is a quantized phase value with wraparound phase, L_k is an accumulated number of phase wraparounds, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

[0065] In Example 9, the subject matter of Example 1, wherein the frequency estimation circuit is configured to estimate the frequency on a quantized phase value-by-quantized phase value basis.

[0066] In Example 10, the subject matter of Example 1, wherein the quantized phase values are in units relative to a period of the VCO signal.

[0067] Example 11 is a wireless communication device, comprising: a baseband processor comprising the subject matter of Example 1, or a Radio Frequency (RF) front end comprising the subject matter of Example 1.

[0068] Example 12 is a method of operating a Digital Phase Locked Loop (DPLL), the comprising: generating, by a Time-to-Digital Converter (TDC) quantized phase values of a Voltage Controlled Oscillator (VCO) signal; determining, by a frequency estimation circuit, wraparound phase of

the quantized phase values; and least-squares estimating, by the frequency estimation circuit, a frequency based on the quantized phase values and the wraparound phase.

[0069] In Example 13, the subject matter of Example 12, wherein the least-squares estimating comprises: determining, by a phase determination circuit, an accumulation of the quantized phase values with the wraparound phase.

[0070] In Example 14, the subject matter of Example 12, wherein the least-squares estimating comprises: determining, by a wraparound phase determination circuit, the wraparound phase of the quantized phase values.

[0071] In Example 15, the subject matter of Example 14, wherein the wraparound phase determining comprises: determining, by a decision circuit, the wraparound phase by comparing a difference between a current quantized phase value and a previous quantized phase value with an expected frequency.

[0072] In Example 16, the subject matter of Example 15, wherein the determining the wraparound phase is in accordance with the following:

$$L_l = \begin{cases} -1, & (\varphi_k - \varphi_{k-1}) - f_{exp} & < -P/2 \\ 0, & \text{else} \\ 1, & (\varphi_k - \varphi_{k-1}) - f_{exp} & > P/2 \end{cases}, \quad L = \sum_{l=1}^{L} L_l,$$

where L is an accumulated number of phase wraparounds, φ_k is the current quantized phase value, φ_{k-1}, is the previous quantized phase value, f_{exp} is an expected frequency, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

[0073] In Example 17, the subject matter of Example 12, wherein the least-squares frequency estimating circuit comprises: determining, by an estimated frequency determination circuit, the estimated frequency by removing the wraparound phase from the quantized phase values.

[0074] In Example 18, the subject matter of Example 16, wherein a value of the period used in the wraparound phase determination is an estimate of the period of the VCO signal.

[0075] In Example 19, the subject matter of Example 12, wherein the estimated frequency is represented as follows: $\hat{f}=b_2{}^*y_k=b_2{}^*\tilde{y}_k+b_2{}^*(L_k\cdot P)$, where $\hat{f}$ is the estimated frequency, b_2 is a predetermined matrix, * is a multiplication operation of a vector by a vector, y_k is a quantized phase value without wraparound phase, $\tilde{y}_k$ is a quantized phase value with wraparound phase, L_k is an accumulated number of phase wraparounds, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

[0076] In Example 20, the subject matter of Example 12, wherein the least-squares frequency estimating comprising: estimating the frequency on a quantized phase value-by-quantized phase value basis.

[0077] In Example 21, the subject matter of Example 12, wherein the quantized phase values are in units relative to a period of the VCO signal.

[0078] Example 22 is a method of fast locking a Digital Phase Locked Loop (DPLL), comprising: setting a constant tuning voltage of a Voltage Controlled Oscillator (VCO) using an open control loop; least-squares estimating a frequency based on quantized phase values and a wraparound phase of a VCO signal; determining a tuning voltage offset

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of the VCO based on the estimated frequency; and updating the tuning voltage of the VCO to compensate for the tuning voltage offset.

[0079] In Example 23, the subject matter of Example 22, after updating the tuning voltage of the VCO, further comprising: resetting filter memories of the VCO; and dynamically updating the tuning voltage of the VCO using a closed control loop.

[0080] Example 24 is a Digital Phase Locked Loop (DPLL), comprising: a Time-to-Digital Converter (TDC) configured generate quantized phase values of a Voltage Controlled Oscillator (VCO) signal; and a frequency estimation means for receiving the quantized phase values, determining wraparound phase of the quantized phase values, and least-squares estimating a frequency based on the quantized phase values and the wraparound phase.

[0081] In Example 25, the subject matter of Example 24, wherein the frequency estimation means comprises: a phase determination mean for determining an accumulation of the quantized phase values with the wraparound phase.

[0082] In Example 26, the subject matter of Example 24, wherein the frequency estimation means comprises: a wraparound phase determination means for determining the wraparound phase of the quantized phase values.

[0083] In Example 27, the subject matter of Example 26, wherein the wraparound phase determination means comprises a decision means for determining the wraparound phase by comparing a difference between a current quantized phase value and a previous quantized phase value with an expected frequency.

[0084] In Example 28, the subject matter of Example 27, wherein the decision means is further for determining wraparound phase in accordance with the following:

$$L_l = \begin{cases} -1, (\varphi_k - \varphi_{k-1}) - f_{exp} & < -P/2 \\ 0, & \text{else} \\ 1, (\varphi_k - \varphi_{k-1}) - f_{exp} & > P/2 \end{cases}, L = \sum_{l=1}^{L} L_l,$$

where L is an accumulated number of phase wraparounds, φ_k is the current quantized phase value, φ_{k-1}, is the previous quantized phase value, f_{exp} is the expected frequency, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

[0085] In Example 29, the subject matter of Example 28, further comprising: an estimated frequency determination means for determining the estimated frequency by removing the wraparound phase from the quantized phase values.

[0086] In Example 30, the subject matter of Example 28, wherein a value of the period used in the wraparound phase determination is an estimate of the period of the VCO signal.

[0087] In Example 31, the subject matter of Example 24, wherein the estimated frequency is represented as follows: $\hat{f} = b_2 * y_k = b_2 * \tilde{y}_k + b_2 * (L_k \cdot P)$, where $\hat{f}$ is the estimated frequency, b_2 is a predetermined matrix, * is a multiplication operation of a vector by a vector, y_k is a quantized phase value without wraparound phase, $\tilde{y}_k$ is a quantized phase value with wraparound phase, L_k is an accumulated number of phase wraparounds, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

[0088] In Example 32, the subject matter of Example 24, wherein the frequency estimation means is further for estimating the frequency on a quantized phase value-by-quantized phase value basis.

[0089] In Example 33, the subject matter of Example 24, wherein the quantized phase values are in units relative to a period of the VCO signal.

[0090] While the foregoing has been described in conjunction with exemplary aspect, it is understood that the term "exemplary" is merely meant as an example, rather than the best or optimal. Accordingly, the disclosure is intended to cover alternatives, modifications and equivalents, which may be included within the scope of the disclosure.

[0091] Although specific aspects have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific aspects shown and described without departing from the scope of the present application. This application is intended to cover any adaptations or variations of the specific aspects discussed herein.

1. A Digital Phase Locked Loop (DPLL), comprising:
  a Time-to-Digital Converter (TDC) configured to generate quantized phase values of a Voltage Controlled Oscillator (VCO) signal; and
  a frequency estimation circuit configured to receive the quantized phase values, determine a wraparound phase of the quantized phase values, and least-squares estimate a frequency based on the quantized phase values and the wraparound phase.

2. The DPLL of claim 1, wherein the frequency estimation circuit comprises:
  a phase determination circuit configured to determine an accumulation of the quantized phase values having the wraparound phase.

3. The DPLL of claim 1, wherein the frequency estimation circuit comprises:
  a wraparound phase determination circuit configured to determine the wraparound phase of the quantized phase values.

4. The DPLL of claim 3, wherein the wraparound phase determination circuit comprises a decision circuit configured to determine the wraparound phase by comparing a difference between a current quantized phase value and a previous quantized phase value with an expected frequency.

5. The DPLL of claim 4, wherein the decision circuit determines the wraparound phase in accordance with the following:

$$L_l = \begin{cases} -1, (\varphi_k - \varphi_{k-1}) - f_{exp} & < -P/2 \\ 0, & \text{else} \\ 1, (\varphi_k - \varphi_{k-1}) - f_{exp} & > P/2 \end{cases}, L = \sum_{l=1}^{L} L_l,$$

where L is an accumulated number of phase wraparounds, φ_k is the current quantized phase value, φ_{k-1}, is the previous quantized phase value, f_{exp} is the expected frequency, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

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6. The DPLL of claim **5**, wherein the frequency estimation circuit comprises:

an estimated frequency determination circuit configured to determine the least-squares estimated frequency by removing the wraparound phase from the quantized phase values.

7. The DPLL of claim **5**, wherein a value of the period used in the wraparound phase determination is an estimate of the period of the VCO signal.

8. The DPLL of claim **1**, wherein the estimated frequency is represented as follows:

$$\hat{f}=b_2*y_k=b_2*\tilde{y}_k+b_2*(L_k\cdot P),$$

where $\hat{f}$ is the estimated frequency, b_2 is a predetermined matrix, * is a multiplication operation of a vector by a vector, y_k is a quantized phase value without the wraparound phase, $\tilde{y}_k$ is a quantized phase value with the wraparound phase, L_k is an accumulated number of phase wraparounds, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

9. The DPLL of claim **1**, wherein the frequency estimation circuit is configured to estimate the frequency on a quantized phase value-by-quantized phase value basis.

10. The DPLL of claim **1**, wherein the quantized phase values are in units relative to a period of the VCO signal.

11. A wireless communication device, comprising:

a baseband processor comprising the DPLL of claim **1**, or

a Radio Frequency (RF) front end comprising the DPLL of claim **1**.

12. A method of operating a Digital Phase Locked Loop (DPLL), the comprising:

generating, by a Time-to-Digital Converter (TDC), quantized phase values of a Voltage Controlled Oscillator (VCO) signal;

determining, by a frequency estimation circuit, a wraparound phase of the quantized phase values; and

least-squares estimating, by the frequency estimation circuit, a frequency based on the quantized phase values and the wraparound phase.

13. The method of claim **12**, wherein the least-squares estimating comprises:

determining, by a phase determination circuit, an accumulation of the quantized phase values having the wraparound phase.

14. The method of claim **12**, wherein the least-squares estimating comprises:

determining, by a wraparound phase determination circuit within the frequency estimation circuit, the wraparound phase of the quantized phase values.

15. The method of claim **14**, wherein the wraparound phase determining comprises:

determining, by a decision circuit within the wraparound phase determination circuit, the wraparound phase by comparing a difference between a current quantized phase value and a previous quantized phase value with an expected frequency.

16. The method of claim **15**, wherein the determining the wraparound phase is in accordance with the following:

$$L_l = \begin{cases} -1, (\varphi_k - \varphi_{k-1}) - f_{exp} & < -P/2 \\ 0, & \text{else} \\ 1, (\varphi_k - \varphi_{k-1}) - f_{exp} & > P/2 \end{cases}, L = \sum_{l=1}^{L} L_l,$$

where L is an accumulated number of phase wraparounds, φ_k is the current quantized phase value, φ_{k-1} is the previous quantized phase value, f_{exp} is an expected frequency, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

17. The method of claim **12**, wherein the least-squares frequency estimating comprises:

determining, by an estimated frequency determination circuit within the frequency estimation circuit, the estimated frequency by removing the wraparound phase from the quantized phase values.

18. The method of claim **16**, wherein a value of the period used in the wraparound phase determination is an estimate of the period of the VCO signal.

19. The method of claim **12**, wherein the estimated frequency is represented as follows:

$$\hat{f}=b_2*y_k=b_2*\tilde{y}_k+b_2*(L_k\cdot P),$$

where $\hat{f}$ is the estimated frequency, b_2 is a predetermined matrix, * is a multiplication operation of a vector by a vector, y_k is a quantized phase value without wraparound phase, $\tilde{y}_k$ is a quantized phase value with wraparound phase, L_k is an accumulated number of phase wraparounds, k is an index number of a phase value, and P is a threshold proportional to a period of the VCO signal.

20. The method of claim **12**, wherein the least-squares frequency estimating comprises:

estimating the frequency on a quantized phase value-by-quantized phase value basis.

21. The method of claim **12**, wherein the quantized phase values are in units relative to a period of the VCO signal.

22. A method of fast locking a Digital Phase Locked Loop (DPLL), comprising:

setting a constant tuning voltage of a Voltage Controlled Oscillator (VCO) using an open control loop;

least-squares estimating a frequency based on quantized phase values and a wraparound phase of a VCO signal;

determining a tuning voltage offset of the VCO based on the estimated frequency; and

updating the tuning voltage of the VCO to compensate for the tuning voltage offset.

23. The method of claim **22**, after updating the tuning voltage of the VCO, further comprising:

resetting filter memories of the VCO; and

dynamically updating the tuning voltage of the VCO using a closed control loop.

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