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(71) Applicant *(for all designated States except US)*: **FAIRCHILD SEMICONDUCTOR CORPORATION** [US/US]; 82 Running Hill Road, M/S 35-4E, South Portland, ME 04106 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **GRANADA, Honorio, T., Jr.** [PH/PH]; 185-C Sanciangko Street, Cebu City (PH). **JOSHI, Rajeev** [IN/US]; 10168 Colby Avenue, Cupertino, CA 95014 (US). **TANGPUZ, Connie** [PH/PH]; 318 Pasance Road, PAJO, Lapulapu City, CEBU 6015 (PH).

(74) Agents: **LEMOND, Kevin, T.** et al.; Townsend and Townsend and Crew LLP, Two Embarcadero Center, 8th Floor, San Francisco, CA 94111-3834 (US).

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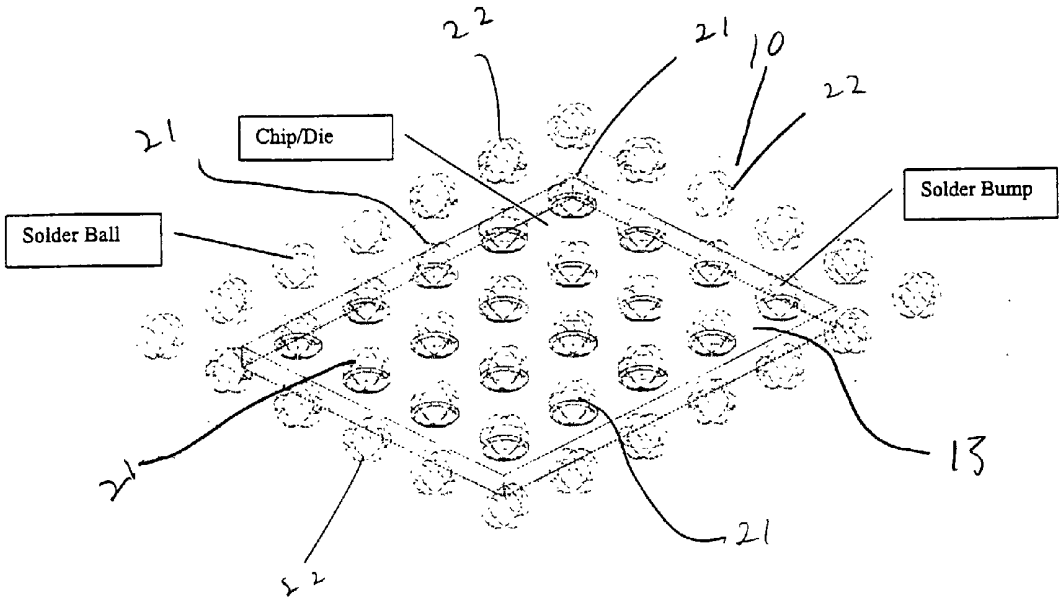
(54) Title: FLIP CHIP SUBSTRATE DESIGN



(57) Abstract: A chip device includes a frame (10) having a die attach cavity (11), a die (13) being positioned in the cavity, solder balls (21, 22).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

FLIP CHIP SUBSTRATE DESIGN

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to a chip device, and more particularly, to discrete power components such as MOSFETs, as well as ICs such as memory circuits that include a leadframe that includes a cavity for receiving the die.

2. Description Of The Prior Art

Chip devices generally include a leadframe and a bumped die attached thereto. Many of the packages are multiple pieces and rely on wire bonding as the interconnect between the die and the package. Additionally, many BGA (ball grid array) substrates do not have the capability for solder balls to be pre-attached or for a cavity to be milled in the substrate to facilitate die attach.

These prior art packages limit the ability to form thin packages. Additionally, the manufacturing processes for these devices are inefficient.

SUMMARY OF THE INVENTION

The present invention provides a chip device that includes a die and a leadframe. The leadframe includes a die attach cavity. The die attach cavity is substantially the same thickness as the die. The die is positioned within the cavity and is attached therein with a standard die attachment procedure.

In accordance with one aspect of the present invention, a plurality of dimples is defined around the periphery of the leadframe the receives solder balls.

In accordance with another aspect of the present invention, the leadframe consists of a copper based alloy.

In accordance with a further aspect of the present invention, the leadframe includes a solderable coating.

The present invention also provides a method of making a memory device. The method includes providing a die and providing a leadframe that includes a die attach cavity. The leadframe includes a plurality of dimples defined around a periphery of the

Leadframe. The die attach cavity has substantially the same thickness as the die. Solder balls are placed into the dimples. The die is flipped into the die attach cavity.

The resulting chip device has enhanced thermal performance since heat is dissipated from the face of the die (where it is generated) as well as from the bottom of the die due to its contact with the leadframe structure. The memory device also has a thinner package comparable to TSSOP stand-off, which is the current trend for miniaturization. The manufacturing process is simplified when compared to conventional assembly processes by eliminating such steps as wire bonding, molding, forming and plating.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred exemplary embodiments, found hereinbelow in conjunction with reference to the drawings in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a flip chip leadframe in accordance with the present invention;

Figure 2 is a perspective view of the flip chip leadframe illustrated in Figure 1 including solder balls and the die; and

Figure 3 is a schematic side view of a bumped die.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a leadframe 10 for use in manufacturing a chip device in accordance with the present invention. The leadframe includes a die attach cavity 11 defined within the leadframe. In a preferred embodiment, a plurality of dimples 12 are defined around the periphery of the leadframe.

As can be seen in Figure 2, a die 13 is placed within the cavity to complete the chip device. Die 13 is preferably a one-piece item that is often referred to in the art as a "bumped die." As can be seen in Figure 3, a bumped die includes die 13, "under bump material" that serves as an intermediate layer 20 between the top surface of the die and solder bump 21, and the solder bumps themselves. Preferably, the under bump material is one of TiW, Cu, Au or an equivalent. In the example illustrated in Figure 3, the under bump material is broken into three layers – Cu plating 20a, sputtered Cu 20b and sputtered Ti 20d.

The die attach pad area is etched out such that the depth of the cavity is the same as the die thickness. Preferably, the leadframe consists of a material made of thermally and electrically conductive metal alloy such as, for example, copper based Eftec 3S. Additionally, in a preferred embodiment, the leadframe is coated with a solderable coating such as Ni:Pd.

Solder balls 22 are placed within the dimples. These solder balls serve as the connection for the drain region of the die since the leadframe is conductive. Solder bumps 21 serve as the connections for the source and gate regions.

The reverse side of the leadframe may be marked with the product code and other manufacturing codes, either at the leadframe fabricator's end or during assembly of the IC packages.

As a result of this structure, a bumped die may be die attached into the leadframe cavity using conventional die attach processes. The solder balls on the bumped die form (both in the cavity and the dimples) the source and gate connections to the PCB with the solder balls on the leadframe forming the drain connections.

Thus, the present invention provides an improved chip device, such as a MOSFET BGA, that has improved thermal performance. The improved thermal performance is due to the fact that heat is dissipated from the face of the die (where it is generated) as well as from the bottom of the die due to its contact with the leadframe structure. Additionally, the present invention provides a chip device that results in a thinner package (generally less than 1 millimeter) comparable to TSSOP stand-off, which is the current trend for miniaturization. The manufacturing process is also simplified since solder ball attach of the leads of the leadframe have been eliminated and conventional assembly process steps, such as wire bonding, molding, forming and plating, have also been eliminated.

Although the invention has been described with reference to specific exemplary embodiments, it will appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A chip device comprising:

a. a die; and

b. a leadframe including a die attach cavity, the die attach cavity having substantially the same thickness as the die;

c. wherein the die is positioned within the die attach cavity and is attached therein.

2. The chip device of claim 1 further comprising a plurality of dimples defined around the periphery of the leadframe that receive solder balls.

3. The chip device of claim 1 wherein the leadframe consists of a copper based alloy.

4. The chip device of claim 3 wherein the leadframe includes a solderable coating.

5. The chip device of claim 1 wherein the die is a bumped die.

6. A chip device comprising:

a. a bumped die;

b. a leadframe including a die attach cavity and a plurality of dimples defined around a periphery of the leadframe, the die attach cavity having substantially the same thickness as the die; and

c. a plurality of solder balls placed within the dimples;

wherein the die is positioned within the cavity and is attached therein.

7. The chip device of claim 6 wherein the leadframe consists of a copper based alloy.

8. The chip device of claim 7 wherein the leadframe includes a solderable coating.

9. A method of making a chip device, the method comprising:

providing a die;

providing a leadframe including a die attach cavity and a plurality of dimples defined around a periphery of the leadframe, the die attach cavity having substantially the same thickness as the die;

placing solder balls into the dimples; and

flipping the die into the die attach cavity and attaching it therein.

10. The method of claim 9 wherein the die provided is a bumped die.

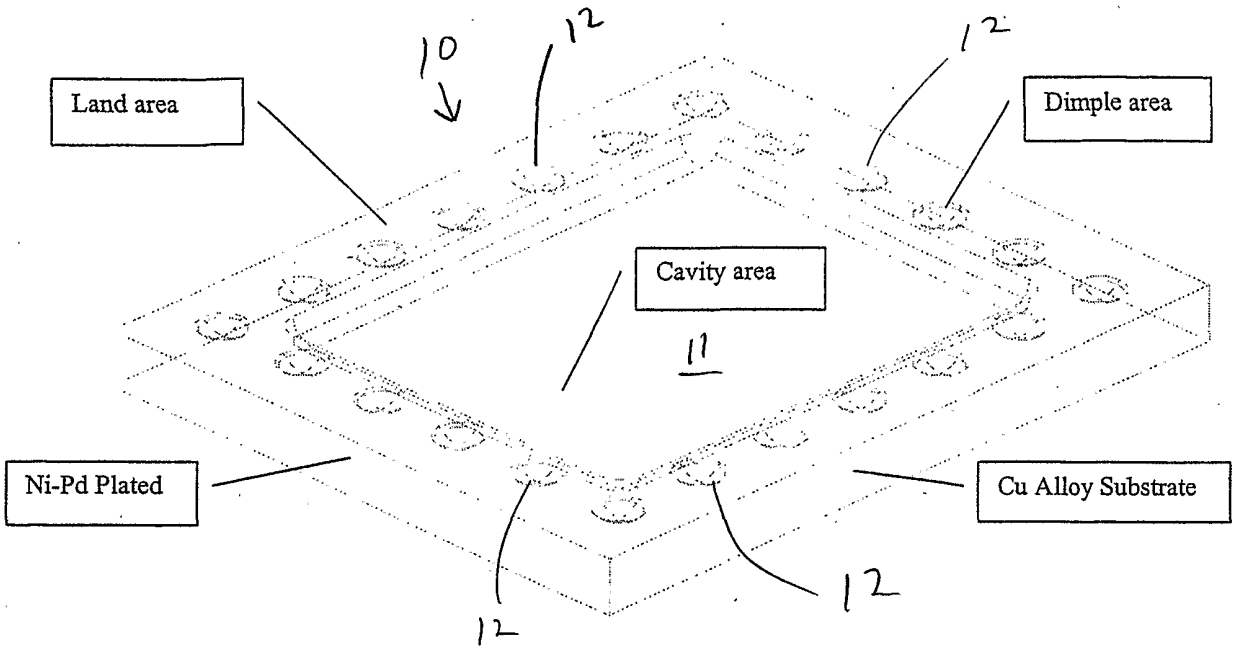

Figure 1

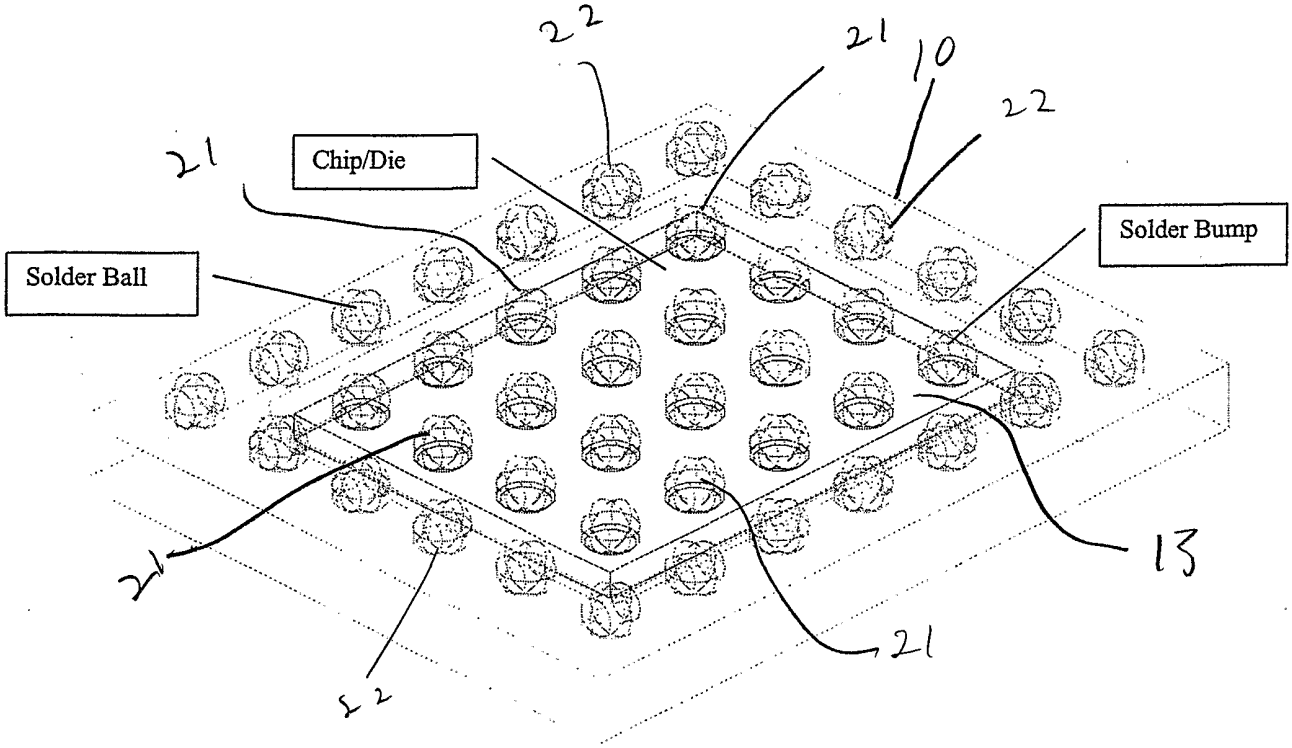

Figure 2

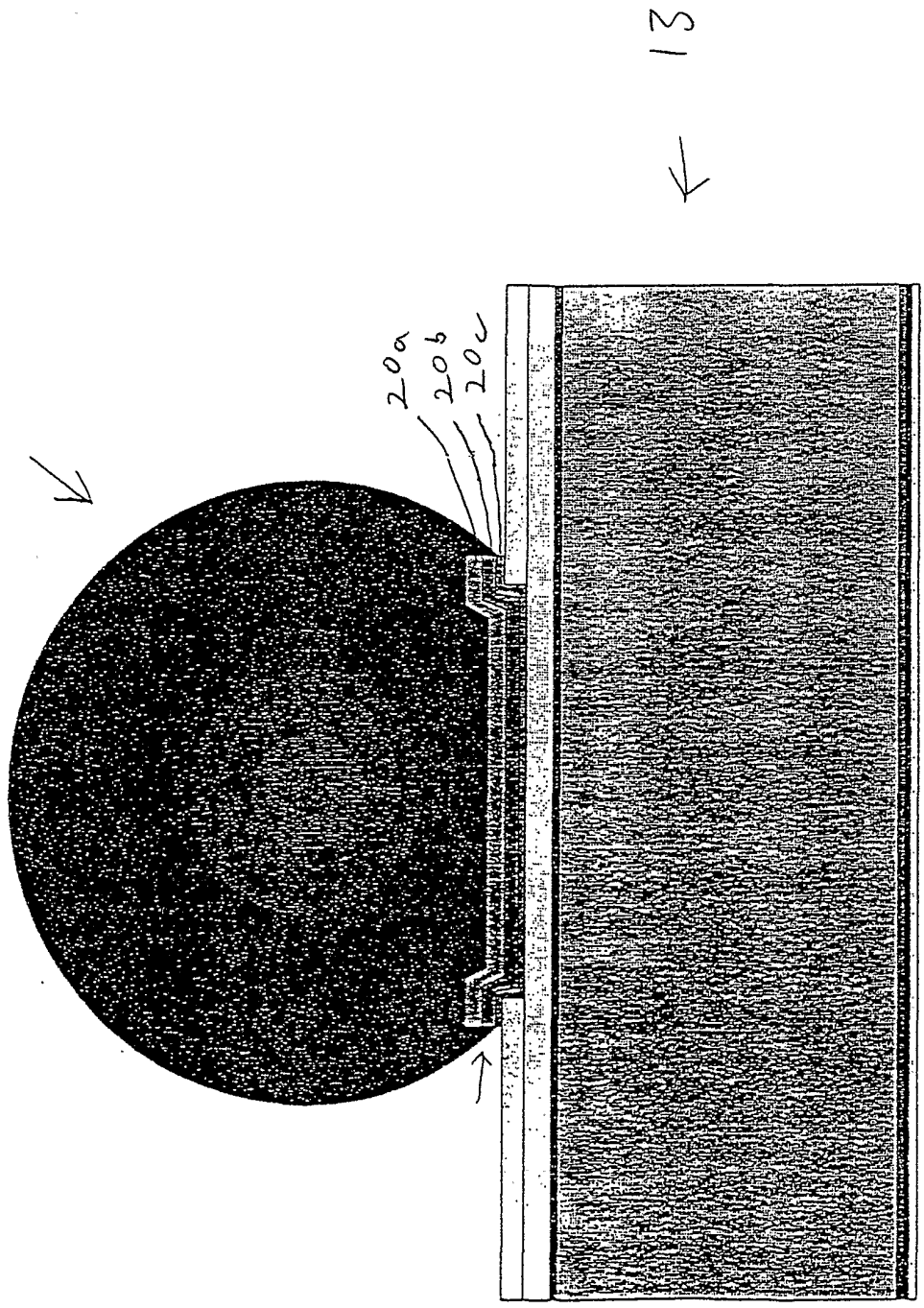

Figure 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/22798

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 23/02
US CL :174/52.4
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/52.4, 52.2. 257/778, 737, 738

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,133,634 A (JOSHI) 17 October 2000 (17.10.2000), FIGS 1-3.	1, 2, 5, 6, 9, 10
X	US 6,031,284 A (SONG) 29 February 2000 (29.02.2000), Fig. 3.	1, 2, 5, 6, 9, 10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703) 305-3230

Authorized officer
Shawn S. Hoppe
HUNG V. NGO
Telephone No. (703) 308-7614

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