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(54) SEMICONDUCTOR DEVICE

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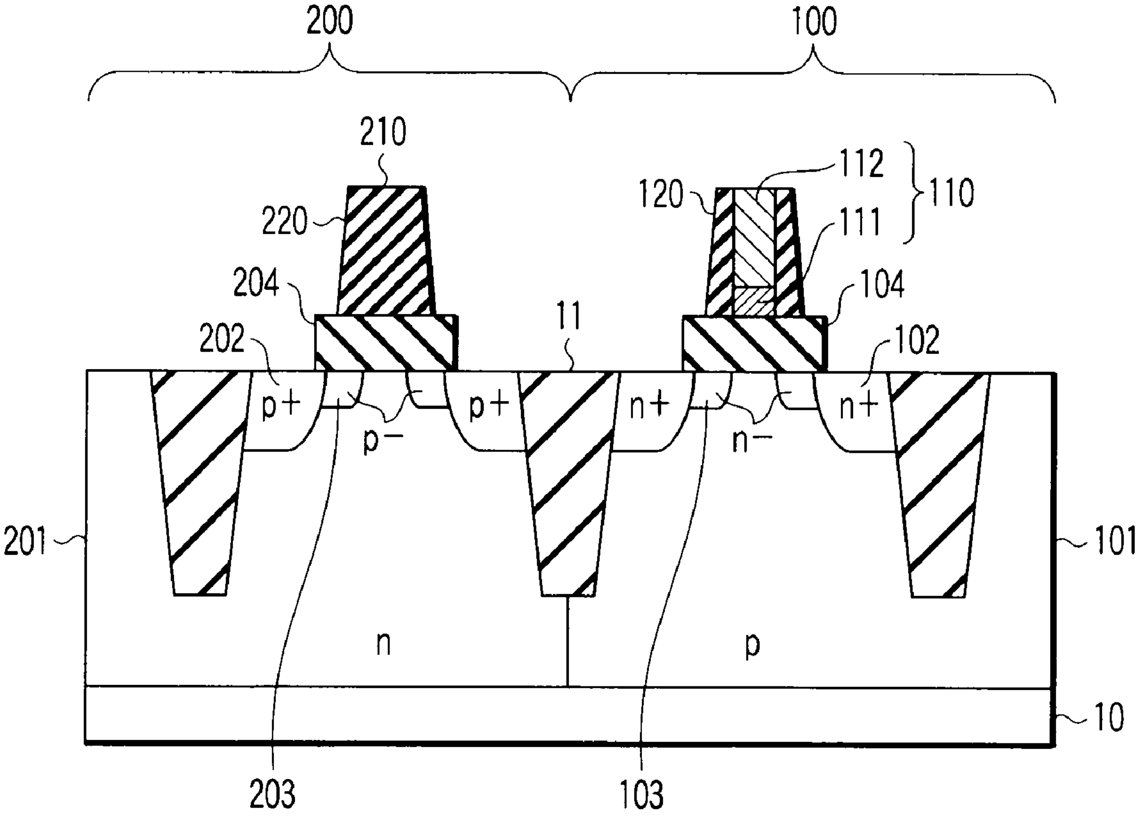
(57) **ABSTRACT**

A semiconductor device has an n-channel MIS transistor and a p-channel MIS transistor on a substrate. The n-channel MIS transistor includes a p-type semiconductor region formed on the substrate, a lower layer gate electrode which is formed via a gate insulating film above the p-type semiconductor region and which is one monolayer or more and 3 nm or less in thickness, and an upper layer gate electrode which is formed on the lower layer gate electrode, whose average electronegativity is 0.1 or more smaller than the average electronegativity of the lower layer gate electrode. The p-channel MIS transistor includes an n-type semiconductor region formed on the substrate and a gate electrode which is formed via a gate insulating film above the n-type semiconductor region and is made of the same metal material as that of the upper layer gate electrode.



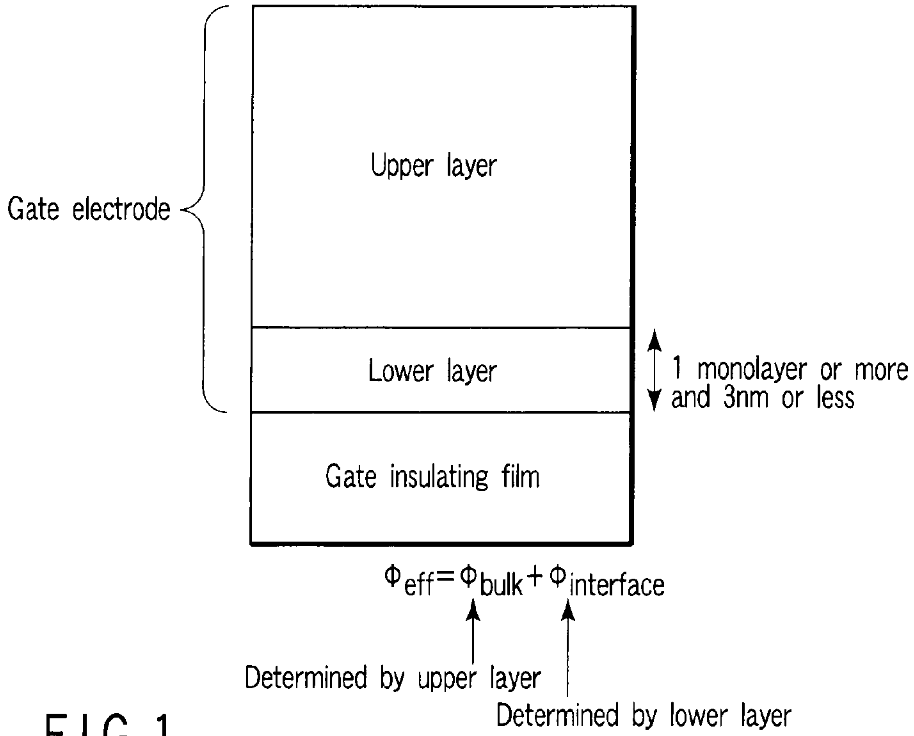

Gate electrode
Upper layer
Lower layer
1 monolayer or more and 3nm or less
Gate insulating film
$\Phi_{eff}=\Phi_{bulk}+\Phi_{interface}$
Determined by upper layer
Determined by lower layer

FIG. 1

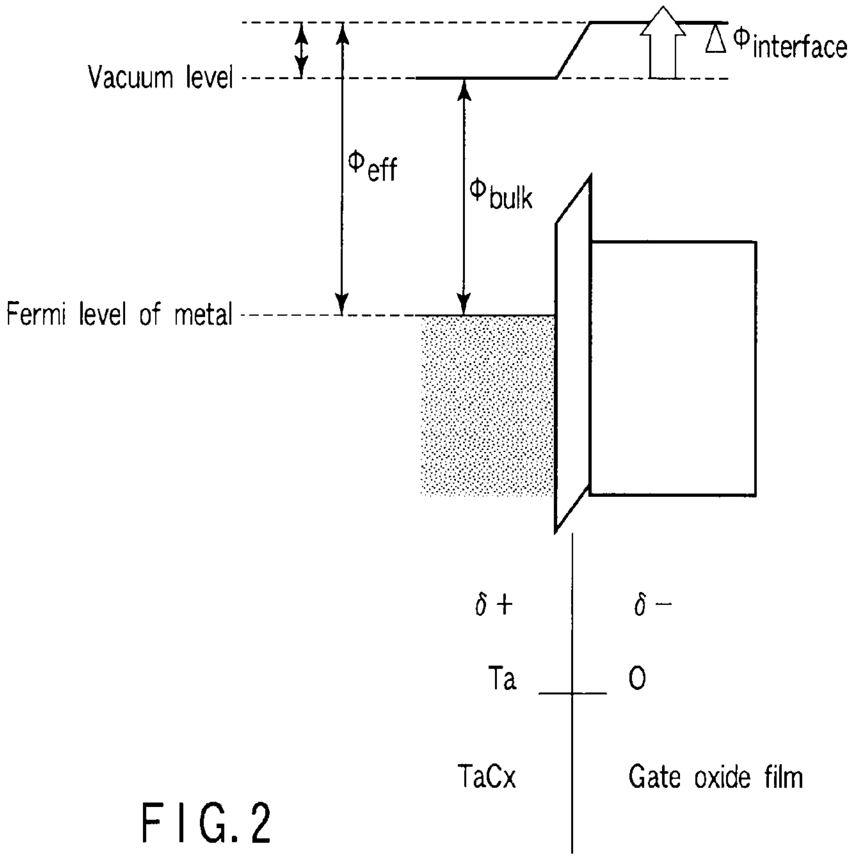

Vacuum level
$\Delta\Phi_{interface}$
Φ_{eff}
Φ_{bulk}
Fermi level of metal
δ+
δ−
Ta
O
TaCx
Gate oxide film

FIG. 2

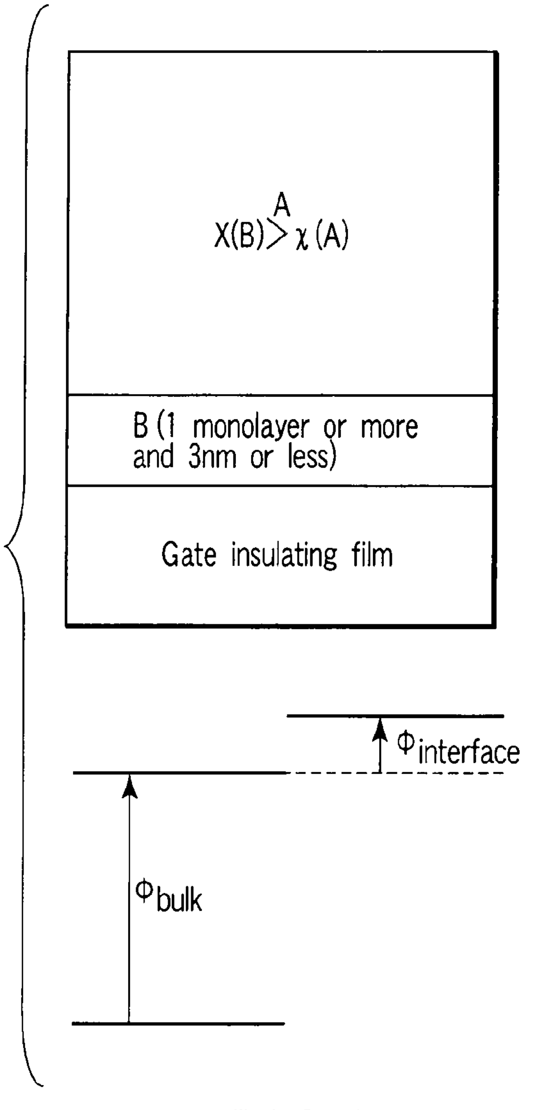

A
X(B)>χ(A)
B (1 monolayer or more and 3nm or less)
Gate insulating film
Φinterface
Φbulk

FIG. 3A

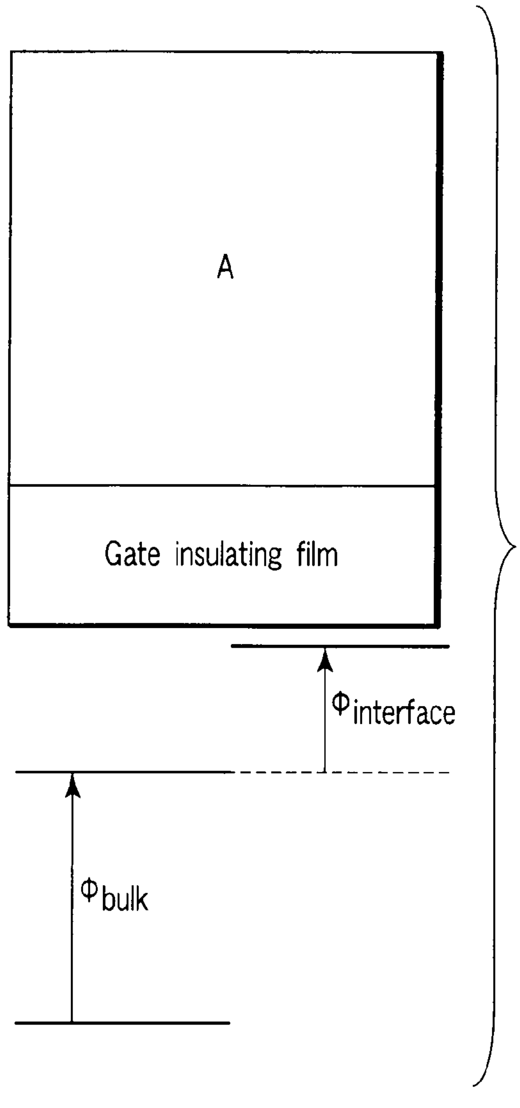

A
Gate insulating film
Φinterface
Φbulk

FIG. 3B

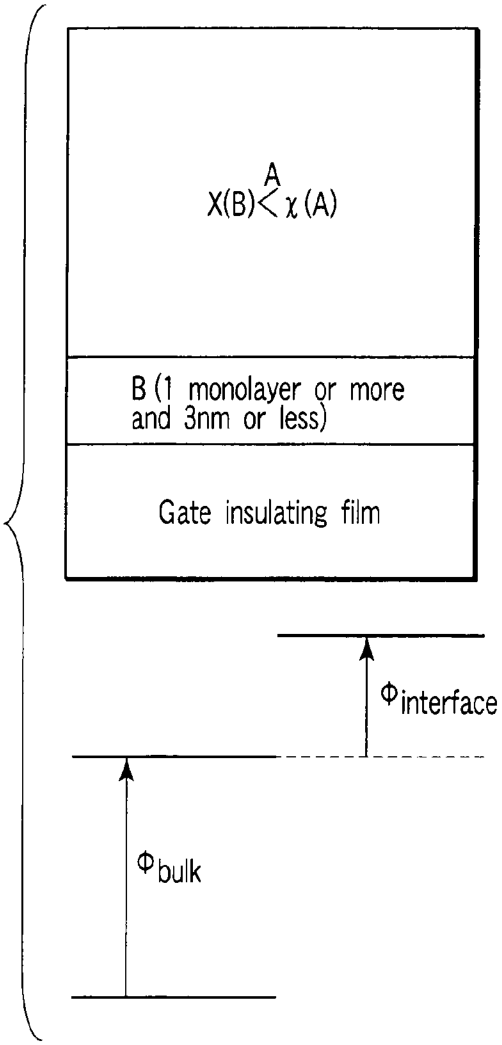

A
X(B)<χ(A)
B (1 monolayer or more and 3nm or less)
Gate insulating film
Φinterface
Φbulk

FIG. 4A

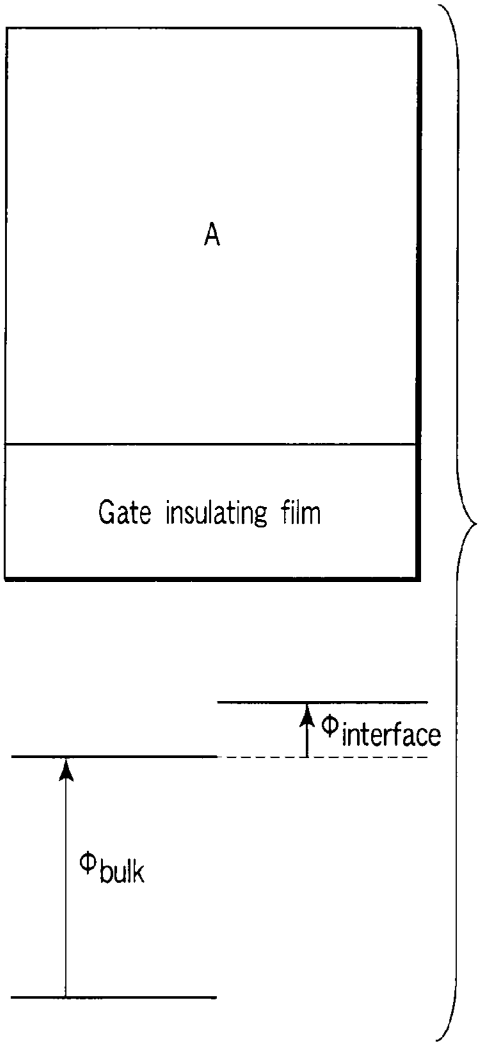
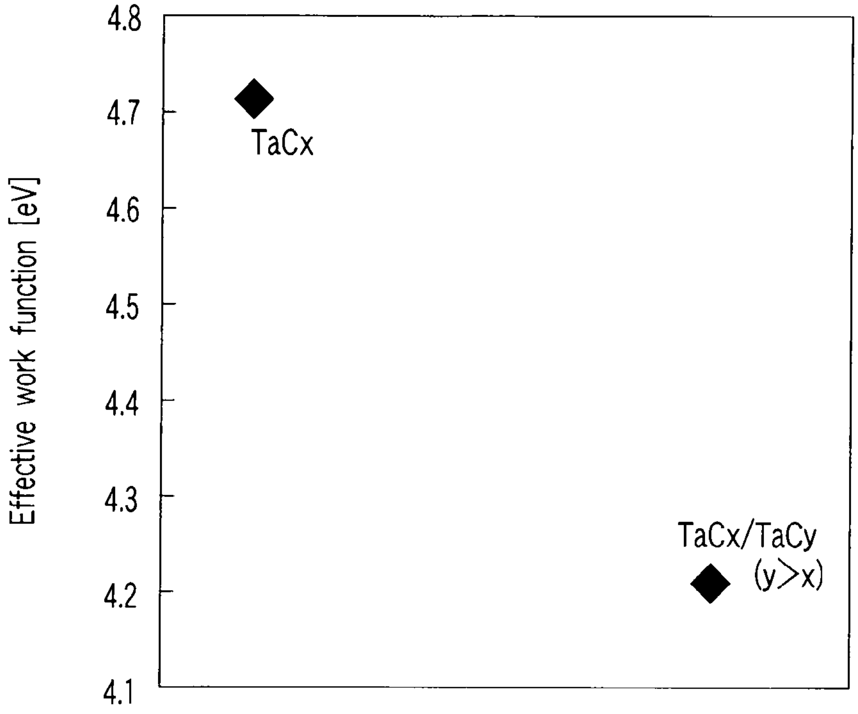
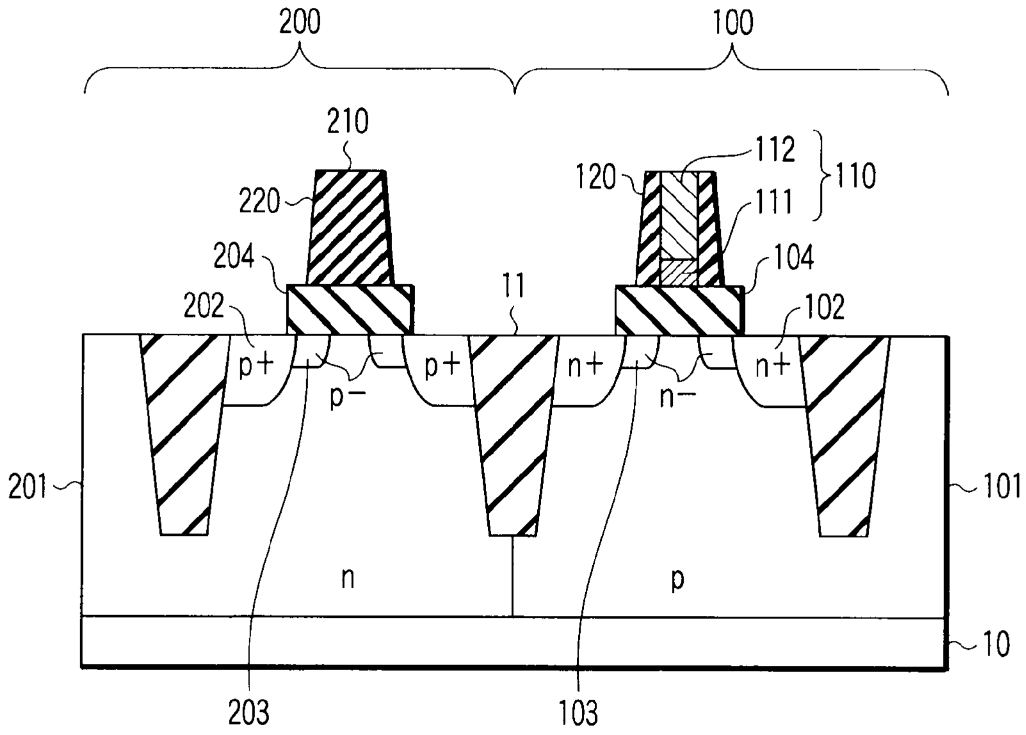

A
Gate insulating film
Φinterface
Φbulk

FIG. 4B


4.8
4.7
4.6
4.5
4.4
4.3
4.2
4.1
Effective work function [eV]
TaCx
TaCx/TaCy
(y>x)

F I G. 5


200
100
210
220
204
202
11
120
112
111
110
104
102
p+
p−
p+
n+
n−
n+
201
101
n
p
10
203
103

F I G. 6

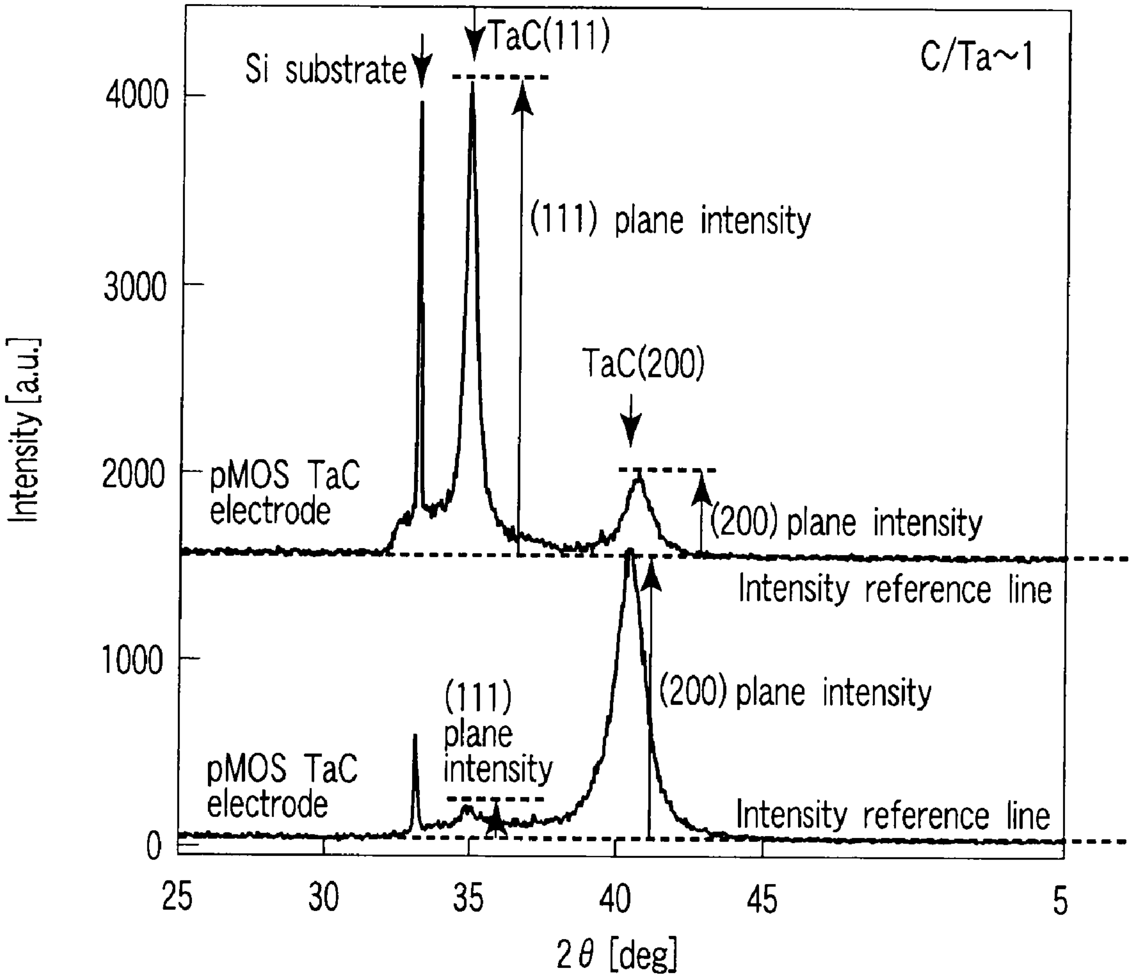

C/Ta~1
Si substrate
TaC(111)
(111) plane intensity
TaC(200)
(200) plane intensity
pMOS TaC electrode
Intensity reference line
(200) plane intensity
(111) plane intensity
pMOS TaC electrode
Intensity reference line
Intensity [a.u.]
4000
3000
2000
1000
0
25
30
35
40
45
5
2θ [deg]

FIG. 7

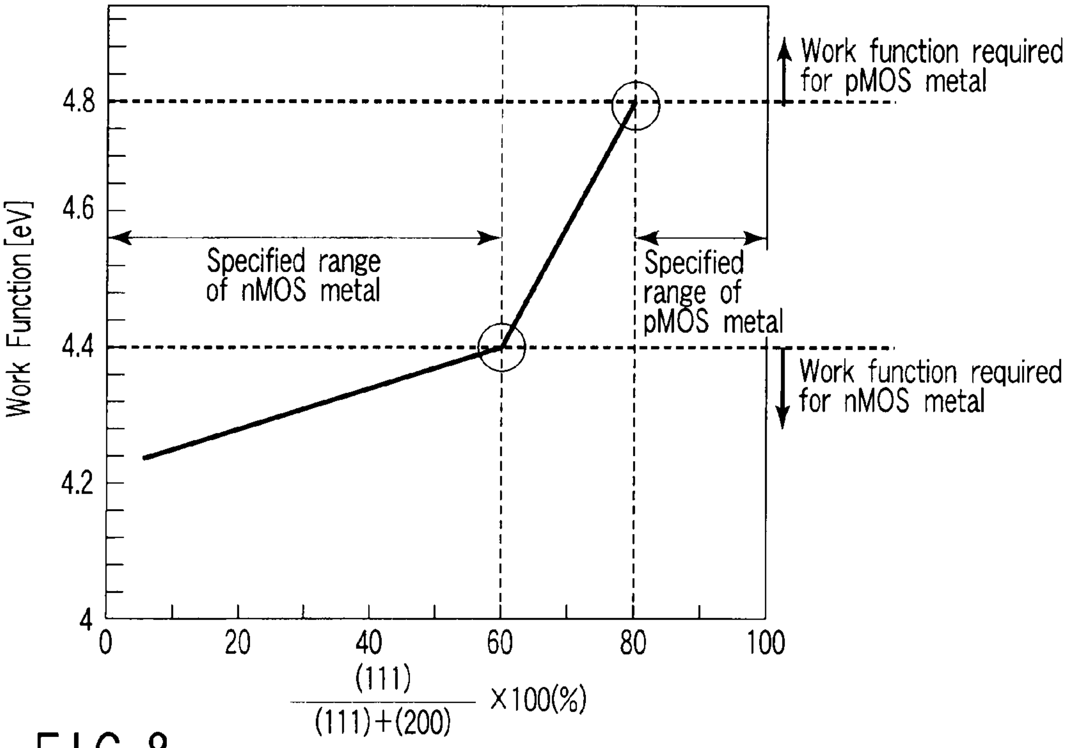

Work function required for pMOS metal
Work function required for nMOS metal
Specified range of nMOS metal
Specified range of pMOS metal
Work Function [eV]
4.8
4.6
4.4
4.2
4
0
20
40
60
80
100
$\frac{(111)}{(111)+(200)}\times 100(\%)$

FIG. 8

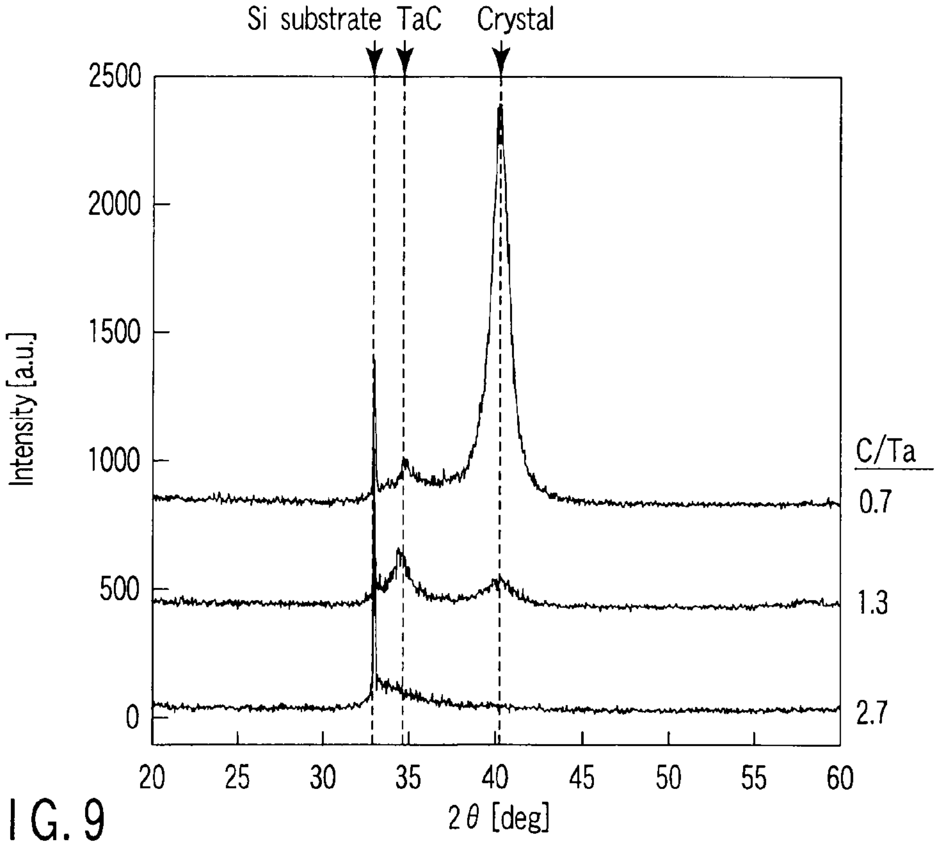

Si substrate
TaC
Crystal
Intensity [a.u.]
2500
2000
1500
1000
500
0
C/Ta
0.7
1.3
2.7
20
25
30
35
40
45
50
55
60
2θ [deg]

FIG. 9

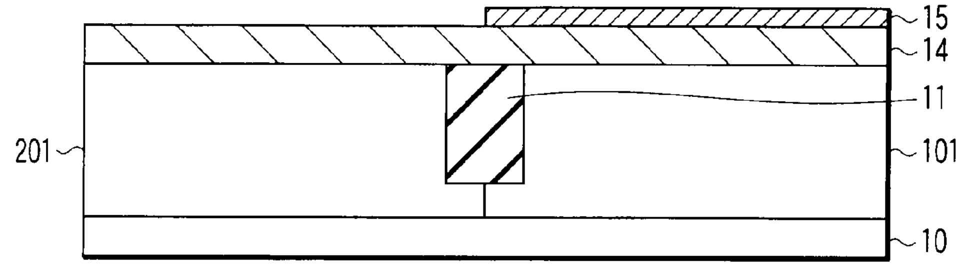


FIG. 10A

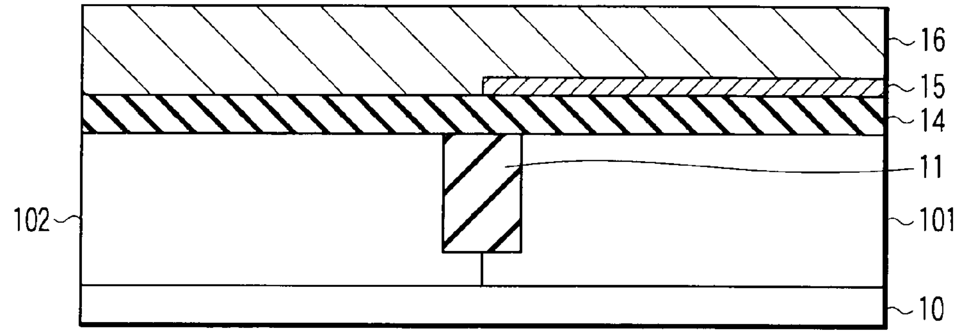


FIG. 10B

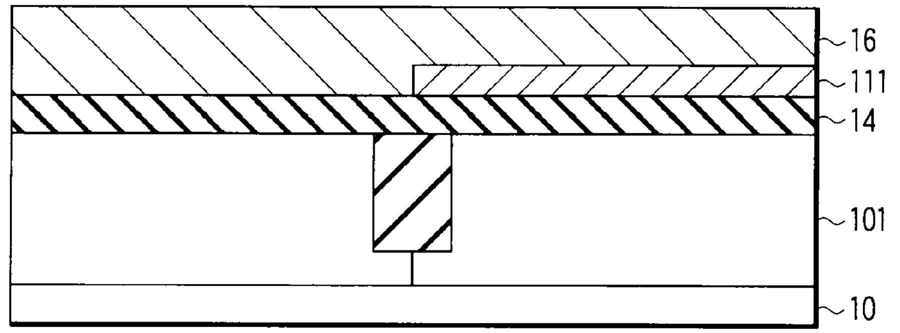


FIG. 10C

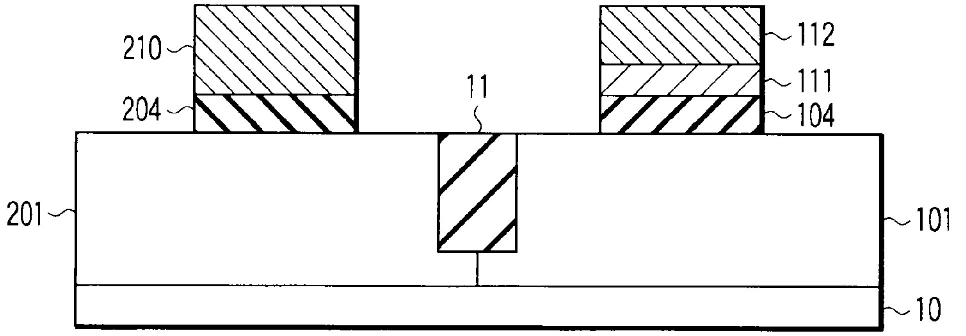


FIG. 10D

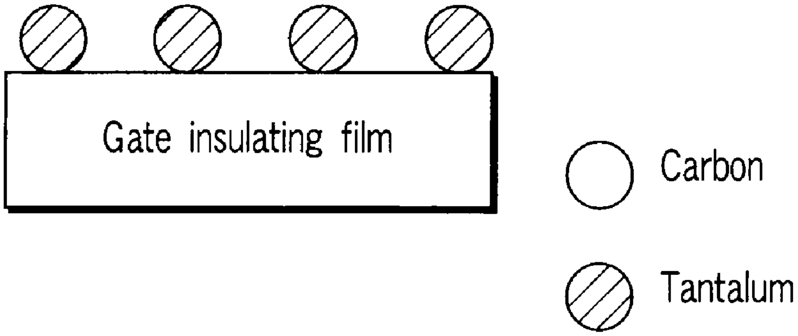


FIG. 11A

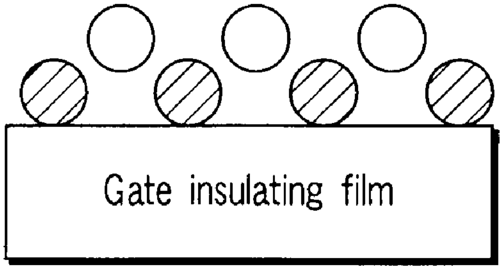


FIG. 11B

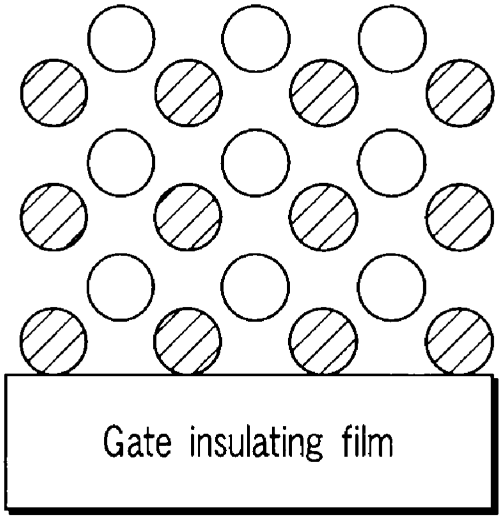
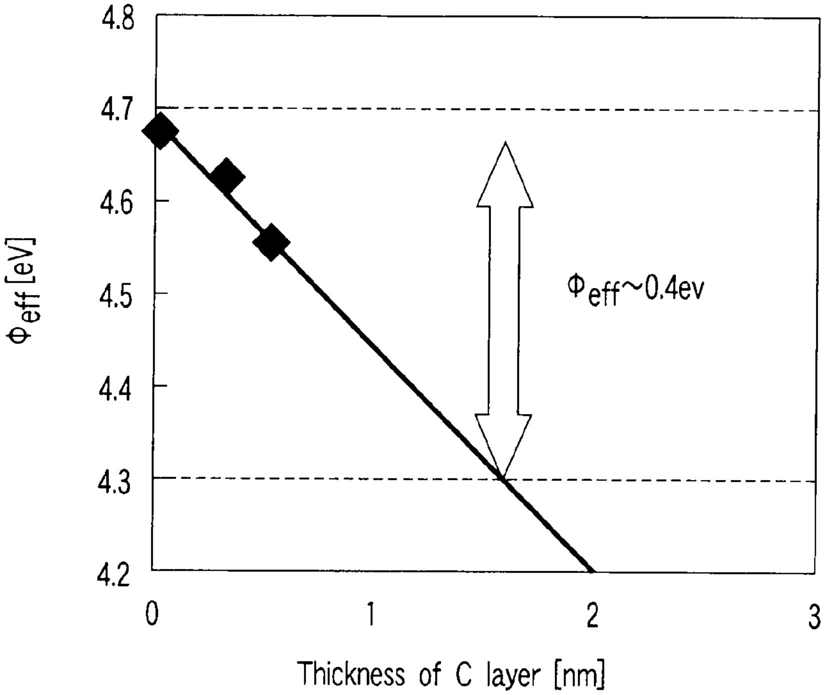
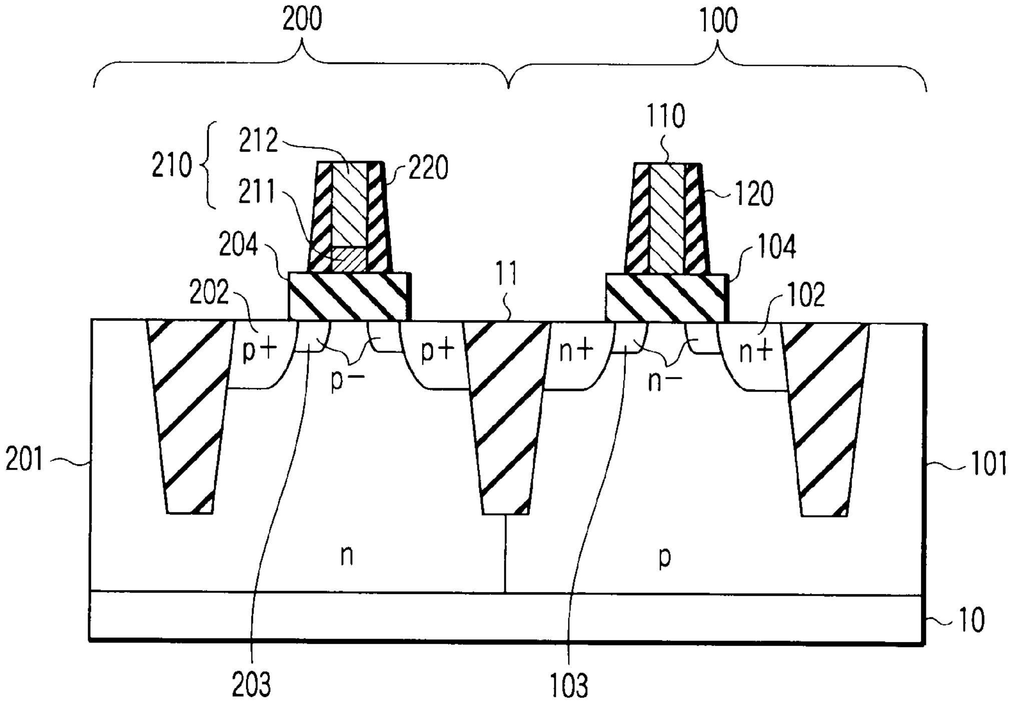


FIG. 11C


4.8
4.7
4.6
4.5
4.4
4.3
4.2
Φ_{eff} [eV]
Φ_{eff}~0.4ev
0
1
2
3
Thickness of C layer [nm]

F I G. 12


200
100
210
212
211
220
110
120
204
104
202
11
102
p+
p−
p+
n+
n−
n+
201
101
n
p
10
203
103

F I G. 13

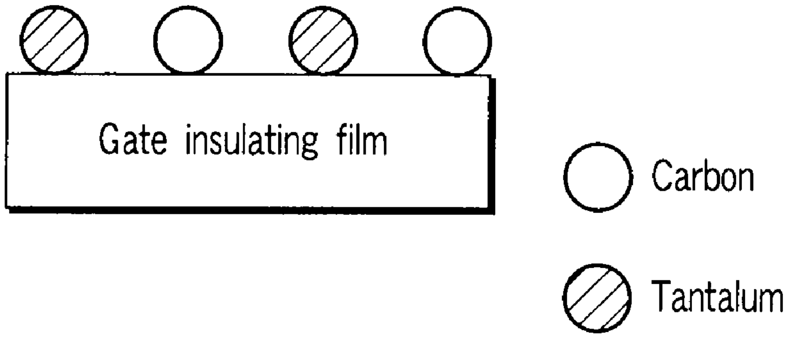


FIG. 14A

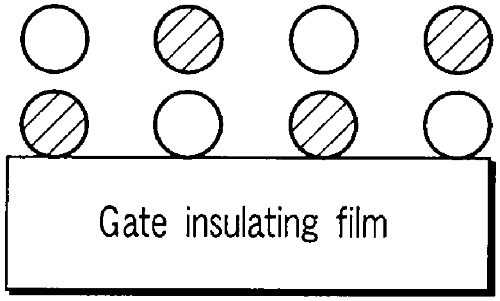


FIG. 14B

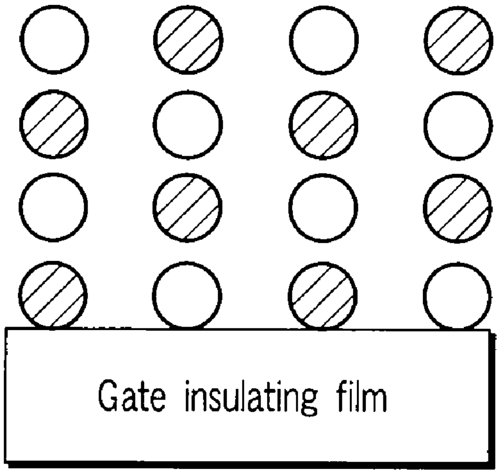
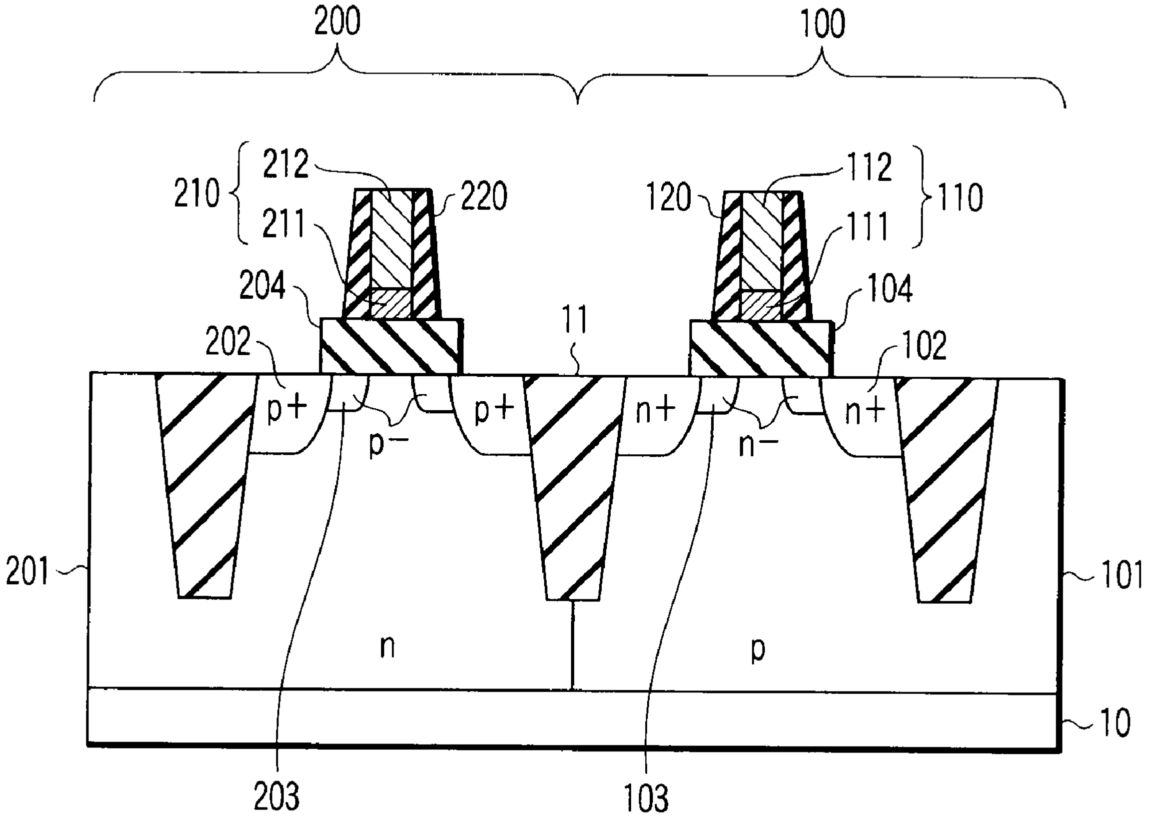


FIG. 14C


200
100
210
212
211
220
120
112
111
110
204
104
202
11
102
p+
p−
p+
n+
n−
n+
201
101
n
p
10
203
103

F I G. 15

SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of and claims the benefit priority from U.S. Ser. No. 11/857,197, filed Sep. 18, 2007, which claims the benefit of priority from Japanese Patent Application No. 2006-329521, filed Dec. 6, 2006, the entire contents of each of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to a semiconductor device where a p-channel Metal Insulator Semiconductor (MIS) transistor and an n-channel MIS transistor each of which has a metal gate have been formed on the same substrate.

[0004] 2. Description of the Related Art

[0005] Recently, attention has been focused on the metal gate techniques for using metal as gate electrode materials in a complementary MIS (CMIS) device where a p-channel MIS transistor and an n-channel MIS transistor are formed on the same substrate. Since metal has as high a charge density as an atom density, when metal is used as a gate electrode, the depletion of the gate electrode can be ignored.

[0006] In a CMIS device using a metal gate electrode, a so-called dual-metal-gate CMIS structure is needed to realize a low threshold voltage. To form a dual-metal-gate CMIS structure, the gate electrode of each of the n-channel MIS transistor and p-channel MIS transistor is needed to have an effective work function close to the conduction band end and valence band end of Si. Specifically, the effective work function of the gate electrode of the p-channel MIS transistor is required to be 0.4 eV or more higher than the effective work function of the n-channel MIS transistor. At present, a general method of realizing this is to configure the gate electrode of the n-channel MIS transistor and that of the p-channel MIS transistor using completely different metal materials (e.g., refer to JP-A 2004-207481 (KOKAI) and U.S. Pat. No. 7,030, 430).

[0007] However, when different metal materials are used for the gate electrode of the n-channel MIS transistor and that of the p-channel MIS transistor, the n-channel MIS transistor and p-channel MIS transistor have to be dealt with separately in forming and processing their gate electrodes. This makes the manufacturing processes complex and causes the problem of increasing the manufacturing cost. In the method disclosed in JP-A 2004-207481 (KOKAI), the work function of each gate electrode is made different by using molybdenum as gate electrode material for the p-channel MIS transistor and n-channel MIS transistor and at the same time introducing carbon into one of them. In this case, the manufacturing process is complicated.

[0008] To realize the introduction of metal gate techniques, it is necessary to find such a dual-metal-gate CMIS structure as prevents the manufacturing processes from becoming complicated as much as possible.

[0009] As described above, the introduction of dual-metal-gate techniques is indispensable for improving the performance of CMIS devices. To realize this, it is necessary to cause the metal material for the gate electrode of the n-channel MIS transistor to differ from that for the gate electrode of the p-channel MIS transistor, which is the factor that makes the manufacturing processes complex and increases the manufacturing cost.

BRIEF SUMMARY OF THE INVENTION

[0010] According to an aspect of the invention, there is a method for manufacturing a semiconductor device having an nMIS transistor and a pMIS transistor, including: forming a p-type semiconductor region and an n-type semiconductor region in a surface of a substrate; forming a first gate insulating film on the p-type semiconductor region and forming a second gate insulating film on the n-type semiconductor region; forming a first metallic film made of a metal material above the second gate insulating film and forming a laminated structure of a second metallic film made of a material having a higher electronegativity than the metal material and a third metallic film made of the metal material above the first gate insulating film; performing heat treatment to form a mixed film obtained by mixing the second metallic film and a part of the third metallic film in such a manner that the mixed film comes into contact with the first gate insulating film; and processing the first metallic film, the third metallic film and the mixed film to have a gate pattern to form a gate electrode for the nMIS transistor above the p-type semiconductor region and form a gate electrode for the pMIS transistor above the n-type semiconductor region.

[0011] According to another aspect of the invention, there is provided a method for manufacturing a semiconductor device having an nMIS transistor and a pMIS transistor, including: forming a p-type semiconductor region and an n-type semiconductor region in a surface of a substrate; forming a first gate insulating film on the p-type semiconductor region and forming a second gate insulating film on the n-type semiconductor region; forming a first metallic film made of a metal material above the first gate insulating film and forming a laminated structure of a second metallic film made of a material having a lower electronegativity than the metal material and a third metallic film made of the metal material above the second gate insulating film; performing heat treatment to form a mixed film obtained by mixing the second metallic film and a part of the third metallic film in such a manner that the mixed film comes into contact with the second gate insulating film; and processing the first metallic film, the third metallic film and the mixed film to have a gate pattern to form a gate electrode for the nMIS transistor above the p-type semiconductor region and form a gate electrode for the pMIS transistor above the n-type semiconductor region.

[0012] According to still another aspect of the invention, there is provided a method for manufacturing a semiconductor device having an nMIS transistor and a pMIS transistor, including: forming a p-type semiconductor region and an n-type semiconductor region in a surface of a substrate; forming a first gate insulating film on the p-type semiconductor region and forming a second gate insulating film on the n-type semiconductor region; forming a laminated structure of a first metallic film made of a metal material and a second metallic film made of a material having a higher electronegativity than the metal material above the first gate insulating film, and forming a laminated structure of a third metallic film made of the metal material and a fourth metallic film made of a material having a lower electronegativity than the metal material above the second gate insulating film; performing heat treatment to form a first mixed film obtained by mixing the second metallic film and a part of the first metallic film in such a manner that the first mixed film comes into contact with the first gate insulating film and form a second mixed film obtained by mixing the fourth metallic film and a part of the third metallic film in such a manner that the second mixed film comes into contact with the second gate insulating film; and processing the first metallic film, the third metallic film, the first mixed film and the second mixed film to have a gate pattern to form a gate electrode for the nMIS transistor above the p-type semiconductor region and form a gate electrode for the pMIS transistor above the n-type semiconductor region.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0013] FIG. **1** shows the relationship between the structure of a gate electrode and the effective work function in the structure;

[0014] FIG. **2** shows an energy band when a dipole is formed at a gate electrode/gate insulating film interface;

[0015] FIG. **3**A shows the relationship between the structure (stacked layer) of the gate electrode and its effective work function;

[0016] FIG. **3**B shows the relationship between the structure (single layer) of the gate electrode and its effective work function;

[0017] FIG. **4**A shows the relationship between the structure (stacked layer) of the gate electrode and its effective work function;

[0018] FIG. **4**B shows the relationship between the structure (single layer) of the gate electrode and its effective work function;

[0019] FIG. **5** shows an effective work function on SiO_2 at a TaC_x electrode and that on SiO_2 at a TaC_x/TaC_y electrode;

[0020] FIG. **6** is a sectional view showing a schematic structure of a semiconductor device according to a first embodiment;

[0021] FIG. **7** is a characteristic diagram showing a change in the orientation of a TaC_x electrode according to a difference in the film forming method;

[0022] FIG. **8** is a characteristic diagram showing the relationship between the orientation of the TaC_x electrode and its work function;

[0023] FIG. **9** is a characteristic diagram showing the relationship between the composition of the TaC_x electrode and a crystalline change;

[0024] FIGS. **10**A to **10**D are sectional views showing the manufacturing processes of a semiconductor device according to the first embodiment;

[0025] FIGS. **11**A to **11**C are pattern diagrams to help explain a method of forming a pMIS TaC_x electrode;

[0026] FIG. **12** is a characteristic diagram showing the relationship between the film thickness of a C layer deposited on the gate insulating film and its work function;

[0027] FIG. **13** is a sectional view showing a schematic structure of a semiconductor device according to a second embodiment;

[0028] FIGS. **14**A to **14**C are pattern diagrams to help explain a method of forming an nMIS TaC_x electrode; and

[0029] FIG. **15** is a sectional view showing a schematic structure of a semiconductor device according to a third embodiment.

DETAILED DESCRIPTION OF THE INVENTION

Overview and Principle of the Invention

[0030] Before the explanation of embodiments of the invention, the principle of the invention will be described.

[0031] The effective work function Φ_{eff} of a gate electrode is expressed by the following equation (1):

$$\Phi_{eff}=\Phi_{bulk}+\Phi_{interface} \tag{1}$$

[0032] Φ_{bulk} is determined by the nature of the bulk part of the gate electrode. $\Phi_{interface}$ is a term determined by the charge distribution at the gate electrode/gate insulating film interface. Suppose there is a gate electrode with a stacked structure including a two-layer structure composed of a lower layer formed on the gate insulating film surface and an upper layer formed on the lower layer. At this time, as shown in FIG. **1**, when the film thickness of the lower layer is 1 monolayer or more and 3 nm or less, Φ_{bulk} is determined mainly by the nature of the upper layer, whereas $\Phi_{interface}$ is determined by the nature of the lower layer.

[0033] $\Phi_{interface}$ depends on the size of a dipole formed when atoms on the gate electrode side combine with atoms on the gate insulating film side. Here, consider a case where the gate electrode is composed of Ta—C alloy and the gate insulating film is composed of oxide.

[0034] FIG. **2** shows an energy band when tantalum (Ta) on the gate electrode side is combined with oxygen (O) on the gate insulating film side. Since the electronegativity x of Ta is 1.5 and the electronegativity x of O is 3.5, if Ta is combined with O, more electrons gather around O with a higher electronegativity x, that is, on the gate insulating film side. At that time, $\Phi_{interface}$ rises and Φ_{eff} increases as shown in FIG. **2**.

[0035] Consider a case where C on the gate electrode side is combined with O on the gate insulating film side. At this time, the electronegativity x of C is 2.5, having a stronger electron attracting force than Ta. Therefore, the cluster of electrons on the insulating film side is smaller than when the Ta—O combination is formed. Accordingly, $\Phi_{interface}$ is smaller that much.

[0036] What has been explained above is described more commonly as follows. If gate insulating films are the same, the more atoms whose electronegativity x is small there are on the gate insulating film side of the gate electrode (that is, the smaller the average x on the gate insulating film side of the gate electrode is), the greater $\Phi_{interface}$ is, whereas the more atoms whose electronegativity x is large there are at the gate insulating film on the gate electrode side (that is, the greater the average x of the gate electrode is), the smaller $\Phi_{interface}$ is. In the specification, the average x means a geometric mean of the electronegativity of elements constituting metal materials. For example, the average x of Ta_xC_y is expressed as:

$$\chi=\sqrt[x+y]{\chi_{Ta}{}^{x}\chi_{c}{}^{y}} \tag{2}$$

[0037] x_{Ta} and x_C are the electronegativity of Ta and that of C, respectively.

[0038] For the reason above-mentioned, as shown in FIGS. **3**A and **3**B, if the average x of the gate electrode lower layer (B) is greater than the x of the gate electrode upper layer (A), $\Phi_{interface}$ of the gate electrode composed of a A/B stacked structure is smaller than $\Phi_{interface}$ of the gate electrode composed of an A single layer. In contrast, if the average x of the gate electrode lower layer (B) is smaller than the average x of the gate electrode upper layer (A), as shown in FIGS. **4**A and **4**B, $\Phi_{interface}$ of the gate electrode composed of an A/B stacked structure is greater than $\Phi_{interface}$ of the gate electrode composed of an A single layer.

[0039] Generally, the greater x is, the greater Φ_{bulk} is. For this reason, when the gate electrode lower layer (B) also has an effect on Φ_{bulk}, the effect on Φ_{bulk} and the effect on Φ_{inter-}

$_{face}$ cancel out each other. Therefore, the gate electrode lower layer (B) has to function only as $\Phi_{interface}$. As described above, this will be realized if the thickness of the gate electrode lower layer (B) is 1 monolayer or more and 3 nm or less. At that time, a difference in $\Phi_{interface}$ is reflected directly in Φ_{eff}.

[0040] The inventors have examined what Φ_{eff} difference occurred when the gate electrode was composed of a stacked structure. The result of the examination has shown that, if the absolute value $\Delta\chi$ of the difference between the average x of the gate electrode upper layer (A) and the average x of the gate electrode lower layer (B) is 0.1 or more, the Φ_{eff} difference ($\Delta\phi_{eff}$) between the MIS transistor composed of an A single layer and the MIS transistor composed of an A/B stacked layer is 0.4 eV or more, which is required to realize a dual-metal-gate CMIS structure. Moreover, the inventors have found that $\Delta\phi_{eff}$ and $\Delta\chi$ have the following relationship:

$$\Delta\Phi_{eff}=0.4\times\Delta\chi/0.1 \quad (3)$$

[0041] FIG. **5** shows actual measurement values of the effective work functions of a gate electrode composed of a stacked structure of TaC_x/TaC_y (y>x) and a gate electrode composed of a TaC_x single layer. Here, SiO_2 was used as the gate insulating film.

[0042] When the gate electrode was a TaC_x single layer (**M1**), the effective work function was about 4.7 eV. When the gate electrode was a TaC_x/TaC_y (y>x) (**M2**), the effective work function was about 4.2 eV. When the atom concentration of the gate electrode **M1** and that of the gate electrode **M2** were examined by a physical analysis, the result showed that the gate electrodes **M1** and **M2** had the same C atom concentration in a region 3 nm or more deeper than the gate insulating film/gate electrode interface. However, the C atom concentration in a region near the gate insulating film of the gate electrode was 52 at. % in the gate electrode **M1** and 63 at. % in the gate electrode **M2**. When these are expressed using the average x, this gives 1.96 for **M1** and 2.07 for **M2**. There is a x difference of 0.1 or more between **M1** and **M2**, which satisfies the condition for obtaining a Φ_{eff} difference of 0.4 eV or more. This fact has shown the validity of the aforementioned principle.

[0043] Hereinafter, referring to the accompanying drawings, embodiments of the invention will be explained. The configuration common to the individual embodiments are indicated by the same reference numerals and repeated explanations will be omitted.

First Embodiment

[0044] FIG. **6** is a sectional view of a schematic structure of a semiconductor device with a dual-metal-gate CMIS structure.

[0045] At the surface of an Si substrate **10** as a semiconductor substrate, a p-type semiconductor region **101** and an n-type semiconductor region **201** are provided. In the p-type semiconductor region **101**, an n-channel MIS transistor **100** is formed. In the n-type semiconductor region **201**, a p-channel MIS transistor **200** is formed. The p-type semiconductor region **101** and n-type semiconductor region **201** are formed to function as so-called wells. At the boundary part between the regions **101** and **201**, an element isolating region **11** to isolate them from each other is formed.

[0046] On the surface of the p-type semiconductor region **101**, a first gate insulating film **104** composed of an Si oxide film is formed. On the gate insulating film **104**, a first gate electrode **110** constituting a stacked structure is formed. A lower layer **111** (a first lower layer gate electrode) of the gate electrode **110** is composed of Ta—C alloy whose thickness is 1 monolayer or more and 3 nm or less. An upper layer (a first upper layer gate electrode) **112** is composed of Ta—C alloy. The average electronegativity x of the lower layer gate electrode **111** is 0.1 or more greater than the average x of the upper layer gate electrode **112**. This is equivalent to the C atom concentration of the lower layer gate electrode **111** being 10 at. % or more higher than the C atom concentration of the upper-layer gate electrode **112**.

[0047] On the surface of the n-type semiconductor region **201**, a second gate insulating film **204** composed of an Si oxide film is formed. On the surface of the gate insulating film **204**, a gate electrode (a second gate electrode) **210** composed of Ta—C alloy is formed. The gate electrode **210**, whose material is the same as that of the first upper layer gate electrode **112**, is formed at the same time the upper layer gate electrode **112** is formed.

[0048] On the gate electrode **210** and upper layer gate electrode **112**, high melting point metal, such as W or TiN, may be formed. In FIG. **6**, the remaining configuration, including an element isolating region **11**, source/drain regions **102**,**202**, extension regions **103**, **203**, and gate sidewall insulating films **120**, **220**, can be formed by conventional semiconductor processes. The sidewall insulating films **120**, **220** are made of the same material and formed at the same time.

[0049] Moreover, the gate insulating films **104**, **204** are made of the same material and formed at the same time. The formative material of the gate insulating films **104**, **204** is not necessarily limited to an Si oxide film and may be another insulating material. That is, the first embodiment is not restricted to a MOS structure and may be applied to a MIS structure.

[0050] Under the aforementioned principle, using the structure of the embodiment makes it possible to realize a dual-metal-gate CMIS structure using a metal gate. The lower layer gate electrode **111** of the gate electrode **110** of the n-channel MIS transistor **100** is very thin and the remaining gate electrode part (the upper layer gate electrode **112**) is made of the same material as that of the gate electrode **210** of the p-channel MIS transistor **200**. Therefore, the etching processes of gates can be carried out collectively, which makes it possible to simplify the manufacturing processes and reduces the manufacturing cost.

[0051] To lower the threshold voltages of both the n-channel MIS transistor **100** and the p-channel MIS transistor **200** sufficiently, it is desirable that the effective work function (Φ_{eff}(N)) of the n-channel MIS transistor **100** should be 4.3 eV or less and the effective work function (Φ_{eff}(P)) of the p-channel MIS transistor **200** should be 4.7 eV or more. In the first embodiment, the gate electrode **210** of the p-channel MIS transistor **200** is composed of a gate electrode single layer. Both Φ_{bulk} and $\Phi_{interface}$ are determined only by the nature of a single layer of TaC. Therefore, it is desirable that the gate electrode **210** should have an effective work function value of 4.7 or more.

[0052] The effective work function of the gate electrode **110** composed of a stacked structure on the n-channel MIS transistor **100** side is lower than the effective work function of the gate electrode **210** because of the electronegativity difference $\Delta\chi$ between the lower layer gate electrode **111** and upper layer gate electrode **112**. For the effective work function Φ_{eff}(N) of the gate electrode of the n-channel MIS transistor

100 to be 4.3 eV or lower, it is seen from equation (3) that $\Delta\chi$ has to satisfy the following expression:

$$\Phi_{eff}(P)-0.4\times\Delta\chi/0.1\leqq 4.3 \qquad (4)$$

[0053] The structure of the gate electrode on the gate insulating film side and the composition and thickness of the gate electrode can be examined by removing the MIS structure Si substrate and making XPS measurements (backside XPS measurements) via the gate insulating film. As the photoelectron detecting angle (TOA) in XPS measurements is made lower, information on the gate electrode in a region shallower than the gate insulating film/gate electrode interface is obtained. As TOA is made higher, information on the gate electrode in a region deeper than the gate insulating film/gate electrode interface is obtained. Therefore, changing TOA makes it possible to examine the composition of the gate electrode at a desired depth from the gate insulating film/gate metal interface. The cross section structure of the gate electrode/gate insulating film can be analyzed by the TEM-EELS method.

[0054] The structure of the gate electrodes **M1** and **M2** in FIG. **5** used in explaining the principle and its composition and thickness were obtained from backside XPS measurements.

[0055] Furthermore, TaC_x with a strong TaC (111) orientation is used effectively as the gate electrode **210** of the p-channel MIS transistor **200**. The reason is that the effective work function of crystallized TaC_x depends on its crystal face and the TaC (111) plane has a particularly high effective work function. This is because the plane in contact with the insulating film is the TaC (111) plane, $\Phi_{interface}$ is large. If the crystalline orientation rate [TaC (111) plane/{TaC (111) plane+TaC (200) plane}] is 80% or more, it is known that the effect will be obtained.

[0056] That is, the gate electrode **210** of the p-channel MIS transistor **200** is composed of TaC_x where the crystalline orientation rate [TaC (111) plane/{TaC (111) plane+TaC (200) plane}] is 80% or more, the effective work function of the gate electrode **210** of the p-channel MIS transistor **200** is greater than the effective work function when uncrystallized Ta—C alloy is used. For this reason, the difference between the effective work function of the gate electrode **110** of the n-channel MIS transistor **100** and the effective work function of the gate electrode **210** of the p-channel transistor **200** can be obtained more easily.

[0057] Even if in the n-channel MIS transistor **100**, TaC_x with a strong TaC (111) orientation is used as the upper layer gate electrode **112**, the effective work function will not become greater as a result control of orientation since the upper layer gate electrode **112** is not directly in contact with the gate insulating film **104**.

[0058] The fact that the work function can be changed by controlling the crystalline orientation has been found and already proposed by the inventors (JP-A 2007-165414 (KOKAI)). Hereinafter, the proposition will be explained briefly.

[0059] Since the work function of a TaC_x electrode was 4.18 eV in the prior art, a TaC_x electrode was generally used only in an n-channel MIS transistor. Even if conventional TaC_x were used for the gate electrode of a p-channel MIS transistor, its threshold voltage would be very high and therefore the CMIS could not operate properly.

[0060] The inventors set the Ta—C composition ratio (C/Ta) to 0.5 to 1.5 and used TaC_x in a crystallized state. Furthermore, the inventors has newly found that making (111) orientation stronger enables a work function of about 4.8 eV close to p^+ silicon to be obtained and increasing the (200) orientation component for (111) orientation enables a work function close to n^+ silicon to be obtained. Then, this was applied to the dual metal gate of the CMIS transistor.

[0061] FIG. **7** shows the result of the experiments to examine the crystalline characteristics of a TaC_x thin film of 100 nm in film thickness. The abscissa indicates angles (2θ) and the ordinate indicates strength. To make it possible to distinguish between the characteristic of a pMIS TaC electrode and that of a NMIS TaC electrode, offsetting is done in the ordinate direction. Both of them have a TaC_x film composition of C/Ta to 1. Depending on a difference in the film forming method, the TaC_x films were divided into those with the strongest (111) diffraction peak and those with the strongest (200) diffracting peak.

[0062] The above description has shown the result of using an analysis sample of a TaC film/gate insulating film/Si substrate. Such experiments can, of course, be performed on a finished transistor. In that case, the gate electrode part of the transistor is cut off by the pickup method used in TEM observation and the cross section of the gate electrode is analyzed by an electron diffraction method, which makes it possible to verify the ratio of (111) orientation to (200) orientation. In this case, since an electron beam in the TEM method is used, the positioning accuracy of the analysis position is high. This makes it easy to verify the orientation of the TaC film in the region in contact with the gate insulating film strongly related to actual threshold voltage control.

[0063] FIG. **8** shows a change in the work function when the orientation is changed as described above. Since TaC_x presents a work function of 4.75 eV or more equivalent to that of p^+ silicon, it is seen that the crystalline orientation rate of the (111) plane shown in expression (5) below has to be 80% or more:

$$\text{Tac (111) peak intensity}/\{\text{TaC (111) peak intensity}+\text{TaC (200) peak intensity}\}\times 100 \qquad (5)$$

[0064] Here, the (111) plane crystalline orientation rate is calculated from expression (5) by determining the absolute value of the TaC (111) peak intensity and TaC (200) peak intensity from the XRD spectrum in FIG. **9**. In place of the peak intensity, a peak area may be used. When the (111) plane crystalline orientation rate is determined, the direction perpendicular to the plane adjacent to the gate insulating film of the gate electrode, that is, the direction of the film thickness of the gate electrode, is used as a reference.

[0065] As described above, TaC_x with a strong TaC (111) orientation is used effectively as the gate electrode **210** of the p-channel MIS transistor **200**.

[0066] Since TaC is used as gate electrode material, the first embodiment has the following advantage.

[0067] As for Ta and C used as gate electrode materials in the first embodiment, the electronegativity x of Ta is 1.5 and the electronegativity x of C is 2.5, with the result that the difference in x between them is large. This means that changing the C composition percentage in TaC_x enables the average electronegativity x to be changed greatly. For example, suppose Mo is used in place of Ta. Since the x of Mo is 2.16 close to that of C, even if the C composition percentage in MoCx is changed, the average electronegativity x cannot be changed greatly.

[0068] Since TaC has excellent heat resistance, it is suitable for gate electrode material. As described above, if a material in which the electronegativity difference between the individual atoms is large as in TaC and which has excellent heat resistance can be used as a gate electrode material. In addition to TaC, TiC, TaN and TiN may be used.

[0069] Furthermore, the lower layer gate electrode **111** of the gate electrode **110** of the n-channel MIS transistor **100** may be composed of Ta—C alloy including impurity atoms. Putting impurity atoms whose electronegativity is higher than that of C in the part of the lower layer gate electrode **111** makes it easier to set the average electronegativity difference between the lower layer gate electrode **111** and upper layer gate electrode **112** to 0.1 or more. For this reason, N, O, F, P, S, Cl, As, Se, Br, and I can be used as impurity atoms. Of them, F, P, and As are particularly preferred because they are established as general impurity dopant in semiconductor manufacturing processes.

[0070] Next, an example of a semiconductor device manufacturing method according to the first embodiment will be explained with reference to FIGS. **10**A to **10**D.

[0071] First, as shown in FIG. **10**A, after a p-type semiconductor region **101** and an n-type semiconductor region **201** isolated with an element isolating region **11** are formed on an Si substrate **10**, gate insulating films **14** (**104**, **204**) are formed at the substrate surface. The gate insulating film may be an oxide film, such as SiO_2, or a high dielectric film. Hafnium nitride silicate (e.g., HfSiON), lanthanum hafnate (e.g., $La_2Hf_2O_7$), and lanthanum aluminate (e.g., $LaAlO_3$) are particularly preferred. Amorphous materials are more preferred. Then, a C layer **15** is selectively deposited only on the gate insulating film **104** on the n-channel MIS transistor **100** side.

[0072] Next, as shown in FIG. **10**B, on the gate insulating film **14** on the p-channel MIS transistor **200** side and on the C layer **15** on the n-channel MIS transistor **100** side, Ta—C alloys **16** (**112**, **210**) are formed simultaneously.

[0073] Here, the alternate arrangement of a Ta layer and a C layer in the film thickness direction is effective in forming a pMIS TaC electrode with (111) plane crystalline orientation rate of 80% or more efficiently as the Ta—C alloy 16. The principle of the film forming method is schematically shown in FIGS. **11**A to **11**C. Tac takes a cubical crystal structure. Its (111) plane has a structure where a Ta layer and a C layer are stacked alternately. Therefore, the same atomic position as that of a TaC (111) plane is formed intentionally, which enables a TaC thin film oriented to a (111) plane to be obtained more efficiently.

[0074] Such a manufacturing method can be realized by an ALD method. Specifically, a Ta source and a C source are supplied layer by layer alternately as shown FIGS. **11**A to **11**C. Here, relatively high vapor pressure materials, such as chloride series, amide series, or imide series, can be used as a Ta source. Acetylene, CH_4, C_2H_4, CCl_4, or CO can be used as a C source.

[0075] Furthermore, the aforementioned manufacturing method can be realized using sputtering techniques. In this case, a multi-cathode sputtering unit with a plurality of cathodes is used and a Ta target and a C target are installed. Sputtering for one layer of Ta target and sputtering for one layer of C target are performed alternately, thereby forming a pMIS TaC thin film.

[0076] Here, the formation of a film on the gate insulating film may be started with C or Ta, which does not have a great effect on the quality of (111) plane orientation.

[0077] Next, the structure shown in FIG. **10**B is heat-treated to mix the C layer **15** and the Ta—C alloy 16 on the C layer **15**, thereby forming a gate electrode lower layer **111**, which produces a structure shown in FIG. **10**C. Here, the composition of the gate electrode lower layer **111** can be controlled by the thickness of the C layer **15**. Actually, the thicker the C layer **15**, the C richer the composition of the gate electrode lower layer **111** becomes. As shown in FIG. **12**, it has been verified that, if the thickness is 1.5 nm or more, the effective work function difference between the n-channel MIS transistor **100** and p-channel MIS transistor **200** is 0.4 eV or more.

[0078] However, if the gate electrode lower layer **111** formed by combining the C layer **15** and the Ta—C alloy of the upper electrode is 3 nm or more, the gate electrode lower layer also has an effect on Φ_{bulk} as described above. To avoid this, it is desirable that the thickness of the C layer **15** should be 2.5 nm or less. Although a method of depositing the C layer **15** is not limited in particular, it is desirable to use an atomic layer deposition (ALD) method capable of forming uniform thin films. Although a method of forming a Ta—C alloy 16 is not limited in particular, for example, CVD techniques, vapor-deposition techniques, or sputtering techniques may be used.

[0079] Next, by lithography and etching, such as RIE, the gate insulating film **14**, Ta—C alloy 16 and the gate electrode lower layer **111** are processed simultaneously with the n-channel MIS transistor **100** and p-channel MIS transistor **200**, which produces a structure shown in FIG. **10**D.

[0080] From this point on, by known processes, extension regions **103**, **203** are formed at the surface of each of the semiconductor regions **101**, **201** with the gate parts as a mask and then gate sidewall insulating films **120**, **220** are formed. Then, with the gate parts and sidewall insulating films **120**, **220** as a mask, source/drain regions **102**, **202** are formed at the surfaces of the semiconductor regions **101**, **201** respectively, which produces a structure shown in FIG. **6**.

[0081] As described above, with the first embodiment, in the dual-metal-gate CMIS structure where the n-channel MIS transistor **100** and p-channel MIS transistor **200** have been formed on the substrate, TaC is used as a gate electrode material, the gate electrode **110** of the n-channel MIS transistor **100** is caused to have a stacked structure of the lower layer gate electrode **111** and upper layer gate electrode **112**, the average electronegativity of the upper layer gate electrode **112** is made 0.1 or more smaller than the average electronegativity of the lower layer gate electrode **111**, and the metal material of the gate electrode **210** of the p-channel MIS transistor **200** is the same as that of the upper layer gate electrode **112** of the n-channel MIS transistor **100**. With this configuration, the effective work function of the gate electrode **210** of the p-channel MIS transistor **200** can be made 0.4 eV or more higher than the effective work function of the gate electrode **110** of the n-channel MIS transistor **100**.

[0082] In this case, since the upper layer gate **112** of the n-channel MIS transistor **100** and the gate electrode **210** of the p-channel MIS transistor **200** have both the same composition of TaC and the lower layer gate electrode **111** of the n-channel MIS transistor **100** is very thin, the etching processes of the gates can be carried out collectively. Furthermore, although the lower layer electrode **111** of the n-channel MIS transistor **100** is made of TaC and differs in composition from the upper layer gate electrode **112** of the n-channel MIS transistor **100** and the gate electrode **210** of the p-channel MIS transistor **200**, they are the same in constituent elements. Therefore, when electrodes are formed, another material is not needed.

Accordingly, it is possible to simplify the manufacturing processes and reduce the manufacturing cost.

Second Embodiment

[0083] FIG. **13** is a sectional view showing a schematic structure of a semiconductor device with a dual-metal-gate CMIS structure.

[0084] A first gate insulating film **104** is formed at the surface of a p-type semiconductor region **101**. On the surface of the gate insulating film **104**, a gate electrode (a first gate electrode) **110** made of Ta—C alloy is formed.

[0085] A second gate insulating film **204** is formed at the surface of an n-type semiconductor region **201**. On the gate insulating film **204**, a second gate electrode **210** with a stacked structure is formed. A lower layer (a second lower layer gate electrode) **211** of the gate electrode **210** is made of Ta—C alloy whose thickness is 1 monolayer or more and 3 nm or less. An upper layer (a second upper layer gate electrode) **212** of the gate electrode is made of Ta—C alloy. Here, the average electronegativity x of the lower layer gate electrode **211** is 0.1 or more smaller than the average electronegativity x of the upper layer gate electrode **212**. This is equivalent to the C atom concentration of the lower layer gate electrode **211** being 10 at. % or more lower than the C atom concentration of the upper layer gate electrode **212**.

[0086] On the gate electrode **110** and upper layer gate electrode **212**, high melting point metal, such as W or TiN, may be further formed. In FIG. **13**, the remaining configuration, including element isolating regions **11**, source/drain regions **102**, **202**, extension regions **103**, **203**, and gate sidewall insulating films **120**, **220**, can be formed by conventional semiconductor processes.

[0087] In contrast to the first embodiment described above, the second embodiment is such that the gate electrode **210** of the p-channel MIS transistor **200** has a stacked structure including an upper layer and a lower layer. Under the same principle as that of the first embodiment, a dual-metal-gate CMIS structure using metal gates can be realized.

[0088] Moreover, as in the first embodiment, the lower layer gate electrode **211** of the gate electrode **210** of the p-channel MIS transistor **200** is very thin and the remaining electrode part (the upper layer gate electrode **212**) is the same as the gate electrode **110** of the n-channel MIS transistor **100**. For this reason, the etching processes of the gates can be carried out collectively, which produces the same effect as that of the first embodiment.

[0089] Furthermore, in contrast to the first embodiment, the second embodiment is such that the gate electrode **110** of the n-channel MIS transistor **100** is composed of a gate electrode single layer and both Φ_{bulk} and $\Phi_{interface}$ are determined only by a single layer of TaC. For this reason, in the second embodiment, to fulfill the expressions $\Phi_{eff}(P) \geqq 4.7$ eV and $\Phi_{eff}(N) \leqq 4.3$ eV, it is seen from equation (3) that the gate electrode **110** has an effective work function of 4.3 or less and the absolute value $\Delta\chi$ of the average electronegativity difference between the gate electrode **110** and gate electrode **210** has to satisfy the following expression:

$$\Phi_{eff}(N)+0.4\times\Delta\chi/0.1\geqq 4.7 \tag{6}$$

[0090] In the second embodiment, TaC_x with a strong TaC (100) orientation is used effectively as the gate electrode **110** of the n-channel MIS transistor **100**. The low effective work function of the TaC (100) plane is used here. It is known that, when the crystalline orientation rate [TaC (111) plane/{TaC (111) plane+TaC (200) plane}] of the TaC (111) plane in the film thickness direction is 60% or less, the effective work function is sufficiently low under the influence of the TaC (100) plane. If the gate electrode **110** of the n-channel MIS transistor **100** is made of TaC_x where the crystalline orientation rate [TaC (111) plane/{TaC (111) plane+TaC (200) plane}] in the TaC (111) plane is 60% or less, the effective work function of the gate electrode **110** of the n-channel MIS transistor **100** is smaller than the effective work function when uncrystallized Ta—C alloy is used. For this reason, the difference between the effective work function of the gate electrode **110** of the n-channel MIS transistor **100** and the effective work function of the gate electrode **210** of the p-channel transistor **200** can be obtained more easily.

[0091] Furthermore, the lower layer gate electrode **211** of the gate electrode **210** of the p-channel MIS transistor **200** may be composed of Ta—C alloy including impurity atoms. Putting impurity atoms whose electronegativity is smaller than that of Ta in the part of the lower layer gate electrode **211** makes it easier to set the average electronegativity difference between the lower layer gate electrode **211** and upper layer gate electrode **212** to 0.1 or more. Therefore, it is desirable that Sc, Y, La, Zr, or Hf should be used as impurity atoms. Moreover, those classified into lanthanoid (Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu), actinoid (Th, Pa, U, Np, Pu, Am, Cm, Bk, Cf, Es, Fm, Md, No, Lr) or alkaline earth metal (Mg, Ca, Sr, Ba, Ra) may be used as impurity atoms.

[0092] A manufacturing method of the second embodiment is basically the same as that of the first embodiment, except that the gate of the n-channel MIS transistor **110** has to be of a single layer and the gate of the p-channel MIS transistor **200** has to be of a stacked layer. This type of device can be manufactured by changing, for example, the process of FIG. **10**A in the manufacturing method of the first embodiment to the process of selectively depositing a Ta layer only on the gate insulating film **204** of the p-channel MIS transistor **200**.

[0093] Furthermore, as explained above, in the second embodiment, when the gate electrode **110** of the n-channel MIS transistor **100** and the upper layer gate electrode **212** of the p-channel MIS transistor **200** are formed, it is desirable to form an NMIS TaC_x electrode where the (111) plane crystalline orientation rate is 60% or less.

[0094] To form an nMIS TaC_x electrode where the (111) plane crystalline orientation rate is 60% or less, it is important to form a film so as to prevent Ta and C from existing alternately in the film thickness direction unlike the formation of the pMIS TaC_x electrode explained in the first embodiment. FIGS. **14**A to **14**C schematically show the film forming principle.

[0095] To form an nMIS TaC_x electrode by CVD techniques, it is important to supply a Ta source and a C source at the same time. This causes a TaC film to be formed, while Ta and C coexist in a single layer, which makes a (111) plane less liable to be formed and instead a (200) plane more liable to be formed. Here, the Ta source and C source may be the same as those used in forming the pMIS TaC_x electrode.

[0096] When sputtering techniques are used, it is desirable to use simultaneous sputtering of the Ta target and C target. In this case, unlike the pMIS TaC_x electrode forming method, sputtering Ta and C at the same time makes the (111) plane less liable to be formed and the (200) plane more liable to be formed. In the second embodiment, a TaC_x film with C/Ta=1.0 was deposited to a thickness of 100 nm by the simultaneous sputtering of the Ta target and C targets, or two targets. The deposition of the film may be carried out CVD techniques or MBE techniques.

[0097] Unlike in the first embodiment, in the second embodiment, the gate electrode **210** of the p-channel MIS transistor **200** is caused to have a stacked structure of the lower layer gate electrode **211** and upper layer gate electrode **212**, the average electronegativity of the upper layer gate electrode **212** is made 0.1 or more greater than the average electronegativity of the lower layer gate electrode **211**, and the metal material of the gate electrode **110** of the n-channel MIS transistor **100** is made the same as that of the upper layer gate electrode **212** of the p-channel MIS transistor **200**. This makes it possible to make the effective work function of the gate electrode **210** of the p-channel MIS transistor **200** 0.4 eV or more higher than the effective work function of the gate electrode **110** of the n-channel MIS transistor **100**.

[0098] In this case, since the upper layer gate **212** of the p-channel MIS transistor **200** and the gate electrode **110** of the n-channel MIS transistor **100** have both the same composition of TaC and the lower layer gate electrode **211** of the p-channel MIS transistor **200** is very thin, the etching processes of the gates can be carried out collectively. Furthermore, although the lower layer electrode **211** of the p-channel MIS transistor **200** is made of TaC and differs in composition from the upper layer gate electrode **212** of the p-channel MIS transistor **200** and the gate electrode **110** of the n-channel MIS transistor **100**, they are the same in constituent elements. Therefore, when electrodes are formed, another material is not needed. Accordingly, the same effect as that of the first embodiment is obtained.

Third Embodiment

[0099] FIG. **15** is a sectional view showing a schematic structure of a semiconductor device with a dual-metal-gate CMIS structure.

[0100] A first gate insulating film **104** is formed at the surface of a p-type semiconductor region **101**. On the gate insulating film **104**, a first gate electrode **110** having a stacked structure is formed. A lower layer (a first lower layer gate electrode) **111** of the gate electrode **110** is composed of Ta—C alloy whose thickness is 1 monolayer or more and 3 nm or less. An upper layer (a first upper layer gate electrode) **112** of the gate electrode is composed of Ta—C alloy. The average electronegativity x of the lower layer gate electrode **111** is greater than the average electronegativity x of the upper layer gate electrode **112**. This is equivalent to the C atom concentration of the lower layer gate electrode **111** being higher than the C atom concentration of the upper layer gate electrode **112**.

[0101] A second gate insulating film **204** is formed at the surface of an n-type semiconductor region **201**. On the surface of the gate insulating film **204**, a second gate electrode **210** having a stacked structure is formed. A lower layer (a second lower layer gate electrode) **211** of the gate electrode **210** is composed of Ta—C alloy whose thickness is 1 monolayer or more and 3 nm or less. An upper layer (a second upper layer gate electrode) **212** of the gate electrode is composed of Ta—C alloy. The average electronegativity x of the lower layer gate electrode **211** is smaller than the average electronegativity x of the upper layer gate electrode **212**. This is equivalent to the C atom concentration of the lower layer gate electrode **211** being lower than the C atom concentration of the upper layer gate electrode **212**. The material of the upper layer gate electrode **212** on the pMIS side is the same as that of the upper gate electrode **112** on the nMIS side. The upper layer gate electrode **212** is formed at the same time the upper layer gate electrode **112** is formed.

[0102] The sum of the absolute value of the difference in average x between the lower layer gate electrode **211** and the upper layer gate electrode **212** and the absolute value of the difference in average x between the lower layer gate electrode **111** and the upper layer gate electrode **112** is 0.1 or more. This is equivalent to the atom density of C at the lower gate electrode **111** being 10 at. % higher than the atom density of C at the lower gate electrode **211**.

[0103] On the upper layer gate electrodes **112**, **212**, high melting point metal, such as W or TiN, may be further formed. In FIG. **15**, the remaining configuration, including element isolating regions **11**, source/drain regions **102**, **202**, extension regions **103**, **203**, and gate sidewall insulating films **120**, **220**, can be formed by conventional semiconductor processes.

[0104] The third embodiment is a combination of the n-channel MIS transistor **100** of the first embodiment and the p-channel MIS transistor **200** of the second embodiment. Although the third embodiment is at a disadvantage in that the number of manufacturing processes increases as compared with the first and second embodiments, it has the advantage of being capable of determining the effective work function difference between the gate electrode of the n-channel MIS transistor **100** and that of the p-channel MIS transistor **200** more easily. That is, since the gate electrode of the n-channel MIS transistor **100** and that of the p-channel MIS transistor **200** both have a stacked structure, the x difference between the upper layer and lower layer of each gate electrode is allowed to be smaller than the x difference between the upper layer and lower layer of the gate electrode in each of the first and second embodiments.

[0105] In the third embodiment, to satisfy the expressions $\Phi_{eff}(P) \geqq 4.7$ eV and $\Phi_{eff}(N) \leqq 4.3$ eV, it follows from equation (3) that the absolute value $\Delta\chi(1)$ of the electronegativity difference between the lower layer gate electrode **111** and upper layer gate electrode **112** and the absolute value $\Delta\chi(2)$ of the electronegativity difference between the lower layer gate electrode **211** and upper layer gate electrode **212** have to satisfy the following expressions:

$$\Phi_{eff}(1) - 0.4 \times \Delta\chi(1)/0.1 \leqq 4.3$$

$$\Phi_{eff}(2) + 0.4 \times \Delta\chi(2)/0.1 \geqq 4.7$$

[0106] Here, $\Phi_{eff}(1)$ and $\Phi_{eff}(2)$ are the Φ_{eff} of a gate electrode composed of the same metal material single layer as that of each of the upper layer gate electrode **112** and upper layer gate electrode **212**.

[0107] The structure of the third embodiment can be manufactured by combining the manufacturing processes of the first embodiment and the manufacturing processes of the second embodiment.

[0108] (Modification)

[0109] This invention is not limited to the above-described embodiments. While in the embodiments, TaC has been used as the gate electrodes, TiC, TaN, or TiN may be used in place of TaC. The thickness of the lower layer gate electrode may be changed suitably, provided that it is in the range of 1 monolayer or more and 3 nm or less. Similarly, the average electronegativity difference between the lower layer gate electrode and upper layer electrode and further the relationship between the atom density of C at the lower gate electrode and the atom density of C at the upper gate electrode may be changed suitably in the scope explained in the embodiments.

Furthermore, the gate insulating film is not limited to a silicon oxide film and may be a silicon nitride film, or a silicon oxidized nitride film, or further another high-k dielectric film.

[0110] Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A method for manufacturing a semiconductor device having an nMIS transistor and a pMIS transistor, comprising:

forming a p-type semiconductor region and an n-type semiconductor region in a surface of a substrate;

forming a first gate insulating film on the p-type semiconductor region and forming a second gate insulating film on the n-type semiconductor region;

forming a first metallic film made of a metal material above the second gate insulating film and forming a laminated structure of a second metallic film made of a material having a higher electronegativity than the metal material and a third metallic film made of the metal material above the first gate insulating film;

performing heat treatment to form a mixed film obtained by mixing the second metallic film and a part of the third metallic film in such a manner that the mixed film comes into contact with the first gate insulating film;

processing the first metallic film, the third metallic film and the mixed film to have a gate pattern to form a gate electrode for the nMIS transistor above the p-type semiconductor region and form a gate electrode for the pMIS transistor above the n-type semiconductor region.

2. The method according to claim **1**, wherein

a film thickness of the mixed film is one monolayer or more and 3 nm or less, and an average electronegativity of the metal material is smaller than an average electronegativity of the mixed film by 0.1 or more.

3. The method according to claim **1**, wherein

an effective work function $\Phi_{eff}(2)$ of the metal material is 4.7 eV or more, and an average electronegativity difference $\Delta\chi(1)$ between the mixed film and the metal material satisfies a following expression:

$$\Phi_{eff}(2)-0.4\times\Delta\chi(1)/0.1\leqq 4.3$$

4. The method according to claim **1**, wherein

the metal material is Ta—C alloy.

5. The method according to claim **4**, wherein

the first metallic film has a crystalline orientation rate [TaC (111) plane/{TaC (111) plane+TaC (200) plane}] of 80% or more in a film thickness direction of the metallic film.

6. The method according to claim **1**, wherein

the metal material is Ti—N alloy.

7. A method for manufacturing a semiconductor device having an nMIS transistor and a pMIS transistor, comprising:

forming a p-type semiconductor region and an n-type semiconductor region in a surface of a substrate;

forming a first gate insulating film on the p-type semiconductor region and forming a second gate insulating film on the n-type semiconductor region;

forming a first metallic film made of a metal material above the first gate insulating film and forming a laminated structure of a second metallic film made of a material having a lower electronegativity than the metal material and a third metallic film made of the metal material above the second gate insulating film;

performing heat treatment to form a mixed film obtained by mixing the second metallic film and a part of the third metallic film in such a manner that the mixed film comes into contact with the second gate insulating film;

processing the first metallic film, the third metallic film and the mixed film to have a gate pattern to form a gate electrode for the nMIS transistor above the p-type semiconductor region and form a gate electrode for the pMIS transistor above the n-type semiconductor region.

8. The method according to claim **7**, wherein

a film thickness of the mixed film is one monolayer or more and 3 nm or less, and an average electronegativity of the metal material is larger than an average electronegativity of the mixed film by 0.1 or more.

9. The method according to claim **7**, wherein

an effective work function $\Phi_{eff}(1)$ of the metal material is 4.3 eV or less, and absolute value of an average electronegativity difference $\Delta\chi(2)$ between the mixed film and the metal material satisfies a following expression:

$$\Phi_{eff}(1)+0.4\times\Delta\chi(2)/0.1\geqq 4.7$$

10. The method according to claim **7**, wherein

the metal material is Ta—C alloy.

11. The method according to claim **10**, wherein

the mixed film is made of Ta—C alloy and a C atom density of the mixed film is 10 at. % or more lower than a C atom density of the metal material.

12. The method according to claim **11**, wherein

the mixed layer is made of a metal material obtained by adding at least one of Sc, Y, La, Zr and Hf to Ta—C alloy.

13. The method according to claim **11**, wherein

the first metallic film has a crystalline orientation rate [TaC (111) plane/{TaC (111) plane+TaC (200) plane}] of 60% or less in a film thickness direction of the metallic film.

14. The method according to claim **7**, wherein

the metal material is Ti—N alloy.

15. A method for manufacturing a semiconductor device having an nMIS transistor and a pMIS transistor, comprising:

forming a p-type semiconductor region and an n-type semiconductor region in a surface of a substrate;

forming a first gate insulating film on the p-type semiconductor region and forming a second gate insulating film on the n-type semiconductor region;

forming a laminated structure of a first metallic film made of a metal material and a second metallic film made of a material having a higher electronegativity than the metal material above the first gate insulating film, and forming a laminated structure of a third metallic film made of the metal material and a fourth metallic film made of a material having a lower electronegativity than the metal material above the second gate insulating film;

performing heat treatment to form a first mixed film obtained by mixing the second metallic film and a part of the first metallic film in such a manner that the first mixed film comes into contact with the first gate insulating film and form a second mixed film obtained by mixing the fourth metallic film and a part of the third metallic film in such a manner that the second mixed film comes into contact with the second gate insulating film;

processing the first metallic film, the third metallic film, the first mixed film and the second mixed film to have a gate pattern to form a gate electrode for the nMIS transistor above the p-type semiconductor region and form a gate electrode for the pMIS transistor above the n-type semiconductor region.

16. The method according to claim **15**, wherein

a film thickness of each of the first mixed film and the second mixed film is one monolayer or more and 3 nm or less, and an average electronegativity of the metal material is smaller than an average electronegativity of the first mixed film and larger than an average electronegativity of the second mixed film.

17. The method according to claim **16**, wherein

a sum of absolute value of an average electronegativity difference $\Delta\chi(1)$ between the first mixed film and the metal material and absolute value of an average electronegativity difference $\Delta\chi(2)$ between the second mixed film and the metal material is 0.1 or more.

18. The method according to claim **15**, wherein

the metal material is Ta—C alloy.

19. The method according to claim **18**, wherein

the first mixed film and the second mixed film are made of Ta—C alloy, a C atom density of the first mixed film is higher than a C atom density of the metal material, a C atom density of the second mixed film is lower than the C atom density of the metal material, and the C atom density of the first mixed film is 10 at. % or more higher than the C atom density of the second mixed film.

20. The method according to claim **15**, wherein

the metal material is Ti—N alloy.

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