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(54) CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCER AND METHOD OF FABRICATING THE SAME

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(52) **U.S. Cl.**
CPC ***B81B 7/007*** (2013.01); ***B81C 1/00301*** (2013.01); ***B06B 1/0292*** (2013.01)

(57) **ABSTRACT**

A capacitive micromachined ultrasonic transducer and a method of fabricating the same are provided. The capacitive micromachined ultrasonic transducer includes a device substrate including a first trench defining a plurality of first portions corresponding to an element and a second trench spaced apart from the first trench; a supporting unit provided on the device substrate, the supporting unit defining a plurality of cavities; a membrane provided on the supporting unit to cover the plurality of cavities; a top electrode electrically connected to a second portion in the second trench through a via hole penetrating through the membrane and the supporting unit; and a through silicon via (TSV) substrate provided on a bottom surface of the device substrate, the TSV substrate including a first via metal connected to the plurality of first portions corresponding to the element and a second via metal connected to the second portion.

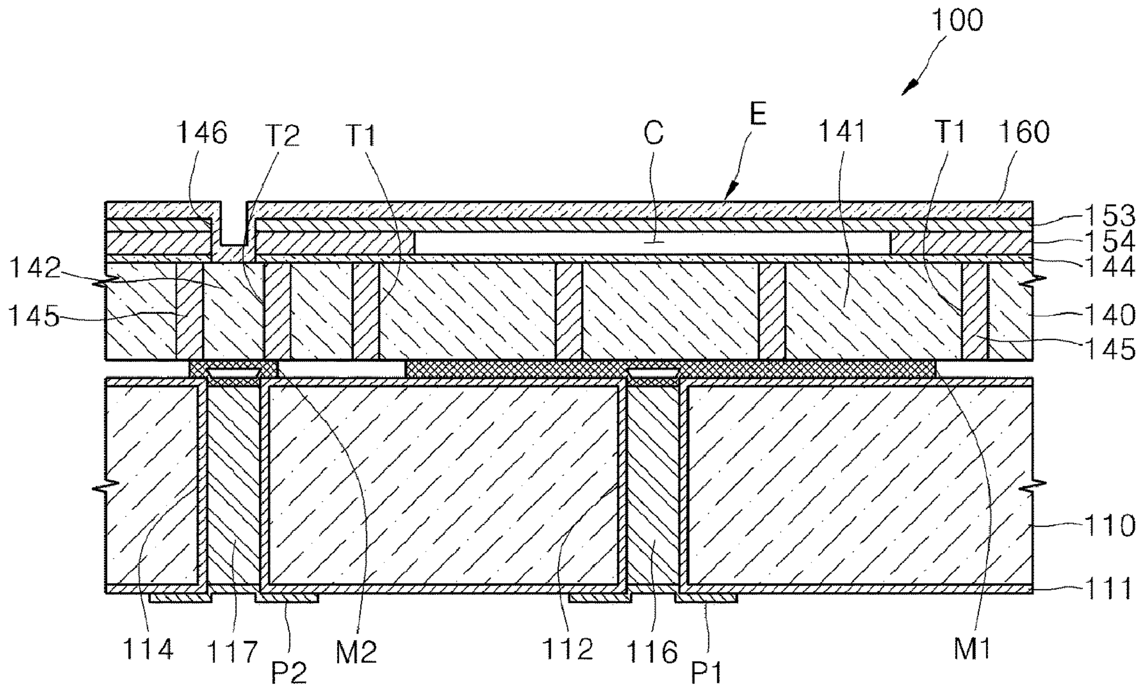


FIG. 1

100
M2
141
E
145
145
T2
M1
T1
III
III'
147

FIG. 2

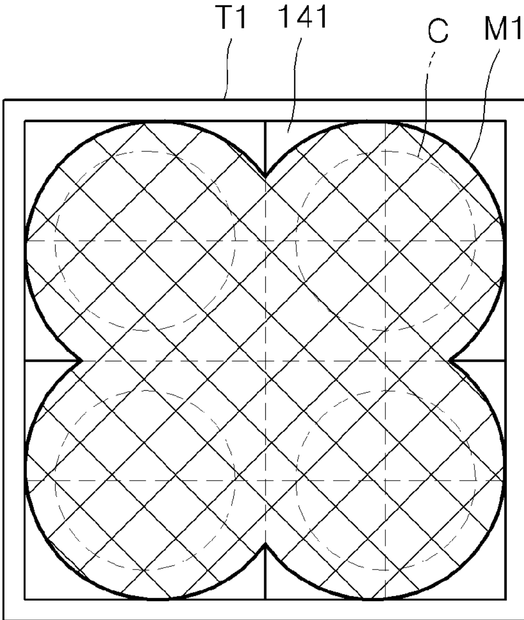


FIG. 3

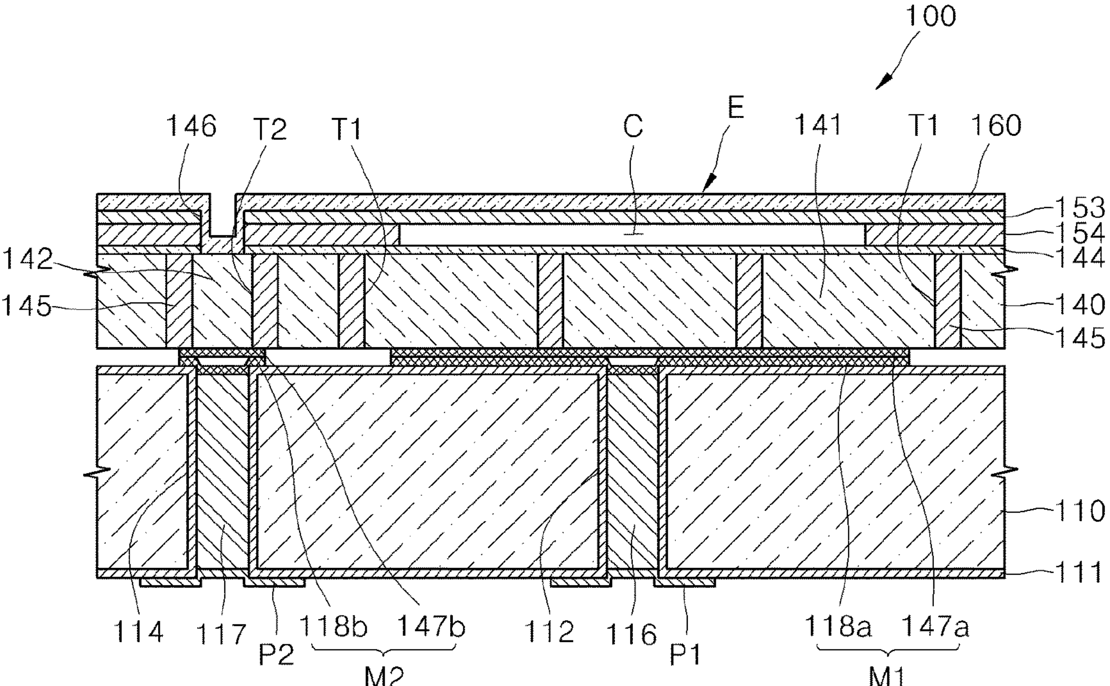


FIG. 4A

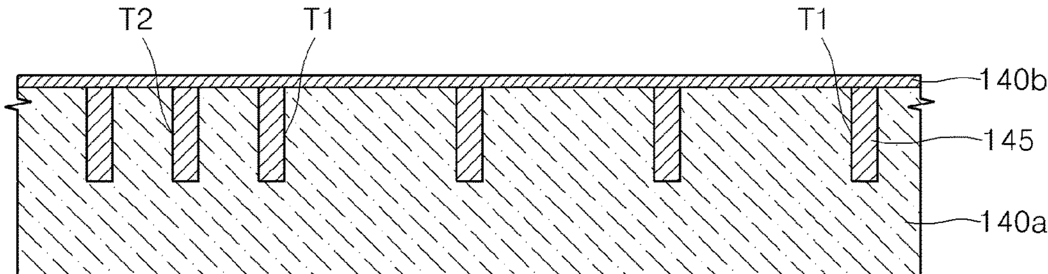


FIG. 4B

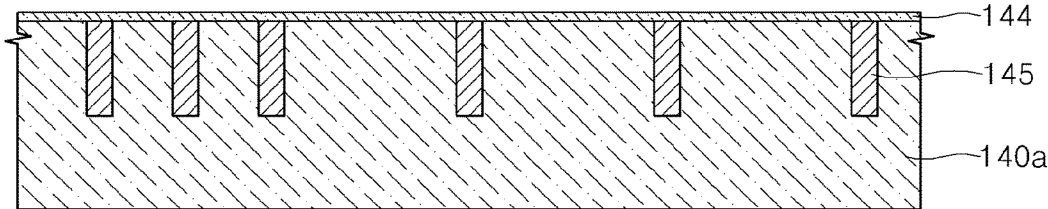


FIG. 4C

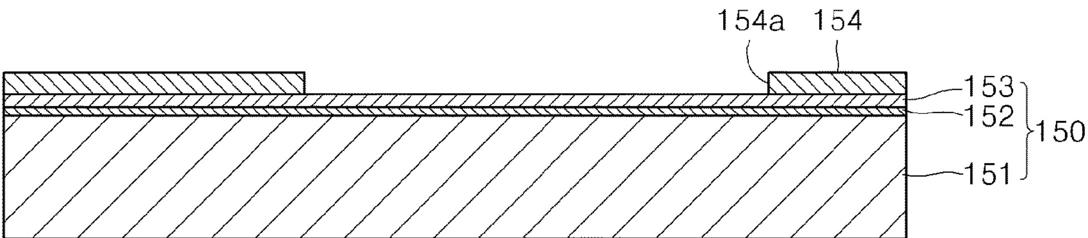


FIG. 4D

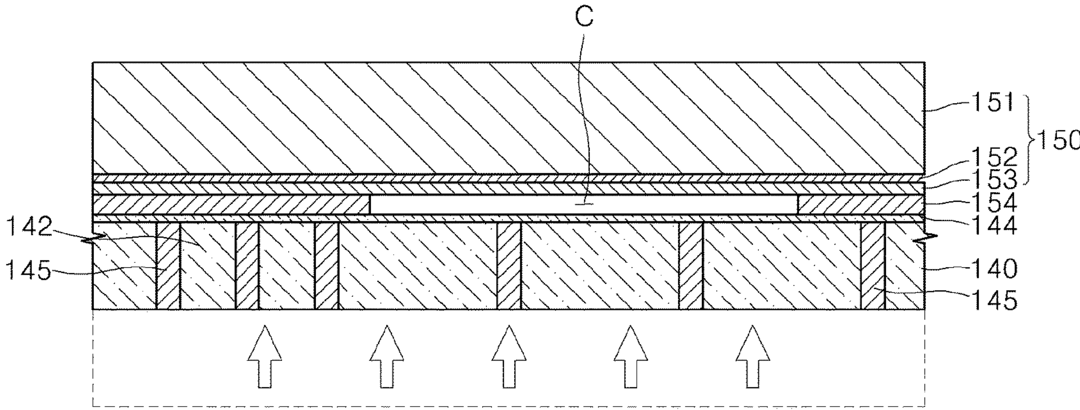


FIG. 4E

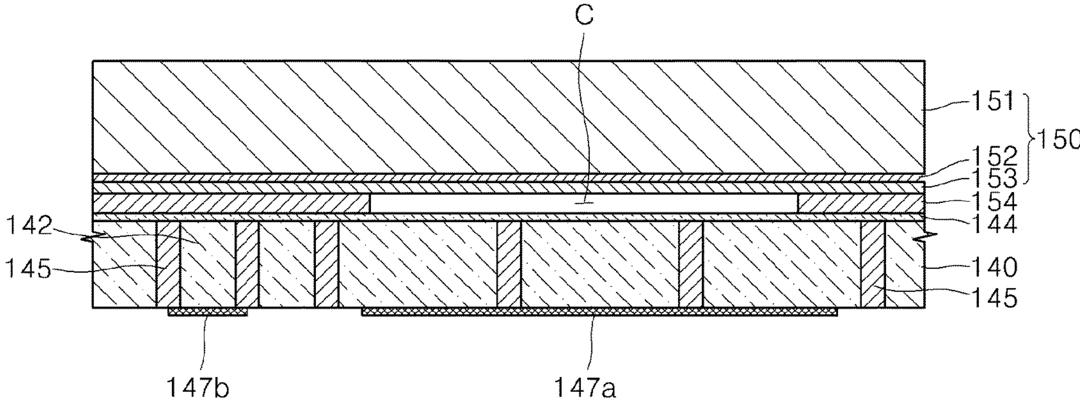


FIG. 4F

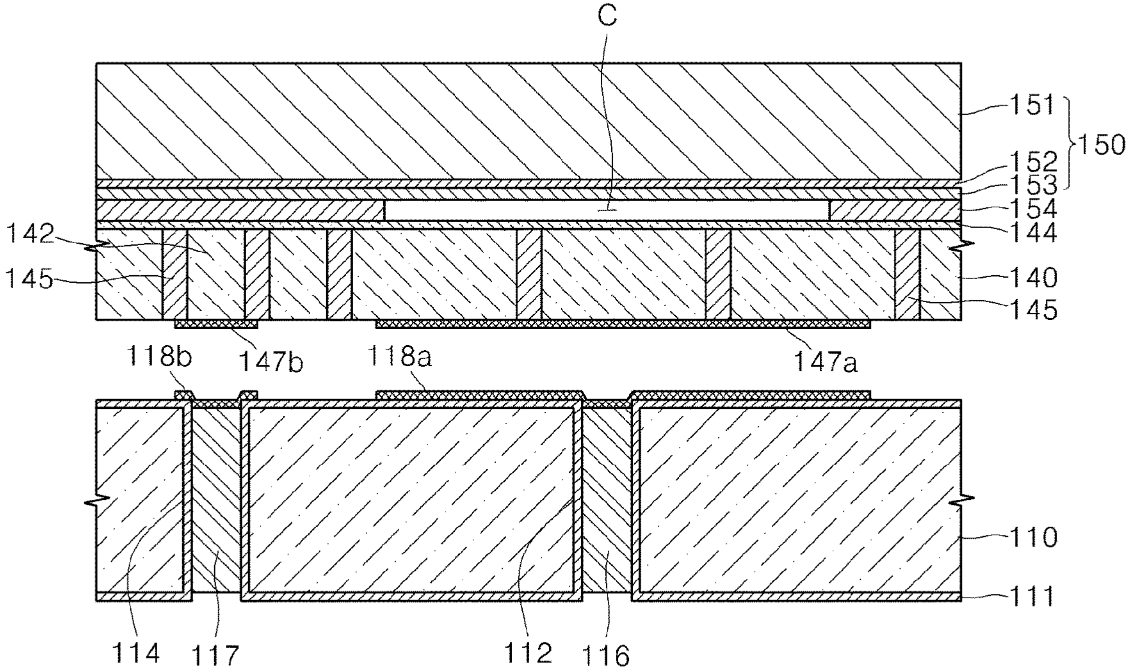


FIG. 4G

C
151
150
152
153
154
142
144
145
140
145
110
111
114
117
P2
M2
112
116
P1
M1

FIG. 4H

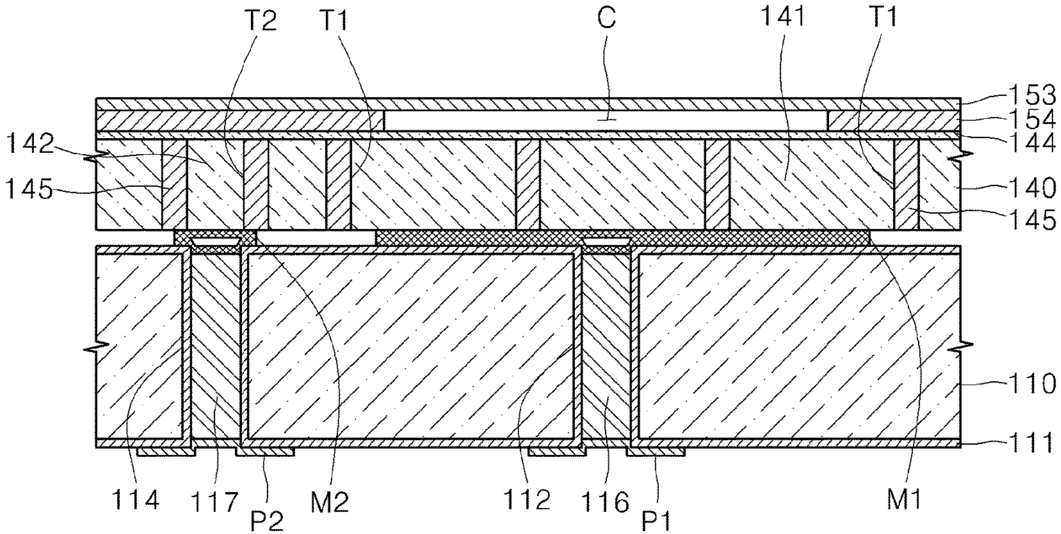
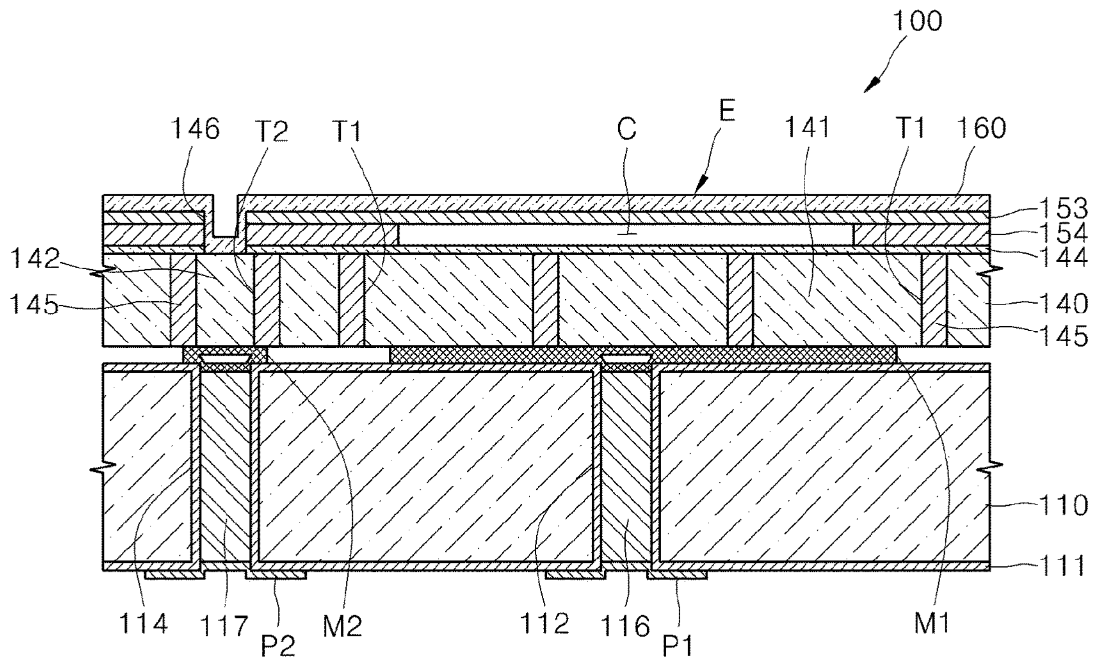


FIG. 4I



CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCER AND METHOD OF FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation application of U.S. patent application Ser. No. 14/286,460, filed May 23, 2014, which claims the benefit of Korean Patent Application No. 10-2013-0141587, filed on Nov. 20, 2013, in the Korean Intellectual Property Office, the disclosures of which are incorporated herein in their entirety by reference.

BACKGROUND

1. Field

[0002] The exemplary embodiments relate to capacitive micromachined ultrasonic transducers using a plurality of conductive material layers defined by trenches as bottom electrodes and methods of fabricating the same.

2. Description of the Related Art

[0003] A micromachined ultrasonic transducer (MUT) is a device capable of converting electric signals into ultrasonic signals or converting ultrasonic signals into electric signals. Such MUTs may be categorized into piezoelectric micromachined ultrasonic transducers (PMUT), capacitive micromachined ultrasonic transducers (CMUT), and magnetic micromachined ultrasonic transducers (MMUT) according to a conversion mechanism.

[0004] A conventional CMUT supplies electricity to a top electrode by using a through via formed in a low-resistance wafer. During formation of the through via, a corner of a through via hole may not be completely coated by a passivation layer, and a metal layer for the through via may contact the low-resistance wafer, and thus, the through via and the low-resistance wafer may be short-circuited. Furthermore, a masking process for forming the through via is required.

SUMMARY

[0005] Exemplary embodiments may provide capacitive micromachined ultrasonic transducers which employ low-resistance wafers for supplying currents to top electrodes without through vias.

[0006] Exemplary embodiments may provide methods of fabricating the capacitive micromachined ultrasonic transducers.

[0007] Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, or may be learned by practice of the presented exemplary embodiments.

[0008] According to an aspect of an exemplary embodiment, there is provided a capacitive micromachined ultrasonic transducer (CMUT) including a first trench defining a plurality of first portions corresponding to an element, and a second trench spaced apart from the first trench; a supporting unit provided on the device substrate, the supporting unit defining a plurality of cavities; a membrane provided on the supporting unit to cover the plurality of cavities; a top electrode electrically connected to a second portion in the second trench through a via hole penetrating through the membrane and the supporting unit; and a through silicon via (TSV) substrate provided on a bottom surface of the device substrate, the TSV substrate including a first via metal connected to the plurality of first portions corresponding to the element and a second via metal connected to the second portion.

[0009] The first trench has a lattice-like shape.

[0010] The device substrate includes a low-resistance silicon.

[0011] A thickness of the device substrate is from about 10 μm to about 50 μm.

[0012] The first trench and the second trench have a same width.

[0013] The width of the first trench and the second trench is from about 1 μm to about 10 μm.

[0014] The first trench and the second trench are filled with an insulating material.

[0015] The CMUT further includes a first bonding metal provided between the plurality of first portions corresponding to the element and the first via metal; and a second bonding metal provided between the second portion and the second via metal.

[0016] The first bonding metal contacts the plurality of first portions formed below the plurality of cavities of the element.

[0017] The CMUT further includes an insulation layer, which is provided between the device substrate and the supporting unit and is penetrated by the via hole, such that the second portion and the top electrode contact each other.

[0018] The CMUT further includes an insulation layer, which is provided between the membrane and the supporting unit and is penetrated by the via hole, such that the second portion and the top electrode contact each other.

[0019] According to another aspect of an exemplary embodiment, there is provided a method of fabricating a capacitive micromachined ultrasonic transducer (CMUT), the method including forming a first trench insulating a plurality of first portions corresponding to an element and a second trench defining a second portion spaced apart from the plurality of first portions, the first trench and the second trench being formed to a predetermined depth from a top surface of a device substrate; forming a supporting unit including an insulation layer defining a plurality of cavities on the top surface of the device substrate or on a first silicon layer of a silicon-on-insulator (SOI) substrate; forming the plurality of cavities between the SOI substrate and the device substrate by bonding the SOI substrate to the top surface of the device substrate; exposing the first trench and the second trench by thinning a bottom surface of the device substrate; bonding a through silicon via (TSV) substrate to the bottom surface of the device substrate, the TSV substrate including a first via metal connected to the plurality of first portions and a second via metal connected to the second portion; exposing the first silicon layer on the supporting unit by removing a buried oxide layer and a second silicon layer of the SOI substrate; exposing the second portion by forming a via hole penetrating through the first silicon layer and the supporting unit; and forming a top electrode on the first silicon layer to contact the second portion through the via hole.

[0020] The device substrate is bonded to the SOI substrate by a silicon direct bonding (SDB) method.

[0021] In the forming of the first trench and the second trench, the first trench and the second trench have a same width.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] These and/or other aspects will become apparent and more readily appreciated from the following description of the exemplary embodiments, taken in conjunction with the accompanying drawings in which:

[0023] FIG. **1** is a schematic bottom view of a capacitive micromachined ultrasonic transducer (CMUT) according to exemplary embodiments;

[0024] FIG. **2** is a schematic bottom view showing the structure of one element region of a CMUT according to exemplary embodiments;

[0025] FIG. **3** is a sectional view taken along a line III-III' of FIG. **1**; and

[0026] FIGS. **4**A through **4**I are sectional diagrams showing respective operations of a method of fabricating a CMUT according to exemplary embodiments.

DETAILED DESCRIPTION

[0027] Reference will now be made in detail to exemplary embodiments, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. In this regard, the present exemplary embodiments may have different forms and should not be construed as being limited to the descriptions set forth herein. Accordingly, the exemplary embodiments are merely described below, by referring to the figures, to explain aspects of the present description. It will be understood that when a layer, region, or component is referred to as being "formed on" another layer, region, or component, it can be directly or indirectly formed on the other layer, region, or component. That is, for example, intervening layers, regions, or components may be present. Like reference numerals refer to like elements throughout, and detailed descriptions thereof will be omitted. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0028] FIG. **1** is a schematic bottom view of a capacitive micromachined ultrasonic transducer (CMUT) **100** according to exemplary embodiments.

[0029] FIG. **1** is a bottom view of a device substrate. Referring to FIG. **1**, a CMUT **100** includes a plurality of elements E. For example, the CMUT **100** may include the elements E arranged in a 16×16 matrix. In FIG. **1**, four elements E are shown for convenience of explanation. The CMUT **100** may also be referred to as an ultrasonic transducer chip.

[0030] A first trench T**1**, which is an insulating trench, is formed at each element E. The first trench T**1** may be formed in a shape of a lattice. A plurality of first portions **141** are formed at each of the elements E by the first trench T**1**. A first bonding metal M**1** is formed to contact the plurality of first portions **141** in the element E.

[0031] A second trench T**2** is formed next to the elements E. A second bonding metal M**2** is formed to contact a second portion (**142** of FIG. **3**) surrounded by the second trench T**2**. The reference numeral **145** denotes an insulating material filling the first trench T**1** and the second trench T**2**.

[0032] FIG. **2** is a schematic bottom view showing the structure of one element region of a CMUT according to exemplary embodiments.

[0033] Referring to FIG. **2**, a plurality of cavities C is formed at the element E. In FIG. **2**, the four cavities C are shown for convenience of explanation. The first bonding metal M**1** is formed to be electrically connected to first portions **141** below the cavities C. Although FIG. **1** shows that the first bonding metal M**1** has a rectangular shape, the exemplary embodiments are not limited thereto. For example, in FIG. **2**, the first bonding metal M**1** may be formed to have a rounded shape to contact the first portions **141** below the cavities C. Furthermore, the first trench T**1** may not be formed at the plurality of first portions **141** formed below the cavities C.

[0034] FIG. **3** is a sectional view taken along a line III-III' of FIG. **1**.

[0035] Referring to FIG. **3**, the CMUT **100** may include a through silicon via (TSV) substrate **110** and a device substrate **140** bonded to the TSV substrate **110**. The TSV substrate **110** and the device substrate **140** may be bonded to each other via eutectic bonding.

[0036] The TSV substrate **110** is formed of a silicon substrate, and a plurality of through holes **112** are formed in the TSV substrate **110**. In each CMUT **100**, the through holes **112** and a through hole **114** for a top electrode are formed to respectively correspond to each element E. An insulation layer **111** is formed on surfaces of the through holes **112**, the through hole **114**, and the TSV substrate **110**. The through holes **112** are filled with a first via metal **116**, whereas the through hole **114** is filled with a second via metal **117**.

[0037] In the device substrate **140**, lattice-like first trench T**1** is formed at each of the elements E. The second trench T**2** for a top electrode is formed to be spaced apart from a region in which the plurality of elements E is formed. The device substrate **140** includes the plurality of first portions **141** surrounded by the first trench T**1** and the second portion **142** surrounded by the second trench T**2**.

[0038] The device substrate **140** is formed of a conductive material, where the thickness thereof may be several tens of μm. Thickness of the device substrate **140** may be from about 10 μm to about 50 μm. The device substrate **140** may be formed of a low-resistance silicon highly doped with an impurity.

[0039] The first portions **141** and the second portion **142** of the device substrate **140** are conductive regions. The first portions **141** of the device substrate **140** may be used as a bottom electrode.

[0040] The first trench T**1** and the second trench T**2** may be filled with an insulating material **145**. The insulating material **145** may be a silicon oxide.

[0041] The device substrate **140** may include an insulation layer **144** formed on a top surface of the device substrate **140**, a supporting unit **154** forming a cavity C, and a membrane **153** on the supporting unit **154** to cover the cavity C. A top electrode **160** may be formed on the membrane **153**. The membrane **153** may be formed of silicon. The supporting unit **154** may be formed of an insulator. The supporting unit **154** may include an oxide, a nitride, etc. For example, the supporting unit **154** may include a silicon oxide.

[0042] In FIG. **3**, the insulation layer **144** is formed on the top surface of the device substrate **140**. However, the exemplary embodiments are not limited thereto. For example, the insulation layer **144** may be formed between the membrane **153** and the supporting unit **154**.

[0043] The top electrode **160** may be formed of Au, Cu, Sn, Ag, Al, Pt, Ti, Ni, Cr, or an alloy thereof.

[0044] The insulation layer **144** may include an oxide, a nitride, etc. For example, the insulation layer **144** may be formed of a silicon nitride.

[0045] Although FIG. **3** shows that one cavity C is formed per element E, the exemplary embodiments are not limited thereto. For example, cavities C may be arranged in the shape of a 5×5 array per element E. A first bonding metal M**1** may be formed to contact the first portions **141** below the cavity C.

[0046] A via hole **146**, which penetrates through the membrane **153**, the supporting unit **154**, and the insulation layer **144** and exposes the second portion **142** of the device substrate **140** surrounded by the second trench T**2**, is formed in the membrane **153**, the supporting unit **154**, and the insulation layer **144**. The top electrode **160** is electrically connected to the second portion **142** of the device substrate **140** via the via hole **146**.

[0047] A first bonding pad **147***a* is formed at the bottom of the device substrate **140** to be connected to the first via metal **116**, and a second bonding pad **147***b* is formed at the bottom of the device substrate **140** to be connected to the second via metal **117**. The first bonding pad **147***a* and the second bonding pad **147***b* may be formed of eutectic bonding metals. For example, for Au—Sn eutectic bonding, the first bonding pad **147***a* and the second bonding pad **147***b* may be formed of an Au-based material and/or a Sn-based material.

[0048] A third bonding pad **118***a* is formed on the first via metal **116** in correspondence to the first bonding pad **147***a*, whereas a fourth bonding pad **118***b* is formed on the second via metal **117** in correspondence to the second bonding pad **147***b*. The third bonding pad **118***a* and the fourth bonding pad **118***b* may be formed of eutectic bonding metals. For example, for Au—Sn eutectic bonding, the third bonding pad **118***a* and the fourth bonding pad **118***b* may be formed of an Au-based material and/or a Sn-based material. The first bonding pad **147***a* and the third bonding pad **118***a* may be eutectically bonded to each other and form the first bonding metal M**1**, whereas the second bonding pad **147***b* and the fourth bonding pad **118***b* may be eutectically bonded to each other and form the second bonding metal M**2**.

[0049] A first electrode pad P**1** connected to the first via metal **116** and a second electrode pad P**2** connected to the second bonding metal M**2** are formed at the bottom of the TSV substrate **110**. A ground voltage may be applied to the second electrode pad P**2**, whereas a driving signal voltage may be applied to the first electrode pad P**1**.

[0050] The driving signal voltage applied to the first electrode pad P**1** is supplied to the first portions **141** via the first via metal **116** and the first bonding metal M**1**.

[0051] The ground voltage applied to the first electrode pad P**2** is supplied to the top electrode **160** via the second via metal **117**, the second bonding metal M**2**, and the second portion **142**.

[0052] The CMUT **100** according to exemplary embodiments uses a device substrate as an electrode or an electric path, while the electric path is only formed in a vertical direction due to a trench. Therefore, it is easy to block an electric connection between a top electrode and a bottom electrode in a horizontal direction.

[0053] Furthermore, there is no trench defining elements, and gaps between elements are reduced, thereby increasing bandwidth of the CMUT **100**.

[0054] Hereinafter, a method of fabricating a CMUT according to exemplary embodiments is explained.

[0055] FIGS. **4**A through **4**I are sectional diagrams showing respective operations of a method of fabricating a CMUT according to an exemplary embodiment. FIGS. **4**A through **4**I are obtained along a line III-III' of FIG. **3**.

[0056] The elements substantially identical to the elements shown in FIGS. **1** and **3** are denoted by the same reference numerals.

[0057] Referring to FIG. **4**A, the first trench T**1** is formed at an element region from the top surface of a device wafer **140***a*, and the second trench T**2** for a top electrode is formed at a region spaced apart from the element region. The first trench T**1** may be formed to have a lattice-like shape with respect to the plurality of elements E of each chip, as shown in FIG. **1**. The second trench T**2** is formed to surround the second portion **142** interconnecting the device wafer **140***a* and a top electrode (**160** of FIG. **3**).

[0058] The first trench T**1** and the second trench T**2** may be formed to have depths from about 10 μm to about 50 μm from the top surface of the device wafer **140***a*. The first trench T**1** and the second trench T**2** may have the same width. When the first trench T**1** and the second trench T**2** have the same width, the first trench T**1** and the second trench T**2** may be formed together by using a single mask. In the related art, since a width of an element defining a trench is different from a width of a via for connecting a top electrode, etching time for the element defining the trench is different from etching time for the via for connecting a top electrode, and thus the element defining the trench and the via for connecting a top electrode are formed using different etching process. However, according to the present exemplary embodiment, the first trench T**1** and the second trench T**2** may be simultaneously formed.

[0059] The first trench T**1** and the second trench T**2** may be formed to have a width from about 1 μm to about 10 μm. If the width of the first trench T**1** and the second trench T**2** is smaller than 1 μm, etching may be difficult due to a high aspect ratio of the trenches T**1** and T**2**. If the width of the first trench T**1** and the second trench T**2** is greater than 10 μm, frequency characteristics of the CMUT **100** may be deteriorated.

[0060] Next, a protection layer covering the first trench T**1** and the second trench T**2** is formed on the top surface of the device wafer **140***a*. The protection layer includes the insulating material **145** filling the first trench T**1** and the second trench T**2** and an insulation layer **140***b* on the device wafer **140***a*. The insulating material **145** and the insulation layer **140***b* may be formed of a silicon oxide. It is not necessary to completely fill the first trench T**1** and the second trench T**2** with the silicon oxide. The insulation layer **140***b* may not be uniformly formed.

[0061] Referring to FIG. **4**B, the insulation layer **140***b* on the device wafer **140***a* is removed. For example, the first trench T**1** and the second trench T**2** are exposed by performing a chemical-mechanical polishing (CMP).

[0062] Next, a first insulation layer **144** is formed on the top surface of the device wafer **140***a*. The first insulation layer **144** may be formed by oxidizing the device wafer **140***a*.

[0063] Referring to FIG. **4**C, a second insulation layer **154** is formed on a first wafer **150**, and an opening **154***a* is formed by patterning the second insulation layer **154**. The first wafer **150** may be a silicon-on-insulator (SOI) wafer. The first wafer **150** may include a first silicon layer **151**, a buried oxide layer **152**, and a second silicon layer **153** that

are stacked in the order stated. The second silicon layer **153** corresponds to the membrane **153** of FIG. **3** and may have a thickness of about 2000 Å.

[0064] The second insulation layer **154** may be formed of a silicon oxide and may be formed by oxidizing the first wafer **150**. The patterned second insulation layer **154** corresponds to the supporting unit **154** of FIG. **3**. A height of the opening **154***a* may be determined based on thickness of the second insulation layer **154**. The thickness of the second insulation layer **154** may be about 4000 Å.

[0065] The opening **154***a* may be formed in the first insulation layer **144** instead of the second insulation layer **154**. Detailed descriptions thereof will be omitted.

[0066] Referring to FIG. **4**D, the first wafer **150** is bonded to the device wafer **140***a*, such that the second insulation layer **154** and the first insulation layer **144** face each other. The device wafer **140***a* may be formed of low-resistance silicon.

[0067] The first wafer **150** and the device wafer **140***a* may be wafer-to-wafer bonded to each other via a silicon direct bonding (SDB). By bonding the first wafer **150** and the device wafer **140***a* to each other, the cavity C, which is an empty space, is formed.

[0068] The device substrate **140** having a thickness from about 10 μm to about 50 μm is formed by thinning the device wafer **140***a*. To this end, the device substrate **140** may be first mechanically lapped, and then a CMP process may be performed thereto. By the thinning operation, the insulating material **145** in the first trench T**1** and the second trench T**2** of the device substrate **140** are exposed.

[0069] Referring to FIG. **4**E, a metal layer is deposited onto the rear surface of the device substrate **140** and the first bonding pad **147***a* and the second bonding pad **147***b* are formed by pattering the metal layer. The first bonding pad **147***a* and the second bonding pad **147***b* may be formed of materials for eutectic bonding. For example, for Au—Sn eutectic bonding, the first bonding pad **147***a* and the second bonding pad **147***b* may be formed of an Au-based material and/or an Sn-based material.

[0070] Referring to FIG. **4**F, the TSV substrate **110** is prepared. A first through hole **112** and a second through hole **114** are formed in the TSV substrate **110**. The first through hole **112** and the second through hole **114** may have widths of about several tens of μm. The first through hole **112** is formed in correspondence to the first portion **141**, whereas the second through hole **114** is formed in correspondence to the second portion **142**.

[0071] A third insulation layer **111** is formed on the TSV substrate **110**. The third insulation layer **111** may be formed by oxidizing the TSV substrate **110**. The third insulation layer **111** may be formed on surfaces of the first through hole **112** and the second through hole **114** and the top surface and the bottom surface of the TSV substrate **110**. The first through hole **112** and the second through hole **114** are filled with metals, thereby forming the first via metal **116** and the second via metal **117**.

[0072] After forming a metal layer on the TSV substrate **110**, the third bonding pad **118***a* and the fourth bonding pad **118***b* are formed by patterning the metal layer. The third bonding pad **118***a* is formed on the first via metal **116** in correspondence to the first bonding pad **147***a*, whereas the fourth bonding pad **118***b* is formed on the second via metal **117** in correspondence to the second bonding pad **147***b*.

[0073] The third bonding pad **118***a* and the fourth bonding pad **118***b* may be formed of eutectic bonding metals. For example, for Au—Sn eutectic bonding, the third bonding pad **118***a* and the fourth bonding pad **118***b* may be formed of an Au-based material and/or a Sn-based material.

[0074] Referring to FIG. **4**G, the TSV substrate **110** and the device wafer **140***a* are bonded to each other at the wafer level. For example, the TSV substrate **110** and the device wafer **140***a* may be eutectically bonded to each other. The eutectic bonding may be based on Au/Sn bonding. According to an exemplary embodiment, the first bonding pad **147***a* and the third bonding pad **118***a* are eutectically bonded to each other and form the first bonding metal M**1**, whereas the second bonding pad **147***b* and the fourth bonding pad **118***b* are eutectically bonded to each other and form the second bonding metal M**2**.

[0075] The first electrode pad P**1** connected to the first via metal **116** and the second electrode pad P**2** connected to the second bonding metal M**2** are formed.

[0076] Referring to FIG. **4**H, the first silicon layer **151** and the buried oxide layer **152** of the first wafer **150** are sequentially removed. The first silicon layer **151** may be first removed via mechanical lapping, and then the remaining portion of the first silicon layer **151** having a thickness of dozens of μm may be removed via dry etching. The buried oxide layer **152** may be removed via wet etching.

[0077] Referring to FIG. **4**I, the via hole **146** is formed in the second silicon layer **153**, the second insulation layer **154**, and the first insulation layer **144** to expose the second portion **142**. The top electrode **160** is formed on the second silicon layer **153**. The top electrode **160** is formed to be electrically connected to the second portion **142**.

[0078] The structure fabricated in the operations described above is diced into individual chips, thereby fabricating a plurality of CMUT chips **100**.

[0079] In the method of fabricating an ultrasonic transducer according to exemplary embodiments, a trench for connecting a top electrode is simultaneously formed with a trench for insulating elements E in a device wafer, and thus, a mask operation for forming a back via, as performed in the related art, is not necessary. Furthermore, short-circuiting between a via metal and a bottom electrode of an element during an operation for forming the back via at a device substrate, which may occur in the related art, may be prevented.

[0080] As described above, according to exemplary embodiments, a CMUT according to exemplary embodiments uses a device substrate as an electrode or an electric path, while the electric path is only formed in a vertical direction due to a trench. Therefore, it is easy to block an electric connection between a top electrode and a bottom electrode in a horizontal direction.

[0081] Furthermore, there is no trench defining elements, and gaps between elements are reduced, thereby increasing a bandwidth of an ultrasonic transducer.

[0082] In the method of fabricating a CMUT according to exemplary embodiments, a trench for connecting a top electrode is simultaneously formed with a trench for insulating elements E in a device wafer, and thus, the overall fabrication process is simplified. Furthermore, short-circuiting between a via metal and a bottom electrode of an element during an operation for forming a back via at a device substrate, which may occur in the related art, may be prevented.

[0083] It should be understood that the exemplary embodiments described therein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each exemplary embodiment should typically be considered as available for other similar features or aspects in other exemplary embodiments.

[0084] While one or more exemplary embodiments have been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the exemplary embodiments as defined by the following claims.

What is claimed is:

1. A method of fabricating a capacitive micromachined ultrasonic transducer (CMUT), the method comprising:

forming a first trench insulating a plurality of first portions corresponding to an element and a second trench defining a second portion spaced apart from the plurality of first portions, the first trench and the second trench being formed to a predetermined depth from a top surface of a device substrate;

forming a supporting unit comprising an insulation layer defining a plurality of cavities on the top surface of the device substrate or on a first silicon layer of a silicon-on-insulator (SOI) substrate;

forming the plurality of cavities between the SOI substrate and the device substrate by bonding the SOI substrate to the top surface of the device substrate;

exposing the first trench and the second trench by thinning a bottom surface of the device substrate;

bonding a through silicon via (TSV) substrate to the bottom surface of the device substrate, the TSV substrate comprising a first via metal connected to the plurality of first portions and a second via metal connected to the second portion;

exposing the first silicon layer on the supporting unit by removing a buried oxide layer and a second silicon layer of the SOI substrate;

exposing the second portion by forming a via hole penetrating through the first silicon layer and the supporting unit; and

forming a top electrode on the first silicon layer to contact the second portion through the via hole.

2. The method of claim **1**, wherein the device substrate comprises a low-resistance silicon.

3. The method of claim **1**, wherein the device substrate is bonded to the SOI substrate using a silicon direct bonding method.

4. The method of claim **1**, wherein the forming of the first trench and the second trench comprises forming the first trench and the second trench to have a same width.

5. The method of claim **4**, wherein the width of the first trench and the second trench is from about 1 μm to about 10 μm.

6. The method of claim **1**, wherein the forming of the first trench and the second trench comprises forming the first trench and the second trench to have a depth from about 10 μm to about 50 μm.

7. The method of claim **1**, further comprising filling the first trench and the second trench with an insulating material.

8. The method of claim **1**, wherein the bonding of the TSV substrate to the bottom surface of the device substrate comprises:

forming a first bonding pad contacting the plurality of first portions and a second bonding pad contacting the second portion on the bottom surface of the device substrate;

forming a third bonding pad on the first via metal of the TSV substrate and a fourth bonding pad on the second via metal of the TSV substrate;

forming the first bonding pad and the second bonding pad to respectively contact the third bonding pad and the fourth bonding pad; and

performing eutectic bonding the first bonding pad and the third bonding pad, and the second bonding pad and the fourth bonding pad.

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