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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title**: DUAL SENSING CURRENT LATCHED SENSE AMPLIFIER

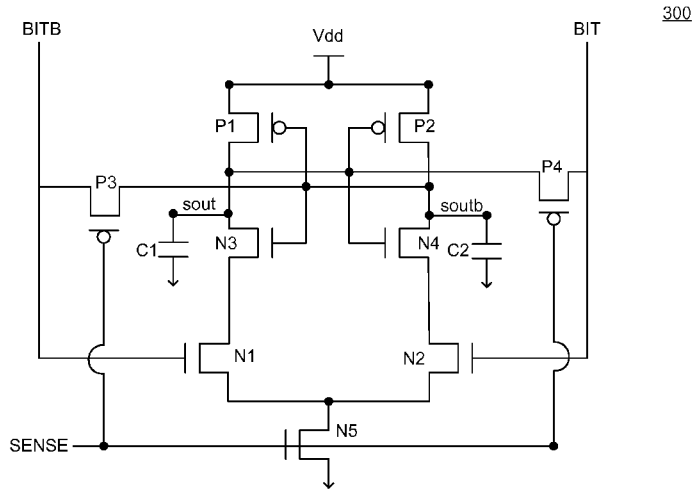

Fig. 3

(57) **Abstract**: A sense amplifier and method thereof are provided. The sense amplifier includes first and second transistors coupled to first and second bit lines, respectively. The first and second transistors are configured to connect the first and second bit lines to a differential amplifier during a first state (e.g., when a differential voltage is present on the first and second bit lines and prior to a sense signal transition) and to isolate the first and second bit lines from the differential amplifier during a second state (e.g., after the sense signal transition). The sense amplifier further includes a third transistor configured to deactivate the differential amplifier during the first state and configured to activate the differential amplifier during the second state.

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DUAL SENSING CURRENT LATCHED SENSE AMPLIFIER

Field of Disclosure

[0001] Disclosed embodiments are related to sense amplifiers circuits and methods. In particular the embodiments relate to dual sensing current latched sense amplifiers.

Background

[0002] Memory devices conventionally include arrays of bit cells that each store a bit of data. Each data bit can represent a logical low ("0") or a logical high ("1"), which may correspond to a state of the bit cell. For example, during a read operation a voltage level at a selected bit cell close to ground may be representative a logical low or "0" and a higher voltage level may be representative of a logical high or "1." Bit lines are coupled to various bit cells in the memory array and couple the bit cells to other components used in read / write operations.

[0003] For example, during a read operation, the voltage / current representing a state of a selected bit cell may be detected via the bit lines coupled to the selected bit cell. A sense amplifier may be coupled to the bit lines to amplify the differential voltage / current to aid in determining the logical state of the bit cell.

[0004] As discussed above, a sense amplifier (SA) is a basic component that is used for operations in memory devices. A commonly used sense amplifier is a current latched sense amplifier (CLSA).

[0005] FIG. 1 illustrates a conventional CLSA 100. Referring to FIG. 1, the CLSA 100 includes NMOS transistors N1 through N5, PMOS transistors P1 through P4 and capacitors C1 and C2. The CLSA 100 receives differential input bit line BIT and inverted bit line BITB, sense signal SENSE and is coupled to a power supply voltage Vdd.

[0006] Referring to FIG. 1, the differential inputs BIT, BITB are applied to gates of NMOS transistors N1 and N2, respectively. The sense signal SENSE is applied to NMOS transistor N5 and PMOS transistors P1 and P4. When the sense signal SENSE is low, transistors P1 and P4 are conducting or “on” and allow capacitors C1 and C2 to charge. When the sense signal SENSE transitions to a higher logic level (e.g., “1”), the current through the gates N1 and N2 will be different if the voltages on differential

inputs BIT and BITB are different. A different current flow through N1/N3 and N2/N4 will cause a voltage difference between output nodes sout and soutb as the capacitors will be discharged at a different rate. If a voltage on one of the output nodes (sout or soutb) reaches a threshold value to turn on one of cross coupled transistors P2 or P3, and turn off one of corresponding transistors N3 or N4, then a corresponding one of nodes sout or soutb will be coupled to Vdd. The other pair of transistors P1/N3 or P2/N4 cross coupled to the output node (sout or soutb) and coupled to Vdd will remain in a state with the PMOS transistor off and the NMOS transistor conducting. Accordingly, one of the output nodes sout or soutb will be latched to a high state and the other output node will be discharged, so the voltage differential between sout and soutb will be further amplified.

[0007] FIG. 2 illustrates another conventional CLSA 200. Referring to FIG. 2, the CLSA 200 includes NMOS transistors N1 through N5, PMOS transistors P1 through P6 and capacitors C1 and C2. The CLSA 200 receives differential inputs BIT and BITB, sense signal SENSE and is coupled to power supply voltage Vdd. The operation of the CLSA 200 is similar to that of the CLSA 100. However, the CLSA 200 differs from CLSA 100 in that the differential inputs BIT and BITB are coupled to nodes sa and sab through PMOS transistors P5 and P6 (which are not present in CLSA 100) prior to a triggering of a sensing operation (when sense signal SENSE is low), which can increase a sensitivity of the CLSA 200 as compared to CLSA 100.

[0008] Thus, CLSA 100 and CLSA 200 are configured to sense voltage differentials in different manners. Also, CLSA 200 is able to achieve greater sensitivity than the CLSA 100 but only at the cost of including additional PMOS transistors, which can increase the layout area, power consumption and leakage of the sense amplifier.

SUMMARY

[0009] Exemplary embodiments are directed to current latched sense amplifiers, related circuits and methods.

[0010] Accordingly, an embodiment can include a current latched sense amplifier comprising: first and second transistors coupled to first and second bit lines, respectively, the first and second transistors configured to couple the first and second bit lines to first and second output nodes of the sense amplifier in a first phase and to isolate the first and second output nodes in a second phase; and third and fourth

transistors having gates coupled to the first and second bit lines and coupled to current paths of the first second and first output nodes, respectively, and configured to be activated during the second phase.

[0011] Another embodiment is directed to a method of sensing a differential between two bit lines, comprising: coupling a first bit line to a first output node of a sense amplifier and a second bit line to a second output node of the sense amplifier, in a first phase to supply an initial differential voltage to the sense amplifier; decoupling the first bit line from the first output node and the second bit line from the second output node during a second phase; and amplifying the initial differential voltage by discharging the first output node based on a voltage on the second bit line and the second output node based on a voltage on the first bit line, in the second phase.

[0012] Another embodiment is directed to an apparatus for sensing a differential between two bit lines, comprising: means for coupling a first bit line to a first output node of a sense amplifier and a second bit line to a second output node of the sense amplifier, in a first phase to supply an initial differential voltage to the sense amplifier; means for decoupling the first bit line from the first output node and the second bit line from the second output node during a second phase; and means for amplifying the initial differential voltage by discharging the first output node based on a voltage on the second bit line and the second output node based on a voltage on the first bit line, in the second phase.

[0013] Another embodiment is directed a method of sensing a differential between two bit lines, comprising: step for coupling a first bit line to a first output node of a sense amplifier and a second bit line to a second output node of the sense amplifier, in a first phase to supply an initial differential voltage to the sense amplifier; step for decoupling the first bit line from the first output node and the second bit line from the second output node during a second phase; and step for amplifying the initial differential voltage by discharging the first output node based on a voltage on the second bit line and the second output node based on a voltage on the first bit line, in the second phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] A more complete appreciation of embodiments and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the

accompanying drawings which are presented solely for illustration and not limitation of the embodiments.

[0015] FIG. 1 illustrates a conventional current latched sense amplifier (CLSA).

[0016] FIG. 2 illustrates another conventional current latched sense amplifier (CLSA).

[0017] FIG. 3 illustrates a current latched sense amplifier (CLSA) according to at least one embodiment.

[0018] FIG. 4 illustrates a flowchart for an exemplary method.

DETAILED DESCRIPTION

[0019] Aspects are disclosed in the following description and related drawings directed to specific embodiments. Alternate embodiments may be devised without departing from the scope of the invention. Additionally, well-known elements will not be described in detail or will be omitted so as not to obscure the relevant details of the disclosed embodiments.

[0020] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any embodiment described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments. Likewise, the term “embodiments” does not require that all embodiments include the discussed feature, advantage or mode of operation.

[0021] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of embodiments. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises", "comprising,", "includes" and/or "including", when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0022] Further, many embodiments are described in terms of sequences of actions to be performed by, for example, elements of a computing device. It will be recognized that various actions described herein can be performed by specific circuits (e.g., application specific integrated circuits (ASICs)), by program instructions being executed by one or more processors, or by a combination of both. Additionally, these sequence of actions described herein can be considered to be embodied entirely within any form of

computer readable storage medium having stored therein a corresponding set of computer instructions that upon execution would cause an associated processor to perform the functionality described herein. Thus, the various aspects of the embodiments may be embodied in a number of different forms, all of which have been contemplated to be within the scope of the claimed subject matter. In addition, for each of the embodiments described herein, the corresponding form of any such embodiments may be described herein as, for example, "logic configured to" perform the described action.

[0023] FIG. 3 illustrates a dual sensing current latch sense amplifier (DSCLSA) 300 according to at least one embodiment. Referring to FIG. 3, the DSCLSA 300 includes NMOS transistors N1 through N5, PMOS transistors P1 through P4 and capacitors C1 and C2. The DSCLSA 300 receives differential bit line inputs BIT and BITB, sense signal SENSE and is coupled to supply voltage Vdd. As previously discussed, the bit lines may be couple to a plurality of bit cells in a memory array. A memory read operation can be coordinated with the DSCLSA 300 such that the sense signal SENSE can be triggered at an appropriate time after a bit cell has been selected to be read. The various control circuits for memory addressing, read and write operations are well known and will not be described herein.

[0024] As illustrated in FIG. 3, any differential voltage between BIT/BITB is provided at sout and soutb at a drain terminal of cross coupled inverted amplifiers P1/N3 and P2/N4 (which can be considered a differential amplifier) and to gates of PMOS transistors P1 and P2, respectively before the DSCLSA 300 is triggered. The differential voltage at sout and soutb is also provided at gates of NMOS transistors N3 and N4.

[0025] Referring to FIG. 3, the voltage differential of bit line BIT, BITB are also applied to the gates of NMOS transistors N1 and N2, respectively, and are also applied to source inputs of PMOS transistors P3 and P4, respectively. The sense signal SENSE is applied to the gates of NMOS transistor N5 and PMOS transistors P3 and P4. As will now be described in greater detail, the DSCLSA 300 is "dual sensing" because the DSCLSA 300 is capable of amplifying a voltage differential at sout and soutb in two different manners, which reinforce each other and increase a sensitivity of the DSCLSA 300.

[0026] It will be appreciated that in a first phase prior to triggering the DSCLSA 300, when the sense signal SENSE is at a low logic level or logic "0", a differential voltage

may already be developed, at least partially, between the nodes sout and soutb. This is because PMOS transistors P3 and P4 are gated on when sense signal SENSE is set to the lower logic level, thereby coupling BIT to node sout and BITB to node soutb.

[0027] In a second phase when the DSCLSA 300 is triggered, the sense signal SENSE transitions from the lower logic level to a higher logic level or "1". PMOS transistors P3 and P4 transition to an "off" state, whereas NMOS transistor N5 transitions to an "on" state. As noted above, the differential bit line inputs BIT, BITB are coupled to the gates of NMOS transistors N1 and N2. Accordingly, when transistor N5 turns on, the differential voltage applied to the gates of NMOS transistors N1 and N2 causes different currents at N1 and N2, respectively. The different currents at NMOS transistors N1 and N2 increases the voltage differential at nodes sout and soutb by discharging capacitors C1 and C2 through transistors N3 and N4, respectively.

[0028] Accordingly, the voltage differential at sout and soutb that is amplified by the DSCLSA 300 is based on an initial differential voltage occurring prior to a transition of the sense signal SENSE from a lower logic level to a higher logic level which enhances the differential voltage determined when the sense signal SENSE transitions to the higher logic level. Also, the enhanced sensitivity of the DSCLSA 300 is provided without an increase in the number of components and without an increase in the area used in the layout of the DSCLSA 300, over the conventional CLSA 100. Additionally, fifth and sixth PMOS transistors P5 and P6, which are present within the CLSA 200 of FIG. 2, need not be included within DSCLSA 300. Accordingly, DSCLSA 300 may occupy less physical space, use less power, and have less leakage compared to CLSA 200 of FIG. 2.

[0029] For example, referring to FIG. 3, assume that sense signal SENSE is set to the lower logic level, and a bit line voltage at BITB is equal to a bit line voltage at BIT. Next, assume during a memory operation the bit line voltage at BITB drops a given amount (e.g., 20 mV). The BIT and BITB bit line voltages pass through PMOS transistors P4 and P3, respectively, until sense signal SENSE transitions to the higher logic level. Thus, sout and soutb are set to different voltages before sense signal SENSE transitions to the higher logic level. For example, this could be during a read operation prior to the DSCLSA 300 being triggered by sense signal SENSE and the output (sout, soutb) being read. Further, it will be appreciated that C1 and C2 do not have a discharge path through N1/N3 and N4/N2, respectively, as transistor N5 will be

non-conducting or "off" prior to the transition of sense signal SENSE to the higher logic level.

[0030] When signal SENSE transitions to the higher logic level to trigger the DSCLSA 300, transistors P3 and P4 turn off, and transistor N5 turns on, thereby providing a current path through transistor N5 and discharge paths through transistors N1/N3 and N2/N4 for capacitors C1 and C2, respectively. Additionally, the voltage differential which has already developed between sout and soutb is provided to the gates of N1 and N2. This differential voltage at the gates of N1 and N2 causes different currents to flow through N1 and N2, which reinforces the initial voltage difference at sout and soutb because the current through the gates N1 and N2 will be different if the voltages on differential inputs BIT and BITB are different. The different current flows through N1/N3 and N2/N4 will cause the voltage difference between output nodes sout and soutb to increase as the capacitors C1 and C2 will be discharged at different rates.

[0031] For example in a first phase, assume that the difference between BIT and BITB is 20 mV prior to the DSCLSA 300 being triggered, as discussed above. This initial voltage differential will be provided to sout and soutb because transistors P3 and P4 are both on. Specifically, the voltage on BIT will be coupled to node sout via transistor P4 and the voltage on BITB will be coupled to soutb via transistor P3. In the second phase, when the DSCLSA 300 is triggered (i.e., SENSE transitions to a high level), transistor N5 is turned on and the current can flow through N1 and N2. The current flowing through N2 will be greater than that of N1, because of the higher voltage on BIT. This in turn will enhance the differential already established between soutb and sout, because the charge on C2 coupled to node soutb will be discharged at a higher rate than C1 coupled to node sout.

[0032] Accordingly, the voltage differential at sout and soutb can be developed in response to a bit line voltage differential by two separate phases (i.e., both before and after SENSE transitions to a high level). This is accomplished without including additional transistors (e.g., as in FIG. 2) which can increase the layout area of the sense amplifier.

[0033] It will be appreciated that embodiments can include various methods for performing the processes, functions and/or algorithms disclosed herein. For example, as illustrated in FIG. 4, an embodiment can include a method of sensing a voltage differential at a sense amplifier. For example, the method can include coupling a first bit line (e.g., BIT) to a first output node (e.g., sout) and a second bit line (e.g., BITB) to

a second output node (soutb), in a first phase to supply an initial differential voltage to the sense amplifier, block 402. During a second phase, the first bit line is decoupled from the first output node and the second bit line is decoupled from the second output node, block 404. Then, initial differential voltage (between sout and soutb) can be amplified by discharging the first output node (sout) based on a voltage on the second bit line (BITB) and the second output node (soutb) based on a voltage on the first bit line, in a second phase, block 406. As discussed above, in the second phase transistors P3 and P4 decouple the bit lines from the output nodes / gars of the cross coupled inverters (P1/N3 and P2/N4), which leaves any differential voltage at the common output / gates. Also, during the second phase transistor N5 is activated, which activates the sense amplifier in that current can flow through the inverters or at least though N3 / N4 to discharge the output nodes if P1 or P2 is gated off. Essentially, the voltage differential will be amplified, because the lower voltage (of the initial differential voltage) will be applied to the gate of the transistor (N1 /N2) coupled in series with the higher voltage node (sout / soutb) and higher voltage will be applied to the gate of the transistor (N1 /N2) coupled in series with the lower voltage node (sout / soutb). Accordingly, the reverse differential is applied to gates of the transistors in the current path of the output nodes.

[0034] It will be appreciated that the method illustrated in the flowchart of FIG. 4 is merely one embodiment and is not intended to limit the various embodiments to the illustrated examples. For example, other functional aspects / sequence of actions discussed herein may be added to the actions discussed in relation to FIG. 4 including alternatives to the actions already described.

[0035] Those of skill in the art will appreciate that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0036] Further, it will be appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above

generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the invention.

[0037] In one or more exemplary embodiments, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM, a solid state memory device, such as a flash-drive, or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0038] It will be appreciated that sense amplifiers, as illustrated for example in FIG. 3, may be included within a mobile phone, portable computer, hand-held personal communication system (PCS) unit, portable data units such as personal data assistants (PDAs), GPS enabled devices, navigation devices, settop boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof. Accordingly, embodiments may include any device which includes sense amplifiers as disclosed herein.

[0039] Further, it will be appreciated that various to memory devices can include an multiple sense amplifiers as disclosed herein. Accordingly, although potions of the foregoing disclosure discuss the sense amplifier in isolation, it will be appreciated that

various embodiments can include devices into which the sense amplifier is integrated, such as memory devices comprising arrays of memory cells and a plurality of sense amplifiers.

[0040] The foregoing disclosed devices and methods may be designed and configured into GDSII and GERBER computer files, stored on a computer readable media. These files are in turn provided to fabrication handlers who fabricate devices based on these files. The resulting products are semiconductor wafers that are then cut into semiconductor die and packaged into a semiconductor chip. The chips are then employed in devices described above.

[0041] Accordingly, embodiments can include machine-readable media or computer-readable media embodying instructions which when executed by a processor transform the processor and any other cooperating elements into a machine for performing the functionalities described herein as provided for by the instructions. Accordingly, the scope of the invention is not limited to illustrated examples and any means for performing the functionality described herein are included in embodiments.

[0042] While the foregoing disclosure shows illustrative embodiments, it should be noted that various changes and modifications could be made herein without departing from the scope of the invention as defined by the appended claims. The functions, steps and/or actions of the method claims in accordance with the embodiments described herein need not be performed in any particular order. Furthermore, although elements of embodiments may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated.

CLAIMS

WHAT IS CLAIMED IS:

1. A current latched sense amplifier comprising:

first and second transistors coupled to first and second bit lines, respectively, the first and second transistors configured to couple the first and second bit lines to first and second output nodes of the sense amplifier in a first phase and to isolate the first and second output nodes in a second phase; and

third and fourth transistors having gates coupled to the first and second bit lines and coupled to current paths of the first second and first output nodes, respectively, and configured to be activated during the second phase.

2. The sense amplifier of claim 1, wherein the first and second transistors are PMOS transistors.

3. The sense amplifier of claim 2, wherein the third and fourth transistors are NMOS transistors.

4. The sense amplifier of claim 3, further comprising:

a fifth transistor having a gate coupled to a sense input and coupled between the third and fourth transistors and a low voltage bus of a supply voltage, wherein the fifth transistor is configured to prevent current flow through the third and fourth transistors during the first phase and to permit current flow through the third and fourth transistors during the second phase.

5. The sense amplifier of claim 4, further comprising:

first and second inverters cross coupled, wherein the first inverter is coupled between a high voltage bus of the supply voltage and the third transistor and wherein the second inverter is coupled between the high voltage bus of the supply voltage and the fourth transistor.

6. The sense amplifier of claim 5, further comprising:

wherein the first and second inverters each comprise a PMOS transistor coupled to an NMOS transistor sharing a common gate input, wherein the common gate of the first inverter is coupled to the first transistor and the first output node and wherein the common gate of the second inverter is coupled to the second transistor and the second output node.

7. The sense amplifier of claim 6, further comprising:

a first capacitor coupled to the first output node and the low voltage bus and a second capacitor coupled between the second output node and the low voltage bus.

8. The sense amplifier of claim 1, wherein the first phase corresponds to a period where a sense signal, received at the sense amplifier, is at a first logic level and wherein the second phase corresponds to a period where the sense signal is at a second logic level.

9. The sense amplifier of claim 8, wherein the first logic level is a low logic level and the second logic level is a high logic level.

10. The sense amplifier of claim 9, wherein the sense signal is coupled to gates of the first and second transistors.

11. The sense amplifier of claim 1, wherein the sense amplifier is integrated into an electronic device, selected from the group consisting of a set top box, music player, video player, entertainment unit, navigation device, mobile phone, portable computer, hand-held personal communication system (PCS) units, communications device, personal digital assistant (PDA), fixed location data unit, and a computer.

12. The sense amplifier of claim 1, wherein the sense amplifier is integrated into a memory array comprising a plurality of sense amplifiers.

13. A method of sensing a differential between two bit lines, comprising:

coupling a first bit line to a first output node of a sense amplifier and a second bit line to a second output node of the sense amplifier, in a first phase to supply an initial differential voltage to the sense amplifier;

decoupling the first bit line from the first output node and the second bit line from the second output node during a second phase; and

amplifying the initial differential voltage by discharging the first output node based on a voltage on the second bit line and the second output node based on a voltage on the first bit line, in the second phase.

14. The method of claim 13, further comprising:

deactivating the sense amplifier via a transistor coupled to a sense input during the first phase; and

activating the sense amplifier via the transistor during the second phase.

15. The method of claim 14, wherein the sense input is at a low logic state during the first phase and a high logic state during the second phase.

16. The method of claim 15, further comprising:
coupling one of the first output node or the second output node to a supply voltage, when the other one of the first output node or the second output node reaches a threshold value.

17. The method of claim 16, wherein the first output node is cross coupled to gates of transistors coupled to the second output node and wherein the second output node is cross coupled to gates of transistors coupled to the first output node.

18. The method of claim 17, wherein a transistor is configured to prevent discharging the first and second output nodes in the first phase and to permit discharging the first and second output nodes in the second phase.

19. The method of claim 13, wherein first and second transistors transfer the initial differential voltage from the first and second bit lines to the output nodes of the sense amplifier during the first phase and wherein the first and second transistors block the initial differential voltage from the first and second bit lines during the second phase.

20. An apparatus for sensing a differential between two bit lines, comprising:
means for coupling a first bit line to a first output node of a sense amplifier and a second bit line to a second output node of the sense amplifier, in a first phase to supply an initial differential voltage to the sense amplifier;

means for decoupling the first bit line from the first output node and the second bit line from the second output node during a second phase; and

means for amplifying the initial differential voltage by discharging the first output node based on a voltage on the second bit line and the second output node based on a voltage on the first bit line, in the second phase.

21. The apparatus of claim 20, further comprising:

means for deactivating the sense amplifier via a transistor coupled to a sense input during the first phase; and

means for activating the sense amplifier via the transistor during the second phase.

22. The apparatus of claim 21, wherein the sense input is at a low logic state during the first phase and a high logic state during the second phase.

23. The apparatus of claim 20, further comprising:

means for coupling one of the first output node or the second output node to a supply voltage, when the other one of the first output node or the second output node reaches a threshold value.

24. The apparatus of claim 23, wherein the first output node is cross coupled to gates of transistors coupled to the second output node and wherein the second output node is cross coupled to gates of transistors coupled to the first output node.

25. The apparatus of claim 24, wherein a transistor is configured to prevent discharging the first and second output nodes in the first phase and to permit discharging the first and second output nodes in the second phase.

26. The apparatus of claim 20, wherein first and second transistors transfer the initial differential voltage from the first and second bit lines to the output nodes of the sense amplifier during the first phase and wherein the first and second transistors block the initial differential voltage from the first and second bit lines during the second phase.

27. The apparatus of claim 20, wherein the apparatus is integrated into an electronic device, selected from the group consisting of a set top box, music player, video player, entertainment unit, navigation device, mobile phone, portable computer, hand-held personal communication system (PCS) units, communications device, personal digital assistant (PDA), fixed location data unit, and a computer.

28. The apparatus of claim 20, wherein the apparatus is integrated into a memory array.

29. A method of sensing a differential between two bit lines, comprising:

step for coupling a first bit line to a first output node of a sense amplifier and a second bit line to a second output node of the sense amplifier, in a first phase to supply an initial differential voltage to the sense amplifier;

step for decoupling the first bit line from the first output node and the second bit line from the second output node during a second phase; and

step for amplifying the initial differential voltage by discharging the first output node based on a voltage on the second bit line and the second output node based on a voltage on the first bit line, in the second phase.

30. The method of claim 29, further comprising:

step for deactivating the sense amplifier via a transistor coupled to a sense input during the first phase; and

step for activating the sense amplifier via the transistor during the second phase.

31. The method of claim 30, wherein the sense input is at a low logic state during the first phase and a high logic state during the second phase.

32. The method of claim 29, further comprising:

step for coupling one of the first output node or the second output node to a supply voltage, when the other one of the first output node or the second output node reaches a threshold value.

33. The method of claim 32, wherein the first output node is cross coupled to gates of transistors coupled to the second output node and wherein the second output node is cross coupled to gates of transistors coupled to the first output node.

34. The method of claim 33, wherein a transistor is configured to prevent discharging the first and second output nodes in the first phase and to permit discharging the first and second output nodes in the second phase.

35. The method of claim 29, wherein first and second transistors transfer the initial differential voltage from the first and second bit lines to the output nodes of the sense

amplifier during the first phase and wherein the first and second transistors block the initial differential voltage from the first and second bit lines during the second phase.

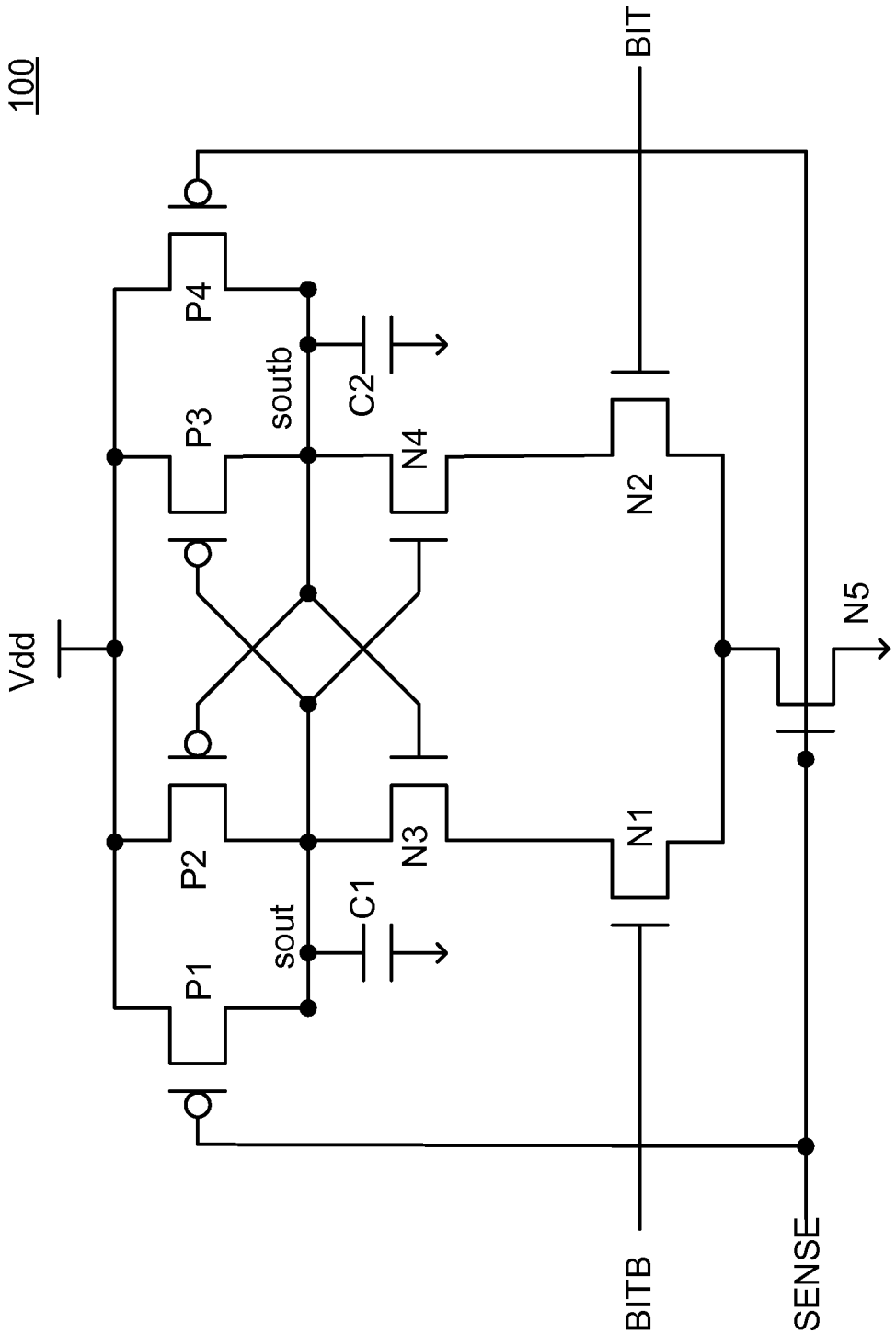

Fig. 1
Conventional Art

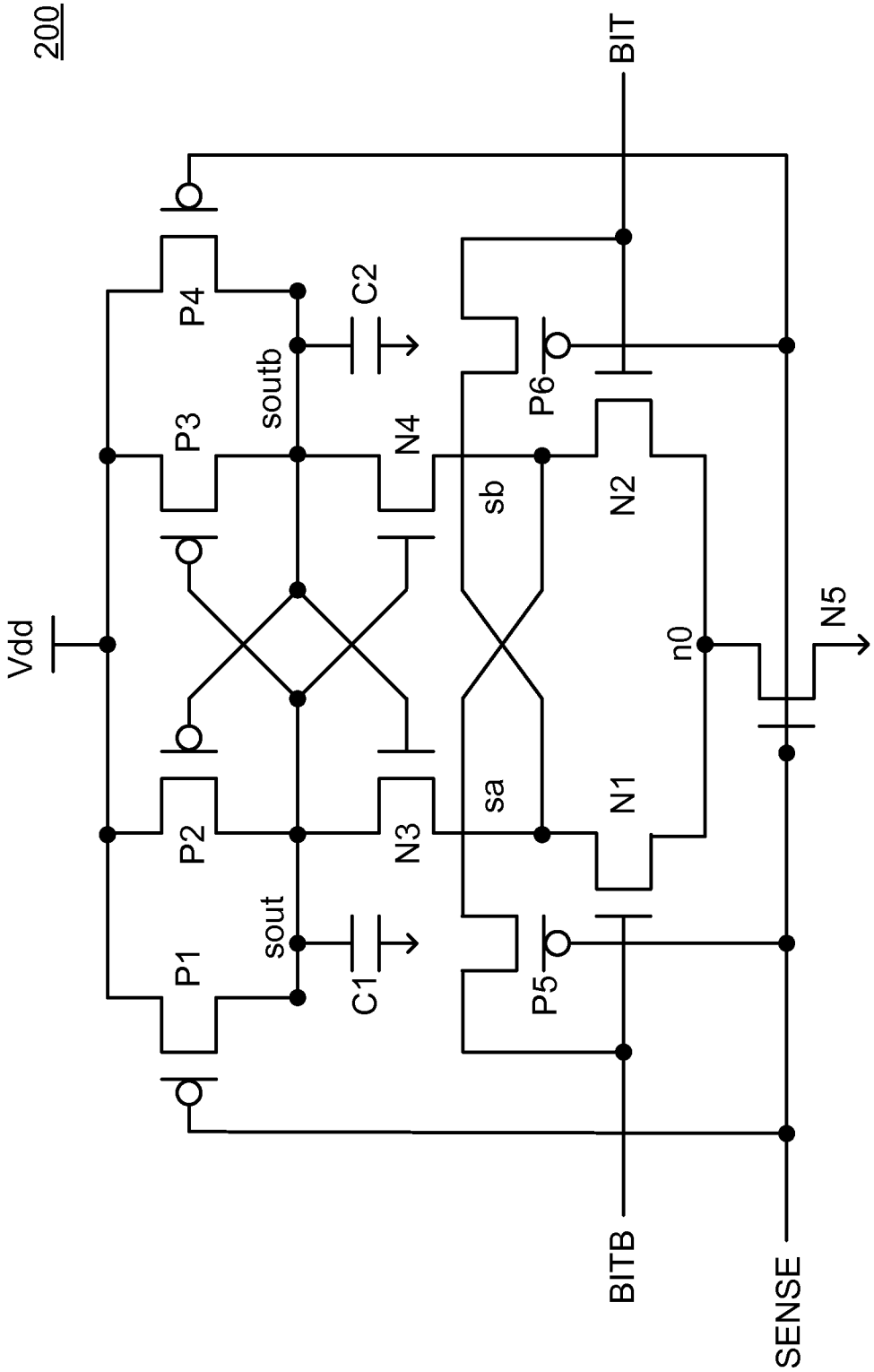

Fig. 2
Conventional Art

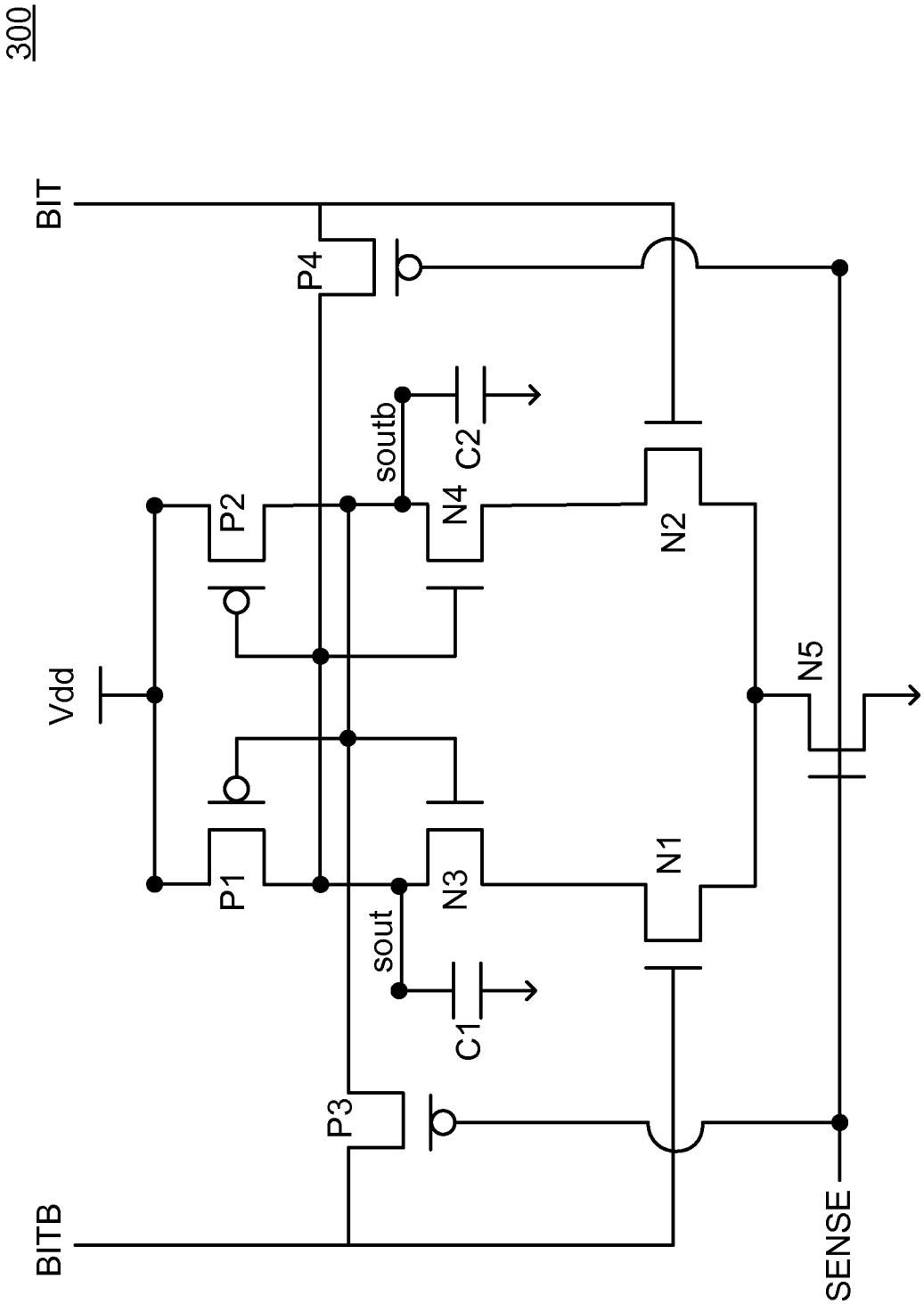

Fig. 3

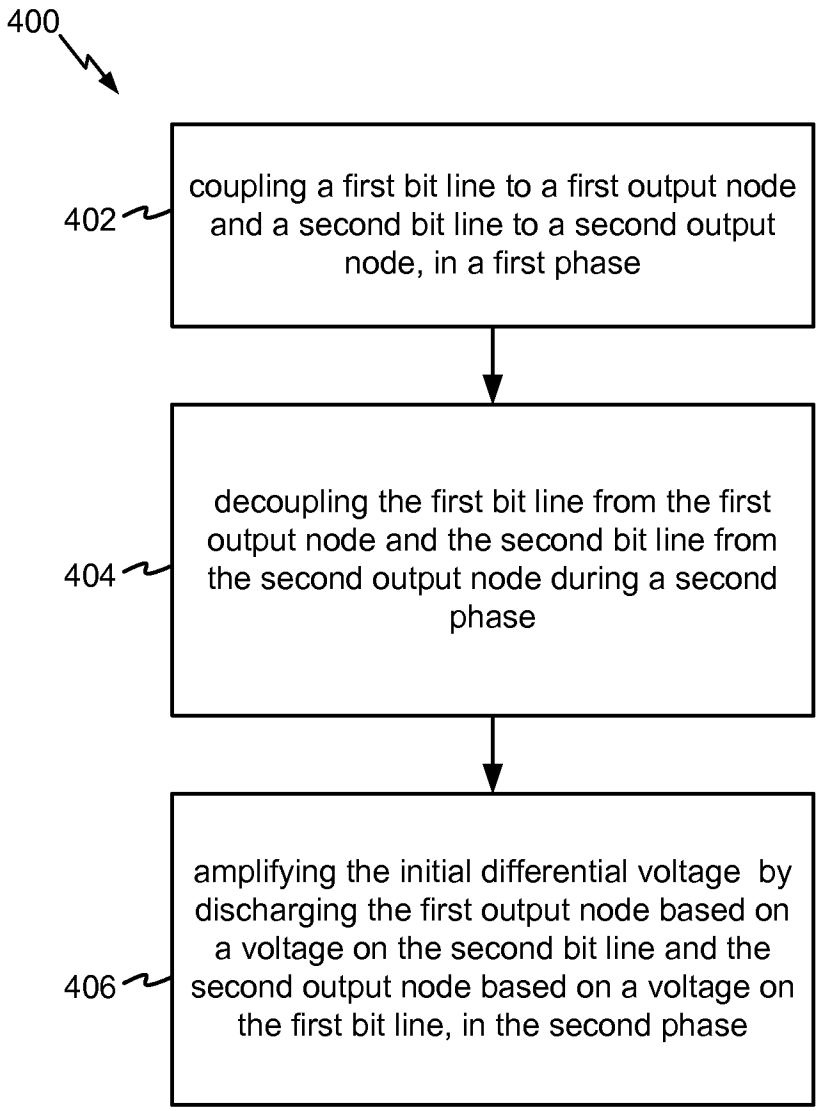
400
402
coupling a first bit line to a first output node and a second bit line to a second output node, in a first phase
404
decoupling the first bit line from the first output node and the second bit line from the second output node during a second phase
406
amplifying the initial differential voltage by discharging the first output node based on a voltage on the second bit line and the second output node based on a voltage on the first bit line, in the second phase

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/029479

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C7/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 687 175 B1 (MIZUNO HIROYUKI [JP] ET AL) 3 February 2004 (2004-02-03)	1,3,5-35
Y	the whole document	2,4

Y	US 2004/136253 A1 (GUPTA ANUJ [IN] ET AL) 15 July 2004 (2004-07-15) the whole document	2,4

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2011	10/05/2011

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2011/029479

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