US 20130320526A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2013/0320526 A1**

(43) **Pub. Date: Dec. 5, 2013**

**Wakisaka et al.**

(54) **SEMICONDUCTOR CONSTRUCT AND MANUFACTURING METHOD THEREOF AS WELL AS SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

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(21) Appl. No.: **13/960,485**

(22) Filed: **Aug. 6, 2013**

**Related U.S. Application Data**

(63) Continuation of application No. 12/828,492, filed on Jul. 1, 2010, now Pat. No. 8,525,335.

(30) **Foreign Application Priority Data**

Jul. 3, 2009 (JP) ................................ 2009-158618
Jul. 3, 2009 (JP) ................................ 2009-158622
Jul. 3, 2009 (JP) ................................ 2009-158629

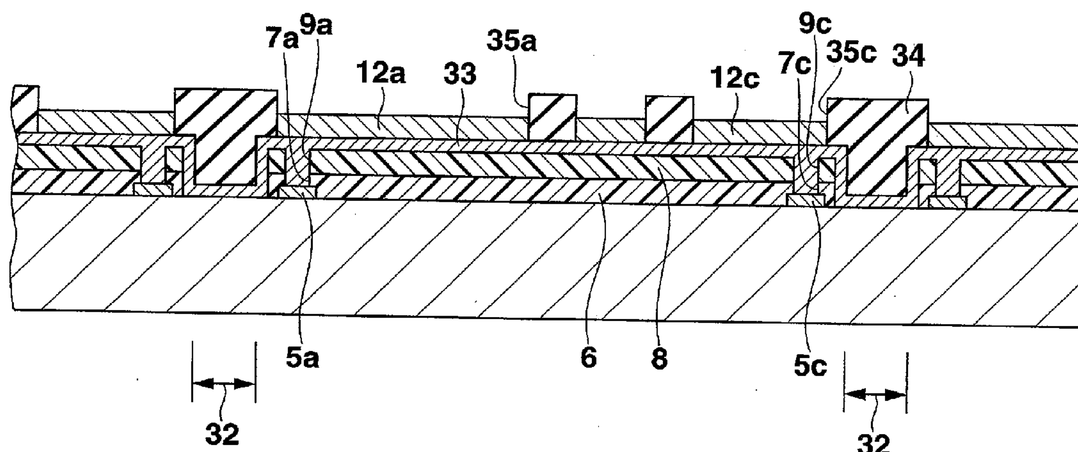
**Publication Classification**

(51) **Int. Cl.**
*H01L 23/00* (2006.01)

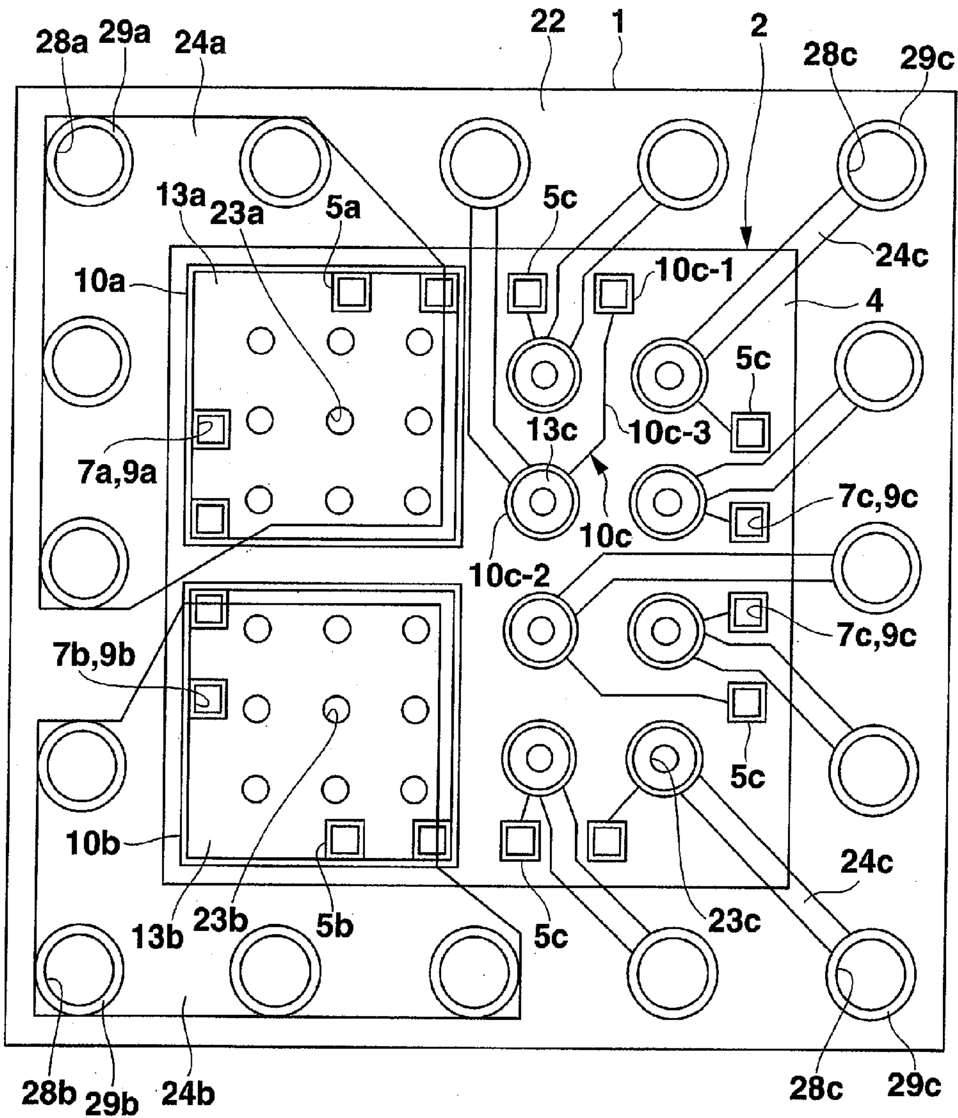
(52) **U.S. Cl.**
CPC ...................................... *H01L 24/14* (2013.01)
USPC ........................................................ **257/737**

(57) **ABSTRACT**

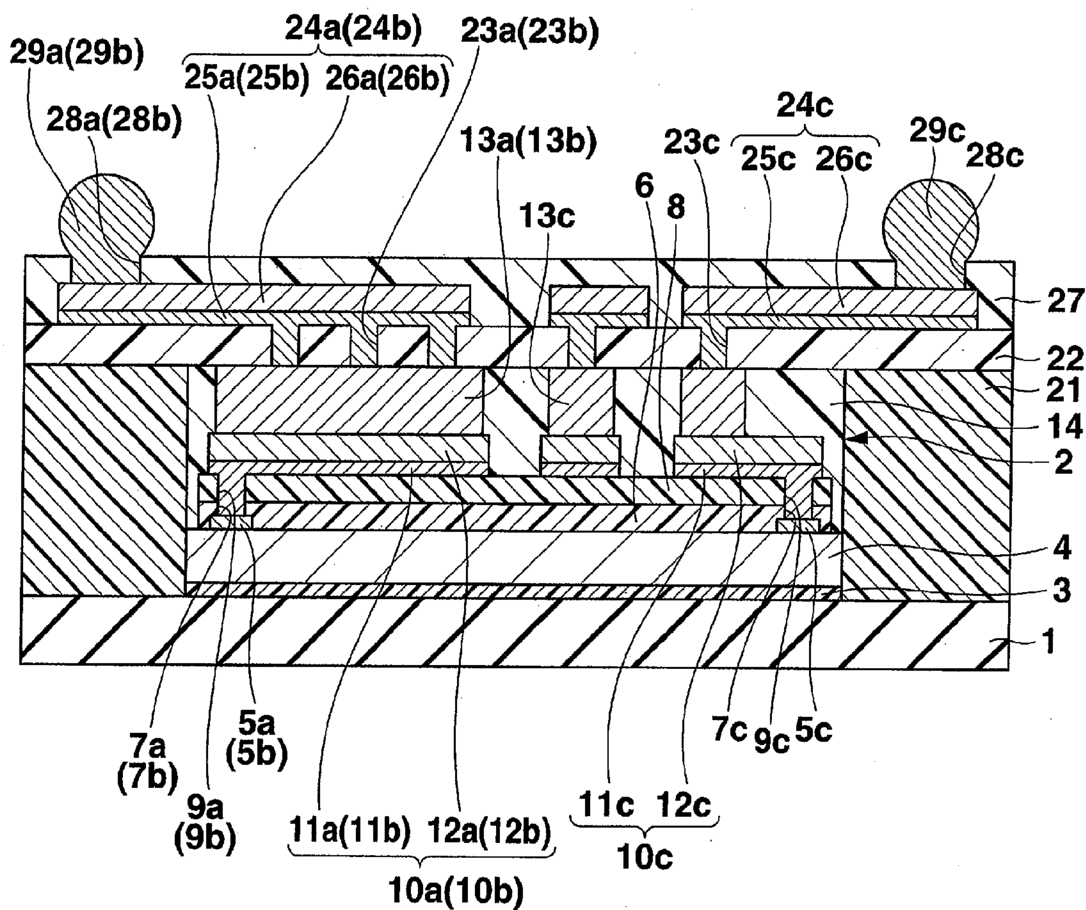
A semiconductor construct includes a semiconductor substrate and connection pads provided on the semiconductor substrate. Some of the connection pads are connected to a common wiring and at least one of the remaining of the connection pads are connected to a wiring. The construct also includes a first columnar electrode provided to be connected to the common wiring and a second columnar electrode provided to be connected to a connection pad portion of the wiring.



# FIG.1



# FIG.2



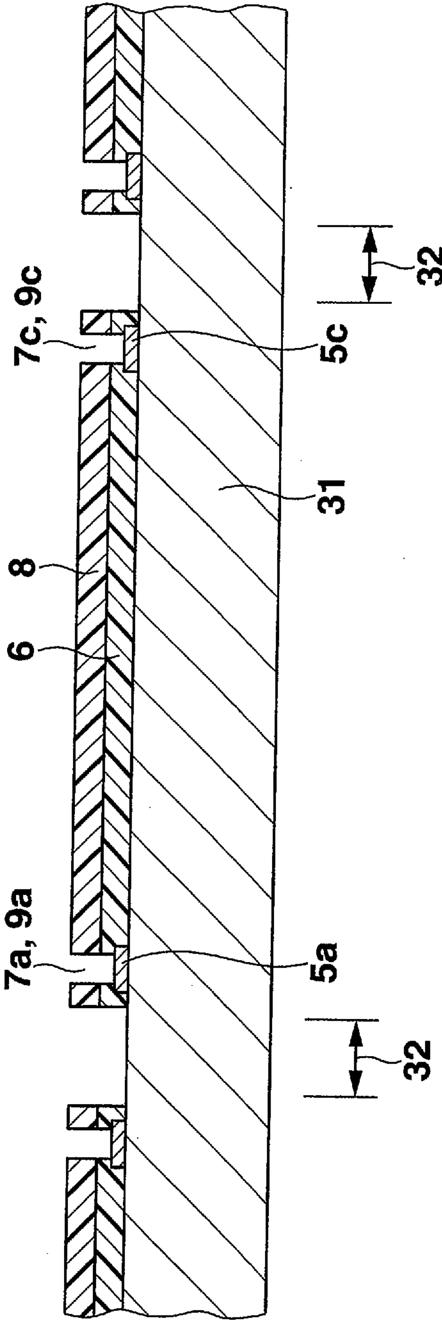


FIG.3
7c, 9c
5c
32
31
8
6
7a, 9a
5a
32

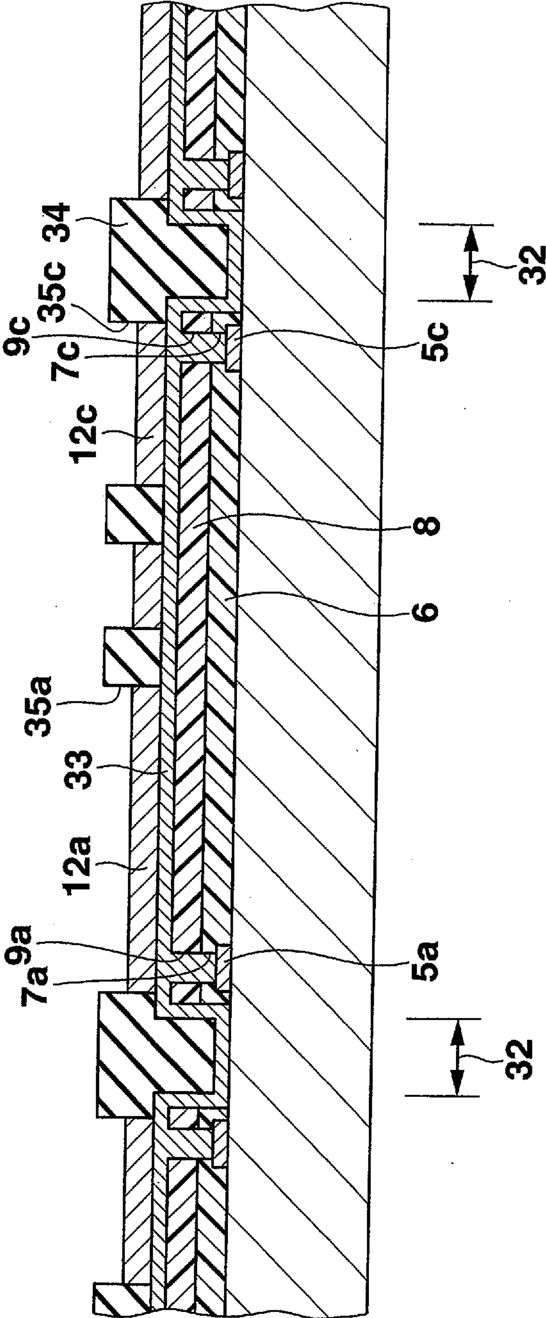



FIG.4

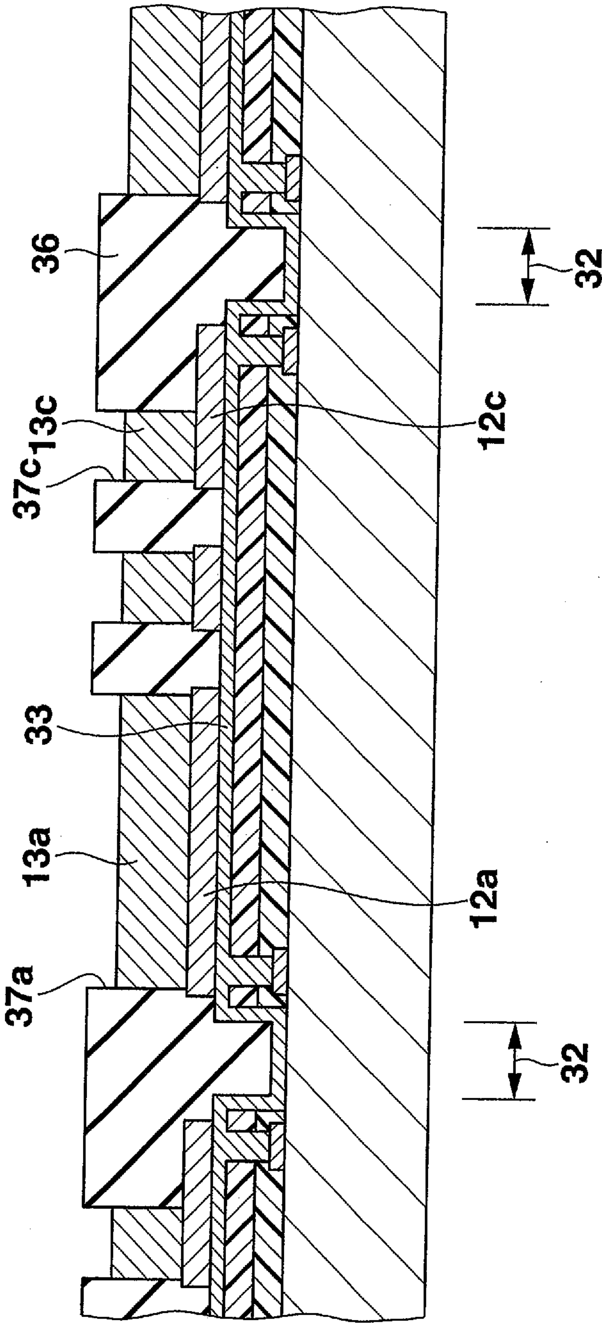



FIG.5

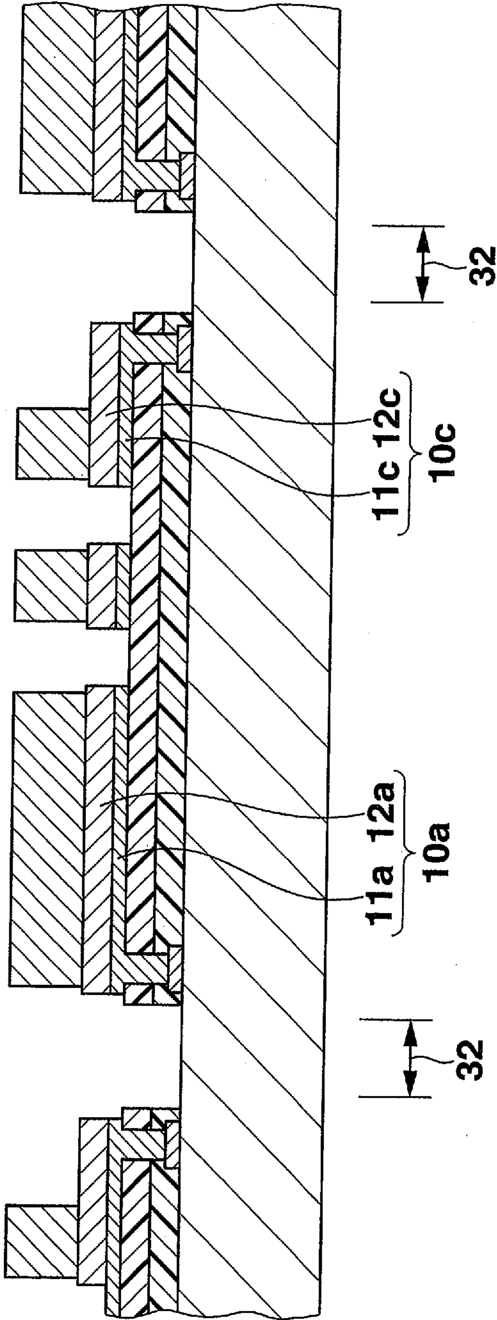


FIG.6
32
12c
11c
10c
12a
11a
10a
32

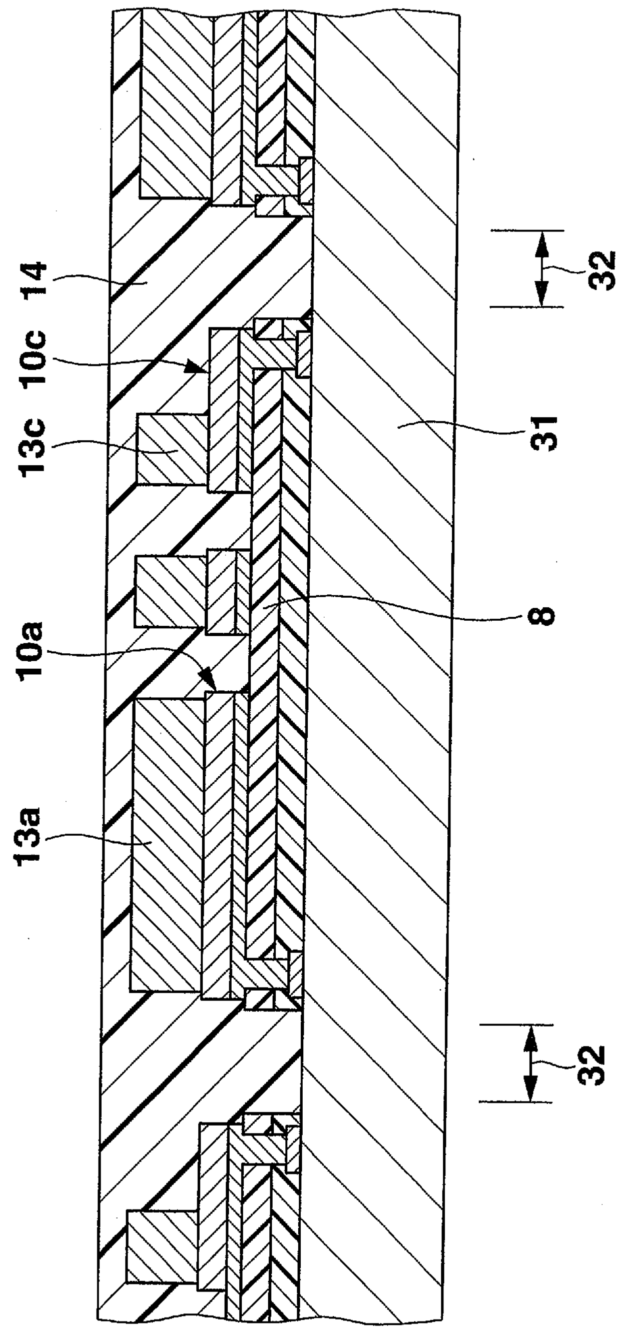



FIG.7

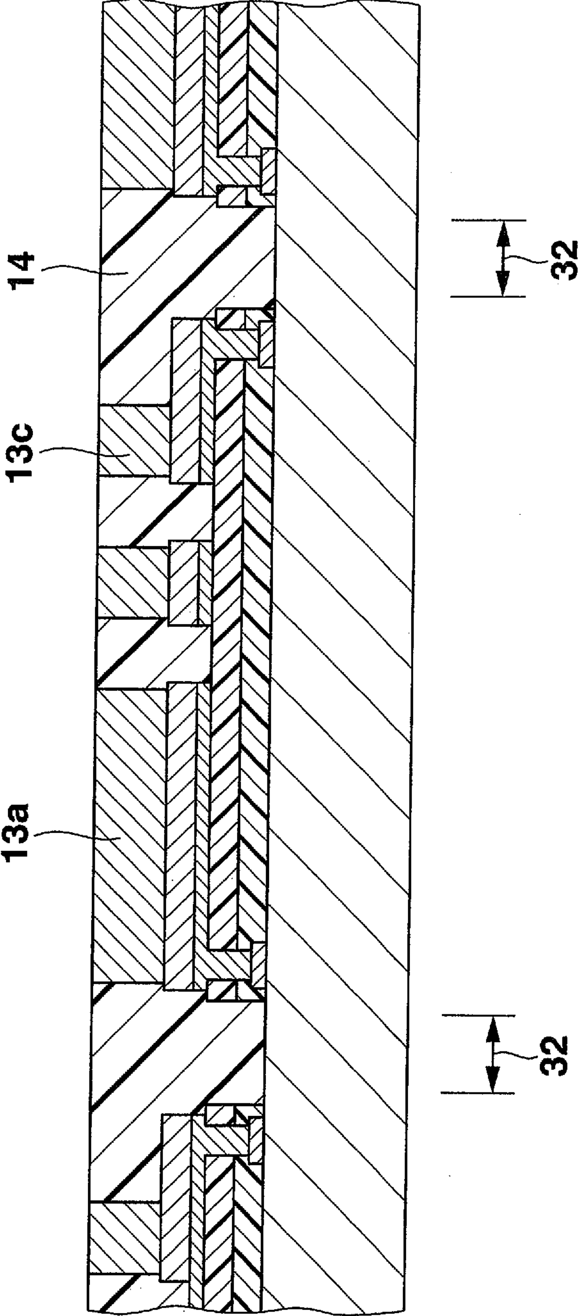



FIG.8

FIG.9

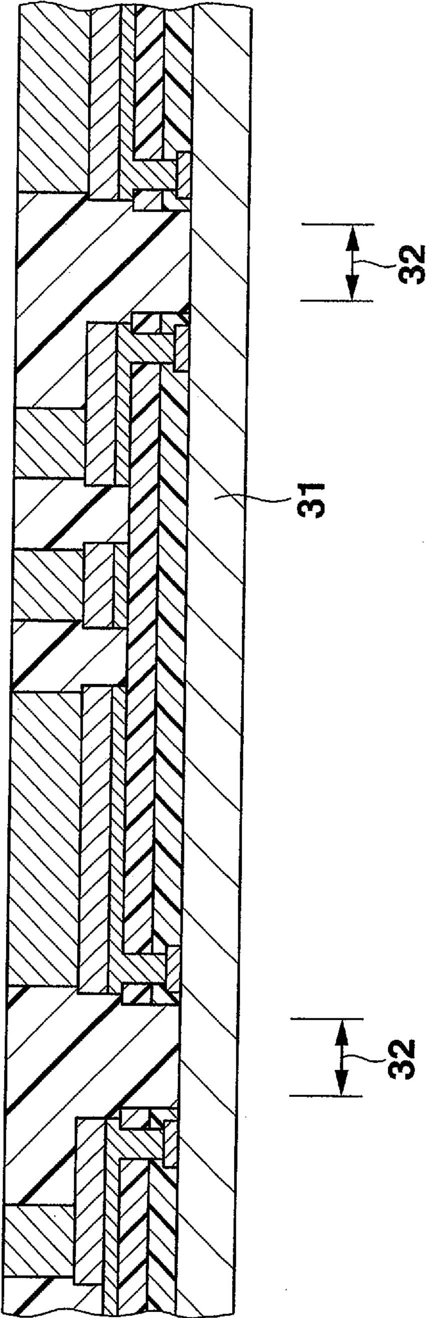
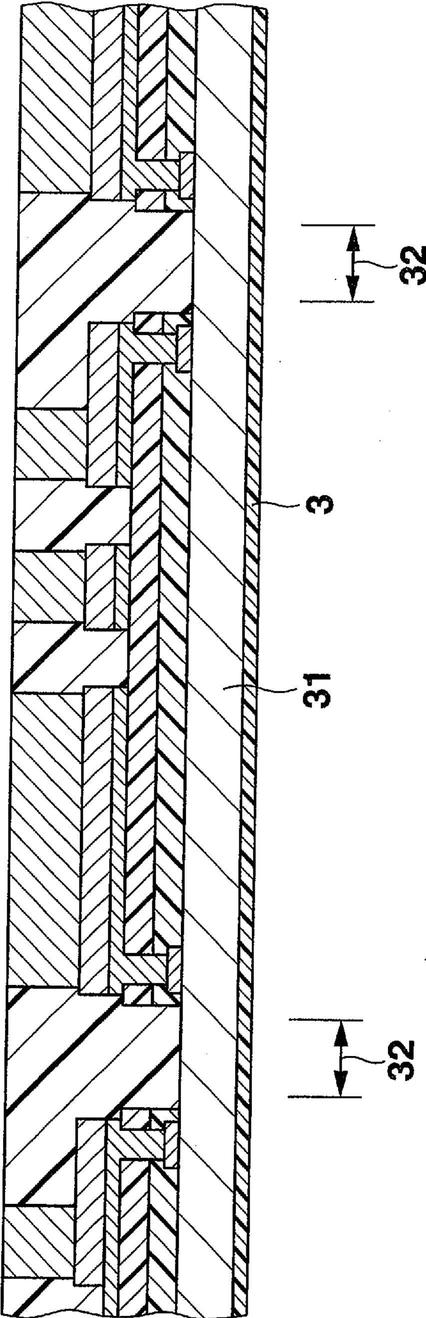


FIG.10



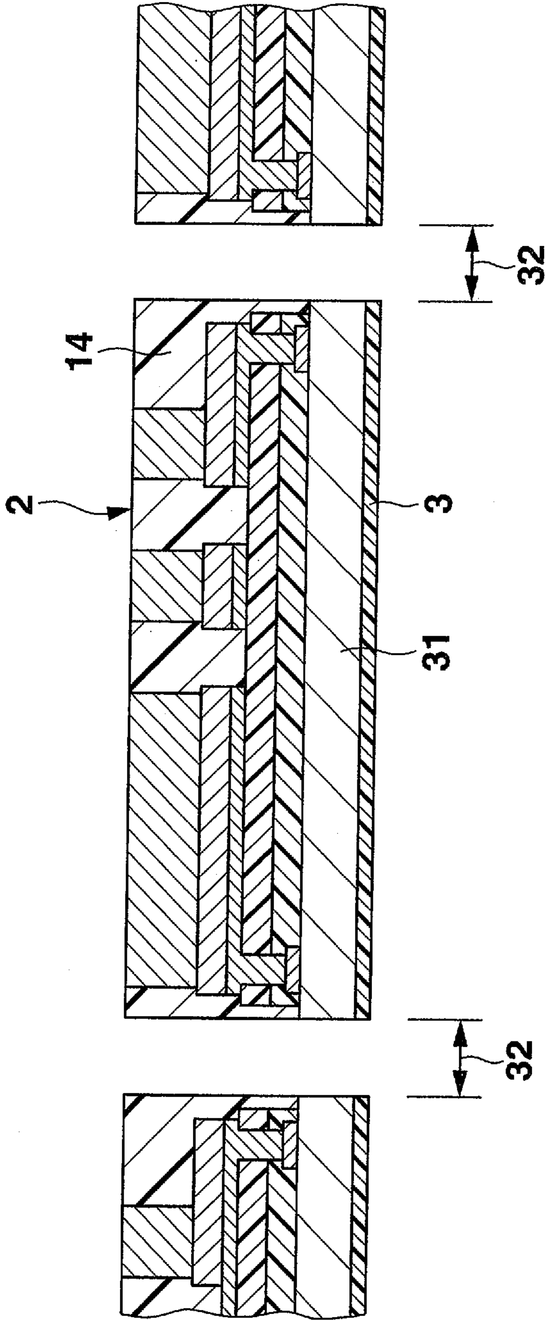


FIG.11
14
2
3
31
32
32

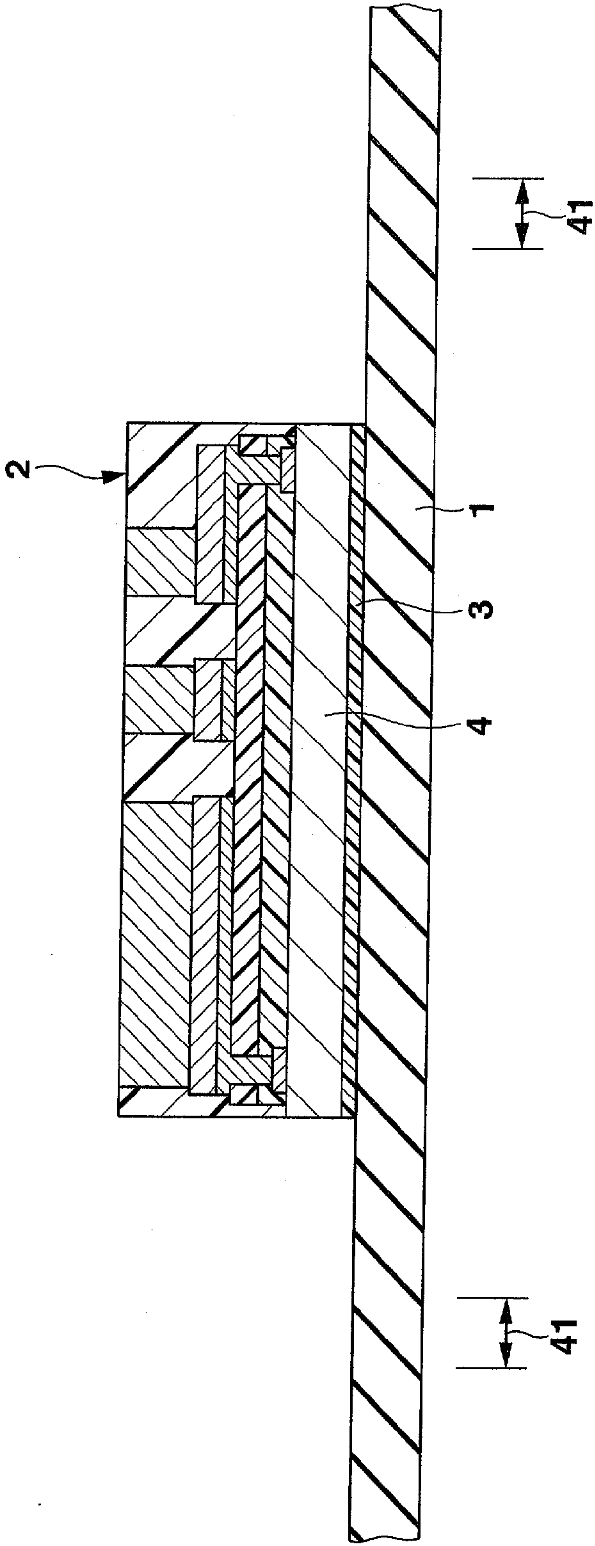



FIG.12

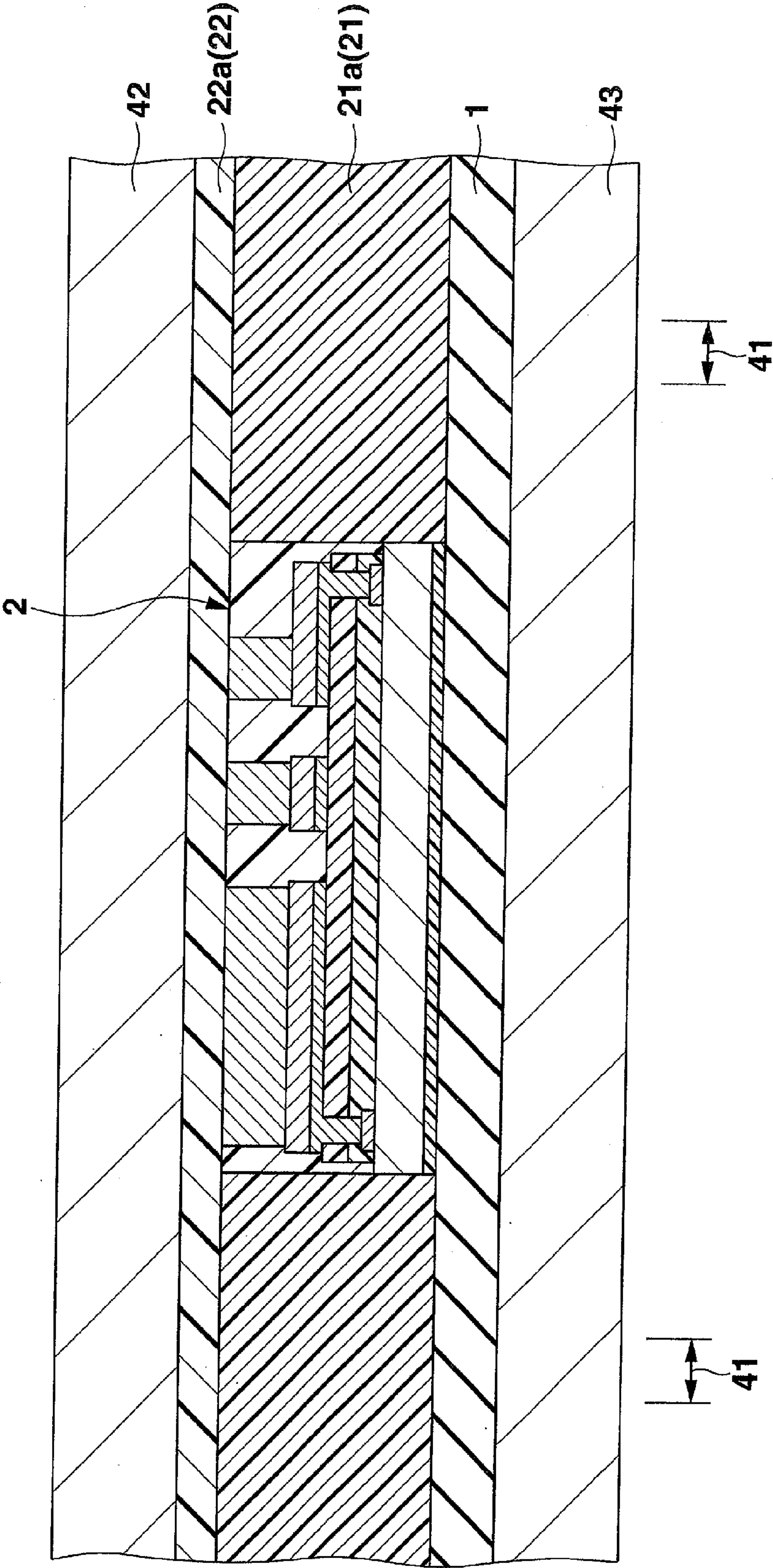



FIG.13

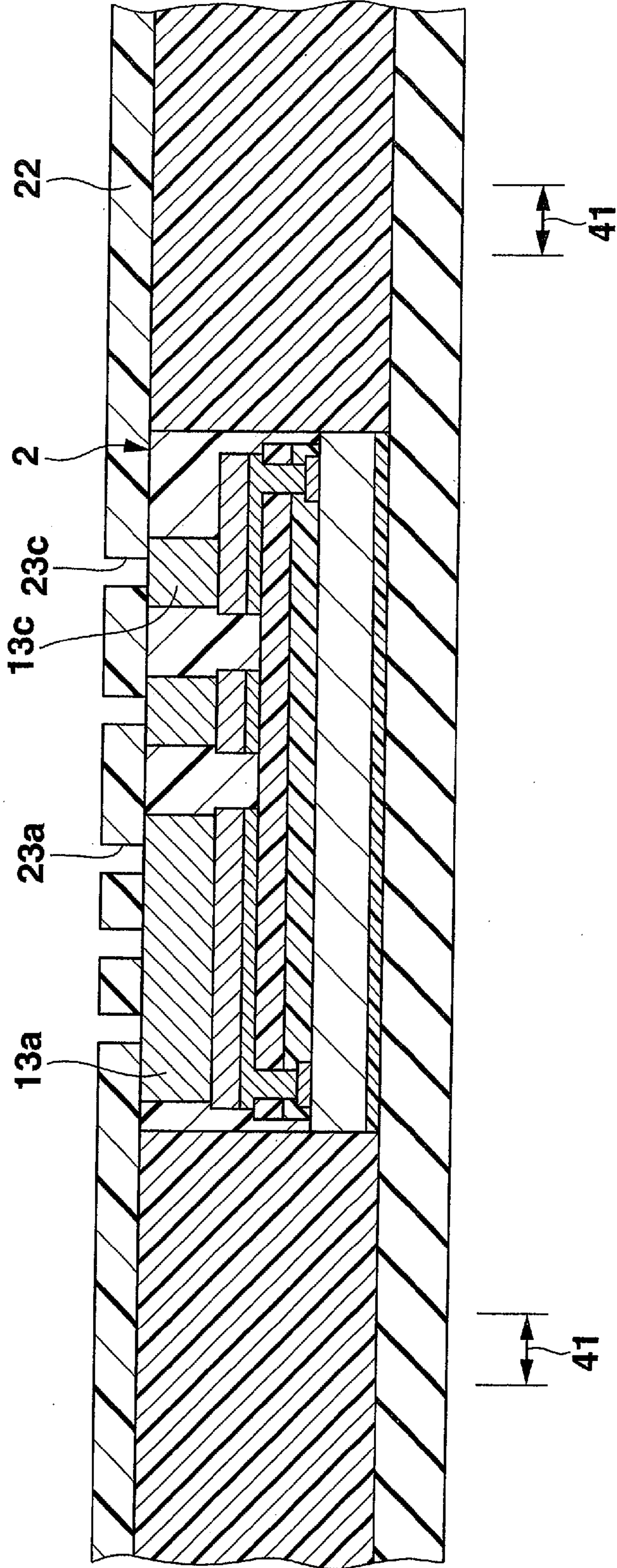


FIG.14
22
2
23c
13c
23a
13a
41
41

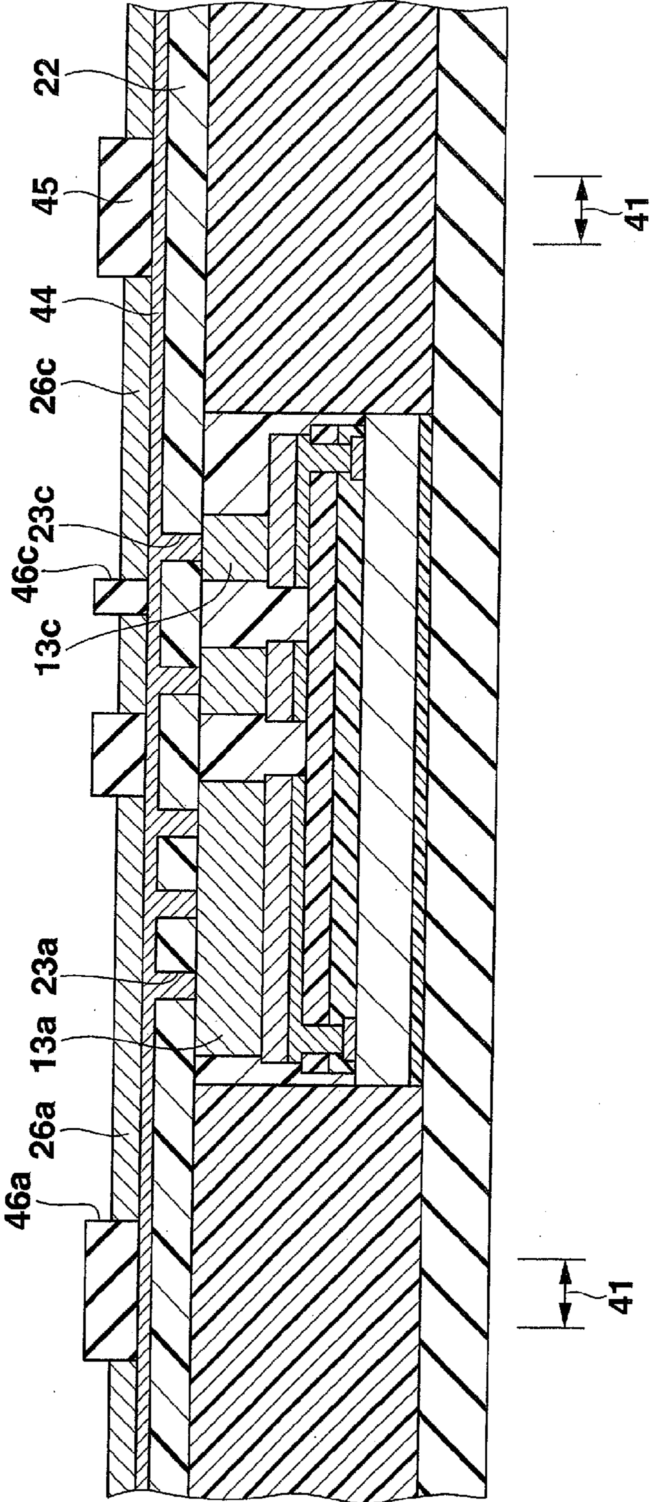
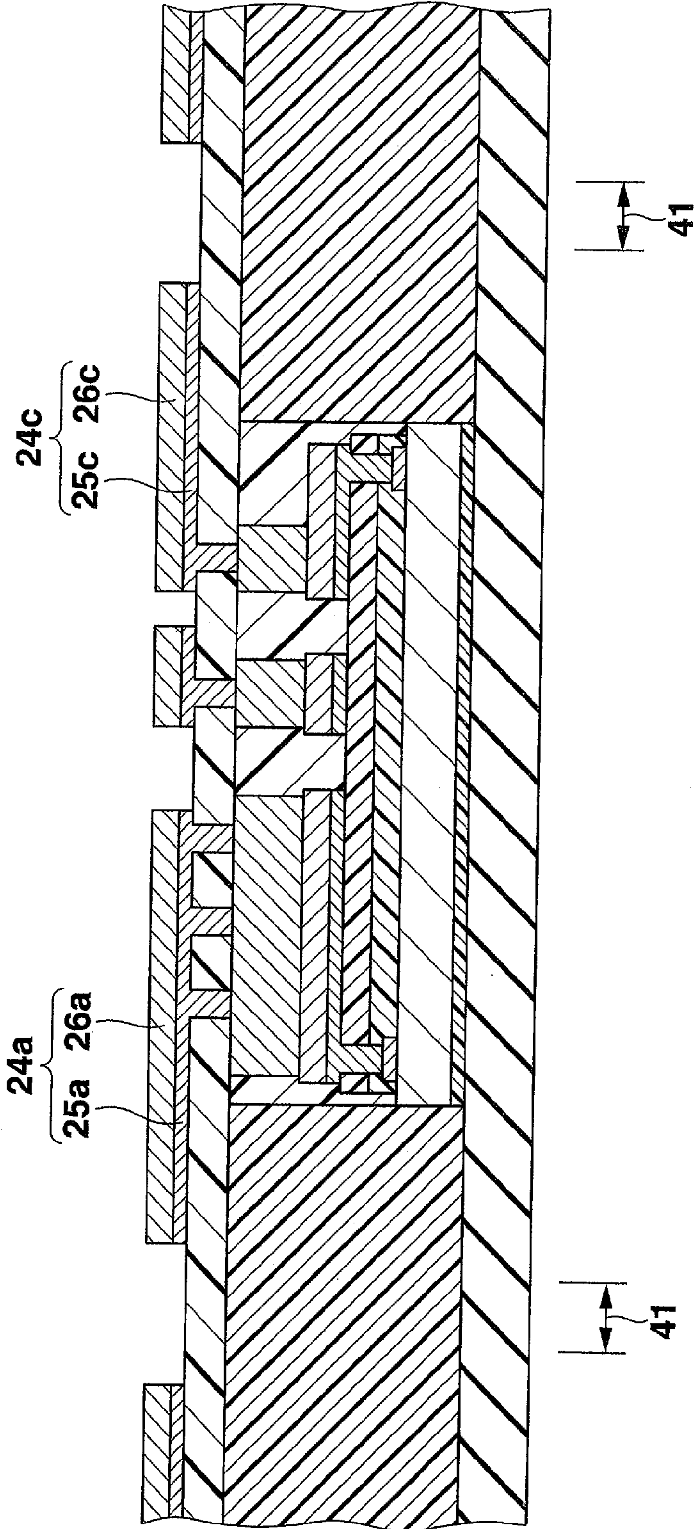



FIG.15

FIG.16



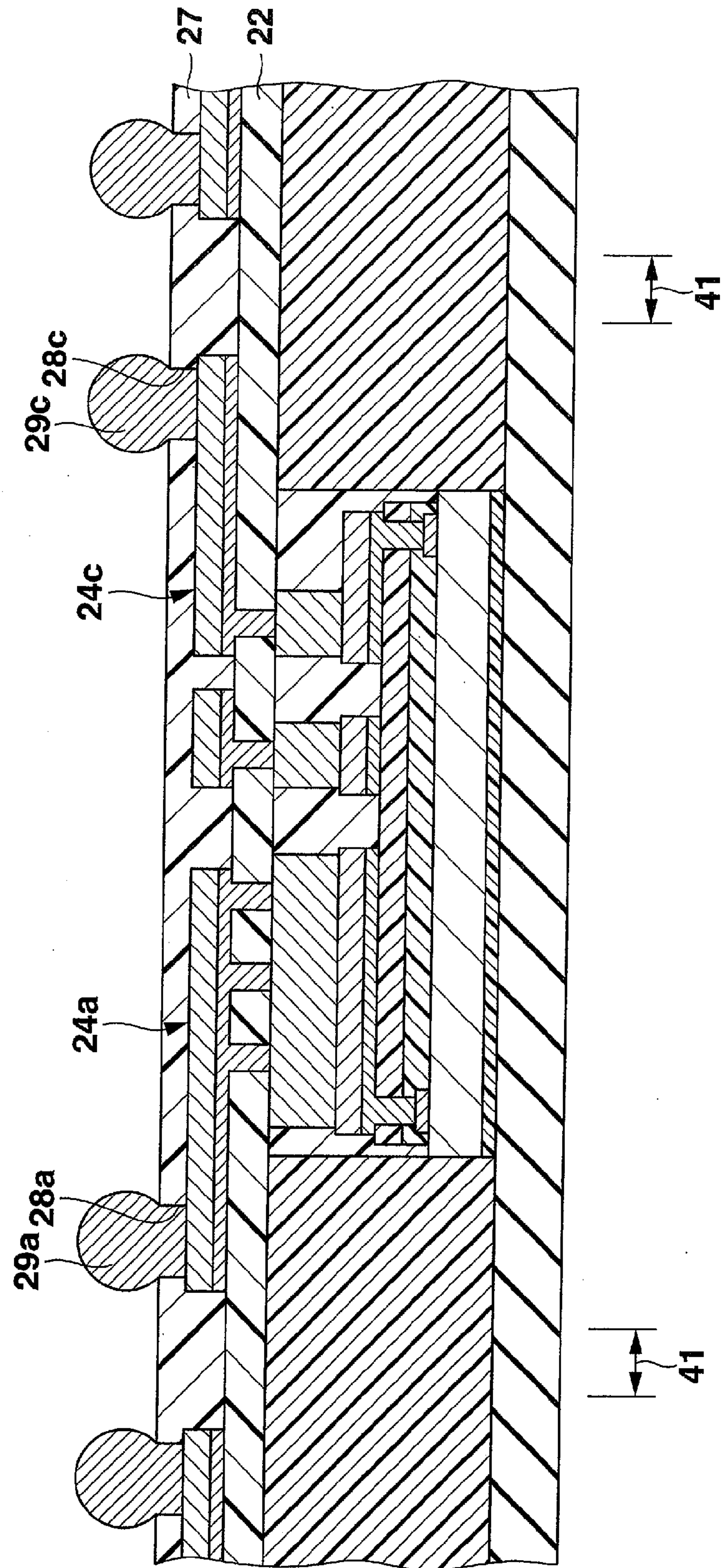


FIG.17
27
22
41
29c
28c
24c
24a
29a
28a
41

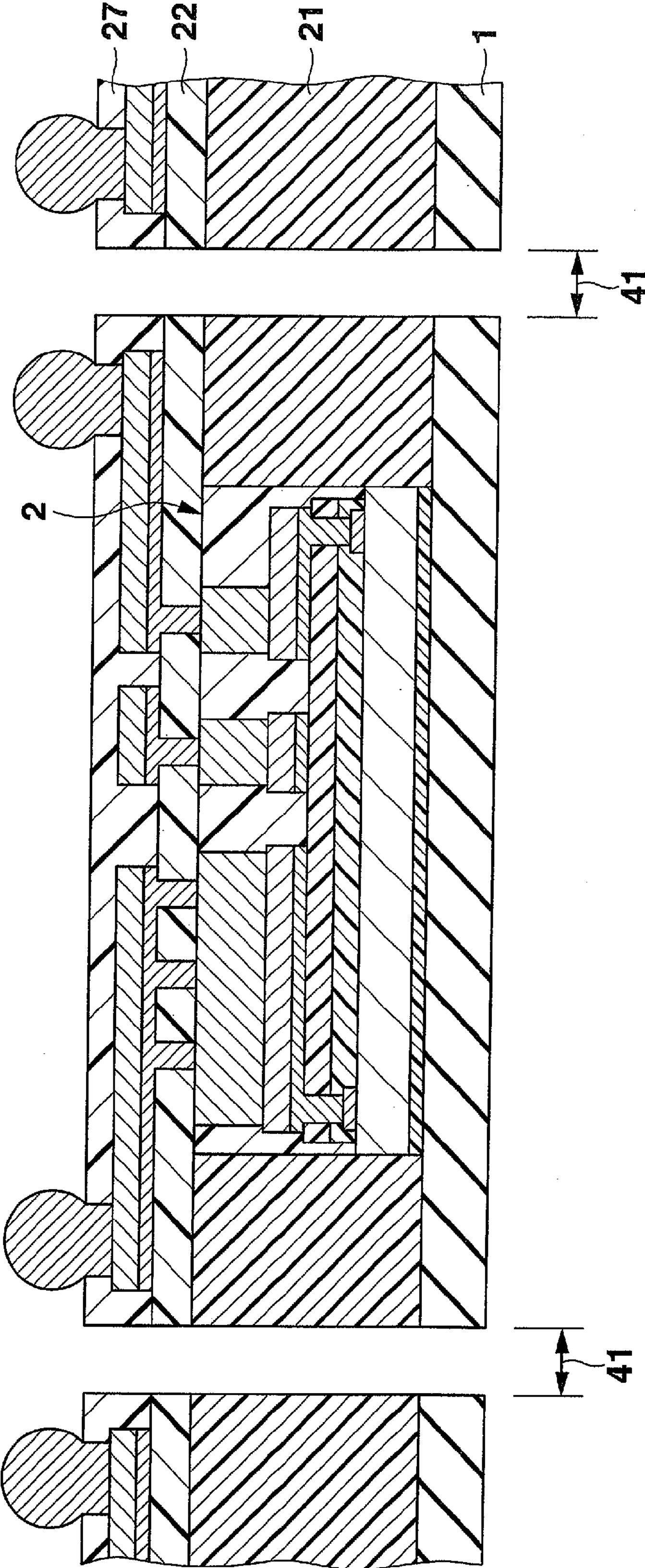



FIG.18

# FIG.19

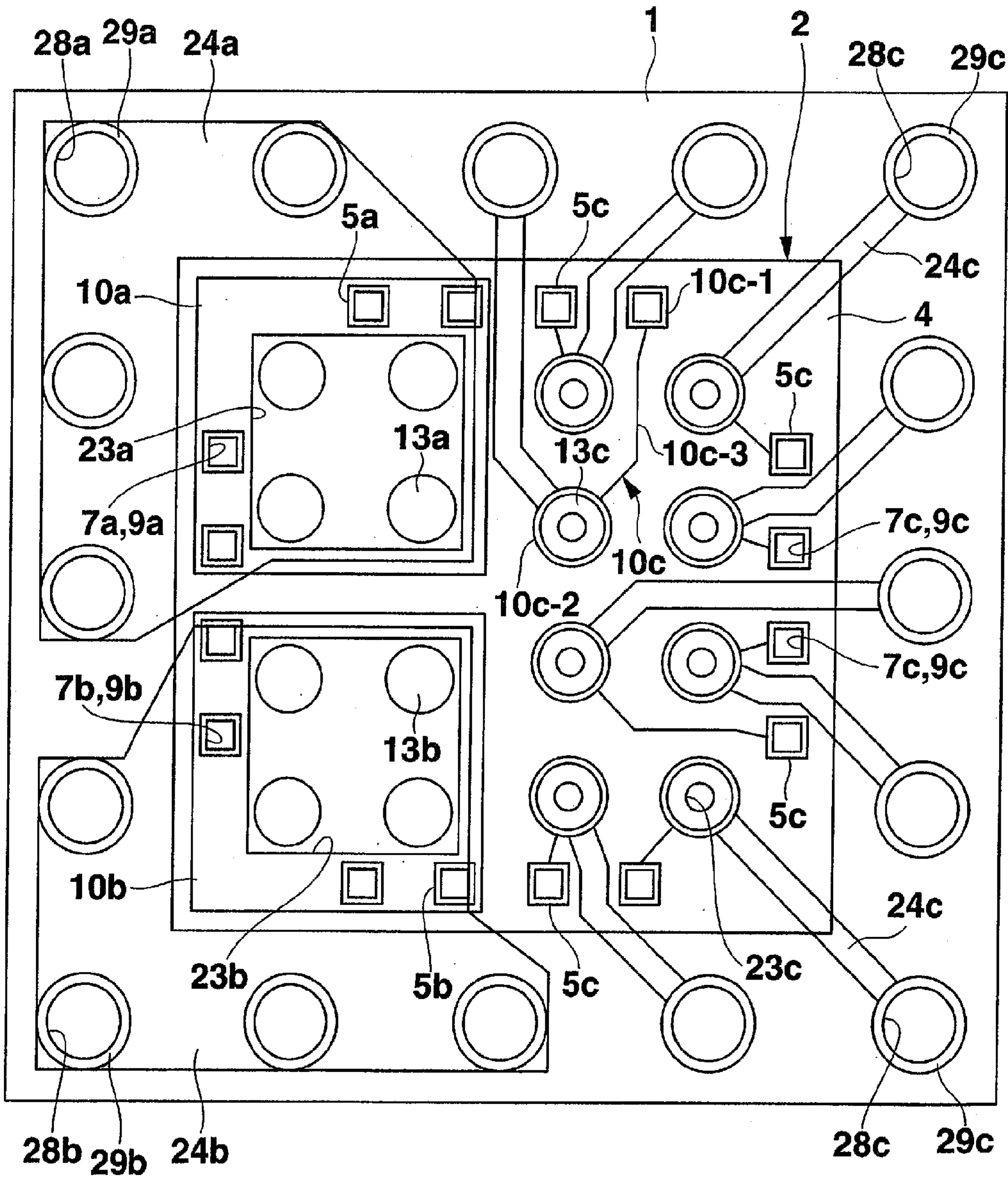


FIG.20

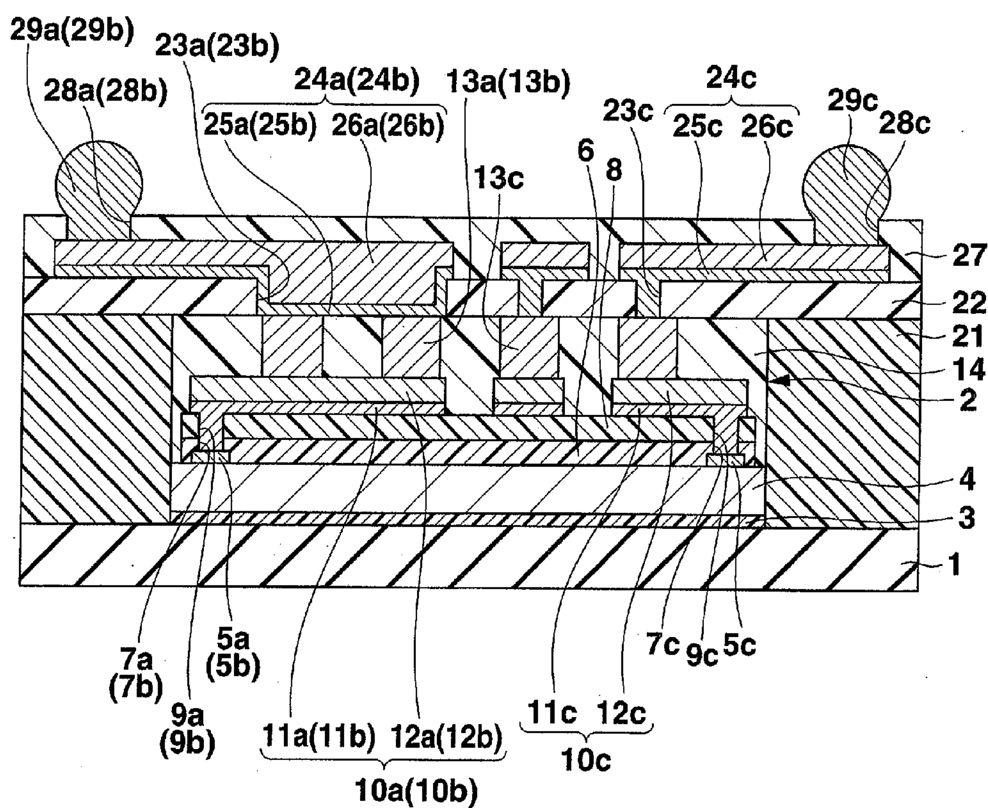
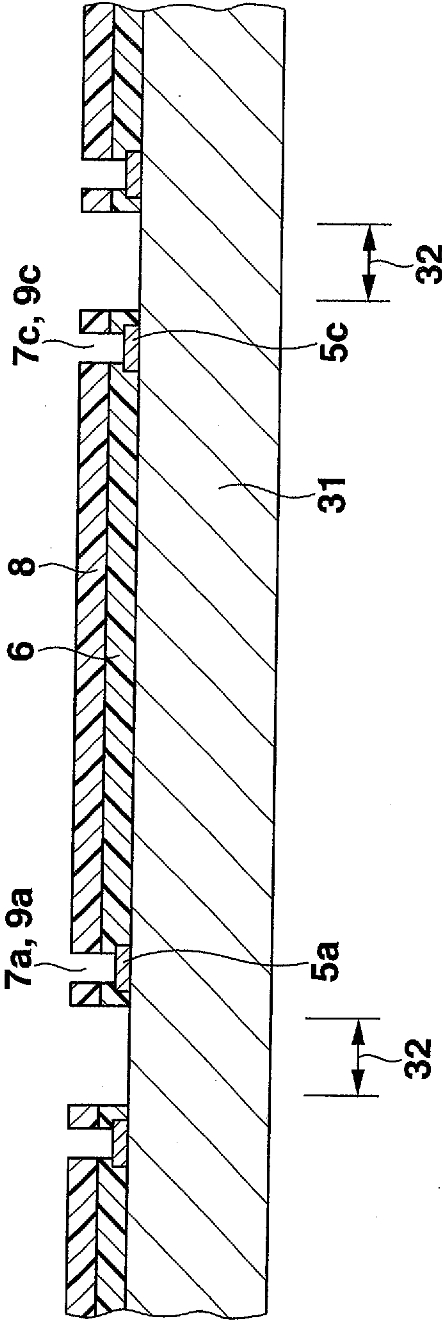


FIG.21



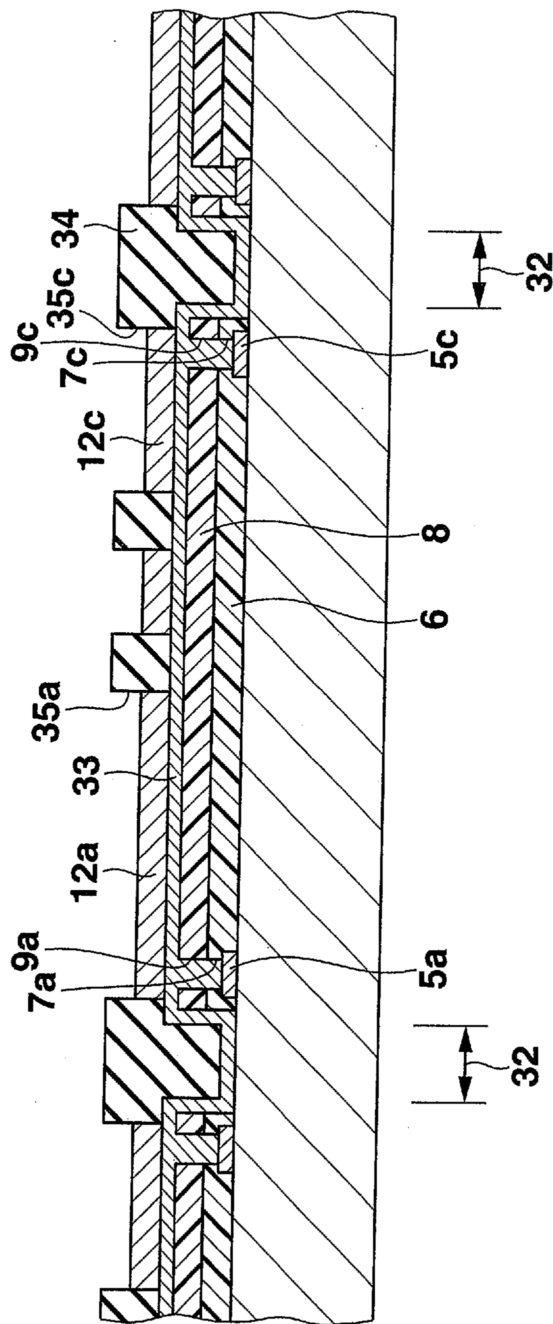


FIG.22
34
35c
9c
7c
12c
35a
33
12a
9a
7a
32
5c
8
6
5a
32

FIG.23

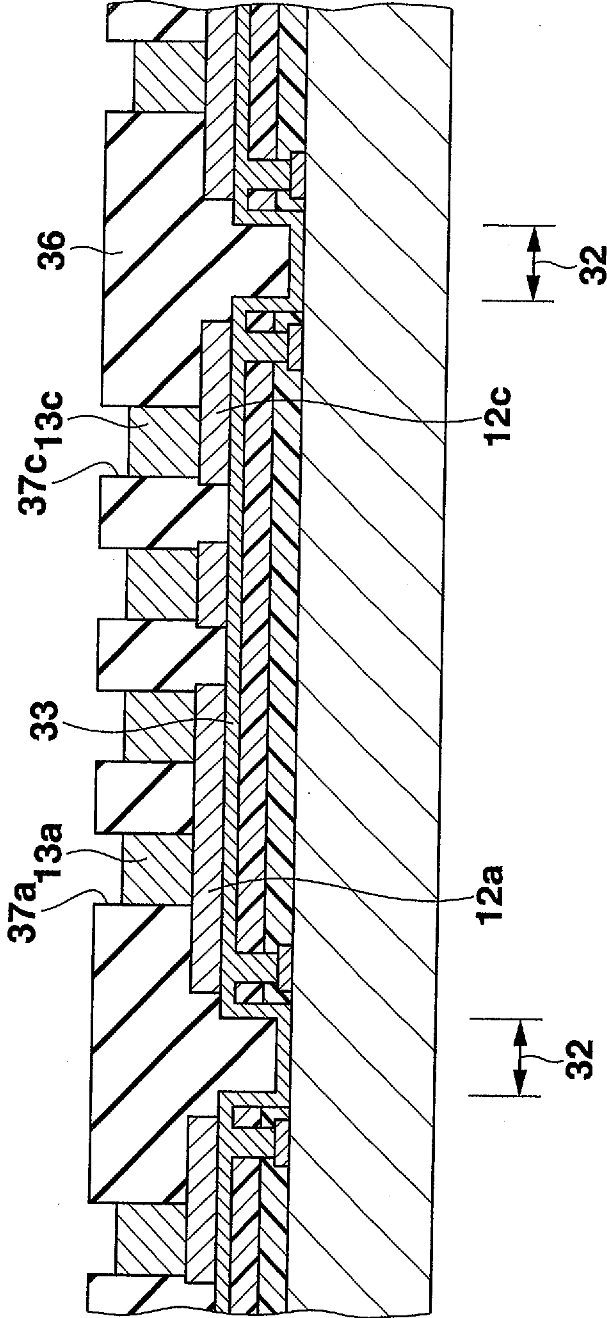


FIG.24

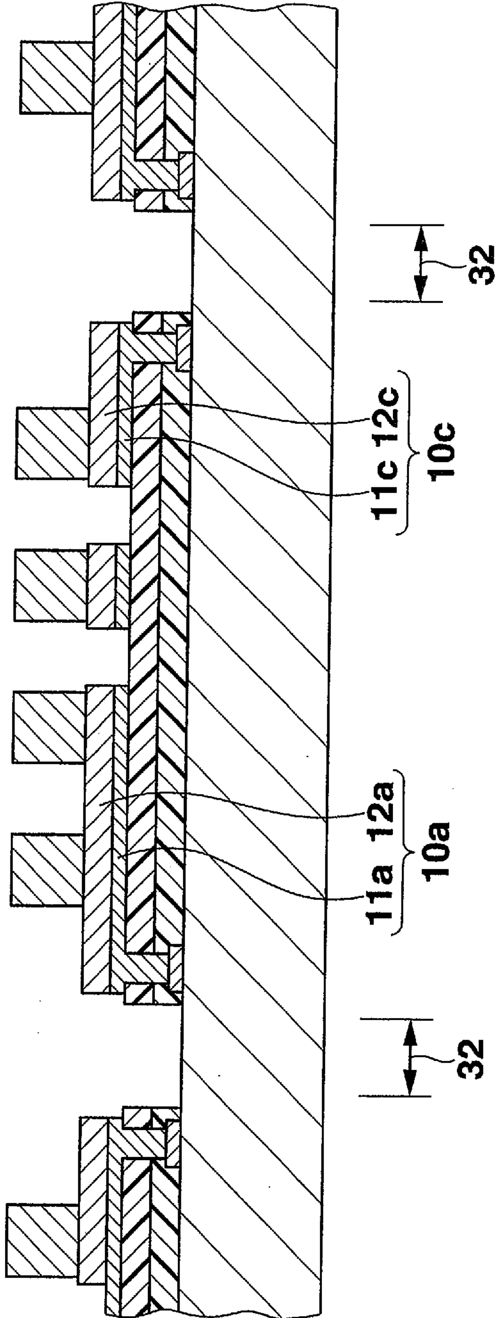
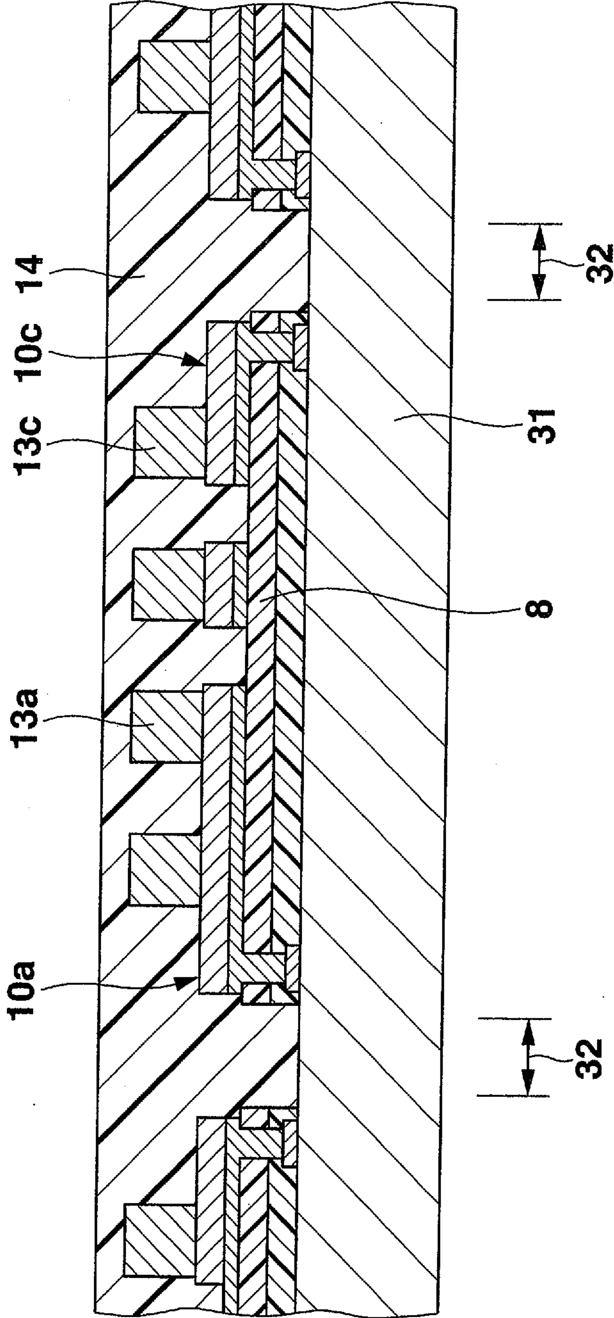


FIG.25



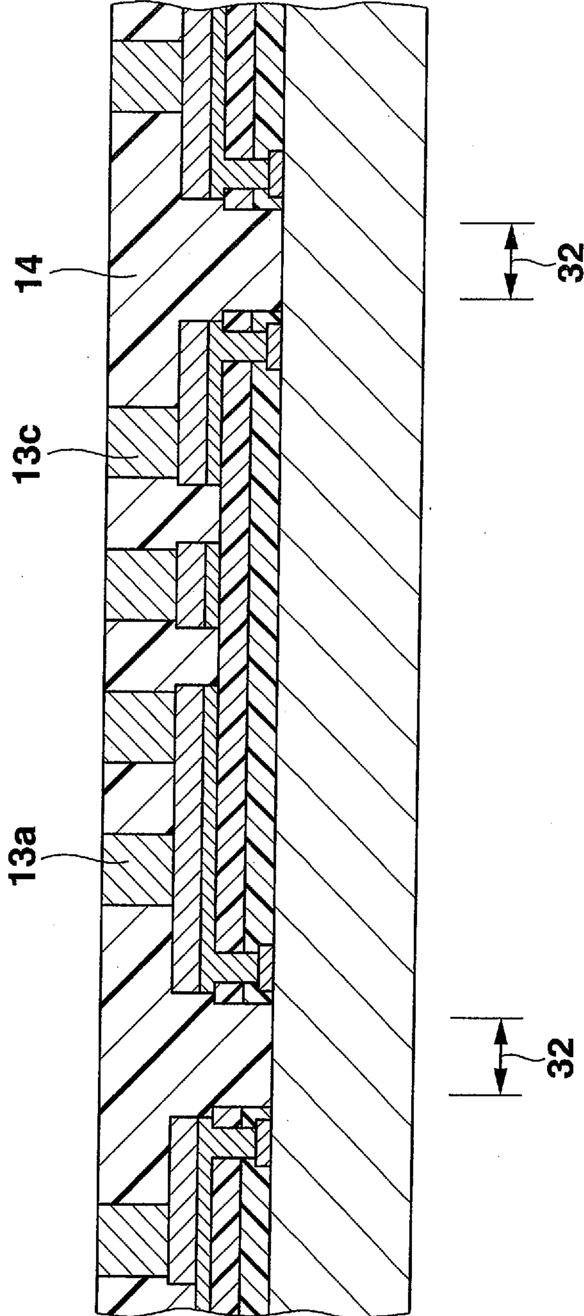
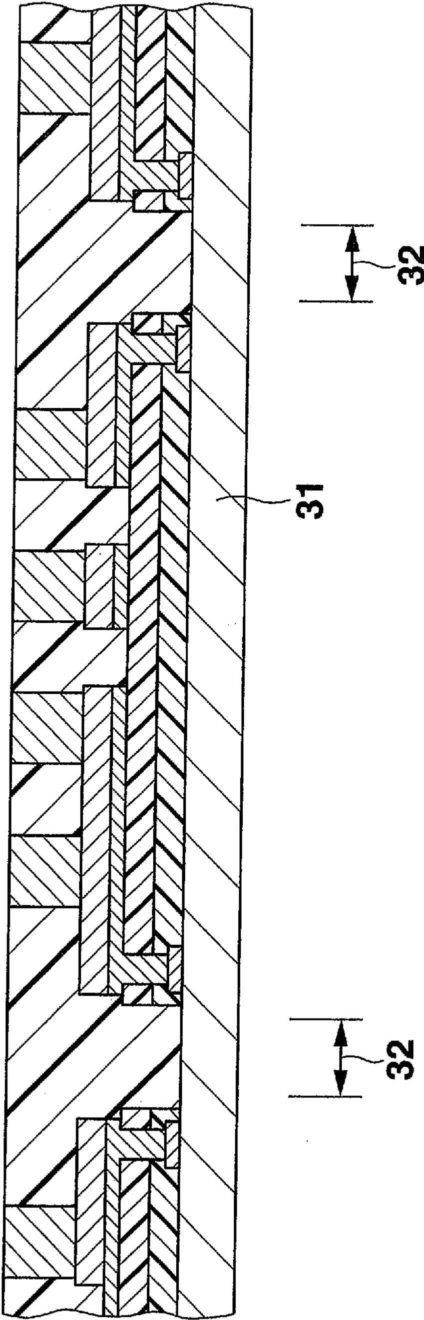


FIG.26
14
13c
13a
32
32

FIG.27



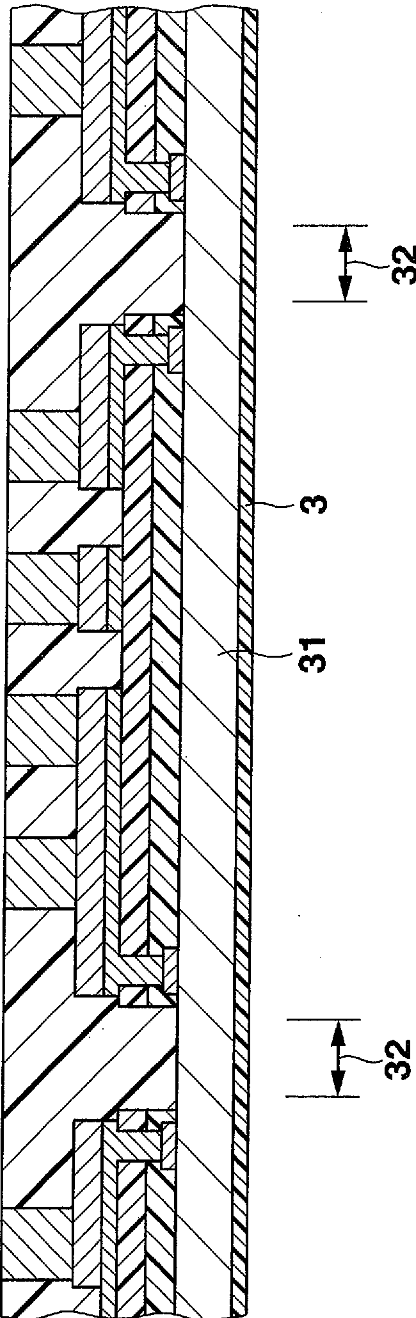



FIG.28

FIG.29

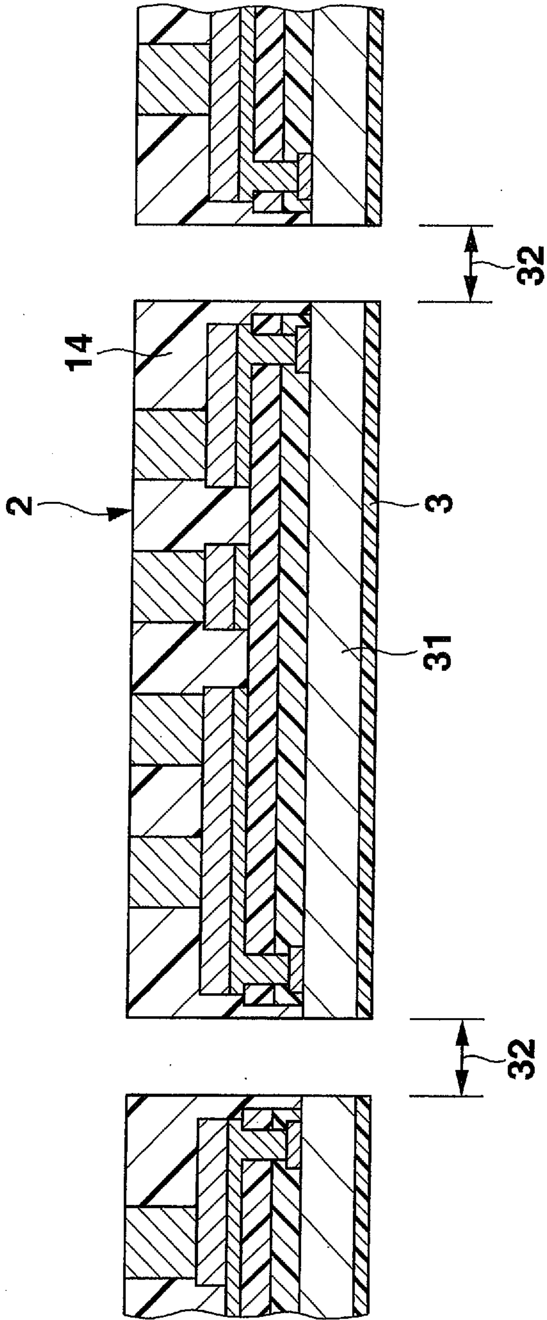
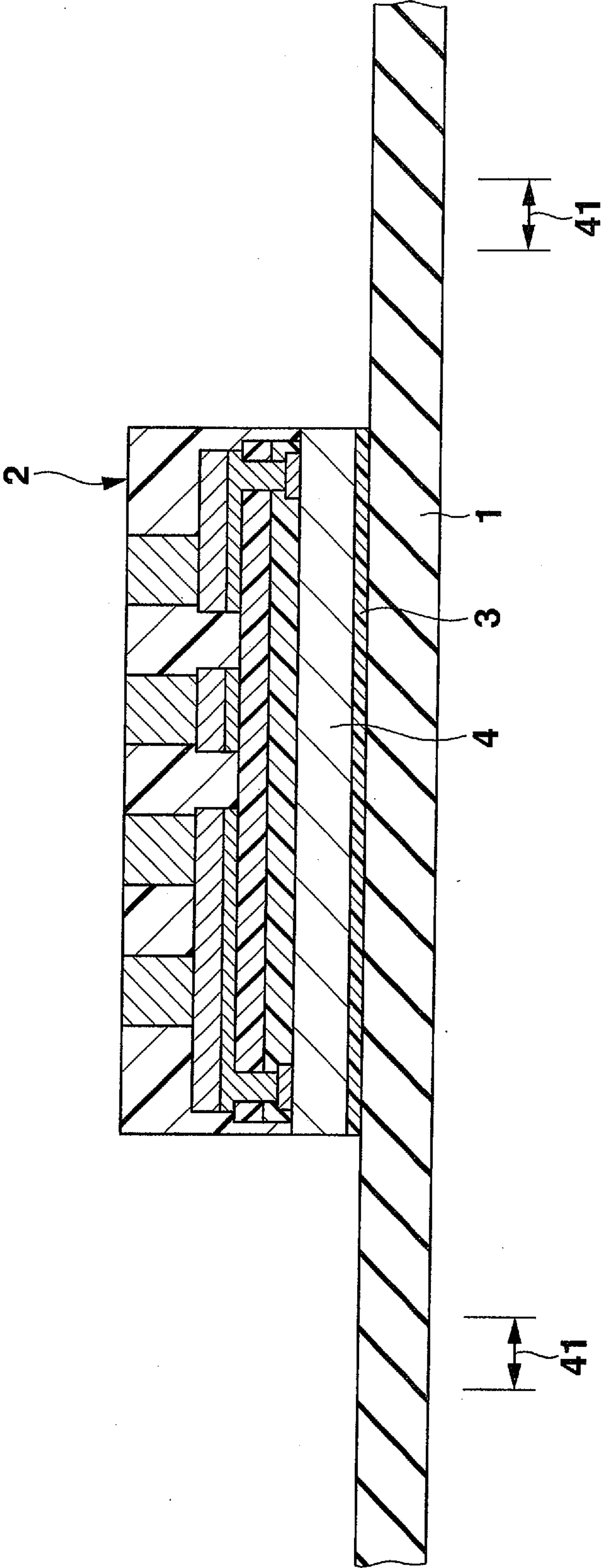


FIG.30



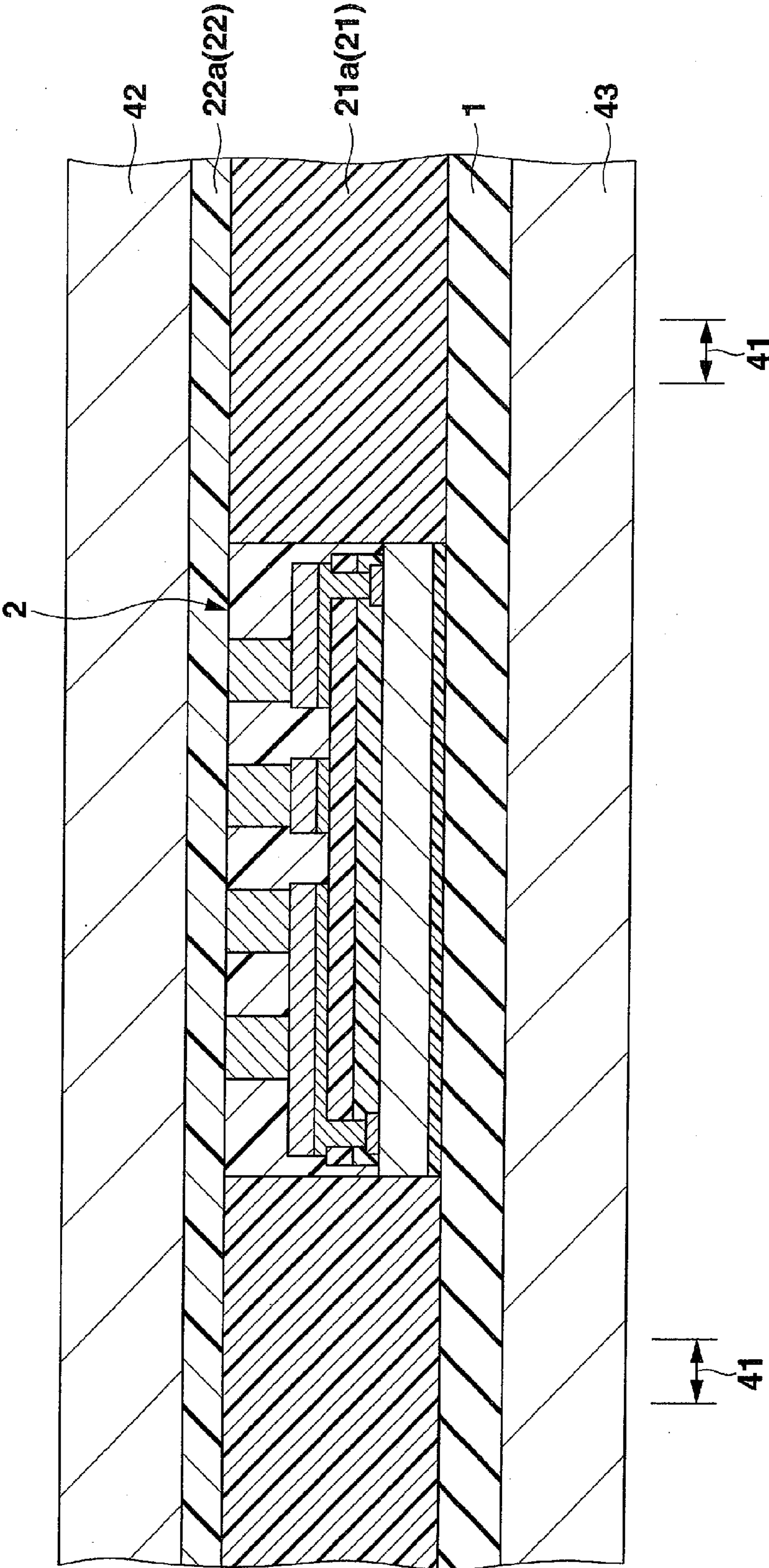


FIG.31
42
22a(22)
21a(21)
1
43
41
2
41

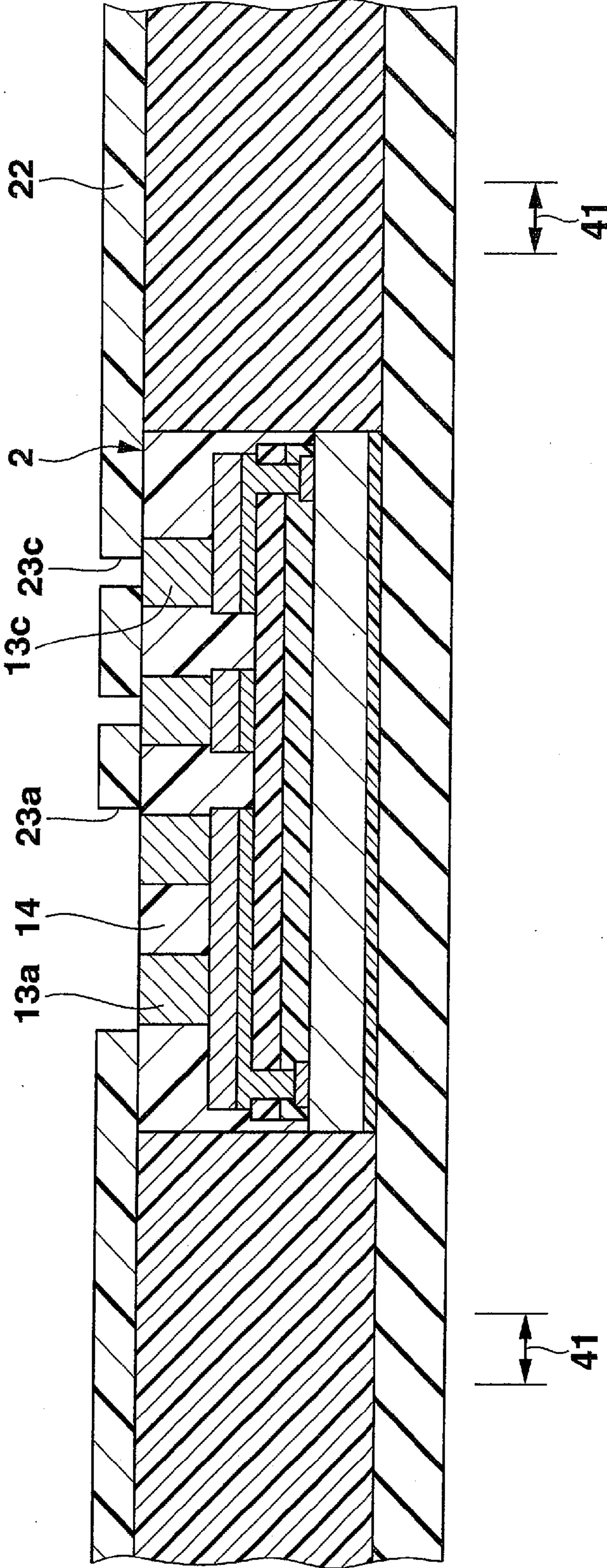



FIG.32

FIG.33

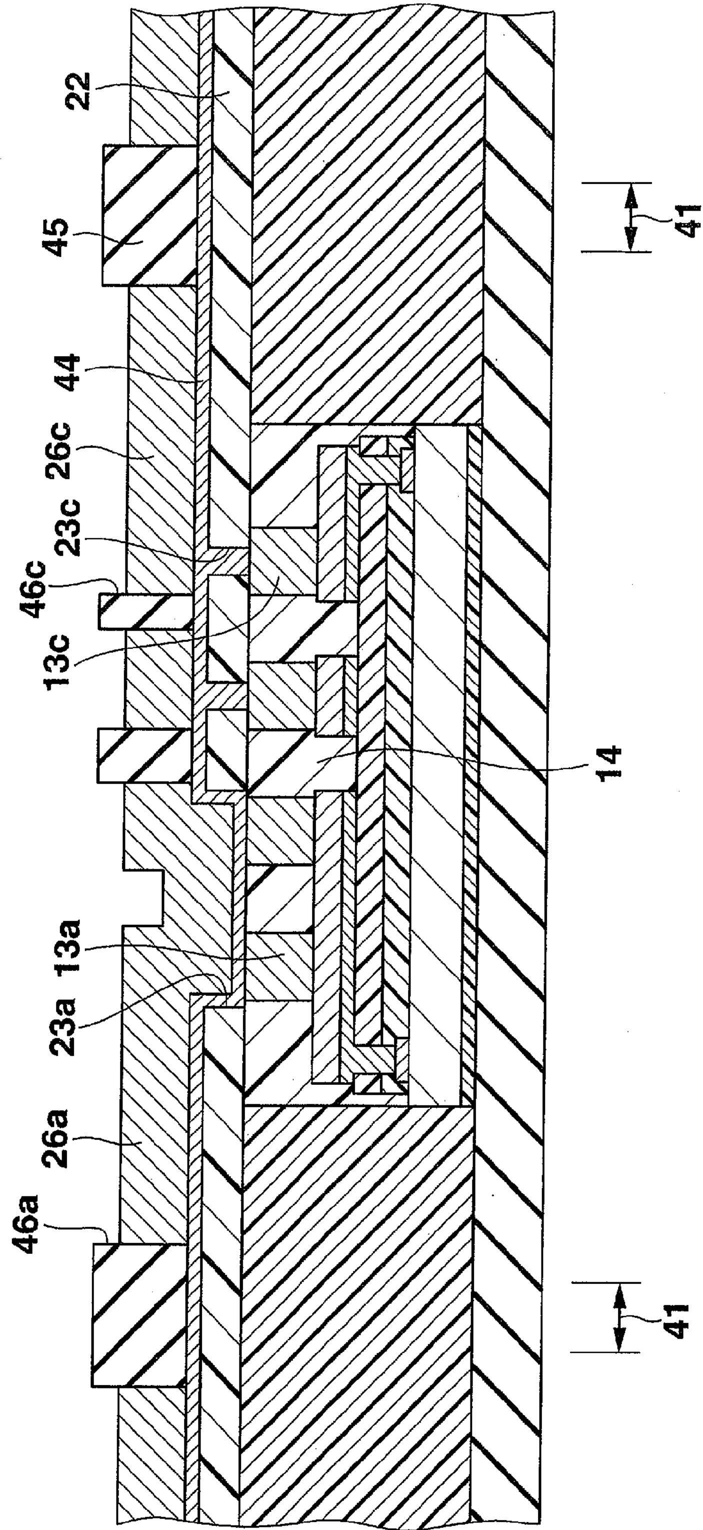


FIG.34

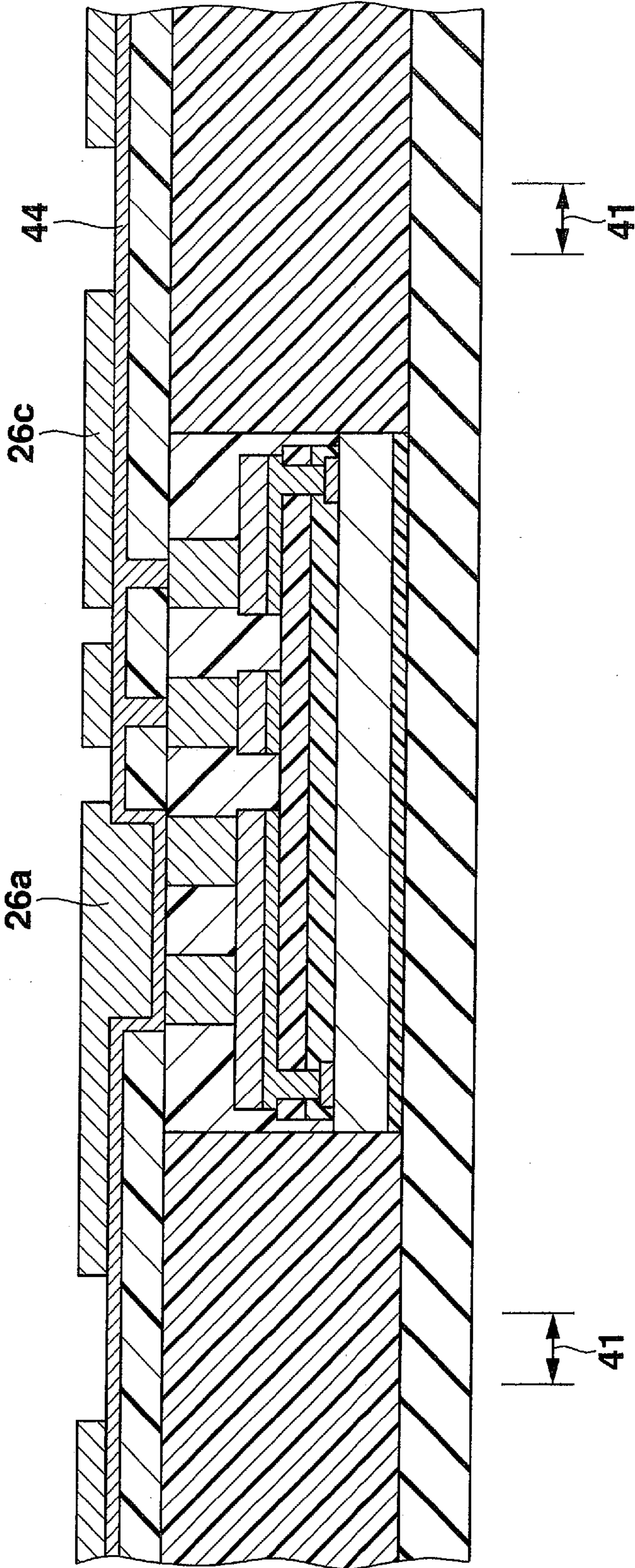
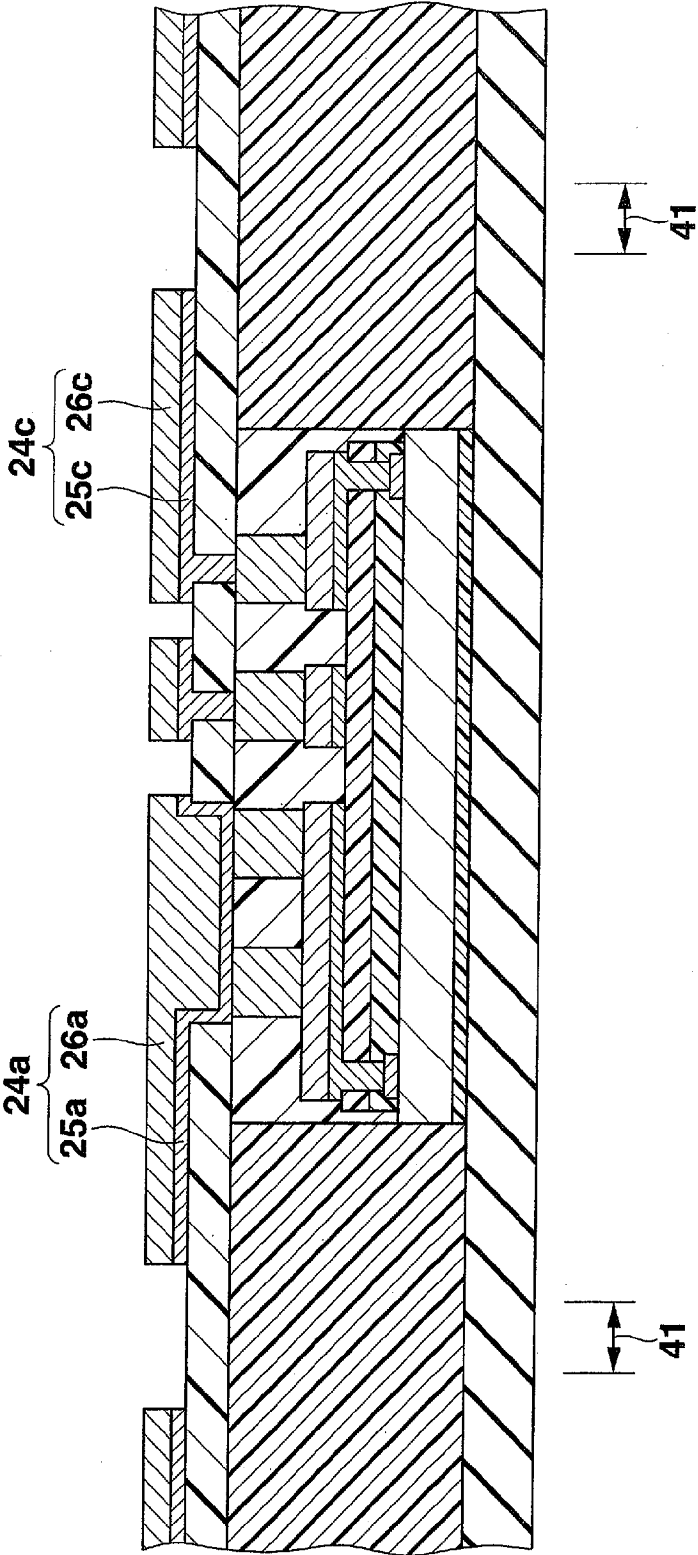


FIG.35



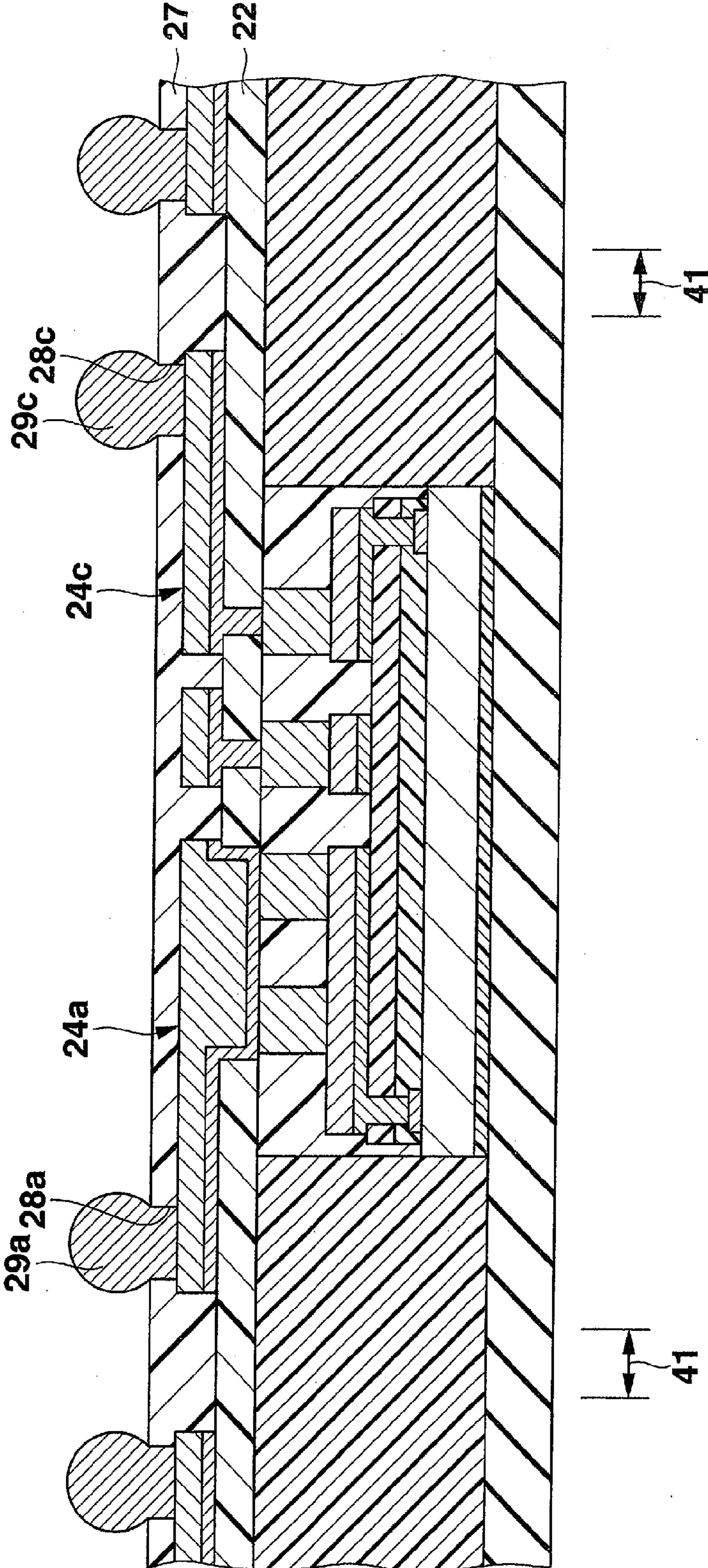


FIG.36
27
22
41
29c
28c
24c
24a
29a
28a
41

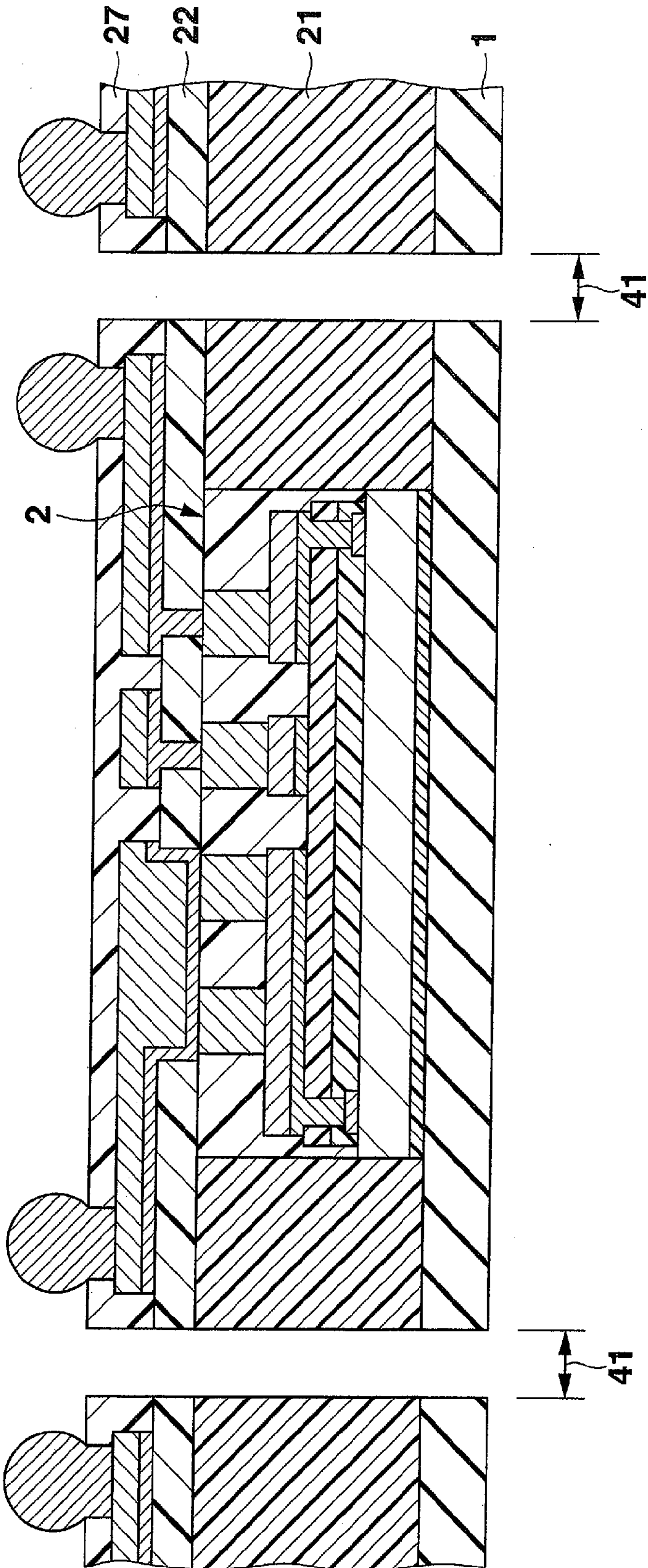
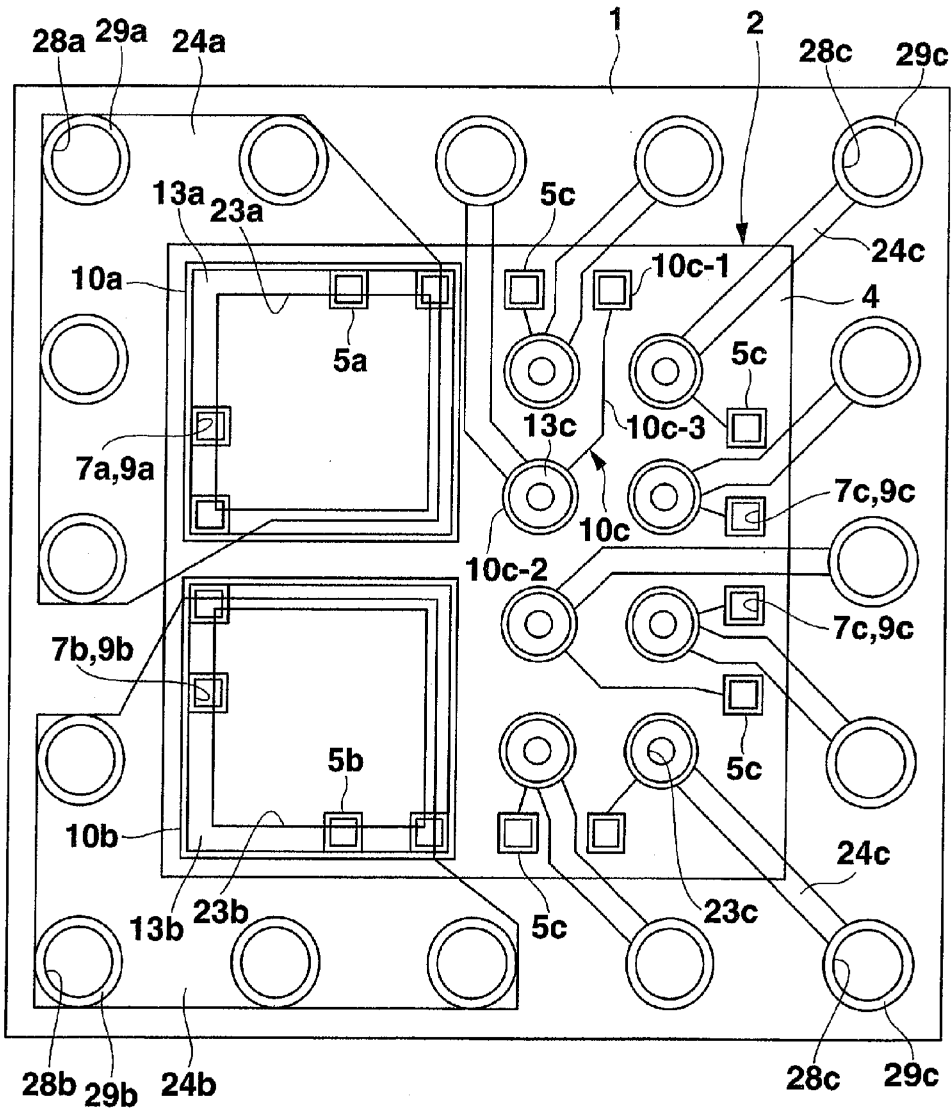
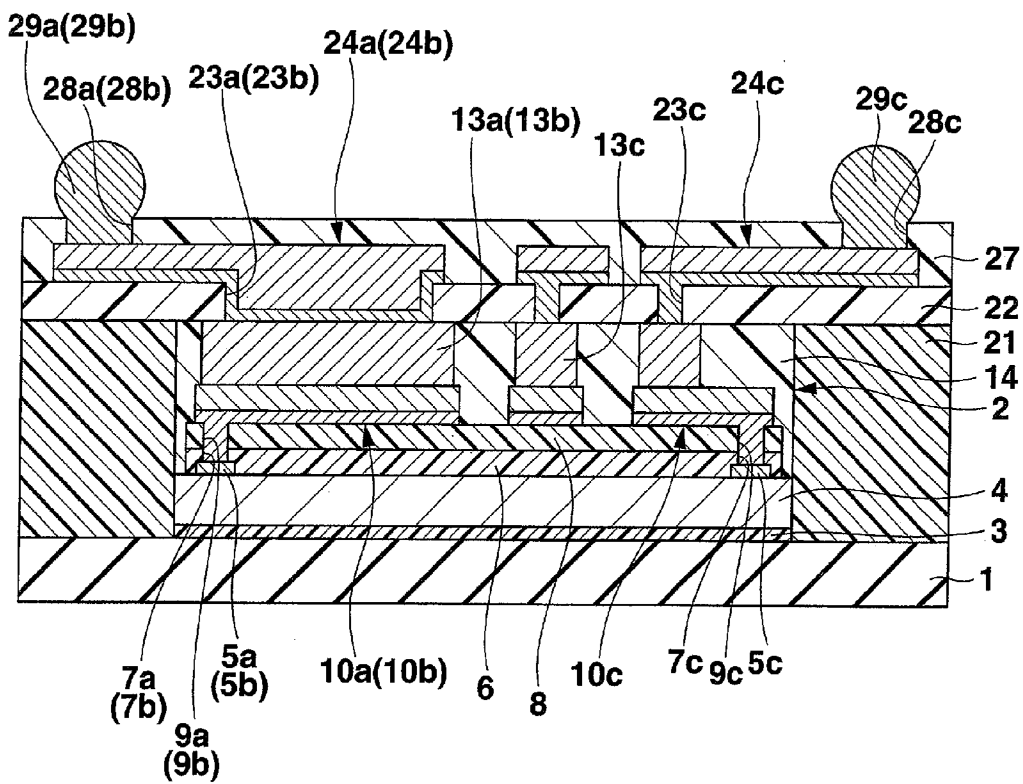



FIG.37

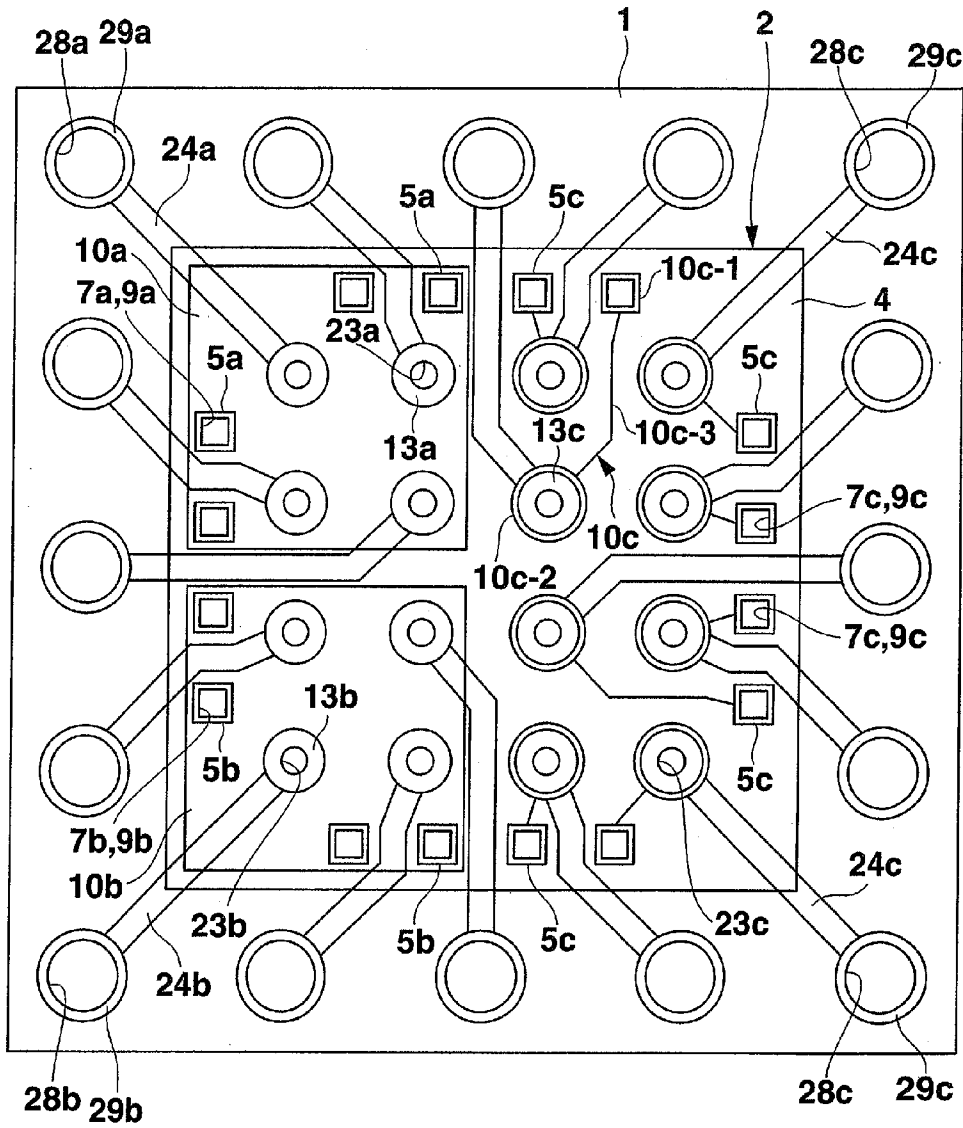
# FIG.38



# FIG.39



# FIG.40



# FIG.41

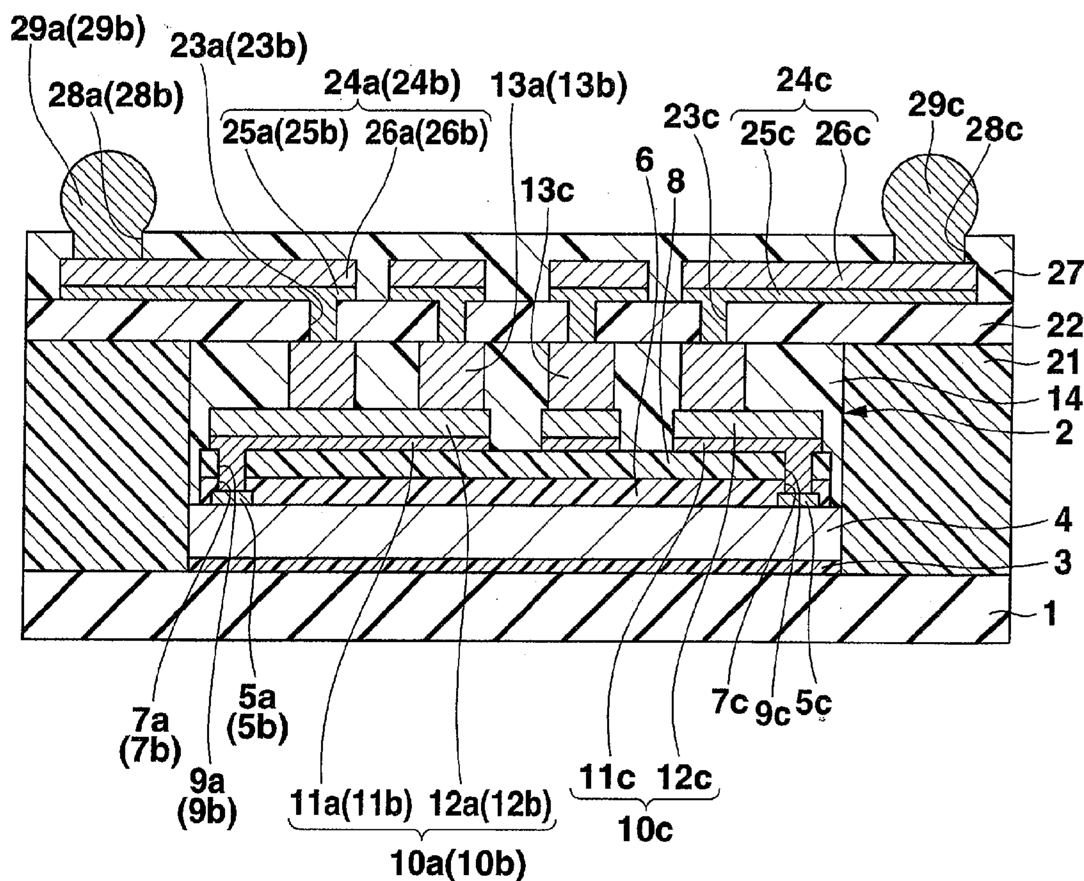


FIG.42

7c, 9c
5c
32
31
8
6
7a, 9a
5a
32

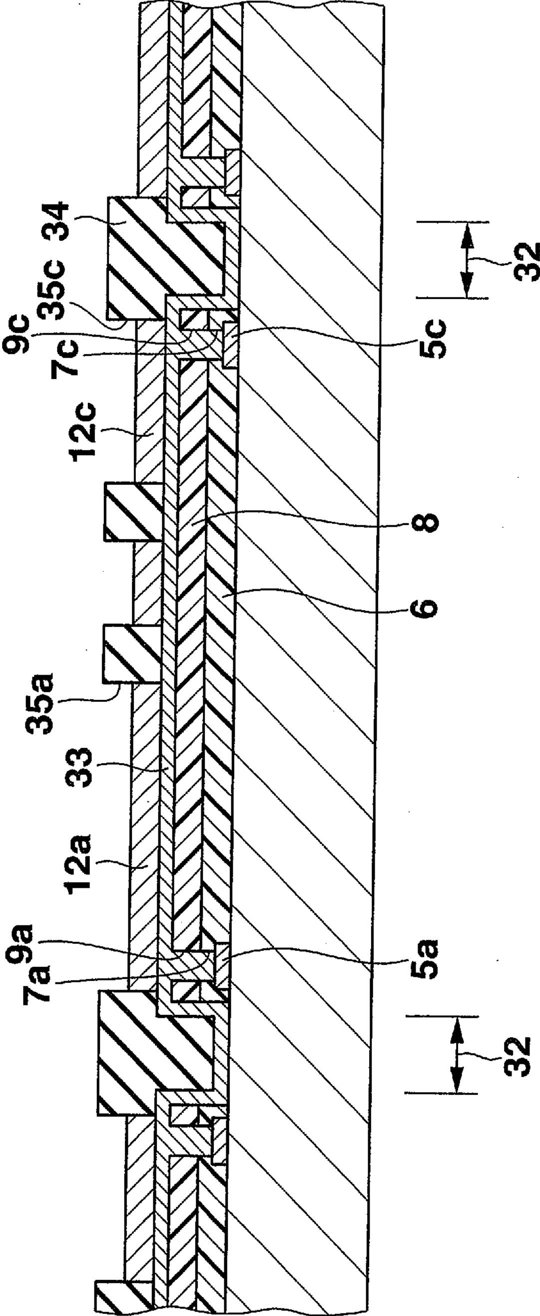


FIG.43
34
35c
9c
7c
5c
32
12c
8
6
35a
33
12a
9a
7a
5a
32

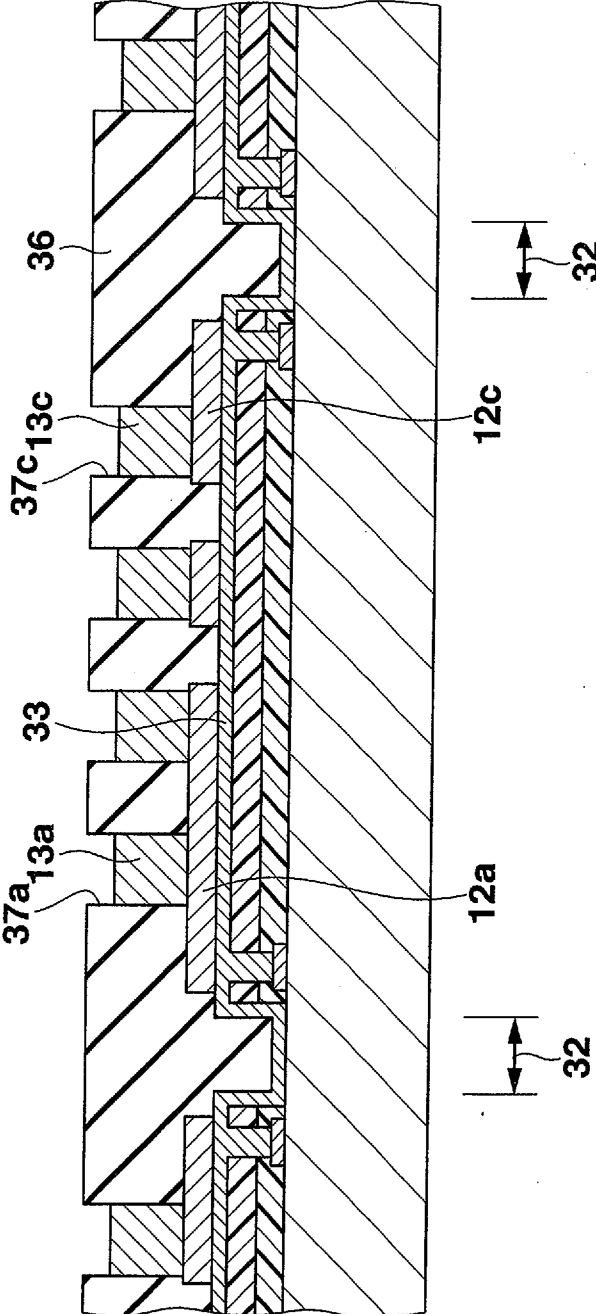


FIG.44
36
37c
13c
12c
33
37a
13a
12a
32
32

FIG.45

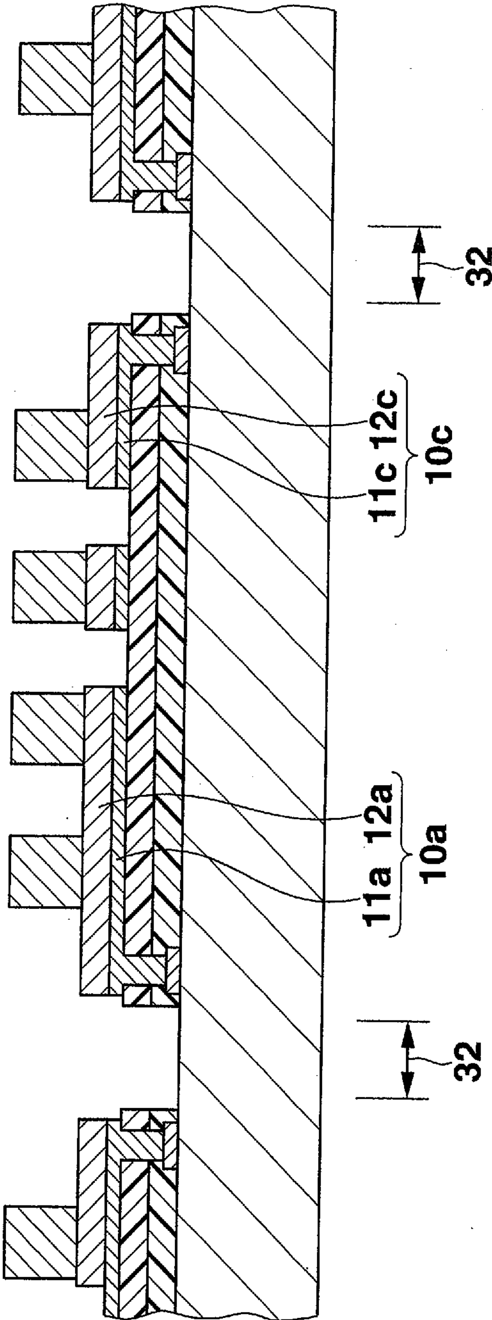


FIG.46

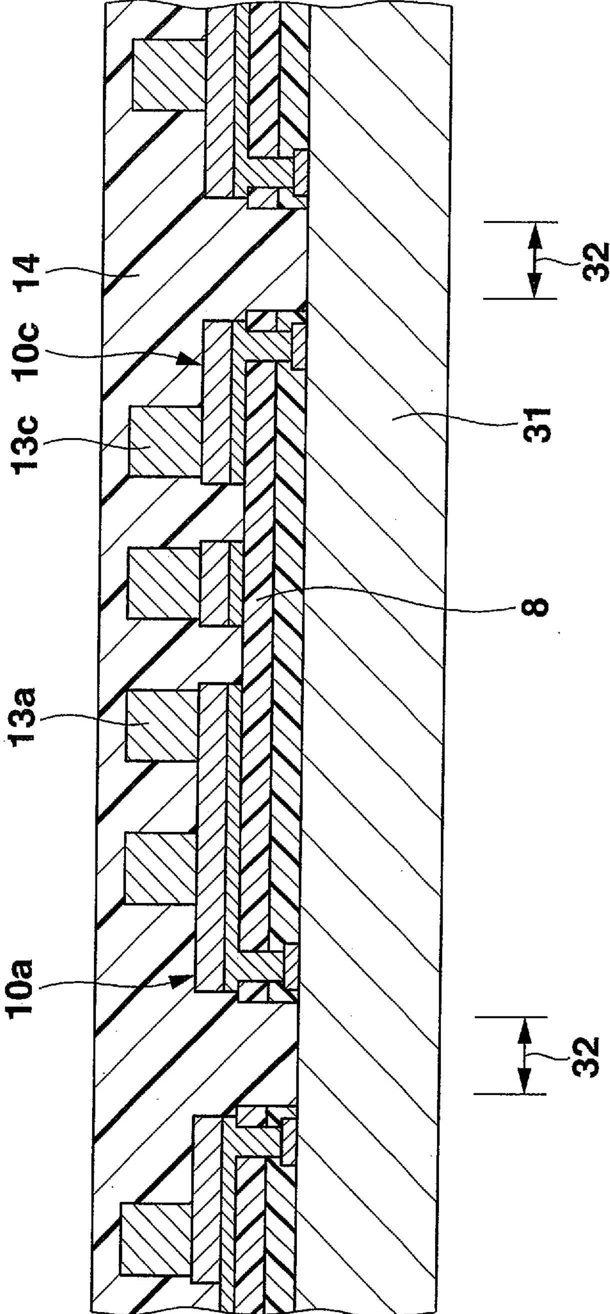


FIG.47

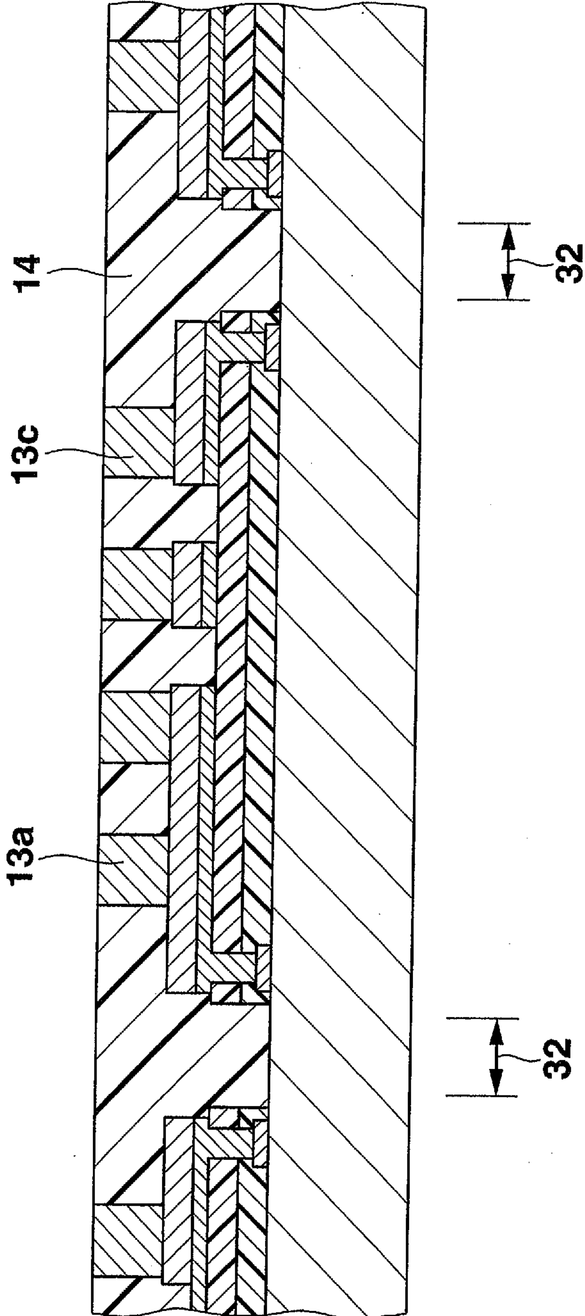


FIG.48

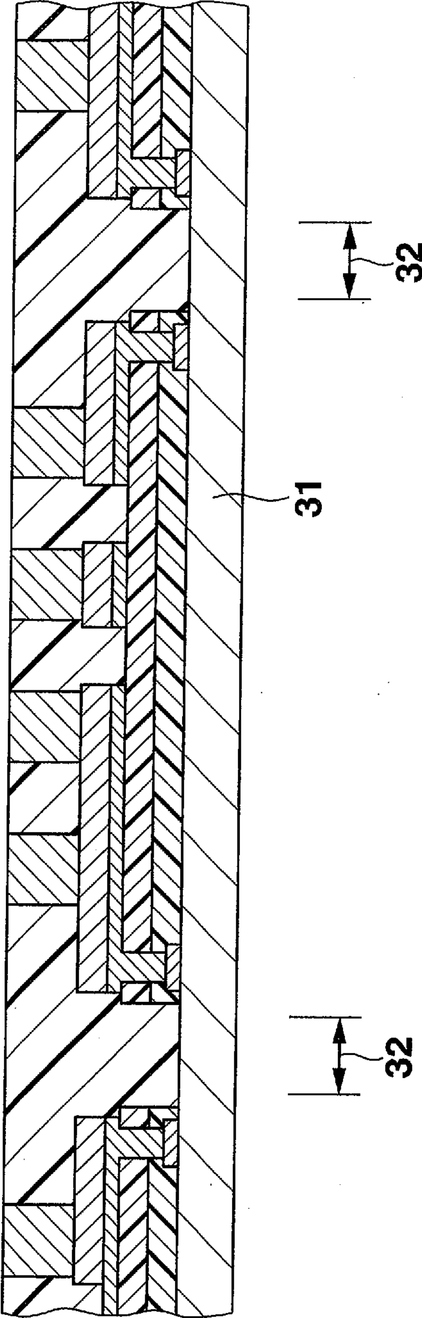
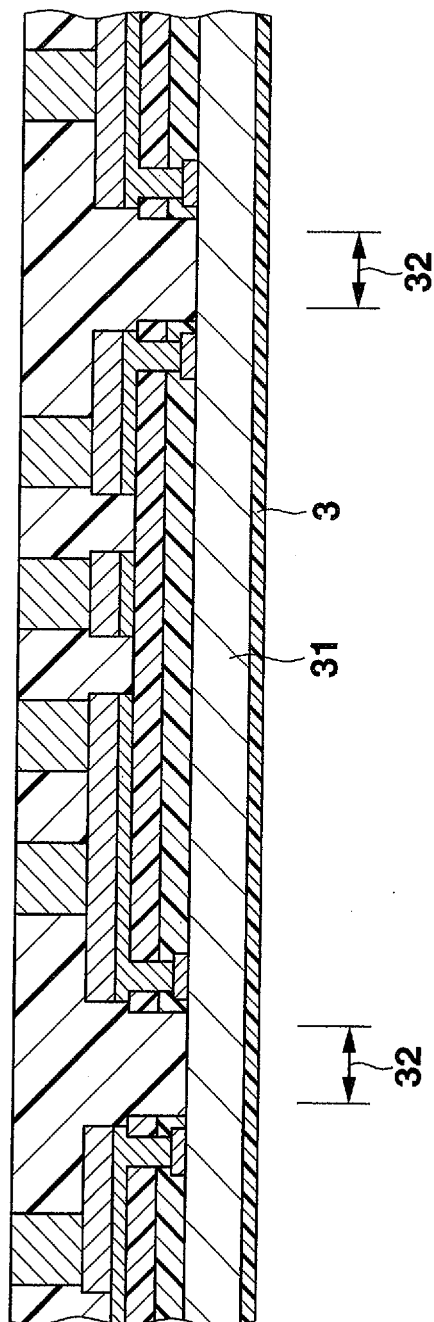


FIG.49



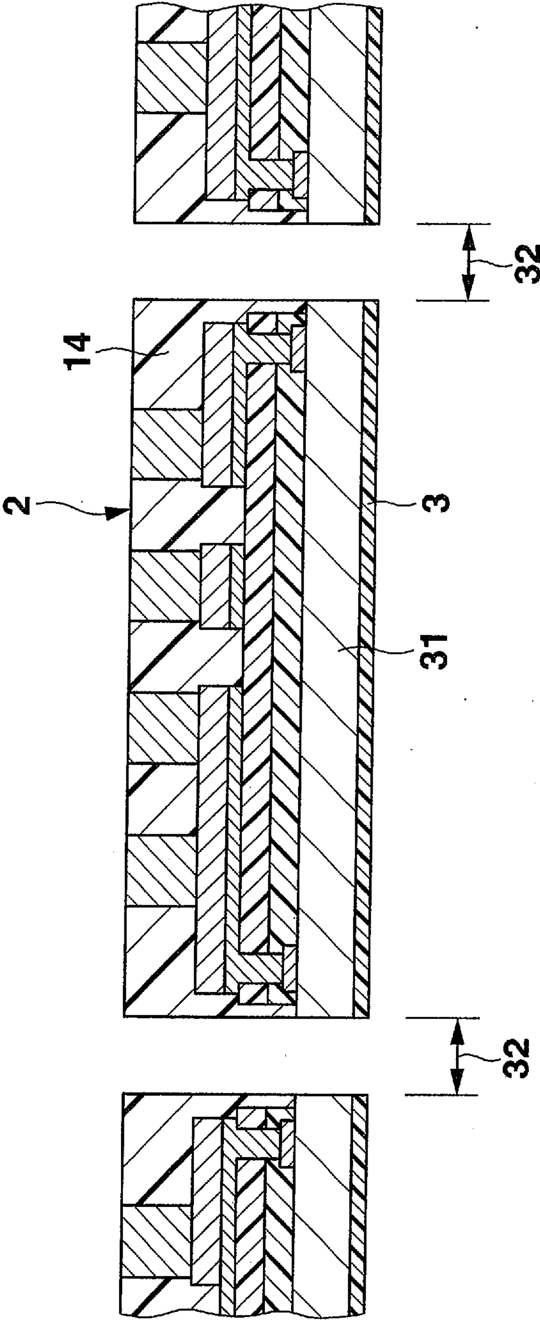



FIG.50

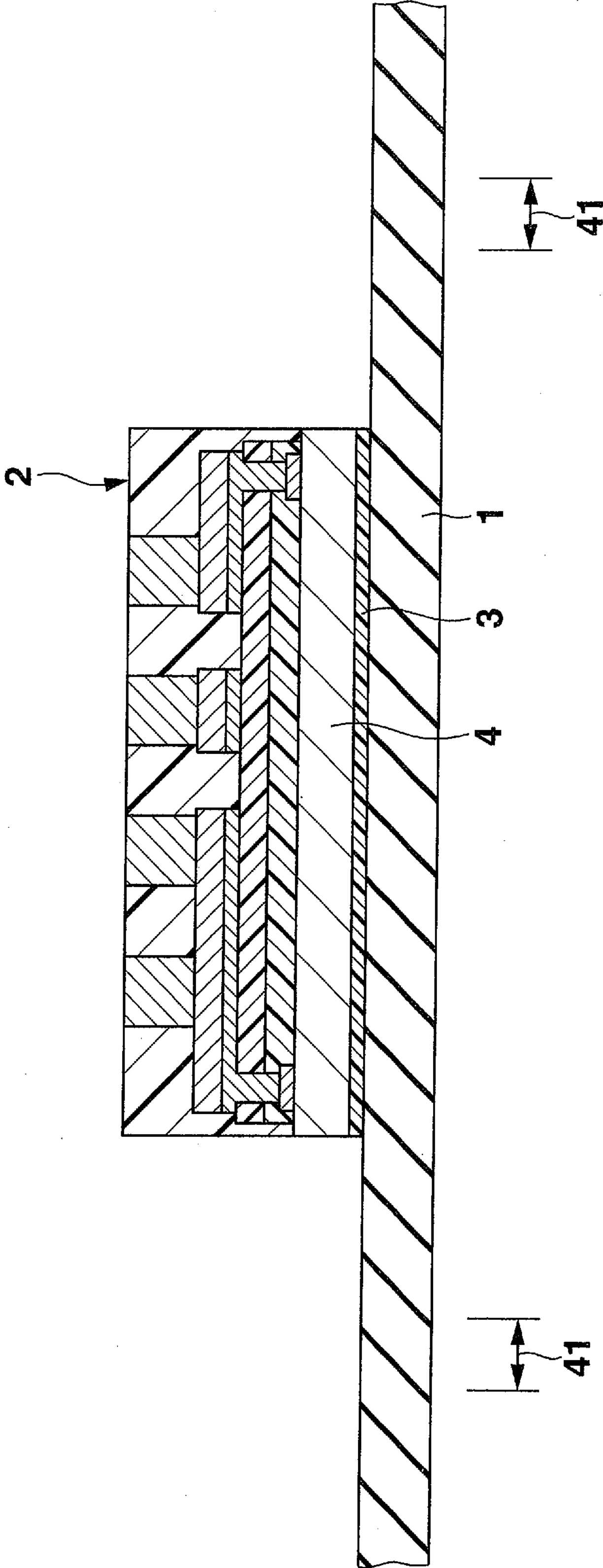


FIG.51
2
1
3
4
41
41

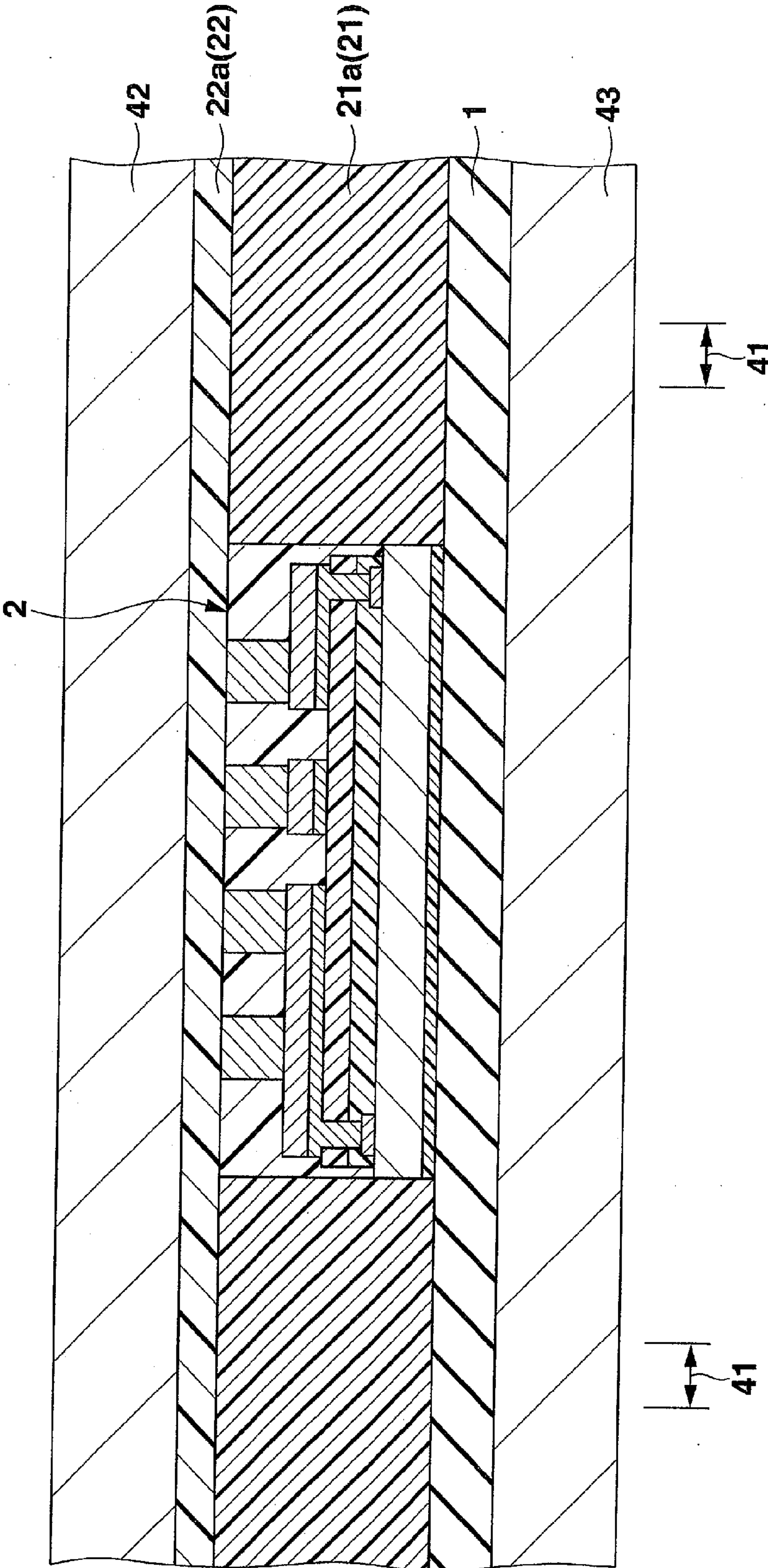
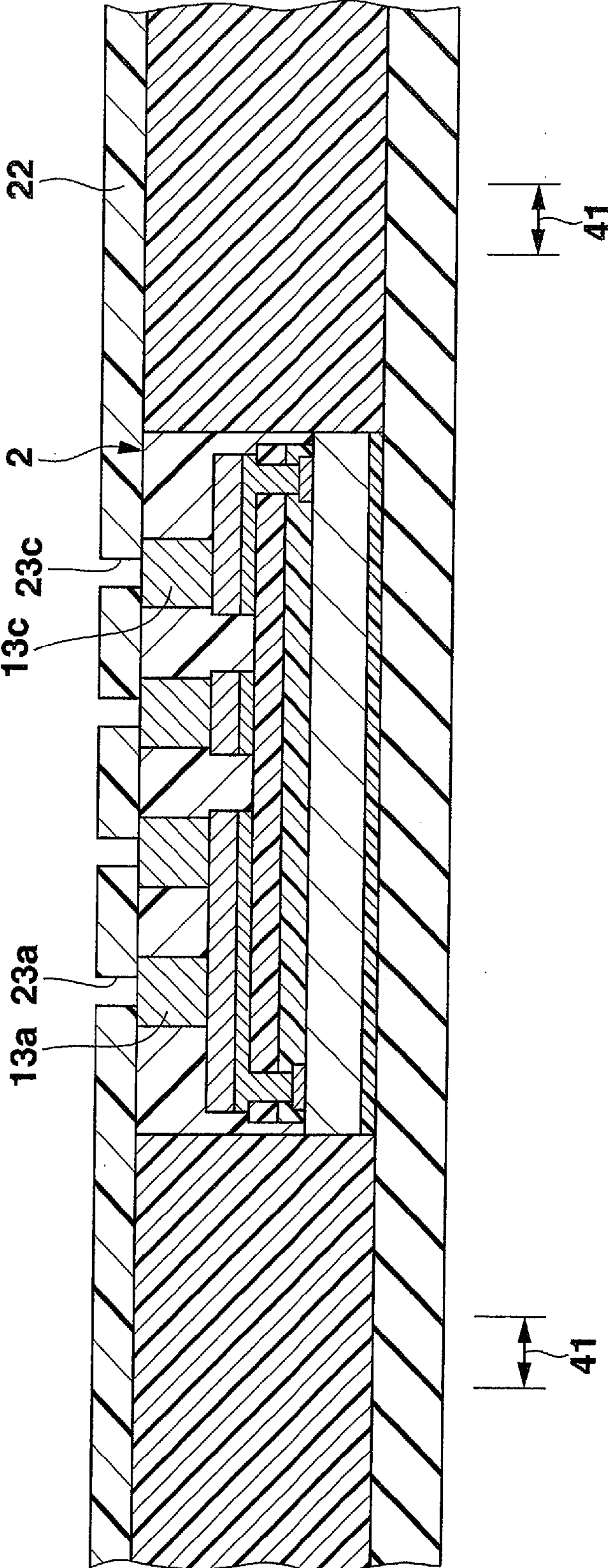



FIG.52

FIG.53



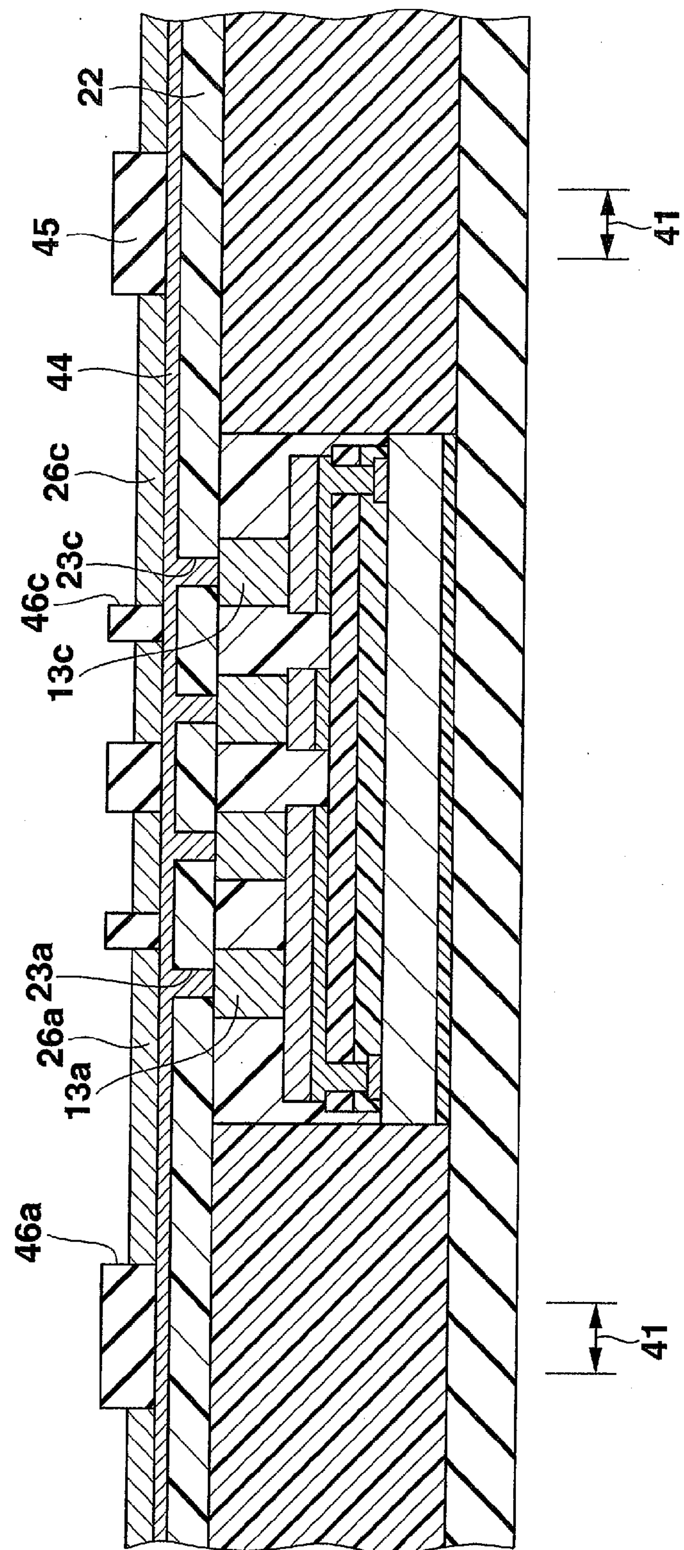



FIG.54

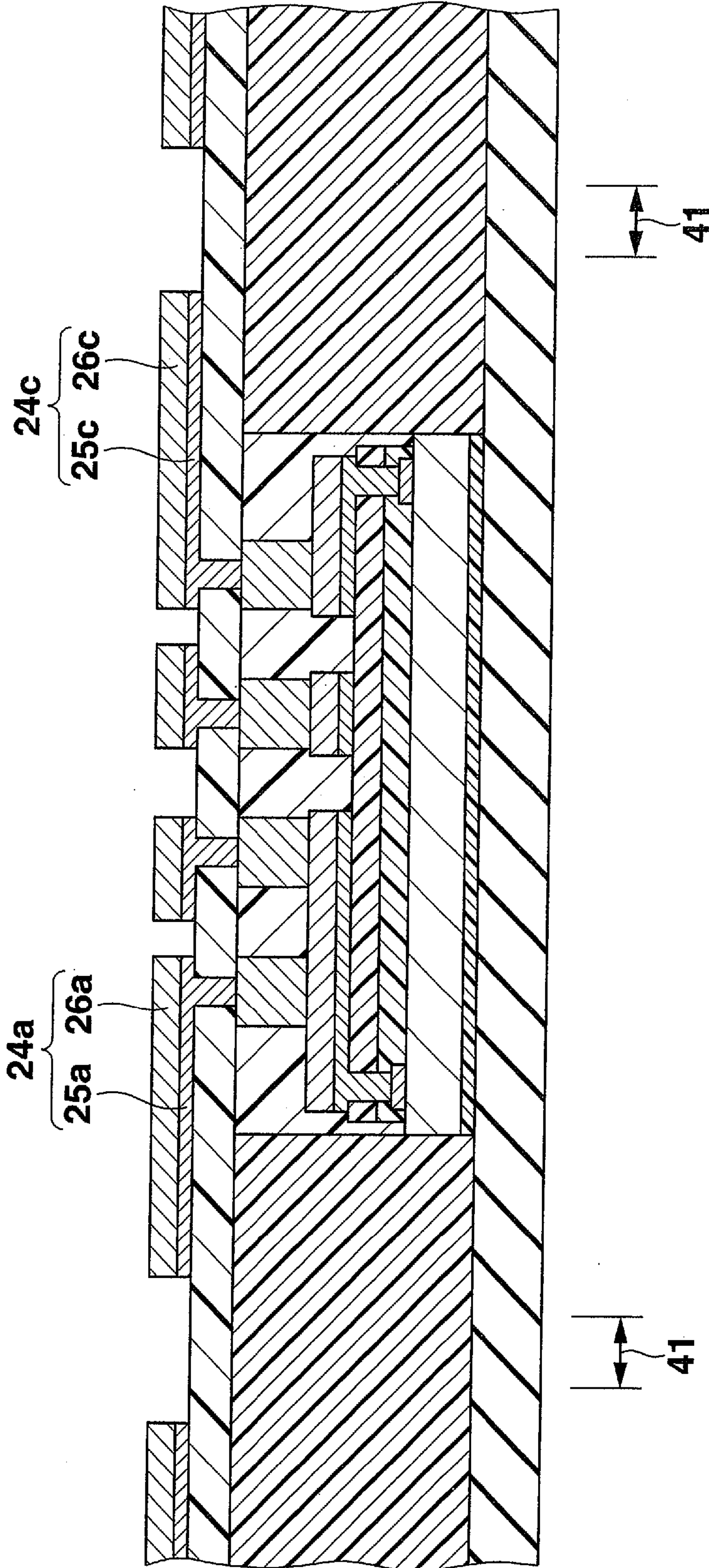



FIG.55

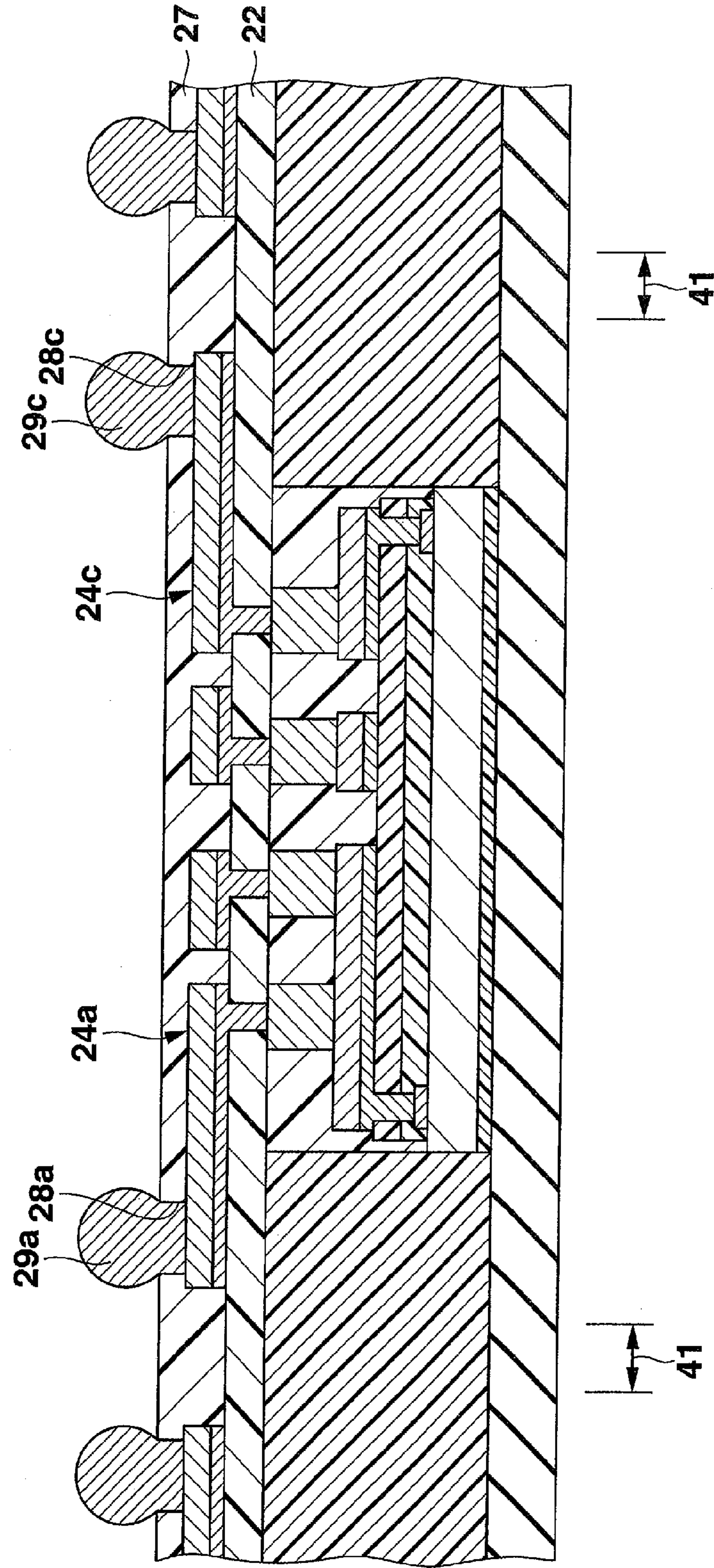



FIG.56

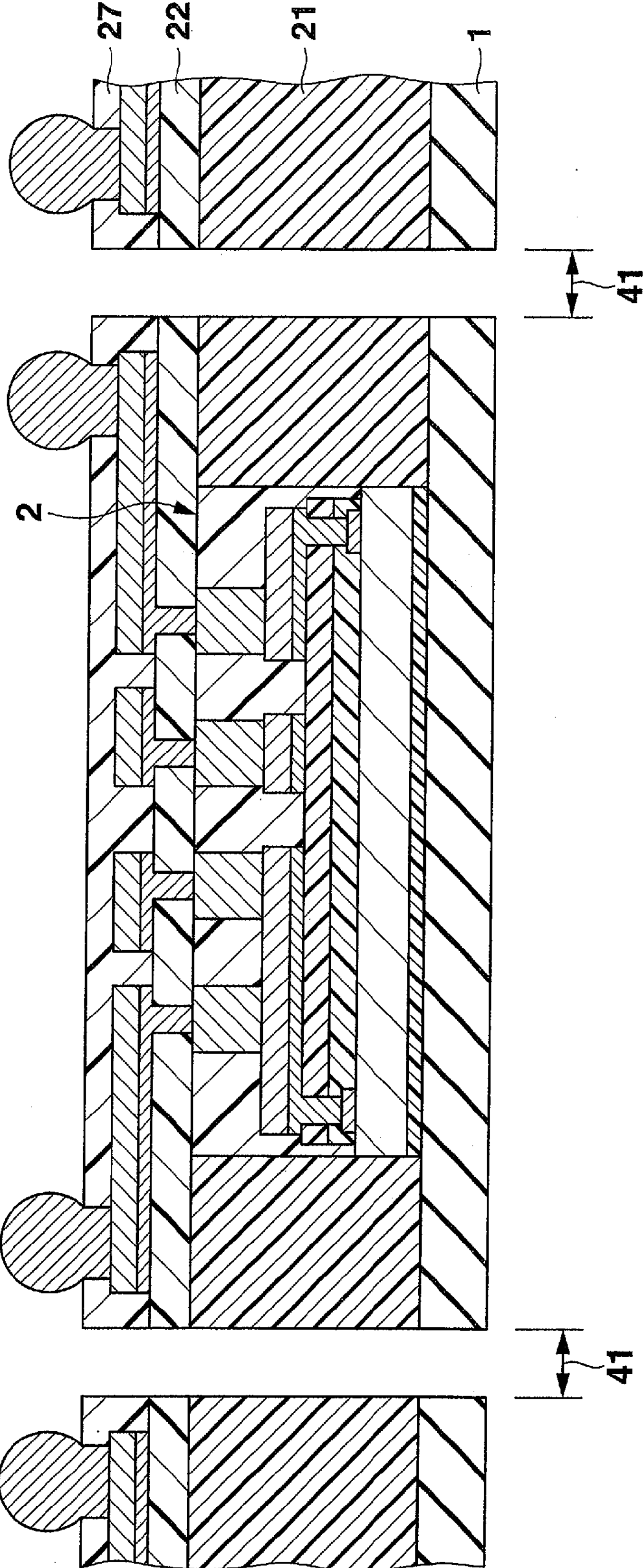
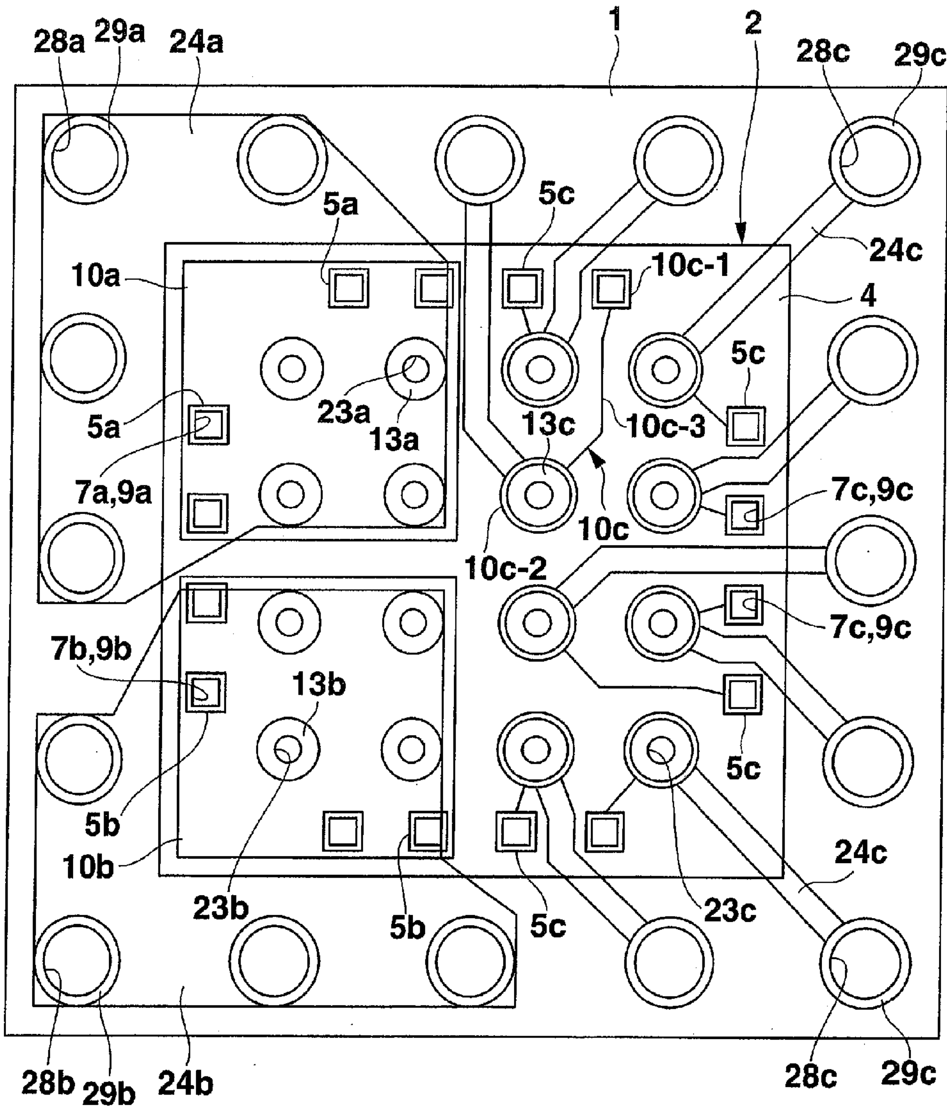
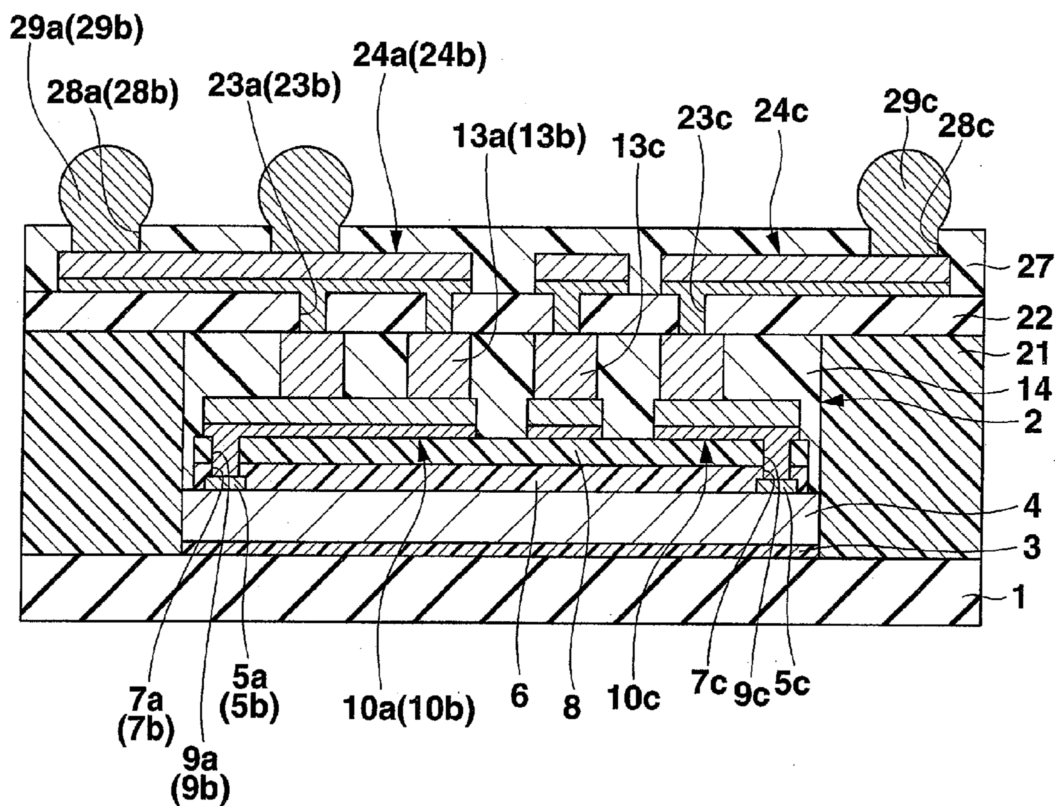


FIG.57
27
22
21
1
41
2
41

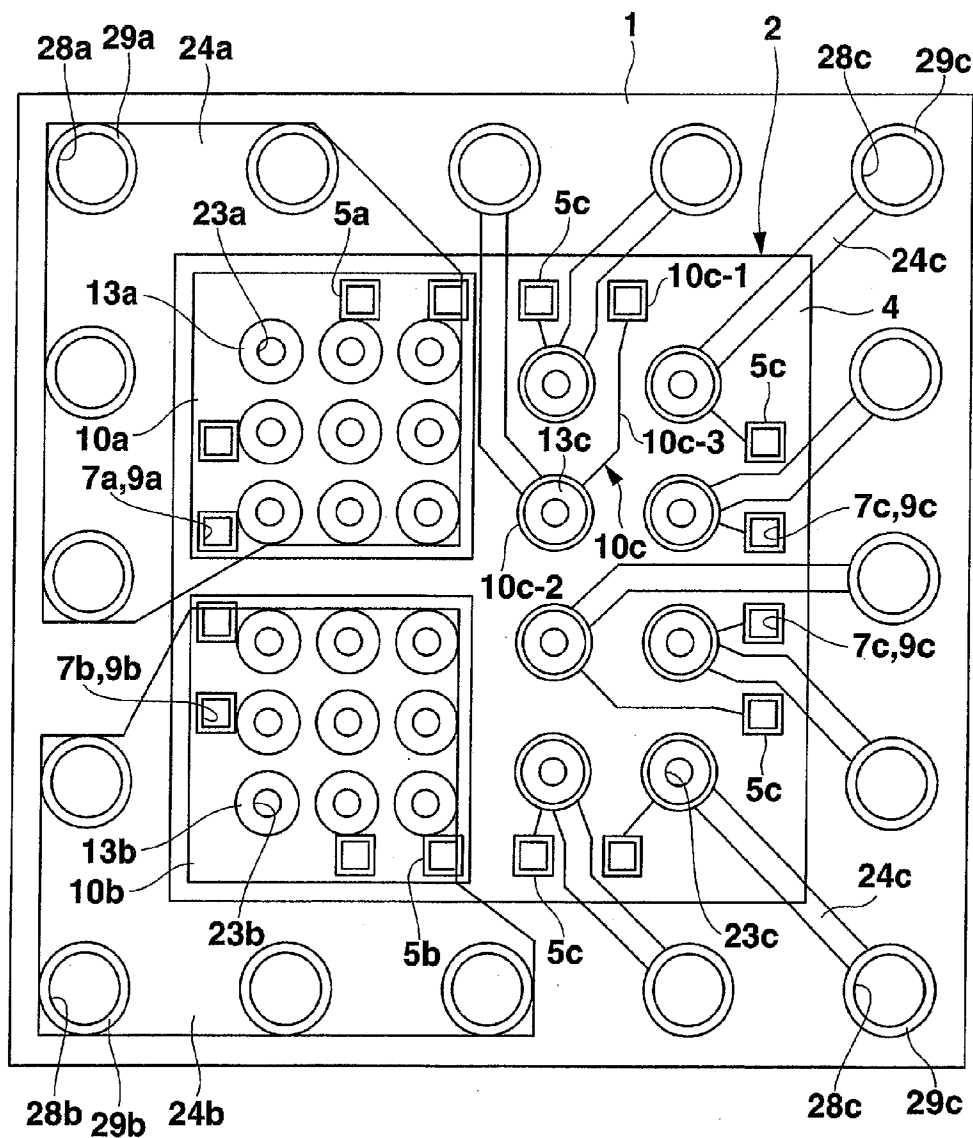
# FIG.58



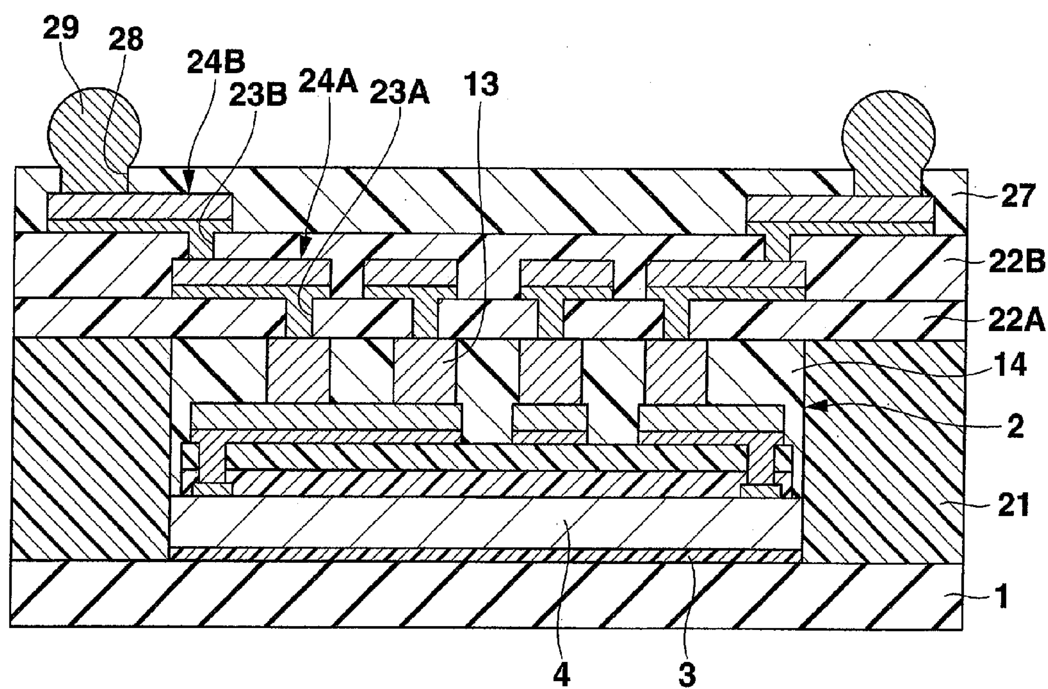
# FIG.59



# FIG.60



# FIG.61



# SEMICONDUCTOR CONSTRUCT AND MANUFACTURING METHOD THEREOF AS WELL AS SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This is a Continuation of U.S. application Ser. No. 12/828,492, filed Jul. 1, 2010, which is based upon and claims the benefit of priority from prior Japanese Patent Applications No. 2009-158618, filed Jul. 3, 2009; No. 2009-158622, filed Jul. 3, 2009; and No. 2009-158629, filed Jul. 3, 2009, the entire contents of all of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

**[0002]** 1. Field of the Invention

**[0003]** This invention relates to a semiconductor construct.

**[0004]** 2. Description of the Related Art

**[0005]** Conventional semiconductor devices include a semiconductor device having a semiconductor construct called a chip size package (CSP) that is fixedly attached to a base plate greater in size than the semiconductor construct (e.g., see Jpn. Pat. Appln. KOKAI Publication No. 2006-12885). In this case, the semiconductor construct called the CSP has a structure that includes a semiconductor substrate, wirings provided on the semiconductor substrate, columnar electrodes respectively provided on connection pads of the wirings, and a sealing film provided around the columnar electrodes.

**[0006]** Furthermore, the lower surface of the semiconductor substrate of the semiconductor construct is fixedly attached to the base plate. An insulating layer is provided on the base plate around the semiconductor construct. An upper insulating film is provided over the semiconductor construct and the insulating layer. Upper wirings are provided on the upper insulating film so as to be connected to the columnar electrodes of the semiconductor construct. The upper wirings, except for its connection pads, are covered with an overcoat film. Solder balls are provided on the connection pads of the upper wirings (e.g., see Jpn. Pat. Appln. KOKAI Publication No. 2006-12885).

**[0007]** In the meantime, the columnar electrodes are respectively provided on the connection pads of the wirings in the semiconductor construct of the above-mentioned conventional semiconductor device. Thus, the relation between the wirings and the columnar electrodes is one-to-one. This is a disadvantage when the line width of the wirings is reduced to about 20 μm or less due to an increase in the number of the wirings and columnar electrodes. In this case, when an excessively high current originating from, for example, a power supply voltage, runs through the wirings, the wirings are burned off and broken.

## BRIEF SUMMARY OF THE INVENTION

**[0008]** According to an aspect of embodiments, a semiconductor construct includes a semiconductor substrate, connection pads provided on the semiconductor substrate, a common wiring provided in a region including a predetermined number of connection pads among the connection pads so as to be connected to the predetermined number of connection pads, a wiring provided to be connected to the remaining of the connection pads, a first columnar electrode provided to be connected to the common wiring, and a second columnar electrode provided to be connected to a connection pad portion of the wiring.

**[0009]** According to another aspect of embodiments, a method of manufacturing a semiconductor construct includes forming a common wiring and a wiring on a semiconductor substrate provided with connection pads, the common wiring being formed in a region including common voltage connection pads among the connection pads so as to be connected to the common voltage connection pads, the wiring being formed so as to be connected to the remaining of the connection pads, and forming a first columnar electrode on the common wiring, and forming a second columnar electrode on a connection pad portion of the wiring.

**[0010]** Advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

**[0011]** The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention, and together with the general description given above and the detailed description of the embodiments given below, serve to explain the principles of the invention.

**[0012]** The present invention will be fully understood by the following detailed description and the accompanying drawings, which only serve to explain the invention and do not limit the scope of the invention. In the drawings:

**[0013]** FIG. **1** is a transmitted plan view of a semiconductor device according to a first embodiment of the invention;

**[0014]** FIG. **2** is a sectional view of a proper part of the semiconductor device shown in FIG. **1**;

**[0015]** FIG. **3** is a sectional view of an initially prepared assembly in one example of a method of manufacturing the semiconductor device shown in FIG. **1** and FIG. **2**;

**[0016]** FIG. **4** is a sectional view of a step following FIG. **3**;

**[0017]** FIG. **5** is a sectional view of a step following FIG. **4**;

**[0018]** FIG. **6** is a sectional view of a step following FIG. **5**;

**[0019]** FIG. **7** is a sectional view of a step following FIG. **6**;

**[0020]** FIG. **8** is a sectional view of a step following FIG. **7**;

**[0021]** FIG. **9** is a sectional view of a step following FIG. **8**;

**[0022]** FIG. **10** is a sectional view of a step following FIG. **9**;

**[0023]** FIG. **11** is a sectional view of a step following FIG. **10**;

**[0024]** FIG. **12** is a sectional view of a step following FIG. **11**;

**[0025]** FIG. **13** is a sectional view of a step following FIG. **12**;

**[0026]** FIG. **14** is a sectional view of a step following FIG. **13**;

**[0027]** FIG. **15** is a sectional view of a step following FIG. **14**;

**[0028]** FIG. **16** is a sectional view of a step following FIG. **15**;

**[0029]** FIG. **17** is a sectional view of a step following FIG. **16**;

**[0030]** FIG. **18** is a sectional view of a step following FIG. **17**;

**[0031]** FIG. **19** is a transmitted plan view of a semiconductor device according to a second embodiment of the invention;

**[0032]** FIG. **20** is a sectional view of a proper part of the semiconductor device shown in FIG. **19**;

**[0033]** FIG. **21** is a sectional view of an initially prepared assembly in one example of a method of manufacturing the semiconductor device shown in FIG. **19** and FIG. **20**;

**[0034]** FIG. **22** is a sectional view of a step following FIG. **21**;

**[0035]** FIG. **23** is a sectional view of a step following FIG. **22**;

**[0036]** FIG. **24** is a sectional view of a step following FIG. **23**;

**[0037]** FIG. **25** is a sectional view of a step following FIG. **24**;

**[0038]** FIG. **26** is a sectional view of a step following

**[0039]** FIG. **25**;

**[0040]** FIG. **27** is a sectional view of a step following FIG. **26**;

**[0041]** FIG. **28** is a sectional view of a step following FIG. **27**;

**[0042]** FIG. **29** is a sectional view of a step following FIG. **28**;

**[0043]** FIG. **30** is a sectional view of a step following FIG. **29**;

**[0044]** FIG. **31** is a sectional view of a step following FIG. **30**;

**[0045]** FIG. **32** is a sectional view of a step following FIG. **31**;

**[0046]** FIG. **33** is a sectional view of a step following FIG. **32**;

**[0047]** FIG. **34** is a sectional view of a step following FIG. **33**;

**[0048]** FIG. **35** is a sectional view of a step following FIG. **34**;

**[0049]** FIG. **36** is a sectional view of a step following FIG. **35**;

**[0050]** FIG. **37** is a sectional view of a step following FIG. **36**;

**[0051]** FIG. **38** is a transmitted plan view of a semiconductor device according to a third embodiment of the invention;

**[0052]** FIG. **39** is a sectional view of a proper part of the semiconductor device shown in FIG. **38**;

**[0053]** FIG. **40** is a transmitted plan view of a semiconductor device according to a fourth embodiment of the invention;

**[0054]** FIG. **41** is a sectional view of a proper part of the semiconductor device shown in FIG. **40**;

**[0055]** FIG. **42** is a sectional view of an initially prepared assembly in one example of a method of manufacturing the semiconductor device shown in FIG. **40** and FIG. **41**;

**[0056]** FIG. **43** is a sectional view of a step following FIG. **42**;

**[0057]** FIG. **44** is a sectional view of a step following FIG. **43**;

**[0058]** FIG. **45** is a sectional view of a step following FIG. **44**;

**[0059]** FIG. **46** is a sectional view of a step following FIG. **45**;

**[0060]** FIG. **47** is a sectional view of a step following FIG. **46**;

**[0061]** FIG. **48** is a sectional view of a step following FIG. **47**;

**[0062]** FIG. **49** is a sectional view of a step following FIG. **48**;

**[0063]** FIG. **50** is a sectional view of a step following FIG. **49**;

**[0064]** FIG. **51** is a sectional view of a step following FIG. **50**;

**[0065]** FIG. **52** is a sectional view of a step following FIG. **51**;

**[0066]** FIG. **53** is a sectional view of a step following FIG. **52**;

**[0067]** FIG. **54** is a sectional view of a step following FIG. **53**;

**[0068]** FIG. **55** is a sectional view of a step following FIG. **54**;

**[0069]** FIG. **56** is a sectional view of a step following FIG. **55**;

**[0070]** FIG. **57** is a sectional view of a step following FIG. **56**;

**[0071]** FIG. **58** is a transmitted plan view of a semiconductor device according to a fifth embodiment of the invention;

**[0072]** FIG. **59** is a sectional view of a proper part of the semiconductor device shown in FIG. **58**;

**[0073]** FIG. **60** is a transmitted plan view of a semiconductor device according to a sixth embodiment of the invention; and

**[0074]** FIG. **61** is a sectional view of a semiconductor device according to a seventh embodiment of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

### First Embodiment

**[0075]** FIG. **1** shows a transmitted plan view of a semiconductor device according to a first embodiment of the invention. FIG. **2** shows a sectional view of a proper part of the semiconductor device shown in FIG. **1**. This semiconductor device includes a base plate **1**. The base plate **1** has a square planar shape, and made of, for example, an epoxy resin containing glass fabric as a base material. The lower surface of a semiconductor construct **2** is bonded to the center of the upper surface of the base plate **1** through a bonding layer **3** made of a die bond material. The semiconductor construct **2** has a square planar shape, and is slightly smaller in size than the base plate **1**.

**[0076]** The semiconductor construct **2**, which is generally called a CSP, includes a silicon substrate (semiconductor substrate) **4**. The lower surface of the silicon substrate **4** is bonded to the center of the upper surface of the base plate **1** through the bonding layer **3**. Elements (not shown) such as a transistor, diode, resistor, and condenser that constitute an integrated circuit having a predetermined function are formed on the upper surface of the silicon substrate **4**. Connection pads **5***a*, **5***b*, **5***c* are provided on the peripheral portion of the upper surface of the silicon substrate **4**. The connection pads **5***a*, **5***b*, **5***c* are made of, for example, an aluminum-based metal, and connected to the elements of the integrated circuit.

**[0077]** Here, by way of example, the four connection pads indicated by the sign **5***a* and arranged on the upper left part of the silicon substrate **4** in FIG. **1** are for a common power supply voltage. The four connection pads indicated by the sign **5***b* and arranged on the lower left part of the silicon substrate **4** are for a common ground voltage. The four connection pads indicated by the sign **5***c* and arranged on the upper right part of the silicon substrate **4** and the four connection pads indicated by the sign **5***c* and arranged on the

lower right part of the silicon substrate **4** are for a normal voltage. Here, in FIG. **2**, the ground voltage connection pads **5***b* and associated parts are substantially similar to the power supply voltage connection pads **5***a* and associated parts, and are therefore indicated by signs in parentheses.

**[0078]** A passivation film (insulating film) **6** made of, for example, silicon oxide is provided on the upper surface of the silicon substrate **4** except for the peripheral portion of the silicon substrate **4** and the centers of the connection pads **5***a*, **5***b*, **5***c*. The centers of the connection pads **5***a*, **5***b*, **5***c* are exposed through openings **7***a*, **7***b*, **7***c* provided in the passivation film **6**. A protective film (insulating film) **8** made of, for example, a polyimide resin is provided on the upper surface of the passivation film **6**. Openings **9***a*, **9***b*, **9***c* are provided in parts of the protective film **8** that correspond to the openings **7***a*, **7***b*, **7***c* of the passivation film **6**.

**[0079]** Wirings **10***a*, **10***b*, **10***c* are provided on the upper surface of the protective film **8**. The wirings **10***a*, **10***b*, **10***c* have a double-layer structure composed of foundation metal layers **11***a*, **11***b*, **11***c* and upper metal layers **12***a*, **12***b*, **12***c*. The foundation metal layers **11***a*, **11***b*, **11***c* are made of, for example, copper and provided on the upper surface of the protective film **8**. The upper metal layers **12***a*, **12***b*, **12***c* are made of copper and provided on the upper surfaces of the foundation metal layers **11**.

**[0080]** In this case, as shown in FIG. **1**, the wiring indicated by the sign **10***a* (common wiring) is solidly disposed on the upper left part of the silicon substrate **4** in a region that has a square planar shape and includes the four power supply voltage connection pads **5***a*. The wiring **10***a* is connected to all of the four power supply voltage connection pads **5***a* via the openings **7***a*, **9***a* of the passivation film **6** and the protective film **8**.

**[0081]** The wiring indicated by the sign **10***b* (common wiring) is solidly disposed on the lower left part of the silicon substrate **4** in a region that has a square planar shape and includes the four ground voltage connection pads **5***b*. The wiring **10***b* is connected to all of the four ground voltage connection pads **5***b* via the openings **7***b*, **9***b* of the passivation film **6** and the protective film **8**.

**[0082]** The wirings indicated by the sign **10***c* are disposed in the right region of the silicon substrate **4**. Each wiring **10***c* has a connection portion **10***c*-**1** connected to the normal voltage connection pad **5***c* via the openings **7***c*, **9***c* of the passivation film **6** and the protective film **8**, a connection pad portion **10***c*-**2** having a circular planar shape, and an extension line **10***c*-**3** extending between the connection portion **10***c*-**1** and the connection pad portion **10***c*-**2**.

**[0083]** Similarly to the wiring **10***a*, a columnar electrode (common columnar electrode, first columnar electrode) **13***a* is solidly provided in the region of the upper surface, except for its peripheral portion, of the wiring indicated by the sign **10***a* and having a square planar shape. The columnar electrode **13***a* is made of copper and has a square planar shape. Similarly to the wiring **10***b*, a columnar electrode (common columnar electrode, first columnar electrode) **13***b* is solidly provided in the region of the upper surface, except for the peripheral portion, of the wiring indicated by the sign **10***b* and having a square planar shape. The columnar electrode **13***b* is made of copper and has a square planar shape. Columnar electrodes (second columnar electrodes) **13***c* are provided on the upper surface of the connection pad portions **10***c*-**2** of the wirings indicated by the sign **10***c*. The columnar electrodes **13***c* are made of copper and have a circular planar shape. Here, as shown in FIG. **1**, eight columnar electrodes **13***c* having a circular planar shape are arranged in matrix form.

**[0084]** A sealing film **14** made of, for example, an epoxy resin is provided around the columnar electrodes **13***a*, **13***b*, **13***c* on the upper surface of the protective film **8** including the wirings **10***a*, **10***b*, **10***c*. The columnar electrodes **13***a*, **13***b*, **13***c* are provided so that the upper surfaces thereof are flush with or several μm lower than the upper surface of the sealing film **14**. The explanation of the structure of the semiconductor construct **2** is completed now.

**[0085]** An insulating layer **21** in a square frame shape is provided on the upper surface of the base plate **1** around the semiconductor construct **2**. For example, the insulating layer **21** is made of a thermosetting resin such as an epoxy resin in which a reinforcer of an inorganic material such as silica fuller is dispersed. Alternatively, the insulating layer **21** is only made of a thermosetting resin such as an epoxy resin.

**[0086]** An upper insulating film **22** is provided on the upper surfaces of the semiconductor construct **2** and the insulating layer **21**. The upper insulating film **22** is made of, for example, a base glass fabric impregnated with a thermosetting resin such as an epoxy resin. Alternatively, the upper insulating film **22** is only made of a thermosetting resin such as an epoxy resin. Openings (first openings) **23***a*, **23***b* having a circular planar shape are provided in parts of the upper insulating film **22** that correspond to predetermined nine points on the surface of the columnar electrodes **13***a*, **13***b* of the semiconductor construct **2** having a square planar shape. Openings (second openings) **23***c* having a circular planar shape are provided in parts of the upper insulating film **22** that correspond to the centers of the upper surfaces of the columnar electrodes **13***c* of the semiconductor construct **2** having a circular planar shape.

**[0087]** In this case, the planar shape of the openings **23***a*, **23***b* is the same as the planar shape of the opening **23***c*. Moreover, both the number of the openings **23***a* and the number of the openings **23***b* are nine, and are greater than the number (four) of the power supply voltage and ground voltage connection pads **5***a*, **5***b* of the semiconductor construct **2**.

**[0088]** Upper wirings **24***a*, **24***b*, **24***c* are provided on the upper surface of the upper insulating film **22**. The upper wirings **24***a*, **24***b*, **24***c* have a double-layer structure composed of foundation metal layers **25***a*, **25***b*, **25***c* and upper metal layers **26***a*, **26***b*, **26***c*. The foundation metal layers **25***a*, **25***b*, **25***c* are made of, for example, copper and provided on the upper surface of the upper insulating film **22**. The upper metal layers **26***a*, **26***b*, **26***c* are made of copper and provided on the upper surfaces of the foundation metal layers **25***a*, **25***b*, **25***c*.

**[0089]** In this case, as shown in FIG. **1**, the upper wiring indicated by the sign **24***a* (common upper wiring, first upper wiring) is solidly disposed on the upper left part of the upper insulating film **22** in a region of the upper insulating film **22** including nine openings **23***a*. The upper wiring **24***a* is connected, via all of the nine openings **23***a* of the upper insulating film **22**, to the predetermined nine points on the surface of the columnar electrode **13***a* of the semiconductor construct **2** having a square planar shape.

**[0090]** The upper wiring indicated by the sign **24***b* (common upper wiring, first upper wiring) is solidly disposed on the lower left part of the upper insulating film **22** in a region of the upper insulating film **22** including nine openings **23***b*. The upper wiring **24***b* is connected, via all of the nine openings **23***b* of the upper insulating film **22**, to the predetermined

nine points on the surface of the ground voltage columnar electrode **13***b* of the semiconductor construct **2** having a square planar shape.

**[0091]** Similarly to the wiring of the semiconductor construct **2** indicated by the sign **10***c*, each upper wiring indicated by the sign **24***c* (second upper wiring) has a connection portion, a connection pad portion, and an extension line extending therebetween. The upper wiring **24***c* is connected, via the opening **23***c* of the upper insulating film **22**, to the center of the upper surface of the columnar electrode **13***c* of the semiconductor construct **2** having a circular planar shape.

**[0092]** An overcoat film **27** made of, for example, a solder resist is provided on the upper surface of the upper insulating film **22** including the upper wirings **24***a*, **24***b*, **24***c*. Openings **28***a*, **28***b* are provided in parts of the overcoat film **27** that correspond to predetermined four points in the peripheral portions of the upper wirings **24***a*, **24***b*. An opening **28***c* is provided in a part of the overcoat film **27** that corresponds to the connection pad portion of the upper wiring **24***c*.

**[0093]** Solder balls **29***a*, **29***b*, **29***c* are provided in and above the openings **28***a*, **28***b*, **28***c* of the overcoat film **27** so that these solder balls are connected to the upper wirings **24***a*, **24***b*, **24***c*. In this case, as shown in FIG. **1**, the solder balls **29***a*, **29***b*, **29***c* are only disposed around the semiconductor construct **2**. Moreover, both the number of the solder balls **29***a* and the number of the solder balls **29***b* are four, and are the same as the number (four) of the power supply voltage and ground voltage connection pads **5***a*, **5***b* of the semiconductor construct **2**.

**[0094]** As described above, in this semiconductor device, the power supply voltage wiring **10***a* and the ground voltage wiring **10***b* of the semiconductor construct **2** are solidly formed in a square planar shape, and each connected to all of the four connection pads **5***a*, **5***b*. This allows the power supply voltage wiring **10***a* and the ground voltage wiring **10***b* not to be burned off even if an excessively high current runs through these wirings.

**[0095]** Furthermore, since the power supply voltage columnar electrode **13***a* and the ground voltage columnar electrode **13***b* of the semiconductor construct **2** are solidly formed, the columnar electrodes **13***a*, **13***b* can be reduced in resistance, and current capacity can thus be improved. Moreover, since the power supply voltage upper wiring **24***a* and the ground voltage upper wiring **24***b* are solidly formed, the upper wirings **24***a*, **24***b* can be reduced in resistance, and current capacity can thus be improved.

**[0096]** Still further, since the number (nine) of the openings **23***a*, **23***b* provided in the upper insulating film **22** on the power supply voltage and ground voltage columnar electrodes **13***a*, **13***b* of the semiconductor construct **2** is greater than the number (four) of the power supply voltage and ground voltage connection pads **5***a*, **5***b*, the connection portions of the openings **23***a*, **23***b* can be reduced in resistance as a whole, and current capacity can thus be further improved.

**[0097]** Here, the sizes of the parts of this semiconductor device are mentioned. The size of the base plate **1** is 3×3 mm. The size of the semiconductor construct **2** is 2×2 mm. The line width of the extension line **10***c*-**3** of the wiring **10***c* of the semiconductor construct **2** is 20 μm. The diameter of the columnar electrode **13***c* of the semiconductor construct **2** having a circular planar shape is 0.2 mm. The pitch of the columnar electrodes **13***c* is 0.4 mm. The diameter of the opening **23***a*, **23***b*, **23***c* of the upper insulating film **22** is 100 μm. The diameter of the solder balls **29***a*, **29***b*, **29***c* is 0.3 mm. The pitch of the solder balls **29***a*, **29***b*, **29***c* is 0.65 mm.

**[0098]** Now, one example of a method of manufacturing this semiconductor device is described. First, one example of a method of manufacturing the semiconductor construct **2** is described. In this case, the ground voltage connection pad **5***b* and associated parts are substantially similar to the power supply voltage connection pads **5***a* and associated parts, and are therefore not described.

**[0099]** First, as shown in FIG. **3**, an assembly is prepared. In this assembly, connection pads **5***a*, **5***c*, a passivation film **6** and a protective film **8** are formed on the upper surface of a silicon substrate in a wafer state (hereinafter referred to as a semiconductor wafer **31**). Further, the centers of the connection pads **5***a*, **5***c* are exposed through openings **7***a*, **7***c* of the passivation film **6** and through openings **9***a*, **9***c* of the protective film **8**.

**[0100]** In this case, the thickness of the semiconductor wafer **31** is greater than the thickness of a silicon substrate **4** shown in FIG. **2**. In FIG. **3**, zones indicated by the sign **32** are dicing streets. The parts of the passivation film **6** and the protective film **8** corresponding to the dicing street **32** and both its sides are removed.

**[0101]** Then, as shown in FIG. **4**, a foundation metal layer **33** is formed on the entire upper surface of the protective film **8** including the upper surfaces of the connection pads **5***a*, **5***c* exposed through openings **7***a*, **7***c* of the passivation film **6** and through openings **9***a*, **9***c* of the protective film **8**. In this case, the foundation metal layer **33** may only be a copper layer formed by electroless plating, may only be a copper layer formed by sputtering, or may be a copper layer formed by sputtering on a thin film layer of, for example, titanium formed by sputtering.

**[0102]** Then, a plating resist film **34** made of a positive liquid resist is patterned and formed on the upper surface of the foundation metal layer **33**. In this case, openings **35***a*, **35***c* are formed in parts of the plating resist film **34** corresponding to regions where upper metal layers **12***a*, **12***c* are to be formed. Further, electrolytic plating with copper is carried out using the foundation metal layer **33** as a plating current path, thereby forming the upper metal layers **12***a*, **12***c* on the upper surface of the foundation metal layer **33** within the openings **35***a*, **35***c* in the plating resist film **34**. Subsequently, the plating resist film **34** is released.

**[0103]** Then, as shown in FIG. **5**, a plating resist film **36** made of a negative dry film resist is patterned and formed on the upper surface of the foundation metal layer **33**. In this case, openings **37***a*, **37***c* are formed in parts of the plating resist film **36** corresponding to parts of the upper metal layer **12***a* except for its peripheral portion (a region where a columnar electrode **13***a* is to be formed) and corresponding to the connection pad portion of the upper metal layer **12***c* (a region where a columnar electrode **13***c* is to be formed).

**[0104]** Then, electrolytic plating with copper is carried out using the foundation metal layer **33** as a plating current path. As a result, the columnar electrode **13***a* is formed on the upper surface of the upper metal layer **12***a* within the openings **37***a* in the plating resist film **36**. Moreover, the columnar electrode **13***c* is formed on the upper surface of the connection pad portion of the upper metal layer **12***c* within the openings **37***c* in the plating resist film **36**. Subsequently, the plating resist film **36** is released.

**[0105]** Then, using the upper metal layers **12***a*, **12***c* as masks, the foundation metal layer **33** located in parts other than parts under the upper metal layers **12***a*, **12***c* is etched and removed. Thus, as shown in FIG. **6**, foundation metal layers

**11***a*, **11***c* remain under the upper metal layers **12***a*, **12***c* alone. In this state, wirings **10***a*, **10***c* having a double-layer structure are formed by the upper metal layers **12***a*, **12***c* and the foundation metal layers **11***a*, **11***c* remaining thereunder.

**[0106]** Then, as shown in FIG. **7**, a sealing film **14** made of, for example, an epoxy resin is formed by, for example, a spin coat method on the upper surface of the semiconductor wafer **31** corresponding to the dicing street **32** and both its sides and on the upper surface of the protective film **8** including the wirings **10***a*, **10***c* and the columnar electrodes **13***a*, **13***c* so that the thickness of this sealing film **14** is slightly greater than the height of the columnar electrodes **13***a*, **13***c*. Thus, in this state, the upper surfaces of the columnar electrodes **13***a*, **13***c* are covered with the sealing film **14**.

**[0107]** Then, the upper side of the sealing film **14** is properly ground to expose the upper surfaces of the columnar electrodes **13***a*, **13***c* as shown in FIG. **8**, and the upper surface of the sealing film **14** including the exposed upper surfaces of the columnar electrodes **13***a*, **13***c* is planarized. Further, as shown in FIG. **9**, the lower side of the semiconductor wafer **31** is properly ground to reduce the thickness of the semiconductor wafer **31**.

**[0108]** Then, as shown in FIG. **10**, a bonding layer **3** is bonded to the lower surface of the semiconductor wafer **31**. The bonding layer **3** is made of a die bond material such as an epoxy resin, and is fixedly attached in a semi-cured state by heating and pressurization to the lower surface of the semiconductor wafer **31**. Further, as shown in FIG. **11**, the sealing film **14**, the semiconductor wafer **31** and the bonding layer **3** are cut along the dicing streets **32**, thereby obtaining semiconductor constructs **2** having the bonding layers **3** on the lower surface.

**[0109]** Now, one example of how to manufacture the semiconductor device shown in FIG. **2** using the semiconductor construct **2** shown in FIG. **11** is described. In this case as well, parts associated with the ground voltage connection pad **5***b* are substantially similar to parts associated with the power supply voltage connection pads **5***a*, and are therefore not described.

**[0110]** First, as shown in FIG. **12**, a base plate **1** is prepared. This base plate **1** is made of, for example, an epoxy resin containing glass fabric as a base material, and has an area that allows the completed semiconductor devices shown in FIG. **2** to be formed thereon. For example, the base plate **1** has, but not exclusively, a square planar shape. In addition, zones indicated by the sign **41** in FIG. **12** correspond to cut lines for division.

**[0111]** Then, the bonding layers **3** fixedly attached to the lower surfaces of the silicon substrates **4** of the semiconductor constructs **2** are bonded to semiconductor construct placement regions on the upper surface of the base plate **1** to leave space in between. In this bonding, the bonding layers **3** are fully cured by heating and pressurization.

**[0112]** Then, as shown in FIG. **13**, a lattice-shaped insulating layer formation sheet **21***a* is positioned by, for example, pins and thus disposed on the upper surface of the base plate **1** around the semiconductor construct **2**. The lattice-shaped insulating layer formation sheet **21***a* is prepared by dispersing a reinforcer in a thermosetting resin such as an epoxy resin, semi-curing the thermosetting resin into a sheet form, and forming square holes in the sheet by, for example, punching.

**[0113]** Then, an upper insulating film formation sheet **22***a* is disposed on the upper surfaces of the semiconductor construct **2** and the insulating layer formation sheet **21***a*. The upper insulating film formation sheet **22***a* is prepared by impregnating, for example, glass fabric with a thermosetting resin such as an epoxy resin, and semi-curing the thermosetting resin into a sheet form.

**[0114]** Then, the insulating layer formation sheet **21***a* and the upper insulating film formation sheet **22***a* are heated and pressurized from the top and bottom using a pair of heating/pressurization plates **42**, **43**. By subsequent cooling, an insulating layer **21** in a square frame shape is formed on the upper surface of the base plate **1** around the semiconductor construct **2**, and an upper insulating film **22** is formed on the upper surfaces of the semiconductor construct **2** and the insulating layer **21**. In this case, the upper surface of the upper insulating film **22** is pressed by the lower surface of the upper heating/pressurization plate **42**, and is therefore a flat surface.

**[0115]** Then, as shown in FIG. **14**, by laser processing to radiate a laser beam, openings **23***a* are formed in parts of the upper insulating film **22** that correspond to predetermined nine points on the upper surface of the columnar electrode **13***a* of the semiconductor construct **2**. Also, an opening **23***c* is formed in a part of the upper insulating film **22** that corresponds to the center of the upper surface of the columnar electrode **13***c* of the semiconductor construct **2**.

**[0116]** Then, as shown in FIG. **15**, a foundation metal layer **44** is formed on the entire upper surface of the upper insulating film **22** including the upper surfaces of the columnar electrodes **13***a*, **13***c* of the semiconductor construct **2** that are exposed through the openings **23***a*, **23***c* of the upper insulating film **22**. In this case as well, the foundation metal layer **44** may only be a copper layer formed by electroless plating, may only be a copper layer formed by sputtering, or may be a copper layer formed by sputtering on a thin film layer of, for example, titanium formed by sputtering.

**[0117]** Then, a plating resist film **45** is patterned and formed on the upper surface of the foundation metal layer **44**. In this case, openings **46***a*, **46***c* are formed in parts of the plating resist film **45** corresponding to regions where upper metal layers **26***a*, **26***c* are to be formed. Further, electrolytic plating with copper is carried out using the foundation metal layer **44** as a plating current path, thereby forming the upper metal layers **26***a*, **26***c* on the upper surface of the foundation metal layer **44** within the openings **46***a*, **46***c* in the plating resist film **45**.

**[0118]** Then, the plating resist film **45** is released. Further, using the upper metal layers **26***a*, **26***c* as masks, the foundation metal layer **44** located in parts other than parts under the upper metal layers **26***a*, **26***c* is etched and removed. Thus, as shown in FIG. **16**, foundation metal layers **25***a*, **25***c* remain under the upper metal layers **26***a*, **26***c* alone. In this state, upper wirings **24***a*, **24***b* are formed by the upper metal layers **26***a*, **26***c* and the foundation metal layers **25***a*, **25***c* remaining thereunder.

**[0119]** Then, as shown in FIG. **17**, an overcoat film **27** made of, for example, a solder resist is formed by, for example, a screen printing method or spin coat method on the upper surface of the upper insulating film **22** including the upper wirings **24***a*, **24***c*. In this case, openings **28***a*, **28***b* are formed in parts of the overcoat film **27** that correspond to predetermined four points of the upper surface of the upper wiring **24***a* and to the connection pad portion of the upper wiring **24***c*.

**[0120]** Then, solder balls **29***a*, **29***c* are formed in and above the openings **28***a*, **28***c* of the overcoat film **27** so that these solder balls are connected to the predetermined four points of the upper surface of the upper wiring **24***a* and to the connec-

tion pad portion of the upper wiring **24***c*. Further, as shown in FIG. **18**, the overcoat film **27**, the upper insulating film **22**, the insulating layer **21** and the base plate **1** are cut along the cut lines **41** between adjacent semiconductor constructs **2**, thereby obtaining semiconductor devices shown in FIG. **2**.

Second Embodiment

**[0121]** FIG. **19** shows a transmitted plan view of a semiconductor device according to a second embodiment of the invention. FIG. **20** shows a sectional view of a proper part of the semiconductor device shown in FIG. **19**. This semiconductor device includes a base plate **1**. The base plate **1** has a square planar shape, and made of, for example, an epoxy resin containing glass fabric as a base material. The lower surface of a semiconductor construct **2** is bonded to the center of the upper surface of the base plate **1** through a bonding layer **3** made of a die bond material. The semiconductor construct **2** has a square planar shape, and is slightly smaller in size than the base plate **1**.

**[0122]** The semiconductor construct **2**, which is generally called a CSP, includes a silicon substrate (semiconductor substrate) **4**. The lower surface of the silicon substrate **4** is bonded to the center of the upper surface of the base plate **1** through the bonding layer **3**. Elements (not shown) such as a transistor, diode, resistor, and condenser that constitute an integrated circuit having a predetermined function are formed on the upper surface of the silicon substrate **4**. Connection pads **5***a*, **5***b*, **5***c* are provided on the peripheral portion of the upper surface of the silicon substrate **4**. The connection pads **5***a*, **5***b*, **5***c* are made of, for example, an aluminum-based metal, and connected to the elements of the integrated circuit.

**[0123]** Here, by way of example, the four connection pads indicated by the sign **5***a* and arranged on the upper left part of the silicon substrate **4** in FIG. **19** are for a common power supply voltage. The four connection pads indicated by the sign **5***b* and arranged on the lower left part of the silicon substrate **4** are for a common ground voltage. The four connection pads indicated by the sign **5***c* and arranged on the upper right part of the silicon substrate **4** and the four connection pads indicated by the sign **5***c* and arranged on the lower right part of the silicon substrate **4** are for a normal voltage. Here, in FIG. **20**, the ground voltage connection pads **5***b* and associated parts are substantially similar to the power supply voltage connection pads **5***a* and associated parts, and are therefore indicated by signs in parentheses.

**[0124]** A passivation film (insulating film) **6** made of, for example, silicon oxide is provided on the upper surface of the silicon substrate **4** except for the peripheral portion of the silicon substrate **4** and the centers of the connection pads **5***a*, **5***b*, **5***c*. The centers of the connection pads **5***a*, **5***b*, **5***c* are exposed through openings **7***a*, **7***b*, **7***c* provided in the passivation film **6**. A protective film (insulating film) **8** made of, for example, a polyimide resin is provided on the upper surface of the passivation film **6**. Openings **9***a*, **9***b*, **9***c* are provided in parts of the protective film **8** that correspond to the openings **7***a*, **7***b*, **7***c* of the passivation film **6**.

**[0125]** Wirings **10***a*, **10***b*, **10***c* are provided on the upper surface of the protective film **8**. The wirings **10***a*, **10***b*, **10***c* have a double-layer structure composed of foundation metal layers **11***a*, **11***b*, **11***c* and upper metal layers **12***a*, **12***b*, **12***c*. The foundation metal layers **11***a*, **11***b*, **11***c* are made of, for example, copper and provided on the upper surface of the protective film **8**. The upper metal layers **12***a*, **12***b*, **12***c* are made of copper and provided on the upper surfaces of the foundation metal layers **11**.

**[0126]** In this case, as shown in FIG. **19**, the wiring indicated by the sign **10***a* (common wiring) is solidly disposed on the upper left part of the silicon substrate **4** in a region that has a square planar shape and includes the four power supply voltage connection pads **5***a*. The wiring **10***a* is connected to all of the four power supply voltage connection pads **5***a* via the openings **7***a*, **9***a* of the passivation film **6** and the protective film **8**.

**[0127]** The wiring indicated by the sign **10***b* (common wiring) is solidly disposed on the lower left part of the silicon substrate **4** in a region that has a square planar shape and includes the four ground voltage connection pads **5***b*. The wiring **10***b* is connected to all of the four ground voltage connection pads **5***b* via the openings **7***b*, **9***b* of the passivation film **6** and the protective film **8**.

**[0128]** The wirings indicated by the sign **10***c* are disposed in the right region of the silicon substrate **4**. Each wiring **10***c* has a connection portion **10***c*-**1** connected to the normal voltage connection pad **5***c* via the openings **7***c*, **9***c* of the passivation film **6** and the protective film **8**, a connection pad portion **10***c*-**2** having a circular planar shape, and an extension line **10***c*-**3** extending between the connection portion **10***c*-**1** and the connection pad portion **10***c*-**2**.

**[0129]** Columnar electrodes (common columnar electrodes, first columnar electrodes) **13***a* are provided at predetermined four points on the upper surface of the wiring indicated by the sign **10***a* and having a square planar shape. The columnar electrodes **13***a* are made of copper and have a circular planar shape. Columnar electrodes (common columnar electrodes, first columnar electrodes) **13***b* are provided at predetermined four points on the upper surface of the wiring indicated by the sign **10***b* and having a square planar shape. The columnar electrodes **13***b* are made of copper and have a circular planar shape. Columnar electrodes (second columnar electrodes) **13***c* are provided on the upper surface of the connection pad portions **10***c*-**2** of the wirings indicated by the sign **10***c*. The columnar electrodes **13***c* are made of copper and have a circular planar shape.

**[0130]** Here, the number of the columnar electrodes **13***a* and the number of the columnar electrodes **13***b* are the same as the number of the power supply voltage connection pads **5***a* and the number of the ground voltage connection pads **5***b*, respectively. Moreover, the columnar electrodes **13***a*, **13***b* have the same shape as the columnar electrodes **13***c*. In addition, as shown in FIG. **19**, a total of 16 columnar electrodes **13***a*, **13***b*, **13***c* are arranged in matrix form.

**[0131]** A sealing film **14** made of, for example, an epoxy resin is provided around the columnar electrodes **13***a*, **13***b*, **13***c* on the upper surface of the protective film **8** including the wirings **10***a*, **10***b*, **10***c*. The columnar electrodes **13***a*, **13***b*, **13***c* are provided so that the upper surfaces thereof are flush with or several μm lower than the upper surface of the sealing film **14**. The explanation of the structure of the semiconductor construct **2** is completed now.

**[0132]** An insulating layer **21** in a square frame shape is provided on the upper surface of the base plate **1** around the semiconductor construct **2**. For example, the insulating layer **21** is made of a thermosetting resin such as an epoxy resin in which a reinforcer of an inorganic material such as silica fuller is dispersed. Alternatively, the insulating layer **21** is only made of a thermosetting resin such as an epoxy resin.

**[0133]** An upper insulating film **22** is provided on the upper surfaces of the semiconductor construct **2** and the insulating layer **21**. The upper insulating film **22** is made of, for example, a base glass fabric impregnated with a thermosetting resin such as an epoxy resin. Alternatively, the upper insulating film **22** is only made of a thermosetting resin such as an epoxy resin.

**[0134]** Openings (first openings) **23***a*, **23***b* having a square planar shape are provided in parts of the upper insulating film **22** that correspond to regions that have a square planar shape and include four columnar electrodes **13***a*, **13***b* of the semiconductor construct **2**. An opening (second opening) **23***c* having a circular planar shape is provided in a part of the upper insulating film **22** that corresponds to the center of the upper surface of the columnar electrode **13***c* of the semiconductor construct **2**.

**[0135]** Upper wirings **24***a*, **24***b*, **24***c* are provided on the upper surface of the upper insulating film **22**. The upper wirings **24***a*, **24***b*, **24***c* have a double-layer structure composed of foundation metal layers **25***a*, **25***b*, **25***c* and upper metal layers **26***a*, **26***b*, **26***c*. The foundation metal layers **25***a*, **25***b*, **25***c* are made of, for example, copper and provided on the upper surface of the upper insulating film **22**. The upper metal layers **26***a*, **26***b*, **26***c* are made of copper and provided on the upper surfaces of the foundation metal layers **25***a*, **25***b*, **25***c*.

**[0136]** In this case, as shown in FIG. **19**, the upper wiring indicated by the sign **24***a* (common upper wiring, first upper wiring) is solidly disposed on the upper left part of the upper insulating film **22** in a region of the upper insulating film **22** including an opening **23***a* having a square planar shape. The upper wiring **24***a* is connected, via one opening **23***a* of the upper insulating film **22** having a square planar shape, to the upper surfaces of all the four power supply voltage columnar electrodes **13***a* of the semiconductor construct **2**. Here, within the opening **23***a* of the upper insulating film **22**, the upper wiring **24***a* is provided on the upper surfaces of the four columnar electrodes **13***a* of the semiconductor construct **2** and on the upper surface of the sealing film **14** therearound.

**[0137]** The upper wiring indicated by the sign **24***b* (common upper wiring, first upper wiring) is solidly disposed on the lower left part of the upper insulating film **22** in a region of the upper insulating film **22** including the opening **23***b* having a square planar shape. The upper wiring **24***b* is connected, via one opening **23***b* of the upper insulating film **22** having a square planar shape, to the upper surfaces of all the four ground voltage columnar electrodes **13***b* of the semiconductor construct **2**. In this case as well, within the opening **23***b* of the upper insulating film **22**, the upper wiring **24***b* is provided on the upper surfaces of the four columnar electrodes **13***b* of the semiconductor construct **2** and on the upper surface of the sealing film **14** therearound.

**[0138]** Similarly to the wiring of the semiconductor construct **2** indicated by the sign **10***c*, each upper wiring indicated by the sign **24***c* (second upper wiring) has a connection portion, a connection pad portion, and an extension line extending therebetween. The upper wiring **24***c* is connected to the center of the upper surface of the columnar electrode **13***c* of the semiconductor construct **2** via the opening **23***c* of the upper insulating film **22** having a circular planar shape. Here, as shown in FIG. **20**, the upper surfaces of the upper wirings **24***a*, **24***b*, **24***c* are flush.

**[0139]** An overcoat film **27** made of, for example, a solder resist is provided on the upper surface of the upper insulating film **22** including the upper wirings **24***a*, **24***b*, **24***c*. Openings **28***a*, **28***b* are provided in parts of the overcoat film **27** that correspond to predetermined four points of the peripheral portion of the upper wirings **24***a*, **24***b*. An opening **28***c* is provided in a part of the overcoat film **27** that corresponds to the connection pad portion of the upper wiring **24***c*.

**[0140]** Solder balls **29***a*, **29***b*, **29***c* are provided in and above the openings **28***a*, **28***b*, **28***c* of the overcoat film **27** so that these solder balls are connected to the upper wirings **24***a*, **24***b*, **24***c*. In this case, as shown in FIG. **19**, the solder balls **29***a*, **29***b*, **29***c* are only disposed around the semiconductor construct **2**. Moreover, both the number of the solder balls **29***a* and the number of the solder balls **29***b* are four, and are the same as the number (four) of the power supply voltage and ground voltage connection pads **5***a*, **5***b* of the semiconductor construct **2**.

**[0141]** As described above, in this semiconductor device, the power supply voltage wiring **10***a* and the ground voltage wiring **10***b* of the semiconductor construct **2** are solidly formed in a square planar shape, and each connected to all of the four connection pads **5***a*, **5***b*. This allows the power supply voltage wiring **10***a* and the ground voltage wiring **10***b* not to be burned off even if an excessively high current runs through these wirings.

**[0142]** Furthermore, since one opening **23***a*, **23***b* having a square planar shape is provided in each of the parts of the upper insulating film **22** that correspond to the four power supply voltage columnar electrodes **13***a* and the four ground voltage columnar electrodes **13***b* of the semiconductor construct **2**. The solidly-formed upper wirings **24***a*, **24***b* are provided on the upper insulating film **22** so that these upper wirings are connected to all the four columnar electrodes **13***a* and all the four columnar electrodes **13***b* of the semiconductor construct **2** via the opening **23***a*, **23***b* of the upper insulating film **22**, the parts corresponding to the opening **23***a*, **23***b* of the upper insulating film **22** can be reduced in resistance, and current capacity can thus be improved.

**[0143]** Here, the sizes of the parts of this semiconductor device are mentioned. The size of the base plate **1** is 3×3 mm. The size of the semiconductor construct **2** is 2×2 mm. The line width of the extension line **10***c*-3 of the wiring **10***c* of the semiconductor construct **2** is 20 μm. The diameter of the columnar electrode **13***a*, **13***b*, **13***c* of the semiconductor construct **2** is 0.2 mm. The pitch of the columnar electrode **13***a*, **13***b*, **13***c* is 0.4 mm. The diameter of the opening **23***c* of the upper insulating film **22** having a circular planar shape is 100 μm. The diameter of the solder balls **29***a*, **29***b*, **29***c* is 0.3 mm. The pitch of the solder balls **29***a*, **29***b*, **29***c* is 0.65 mm.

**[0144]** Now, one example of a method of manufacturing this semiconductor device is described. First, one example of a method of manufacturing the semiconductor construct **2** is described. In this case, the ground voltage connection pad **5***b* and associated parts are substantially similar to the power supply voltage connection pads **5***a* and associated parts, and are therefore not described.

**[0145]** First, as shown in FIG. **21**, an assembly is prepared. In this assembly, connection pads **5***a*, **5***c*, a passivation film **6** and a protective film **8** are formed on the upper surface of a silicon substrate in a wafer state (hereinafter referred to as a semiconductor wafer **31**). Further, the centers of the connection pads **5***a*, **5***c* are exposed through openings **7***a*, **7***c* of the passivation film **6** and through openings **9***a*, **9***c* of the protective film **8**.

**[0146]** In this case, the thickness of the semiconductor wafer **31** is greater than the thickness of a silicon substrate **4** shown in FIG. **20**. In FIG. **21**, zones indicated by the sign **32** are dicing streets. The parts of the passivation film **6** and the protective film **8** corresponding to the dicing street **32** and both its sides are removed.

**[0147]** Then, as shown in FIG. **22**, a foundation metal layer **33** is formed on the entire upper surface of the protective film **8** including the upper surfaces of the connection pads **5***a*, **5***c* exposed through openings **7***a*, **7***c* of the passivation film **6** and through openings **9***a*, **9***c* of the protective film **8**. In this case, the foundation metal layer **33** may only be a copper layer formed by electroless plating, may only be a copper layer formed by sputtering, or may be a copper layer formed by sputtering on a thin film layer of, for example, titanium formed by sputtering.

**[0148]** Then, a plating resist film **34** made of a positive liquid resist is patterned and formed on the upper surface of the foundation metal layer **33**. In this case, openings **35***a*, **35***c* are formed in parts of the plating resist film **34** corresponding to regions where upper metal layers **12***a*, **12***c* are to be formed. Further, electrolytic plating with copper is carried out using the foundation metal layer **33** as a plating current path, thereby forming the upper metal layers **12***a*, **12***c* on the upper surface of the foundation metal layer **33** within the openings **35***a*, **35***c* in the plating resist film **34**. Subsequently, the plating resist film **34** is released.

**[0149]** Then, as shown in FIG. **23**, a plating resist film **36** made of a negative dry film resist is patterned and formed on the upper surface of the foundation metal layer **33**. In this case, openings **37***a*, **37***c* are formed in parts of the plating resist film **36** corresponding to predetermined four points of the upper metal layer **12***a* (a region where a columnar electrode **13***a* is to be formed) and corresponding to the connection pad portion of the upper metal layer **12***c* (a region where a columnar electrode **13***c* is to be formed).

**[0150]** Then, electrolytic plating with copper is carried out using the foundation metal layer **33** as a plating current path. As a result, the columnar electrode **13***a* is formed on the upper surface of the upper metal layer **12***a* within the openings **37***a* in the plating resist film **36**. Moreover, the columnar electrode **13***c* is formed on the upper surface of the connection pad portion of the upper metal layer **12***c* within the openings **37***c* in the plating resist film **36**. Subsequently, the plating resist film **36** is released.

**[0151]** Then, using the upper metal layers **12***a*, **12***c* as masks, the foundation metal layer **33** located in parts other than parts under the upper metal layers **12***a*, **12***c* is etched and removed. Thus, as shown in FIG. **24**, foundation metal layers **11***a*, **11***c* remain under the upper metal layers **12***a*, **12***c* alone. In this state, wirings **10***a*, **10***c* having a double-layer structure are formed by the upper metal layers **12***a*, **12***c* and the foundation metal layers **11***a*, **11***c* remaining thereunder.

**[0152]** Then, as shown in FIG. **25**, a sealing film **14** made of, for example, an epoxy resin is formed by, for example, the spin coat method on the upper surface of the semiconductor wafer **31** corresponding to the dicing street **32** and both its sides and on the upper surface of the protective film **8** including the wirings **10***a*, **10***c* and the columnar electrodes **13***a*, **13***c* so that the thickness of this sealing film **14** is slightly greater than the height of the columnar electrodes **13***a*, **13***c*. Thus, in this state, the upper surfaces of the columnar electrodes **13***a*, **13***c* are covered with the sealing film **14**.

**[0153]** Then, the upper side of the sealing film **14** is properly ground to expose the upper surfaces of the columnar electrodes **13***a*, **13***c* as shown in FIG. **26**, and the upper surface of the sealing film **14** including the exposed upper surfaces of the columnar electrodes **13***a*, **13***c* is planarized. Further, as shown in FIG. **27**, the lower side of the semiconductor wafer **31** is properly ground to reduce the thickness of the semiconductor wafer **31**.

**[0154]** Then, as shown in FIG. **28**, a bonding layer **3** is bonded to the lower surface of the semiconductor wafer **31**. The bonding layer **3** is made of a die bond material such as an epoxy resin, and is fixedly attached in a semi-cured state by heating and pressurization to the lower surface of the semiconductor wafer **31**. Further, as shown in FIG. **29**, the sealing film **14**, the semiconductor wafer **31** and the bonding layer **3** are cut along the dicing streets **32**, thereby obtaining semiconductor constructs **2** having the bonding layers **3** on the lower surface.

**[0155]** Now, one example of how to manufacture the semiconductor device shown in FIG. **20** using the semiconductor construct **2** shown in FIG. **29** is described. In this case as well, parts associated with the ground voltage connection pad **5***b* are substantially similar to parts associated with the power supply voltage connection pads **5***a*, and are therefore not described.

**[0156]** First, as shown in FIG. **30**, a base plate **1** is prepared. This base plate **1** is made of, for example, an epoxy resin containing glass fabric as a base material, and has an area that allows the completed semiconductor devices shown in FIG. **20** to be formed thereon. For example, the base plate **1** has, but not exclusively, a square planar shape. In addition, zones indicated by the sign **41** in FIG. **30** correspond to cut lines for division.

**[0157]** Then, the bonding layers **3** fixedly attached to the lower surfaces of the silicon substrates **4** of the semiconductor constructs **2** are bonded to semiconductor construct placement regions on the upper surface of the base plate **1** to leave space in between. In this bonding, the bonding layers **3** are fully cured by heating and pressurization.

**[0158]** Then, as shown in FIG. **31**, a lattice-shaped insulating layer formation sheet **21***a* is positioned by, for example, pins and thus disposed on the upper surface of the base plate **1** around the semiconductor construct **2**. The lattice-shaped insulating layer formation sheet **21***a* is prepared by dispersing a reinforcer in a thermosetting resin such as an epoxy resin, semi-curing the thermosetting resin into a sheet form, and forming square holes in the sheet by, for example, punching.

**[0159]** Then, an upper insulating film formation sheet **22***a* is disposed on the upper surfaces of the semiconductor construct **2** and the insulating layer formation sheet **21***a*. The upper insulating film formation sheet **22***a* is prepared by impregnating, for example, glass fabric with a thermosetting resin such as an epoxy resin, and semi-curing the thermosetting resin into a sheet form.

**[0160]** Then, the insulating layer formation sheet **21***a* and the upper insulating film formation sheet **22***a* are heated and pressurized from the top and bottom using a pair of heating/pressurization plates **42**, **43**. By subsequent cooling, an insulating layer **21** in a square frame shape is formed on the upper surface of the base plate **1** around the semiconductor construct **2**, and an upper insulating film **22** is formed on the upper surfaces of the semiconductor construct **2** and the insulating layer **21**. In this case, the upper surface of the upper

insulating film **22** is pressed by the lower surface of the upper heating/pressurization plate **42**, and is therefore a flat surface.

**[0161]** Then, as shown in FIG. **32**, by laser processing to radiate a laser beam, an opening **23***a* having a square planar shape is formed in a part of the upper insulating film **22** that corresponds to a region of the semiconductor construct **2** having a square planar shape and including the four columnar electrodes **13***a*. Also, an opening **23***c* having a circular planar shape is formed in a part of the upper insulating film **22** that corresponds to the center of the upper surface of the columnar electrode **13***c* of the semiconductor construct **2**.

**[0162]** In this state, the upper surface of the sealing film **14** around the columnar electrodes **13***a* is exposed through the opening **23***a* having a square planar shape.

**[0163]** Then, as shown in FIG. **33**, a foundation metal layer **44** is formed on the entire upper surface of the upper insulating film **22** including the upper surfaces of the columnar electrodes **13***a* and the sealing film **14** of the semiconductor construct **2** that are exposed through the opening **23***a* of the upper insulating film **22** and including the upper surface of the columnar electrode **13***c* of the semiconductor construct **2** exposed through the opening **23***c* of the upper insulating film **22**. In this case as well, the foundation metal layer **44** may only be a copper layer formed by electroless plating, may only be a copper layer formed by sputtering, or may be a copper layer formed by sputtering on a thin film layer of, for example, titanium formed by sputtering.

**[0164]** Then, a plating resist film **45** is patterned and formed on the upper surface of the foundation metal layer **44**. In this case, openings **46***a*, **46***c* are formed in parts of the plating resist film **45** corresponding to regions where upper metal layers **26***a*, **26***c* are to be formed. Further, electrolytic plating with copper is carried out using the foundation metal layer **44** as a plating current path, thereby forming the upper metal layers **26***a*, **26***c* on the upper surface of the foundation metal layer **44** within the openings **46***a*, **46***c* in the plating resist film **45**.

**[0165]** In this case, since the copper plating is isotropically formed on the upper surface of the foundation metal layer **44**, the thinnest portion of the upper metal layer **26***a* formed on the upper surface of the foundation metal layer **44** within the opening **23***a* of the upper insulating film **22** is set at a thickness equal to or greater than the thickness of the upper metal layer **26***a* shown in FIG. **20**. Then, the plating resist film **45** is released. Further, the upper side of the upper metal layers **26***a*, **26***c* is properly ground so that the upper surfaces of the upper metal layers **26***a*, **26***c* may be flush, as shown in FIG. **34**.

**[0166]** Then, using the upper metal layers **26***a*, **26***c* as masks, the foundation metal layer **44** located in parts other than parts under the upper metal layers **26***a*, **26***c* is etched and removed. Thus, as shown in FIG. **35**, foundation metal layers **25***a*, **25***c* remain under the upper metal layers **26***a*, **26***c* alone. In this state, upper wirings **24***a*, **24***c* are formed by the upper metal layers **26***a*, **26***c* and the foundation metal layers **25***a*, **25***c* remaining thereunder.

**[0167]** Then, as shown in FIG. **36**, an overcoat film **27** made of, for example, a solder resist is formed by, for example, the screen printing method or spin coat method on the upper surface of the upper insulating film **22** including the upper wirings **24***a*, **24***c*. In this case, openings **28***a*, **28***b* are formed in parts of the overcoat film **27** that correspond to predetermined four points of the upper surface of the upper wiring **24***a* and to the connection pad portion of the upper wiring **24***c*.

**[0168]** Then, solder balls **29***a*, **29***c* are formed in and above the openings **28***a*, **28***c* of the overcoat film **27** so that these solder balls are connected to the predetermined four points of the upper surface of the upper wiring **24***a* and to the connection pad portion of the upper wiring **24***c*. Further, as shown in FIG. **37**, the overcoat film **27**, the upper insulating film **22**, the insulating layer **21** and the base plate **1** are cut along the cut lines **41** between adjacent semiconductor constructs **2**, thereby obtaining semiconductor devices shown in FIG. **20**.

## Third Embodiment

**[0169]** FIG. **38** shows a transmitted plan view of a semiconductor device according to a third embodiment of the invention. FIG. **39** shows a sectional view of a proper part of the semiconductor device shown in FIG. **38**. This semiconductor device is different from the semiconductor device shown in FIG. **19** and FIG. **20** in that, in a semiconductor construct **2**, columnar electrodes **13***a*, **13***b* having a square planar shape are solidly provided, in similar fashion to power supply voltage and ground voltage wirings that are indicated by the signs **10***a*, **10***b* and have a square planar shape, in regions of the upper surfaces of the wirings **10***a*, **10***b* except for the peripheral portions thereof.

**[0170]** In this case, openings **23***a*, **23***b* of an upper insulating film **22** are provided in parts corresponding to the upper surfaces of the columnar electrodes **13***a*, **13***b* except for the peripheral portions thereof. Further, upper wirings **24***a*, **24***b* are connected, via the openings **23***a*, **23***b* of the upper insulating film **22**, to the upper surfaces of the columnar electrodes **13***a*, **13***b* except for the peripheral portions thereof.

**[0171]** As described above, since the power supply voltage columnar electrode **13***a* and the ground voltage columnar electrode **13** of the semiconductor construct **2** are solidly formed in this semiconductor device, the columnar electrodes **13***a*, **13***b* can be reduced in resistance, and current capacity can thus be further improved.

## Fourth Embodiment

**[0172]** FIG. **40** shows a transmitted plan view of a semiconductor device according to a fourth embodiment of the invention. FIG. **41** is a sectional view of a proper part of the semiconductor device shown in FIG. **41**. This semiconductor device includes a base plate **1**. The base plate **1** has a square planar shape, and made of, for example, an epoxy resin containing glass fabric as a base material. The lower surface of a semiconductor construct **2** is bonded to the center of the upper surface of the base plate **1** through a bonding layer **3** made of a die bond material. The semiconductor construct **2** has a square planar shape, and is slightly smaller in size than the base plate **1**.

**[0173]** The semiconductor construct **2**, which is generally called a CSP, includes a silicon substrate (semiconductor substrate) **4**. The lower surface of the silicon substrate **4** is bonded to the center of the upper surface of the base plate **1** through the bonding layer **3**. Elements (not shown) such as a transistor, diode, resistor, and condenser that constitute an integrated circuit having a predetermined function are formed on the upper surface of the silicon substrate **4**. Connection pads **5***a*, **5***b*, **5***c* are provided on the peripheral portion of the upper surface of the silicon substrate **4**. The connection pads **5***a*, **5***b*, **5***c* are made of, for example, an aluminum-based metal, and connected to the elements of the integrated circuit.

**[0174]** Here, by way of example, the four connection pads indicated by the sign **5***a* and arranged on the upper left part of the silicon substrate **4** in FIG. **40** are for a common power supply voltage. The four connection pads indicated by the sign **5***b* and arranged on the lower left part of the silicon substrate **4** are for a common ground voltage. The four connection pads indicated by the sign **5***c* and arranged on the upper right part of the silicon substrate **4** and the four connection pads indicated by the sign **5***c* and arranged on the lower right part of the silicon substrate **4** are for a normal voltage. Here, in FIG. **41**, the ground voltage connection pads **5***b* and associated parts are substantially similar to the power supply voltage connection pads **5***a* and associated parts, and are therefore indicated by signs in parentheses.

**[0175]** A passivation film (insulating film) **6** made of, for example, silicon oxide is provided on the upper surface of the silicon substrate **4** except for the peripheral portion of the silicon substrate **4** and the centers of the connection pads **5***a*, **5***b*, **5***c*. The centers of the connection pads **5***a*, **5***b*, **5***c* are exposed through openings **7***a*, **7***b*, **7***c* provided in the passivation film **6**. A protective film (insulating film) **8** made of, for example, a polyimide resin is provided on the upper surface of the passivation film **6**. Openings **9***a*, **9***b*, **9***c* are provided in parts of the protective film **8** that correspond to the openings **7***a*, **7***b*, **7***c* of the passivation film **6**.

**[0176]** Wirings **10***a*, **10***b*, **10***c* are provided on the upper surface of the protective film **8**. The wirings **10***a*, **10***b*, **10***c* have a double-layer structure composed of foundation metal layers **11***a*, **11***b*, **11***c* and upper metal layers **12***a*, **12***b*, **12***c*. The foundation metal layers **11***a*, **11***b*, **11***c* are made of, for example, copper and provided on the upper surface of the protective film **8**. The upper metal layers **12***a*, **12***b*, **12***c* are made of copper and provided on the upper surfaces of the foundation metal layers **11**.

**[0177]** In this case, as shown in FIG. **40**, the wiring indicated by the sign **10***a* (common wiring) is solidly disposed on the upper left part of the silicon substrate **4** in a region that has a square planar shape and includes the four power supply voltage connection pads **5***a*. The wiring **10***a* is connected to all of the four power supply voltage connection pads **5***a* via the openings **7***a*, **9***a* of the passivation film **6** and the protective film **8**.

**[0178]** The wiring indicated by the sign **10***b* (common wiring) is solidly disposed on the lower left part of the silicon substrate **4** in a region that has a square planar shape and includes the four ground voltage connection pads **5***b*. The wiring **10***b* is connected to all of the four ground voltage connection pads **5***b* via the openings **7***b*, **9***b* of the passivation film **6** and the protective film **8**.

**[0179]** The wirings indicated by the sign **10***c* are disposed in the right region of the silicon substrate **4**. Each wiring **10***c* has a connection portion **10***c*-**1** connected to the normal voltage connection pad **5***c* via the openings **7***c*, **9***c* of the passivation film **6** and the protective film **8**, a connection pad portion **10***c*-**2** having a circular planar shape, and an extension line **10***c*-**3** extending between the connection portion **10***c*-**1** and the connection pad portion **10***c*-**2**.

**[0180]** Columnar electrodes (common columnar electrodes, first columnar electrodes) **13***a* made of copper are provided at predetermined four points on the upper surface of the wiring indicated by the sign **10***a* and having a square planar shape. Columnar electrodes (common columnar electrodes, first columnar electrodes) **13***b* made of copper are provided at predetermined four points on the upper surface of the wiring indicated by the sign **10***b* and having a square planar shape. A columnar electrode (second columnar electrode) **13***c* made of copper is provided on the upper surface of the connection pad portion **10***c*-**2** of the wiring indicated by the sign **10***c*. Here, as shown in FIG. **40**, a total of 16 columnar electrodes **13***a*, **13***b*, **13***c* are arranged in matrix form.

**[0181]** A sealing film **14** made of, for example, an epoxy resin is provided around the columnar electrodes **13***a*, **13***b*, **13***c* on the upper surface of the protective film **8** including the wirings **10***a*, **10***b*, **10***c*. The columnar electrodes **13***a*, **13***b*, **13***c* are provided so that the upper surfaces thereof are flush with or several μm lower than the upper surface of the sealing film **14**. The explanation of the structure of the semiconductor construct **2** is completed now.

**[0182]** An insulating layer **21** in a square frame shape is provided on the upper surface of the base plate **1** around the semiconductor construct **2**. For example, the insulating layer **21** is made of a thermosetting resin such as an epoxy resin in which a reinforcer of an inorganic material such as silica fuller is dispersed. Alternatively, the insulating layer **21** is only made of a thermosetting resin such as an epoxy resin.

**[0183]** An upper insulating film **22** is provided on the upper surfaces of the semiconductor construct **2** and the insulating layer **21**. The upper insulating film **22** is made of, for example, a base glass fabric impregnated with a thermosetting resin such as an epoxy resin. Alternatively, the upper insulating film **22** is only made of a thermosetting resin such as an epoxy resin. Openings **23***a*, **23***b*, **23***c* are provided in parts of the upper insulating film **22** that correspond to the centers of the upper surfaces of the columnar electrodes **13***a*, **13***b*, **13***c* of the semiconductor construct **2**.

**[0184]** Upper wirings **24***a*, **24***b*, **24***c* are provided on the upper surface of the upper insulating film **22**. The upper wirings **24***a*, **24***b*, **24***c* have a double-layer structure composed of foundation metal layers **25***a*, **25***b*, **25***c* and upper metal layers **26***a*, **26***b*, **26***c*. The foundation metal layers **25***a*, **25***b*, **25***c* are made of, for example, copper and provided on the upper surface of the upper insulating film **22**. The upper metal layers **26***a*, **26***b*, **26***c* are made of copper and provided on the upper surfaces of the foundation metal layers **25***a*, **25***b*, **25***c*.

**[0185]** In this case, similarly to the wiring of the semiconductor construct **2** indicated by the sign **10***c*, each of the upper wirings **24***a*, **24***b*, **24***c* includes a connection portion, a connection pad portion, and an extension line extending therebetween. The connection portions of the upper wirings (common upper wirings, first upper wirings) **24***a*, **24***b* are connected to the upper surfaces of the columnar electrodes **13***a*, **13***b* of the semiconductor construct **2** via the openings **23***a*, **23***b* of the upper insulating film **22**. The connection portion of the upper wiring (second upper wiring) **24***c* is connected to the upper surface of the columnar electrode **13***c* of the semiconductor construct **2** via the opening **23***c* of the upper insulating film **22**.

**[0186]** An overcoat film **27** made of, for example, a solder resist is provided on the upper surface of the upper insulating film **22** including the upper wirings **24***a*, **24***b*, **24***c*. Openings **28***a*, **28***b*, **28***c* are provided in parts of the overcoat film **27** that correspond to the connection pad portions of the upper wirings **24***a*, **24***b*, **24***c*. Solder balls **29***a*, **29***b*, **29***c* are provided in and above the openings **28***a*, **28***b*, **28***c* so that these solder balls are connected to the connection pad portions of the upper wirings **24***a*, **24***b*, **24***c*. Here, as shown in FIG. **40**, the connection pad portions of the upper wirings **24***a*, **24***b*, **24***c*

and the solder balls **29**a, **29**b, **29**c are only disposed around the semiconductor construct **2**.

**[0187]** As described above, in this semiconductor device, the power supply voltage wiring **10**a and the ground voltage wiring **10**b of the semiconductor construct **2** are solidly formed in a square planar shape, and each connected to all of the four connection pads **5**a, **5**b. This allows the power supply voltage wiring **10**a and the ground voltage wiring **10**b not to be burned off even if an excessively high current runs through these wirings.

**[0188]** Here, the sizes of the parts of this semiconductor device are mentioned. The size of the base plate **1** is 3×3 mm. The size of the semiconductor construct **2** is 2×2 mm. The line width of the extension line **10**c-**3** of the wiring **10**c of the semiconductor construct **2** is 20 μm. The diameter of the columnar electrode **13**a, **13**b, **13**c of the semiconductor construct **2** is 0.2 mm. The pitch of the columnar electrode **13**a, **13**b, **13**c is 0.4 mm. The diameter of the opening **23** of the upper insulating film **22** is 100 μm. The diameter of the connection pad portion of the upper wiring is 0.3 mm. The pitch of the connection pad portion of the upper wiring is 0.65 mm.

**[0189]** In the meantime, since the base plate **1** is greater in size than the semiconductor construct **2**, even if the extension line **10**c-**3** of the normal voltage wiring **10**c of the semiconductor construct **2** has a relatively small line width of 20 μm, the extension line of the upper wiring **24**a, **24**b, **24**c can have a relatively great line width of about 100 μm. This makes it possible to prevent the power supply voltage upper wiring **24**a and the ground voltage upper wiring **24**b from being easily burned off even if an excessively high current runs through these upper wirings.

**[0190]** Now, one example of a method of manufacturing this semiconductor device is described. First, one example of a method of manufacturing the semiconductor construct **2** is described. In this case, the ground voltage connection pad **5**b and associated parts are substantially similar to the power supply voltage connection pads **5**a and associated parts, and are therefore not described.

**[0191]** First, as shown in FIG. **42**, an assembly is prepared. In this assembly, connection pads **5**a, **5**c, a passivation film **6** and a protective film **8** are formed on the upper surface of a silicon substrate in a wafer state (hereinafter referred to as a semiconductor wafer **31**). Further, the centers of the connection pads **5**a, **5**c are exposed through openings **7**a, **7**c of the passivation film **6** and through openings **9**a, **9**c of the protective film **8**.

**[0192]** In this case, the thickness of the semiconductor wafer **31** is greater than the thickness of a silicon substrate **4** shown in FIG. **41**. In FIG. **42**, zones indicated by the sign **32** are dicing streets. The parts of the passivation film **6** and the protective film **8** corresponding to the dicing street **32** and both its sides are removed.

**[0193]** Then, as shown in FIG. **43**, a foundation metal layer **33** is formed on the entire upper surface of the protective film **8** including the upper surfaces of the connection pads **5**a, **5**c exposed through openings **7**a, **7**c of the passivation film **6** and through openings **9**a, **9**c of the protective film **8**. In this case, the foundation metal layer **33** may only be a copper layer formed by electroless plating, may only be a copper layer formed by sputtering, or may be a copper layer formed by sputtering on a thin film layer of, for example, titanium formed by sputtering.

**[0194]** Then, a plating resist film **34** made of a positive liquid resist is patterned and formed on the upper surface of the foundation metal layer **33**. In this case, openings **35**a, **35**c are formed in parts of the plating resist film **34** corresponding to regions where upper metal layers **12**a, **12**c are to be formed. Further, electrolytic plating with copper is carried out using the foundation metal layer **33** as a plating current path, thereby forming the upper metal layers **12**a, **12**c on the upper surface of the foundation metal layer **33** within the openings **35**a, **35**c in the plating resist film **34**. Subsequently, the plating resist film **34** is released.

**[0195]** Then, as shown in FIG. **44**, a plating resist film **36** made of a negative dry film resist is patterned and formed on the upper surface of the foundation metal layer **33**. In this case, openings **37**a, **37**c are formed in parts of the plating resist film **36** corresponding to predetermined four points of the upper metal layer **12**a (a region where a columnar electrode **13**a is to be formed) and corresponding to the connection pad portion of the upper metal layer **12**c (a region where a columnar electrode **13**c is to be formed).

**[0196]** Then, electrolytic plating with copper is carried out using the foundation metal layer **33** as a plating current path. As a result, the columnar electrodes **13**a, **13**c are formed on the upper surface of the upper metal layer **12**a within the openings **37**a in the plating resist film **36** and on the upper surface of the connection pad portion of the upper metal layer **12**c within the openings **37**c in the plating resist film **36**. Subsequently, the plating resist film **36** is released.

**[0197]** Then, using the upper metal layers **12**a, **12**c as masks, the foundation metal layer **33** located in parts other than parts under the upper metal layers **12**a, **12**c is etched and removed. Thus, as shown in FIG. **45**, foundation metal layers **11**a, **11**c remain under the upper metal layers **12**a, **12**c alone. In this state, wirings **10**a, **10**c having a double-layer structure are formed by the upper metal layers **12**a, **12**c and the foundation metal layers **11**a, **11**c remaining thereunder.

**[0198]** Then, as shown in FIG. **46**, a sealing film **14** made of, for example, an epoxy resin is formed by, for example, the spin coat method on the upper surface of the semiconductor wafer **31** corresponding to the dicing street **32** and both its sides and on the upper surface of the protective film **8** including the wirings **10**a, **10**c and the columnar electrodes **13**a, **13**c so that the thickness of this sealing film **14** is slightly greater than the height of the columnar electrodes **13**a, **13**c. Thus, in this state, the upper surfaces of the columnar electrodes **13**a, **13**c are covered with the sealing film **14**.

**[0199]** Then, the upper side of the sealing film **14** is properly ground to expose the upper surfaces of the columnar electrodes **13**a, **13**c as shown in FIG. **47**, and the upper surface of the sealing film **14** including the exposed upper surfaces of the columnar electrodes **13**a, **13**c is planarized. Further, as shown in FIG. **48**, the lower side of the semiconductor wafer **31** is properly ground to reduce the thickness of the semiconductor wafer **31**.

**[0200]** Then, as shown in FIG. **49**, a bonding layer **3** is bonded to the lower surface of the semiconductor wafer **31**. The bonding layer **3** is made of a die bond material such as an epoxy resin, and is fixedly attached in a semi-cured state by heating and pressurization to the lower surface of the semiconductor wafer **31**. Further, as shown in FIG. **50**, the sealing film **14**, the semiconductor wafer **31** and the bonding layer **3** are cut along the dicing streets **32**, thereby obtaining semiconductor constructs **2** having the bonding layers **3** on the lower surface.

**[0201]** Now, one example of how to manufacture the semiconductor device shown in FIG. **41** using the semiconductor construct **2** shown in FIG. **50** is described. In this case as well, parts associated with the ground voltage connection pad **5***b* are substantially similar to parts associated with the power supply voltage connection pads **5***a*, and are therefore not described.

**[0202]** First, as shown in FIG. **51**, a base plate **1** is prepared. This base plate **1** is made of, for example, an epoxy resin containing glass fabric as a base material, and has an area that allows the completed semiconductor devices shown in FIG. **41** to be formed thereon. For example, the base plate **1** has, but not exclusively, a square planar shape. In addition, zones indicated by the sign **41** in FIG. **51** correspond to cut lines for division.

**[0203]** Then, the bonding layers **3** fixedly attached to the lower surfaces of the silicon substrates **4** of the semiconductor constructs **2** are bonded to semiconductor construct placement regions on the upper surface of the base plate **1** to leave space in between. In this bonding, the bonding layers **3** are fully cured by heating and pressurization.

**[0204]** Then, as shown in FIG. **52**, a lattice-shaped insulating layer formation sheet **21***a* is positioned by, for example, pins and thus disposed on the upper surface of the base plate **1** around the semiconductor construct **2**. The lattice-shaped insulating layer formation sheet **21***a* is prepared by dispersing a reinforcer in a thermosetting resin such as an epoxy resin, semi-curing the thermosetting resin into a sheet form, and forming square holes in the sheet by, for example, punching.

**[0205]** Then, an upper insulating film formation sheet **22***a* is disposed on the upper surfaces of the semiconductor construct **2** and the insulating layer formation sheet **21***a*. The upper insulating film formation sheet **22***a* is prepared by impregnating, for example, glass fabric with a thermosetting resin such as an epoxy resin, and semi-curing the thermosetting resin into a sheet form.

**[0206]** Then, the insulating layer formation sheet **21***a* and the upper insulating film formation sheet **22***a* are heated and pressurized from the top and bottom using a pair of heating/pressurization plates **42**, **43**. By subsequent cooling, an insulating layer **21** in a square frame shape is formed on the upper surface of the base plate **1** around the semiconductor construct **2**, and an upper insulating film **22** is formed on the upper surfaces of the semiconductor construct **2** and the insulating layer **21**. In this case, the upper surface of the upper insulating film **22** is pressed by the lower surface of the upper heating/pressurization plate **42**, and is therefore a flat surface.

**[0207]** Then, as shown in FIG. **53**, by laser processing to radiate a laser beam, openings **23***a*, **23***c* are formed in parts of the upper insulating film **22** that correspond to the centers of the upper surfaces of the columnar electrodes **13***a*, **13***c* of the semiconductor construct **2**.

**[0208]** Then, as shown in FIG. **54**, a foundation metal layer **44** is formed on the entire upper surface of the upper insulating film **22** including the upper surfaces of the columnar electrodes **13***a*, **13***c* of the semiconductor construct **2** that are exposed through the openings **23***a*, **23***c* of the upper insulating film **22**. In this case as well, the foundation metal layer **44** may only be a copper layer formed by electroless plating, may only be a copper layer formed by sputtering, or may be a copper layer formed by sputtering on a thin film layer of, for example, titanium formed by sputtering.

**[0209]** Then, a plating resist film **45** is patterned and formed on the upper surface of the foundation metal layer **44**. In this case, openings **46***a*, **46***c* are formed in parts of the plating resist film **45** corresponding to regions where upper metal layers **26***a*, **26***c* are to be formed. Further, electrolytic plating with copper is carried out using the foundation metal layer **44** as a plating current path, thereby forming the upper metal layers **26***a*, **26***c* on the upper surface of the foundation metal layer **44** within the openings **46***a*, **46***c* in the plating resist film **45**.

**[0210]** Then, the plating resist film **45** is released. Further, using the upper metal layers **26***a*, **26***c* as masks, the foundation metal layer **44** located in parts other than parts under the upper metal layers **26***a*, **26***c* is etched and removed. Thus, as shown in FIG. **55**, foundation metal layers **25***a*, **25***c* remain under the upper metal layers **26***a*, **26***c* alone. In this state, upper wirings **24***a*, **24***b* are formed by the upper metal layers **26***a*, **26***c* and the foundation metal layers **25***a*, **25***c* remaining thereunder.

**[0211]** Then, as shown in FIG. **56**, an overcoat film **27** made of, for example, a solder resist is formed by, for example, the screen printing method or spin coat method on the upper surface of the upper insulating film **22** including the upper wirings **24***a*, **24***c*. In this case, openings **28***a*, **28***c* are formed in parts of the overcoat film **27** that correspond to the connection pad portions of the upper wirings **24***a*, **24***c*.

**[0212]** Then, solder balls **29***a*, **29***c* are formed in and above the openings **28***a*, **28***c* of the overcoat film **27** so that these solder balls are connected to the connection pad portions of the upper wirings **24***a*, **24***c*. Further, as shown in FIG. **57**, the overcoat film **27**, the upper insulating film **22**, the insulating layer **21** and the base plate **1** are cut along the cut lines **41** between adjacent semiconductor constructs **2**, thereby obtaining semiconductor devices shown in FIG. **41**.

### Fifth Embodiment

**[0213]** FIG. **58** shows a transmitted plan view of a semiconductor device according to a fifth embodiment of the invention. FIG. **59** shows a sectional view of a proper part of the semiconductor device shown in FIG. **58**. This semiconductor device is different from the semiconductor device shown in FIG. **40** and FIG. **41** in that a solidly-formed power supply voltage upper wiring **24***a* and a solidly-formed ground voltage upper wiring **24***b* are provided instead of the above-mentioned power supply voltage upper wiring **24***a* and the ground voltage upper wiring **24***b*. The power supply voltage upper wiring **24***a* is provided in a region that includes four power supply voltage columnar electrodes **13***a* and includes places where four power supply voltage solder balls **29***a* are arranged. The ground voltage upper wiring **24***b* is provided in a region that includes four ground voltage columnar electrodes **13***b* and includes places where four ground voltage solder balls **29***b* are arranged.

**[0214]** As described above, since the power supply voltage upper wiring **24***a* and the ground voltage upper wiring **24***b* are solidly formed in this semiconductor device, the upper wirings **24***a*, **24***b* can be reduced in resistance, and current capacity can thus be improved, as compared with the semiconductor device shown in FIG. **40** and FIG. **41**.

### Sixth Embodiment

**[0215]** FIG. **60** shows a transmitted plan view of a semiconductor device according to a sixth embodiment of the invention. This semiconductor device is different from the semiconductor device shown in FIG. **48** in that nine power

supply voltage columnar electrodes **13**_a_ are provided in matrix form on the upper surface of a solidly-formed power supply voltage upper wiring **24**_a_ and in that nine ground voltage columnar electrodes **13**_b_ are provided in matrix form on the upper surface of a solidly-formed ground voltage upper wiring **24**_b_.

**[0216]** Thus, since this semiconductor device has nine power supply voltage columnar electrodes **13**_a_ and nine ground voltage columnar electrodes **13**_b_, the parts corresponding to the columnar electrodes **13**_a_, **13**_b_ can be reduced in resistance as a whole, and current capacity can thus be improved, as compared with the semiconductor device shown in FIG. **58** and FIG. **59**. In this case, the pitch of the columnar electrodes **13**_a_, **13**_b_ is, by way of example, 0.25.

Seventh Embodiment

**[0217]** FIG. **61** shows a sectional view of a semiconductor device according to a seventh embodiment of the invention. This semiconductor device is greatly different from the semiconductor device shown in FIG. **41** in that two upper insulating films and two upper wirings are provided. That is, on the upper surface of a first upper insulating film **22**A including a first upper wiring **24**A, a second upper insulating film **22**B made of the same material as the first upper insulating film **22**A is provided. On the upper surface of the second upper insulating film **22**B, a second upper insulating film **24**B similar in structure to the first upper wiring **24**A is provided.

**[0218]** One end of the first upper wiring **24**A is connected to a columnar electrode **13** via an opening **23**A of the first upper insulating film **22**A. One end of the second upper insulating film **24**B is connected to the connection pad portion of the first upper wiring **24**A via an opening **23**B of the second upper insulating film **22**B. A solder ball **29** is connected to the connection pad portion of the second upper insulating film **24**B via an opening **28** of an overcoat film **27**. In addition, three or more upper insulating films and three or more upper wirings may be provided.

**[0219]** Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

**1**. (canceled)

**2**. A semiconductor device comprising:
- a semiconductor substrate;
- connection pads provided on the semiconductor substrate, the connection pads comprising common power supply voltage connection pads, common ground voltage connection pads, and normal voltage connection pads;
- an insulating film provided on the semiconductor substrate and having openings in regions corresponding to the connection pads;
- at least one first common wiring serving for a power supply voltage and provided solidly on the insulating film so as to be connected to the common power supply voltage connection pads via corresponding openings in the insulating film;
- at least one second common wiring serving for a ground voltage and provided solidly on the insulating film so as to be connected to the common ground voltage connection pads via corresponding openings in the insulating film; and
- at least two normal wirings each provided on the insulating film so as to be connected to a normal voltage connection pad via a corresponding opening in the insulating film.

**3**. The semiconductor device according to claim **2**, wherein a line width of the at least two normal wirings is approximately 20 μm or less.

**4**. The semiconductor device according to claim **2**, further comprising:
- at least one first electrode provided on the at least one first common wiring;
- at least one second electrode provided on the at least one second common wiring; and
- at least two third electrodes provided on connection pad portions of the at least two normal wirings, respectively,
- wherein the first, second, third electrodes have a substantially same shape.

**5**. The semiconductor device according to claim **4**, wherein at least one of:
- (i) the at least one first electrode comprises at least two first electrodes, and a distance between the at least two first electrodes is smaller than a distance between the at least two third electrodes, and
- (ii) the at least one second electrode comprises at least two second electrodes, and a distance between the at least two second electrodes is smaller than a distance between the at least two third electrodes.

**6**. The semiconductor device according to claim **2**, wherein a total number of the common power supply voltage connection pads and the common ground voltage connection pads is not less than a total number of the normal voltage connection pads.

**7**. The semiconductor device according to claim **6**, wherein at least one of:
- (i) the first common wiring is connected to a third common wiring provided solidly and serving for the power supply voltage, and
- (ii) the second common wiring is connected to a fourth common wiring provided solidly and serving for the ground voltage.

**8**. The semiconductor device according to claim **7**, wherein at least one of:
- (i) the first and third common wirings are connected via at least two first connection portions, and a distance between the at least two first connection portions is smaller than a distance between the at least two normal wirings, and
- (ii) the second and fourth common wirings are connected via at least two second connection portions, and a distance between the at least two second connection portions is smaller than the distance between the normal wirings.

**9**. The semiconductor device according to claim **2**, wherein:
- the insulating film comprises a passivation film and a protective film;
- the first common wiring, the second common wiring, and the normal wirings have a double-layer structure comprising foundation metal layers and upper metal layers; and

the foundation metal layers are provided on an upper surface of the protective film, and the upper metal layers are provided on upper surfaces of the foundation metal layers.

**10**. The semiconductor device according to claim **4**,

wherein the first, second, and third electrodes are columnar electrodes made of copper, and

wherein the semiconductor device further comprises a sealing film provided around the first, second, and third electrodes.

**11**. The semiconductor device according to claim **4**, wherein one of the first and second electrodes is disposed in a region other than for a peripheral portion of the semiconductor substrate.

**12**. A semiconductor device comprising:

a semiconductor substrate;

connection pads provided on the semiconductor substrate, the connection pads comprising common voltage connection pads and normal voltage connection pads;

an insulating film provided on the semiconductor substrate and having openings in regions corresponding to the connection pads;

at least one common wiring provided solidly on the insulating film so as to be connected to the common voltage connection pads via corresponding openings in the insulating film;

at least two normal wirings each provided on the insulating film so as to be connected to a normal voltage connection pad via a corresponding opening in the insulating film;

at least one first electrode provided on the first common wiring;

at least two second electrodes provided on connection pad portions of the at least two normal wirings, respectively;

an upper insulating film having at least one first opening in a part corresponding to the first electrode and at least two second openings in parts corresponding to the second electrodes;

at least one first upper wiring provided to be connected to the first electrode via the first opening; and

at least two second upper wirings provided to be connected to the second electrodes via the second openings.

**13**. The semiconductor device according to claim **12**, wherein the at least one common wiring comprises two common wirings, one of the common wirings serving for a power supply voltage and the other common wiring serving for a ground voltage.

**14**. The semiconductor device according to claim **13**, wherein a line width of the at least two normal wirings is approximately 20 μm or less.

**15**. The semiconductor device according to claim **12**, wherein a total number of the common voltage connection pads is not less than a total number of the normal voltage connection pads.

**16**. The semiconductor device according to claim **12**, wherein the at least one first upper wiring is an upper common wiring provided solidly on the upper insulating film, and the common wiring is connected to the upper common wiring via the at least one first electrode.

**17**. The semiconductor device according to claim **16**, wherein a total area of the upper common wiring is larger than a total area of the common wiring.

**18**. The semiconductor device according to claim **12**, wherein the at least one first electrode comprises at least two first electrodes, and a distance between the at least two first electrodes is smaller than a distance between the at least two second electrodes.

**19**. The semiconductor device according to claim **15**, wherein:

the insulating film comprises a passivation film and a protective film;

the common wiring, the normal wirings, and the first and second upper wirings have a double-layer structure comprising foundation metal layers and upper metal layers;

the foundation metal layers of the common wiring and the normal wirings are provided on an upper surface of the insulating film, and the foundation metal layers of the first and second upper wirings are provided on an upper surface of the upper insulating film, and

the upper metal layers are made of copper and provided on upper surfaces of the foundation metal layers.

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