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(54) **APPARATUSES AND METHODS FOR ENCODING AND DECODING OF SIGNAL LINES FOR MULTI-LEVEL COMMUNICATION ARCHITECTURES**

(71) Applicant: **MICRON TECHNOLOGY, INC.**, BOISE, ID (US)

(72) Inventors: **Timothy Hollis**, Meridian, ID (US); **Roy E. Greeff**, Boise, ID (US)

(73) Assignee: **MICRON TECHNOLOGY, INC.**, BOISE, ID (US)

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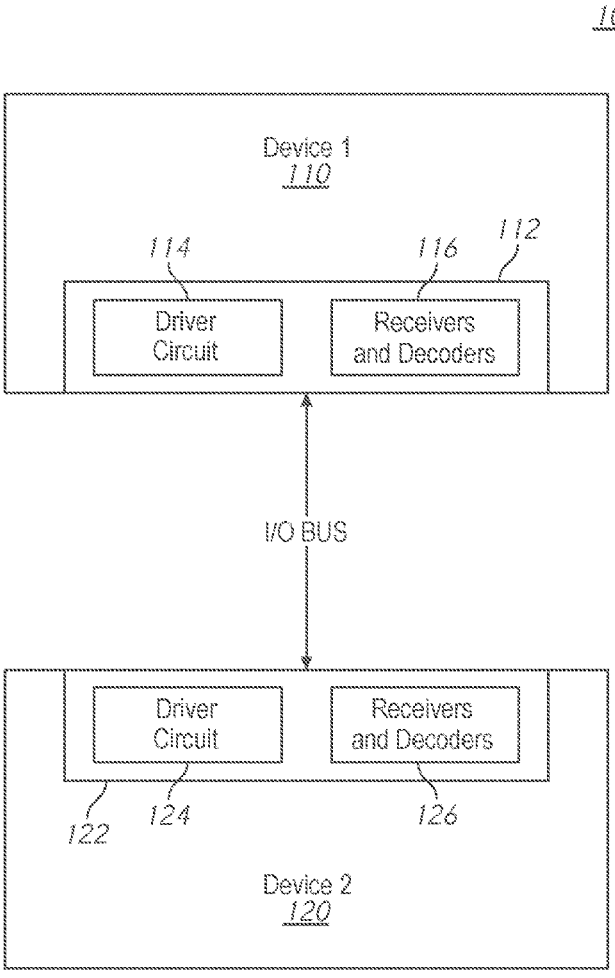
(52) **U.S. Cl.**

CPC ***G06F 3/0613*** (2013.01); ***H04L 25/4923*** (2013.01); ***G06F 13/4234*** (2013.01); ***G06F 3/0607*** (2013.01); ***G11C 7/1072*** (2013.01); ***G06F 13/4022*** (2013.01); ***G06F 13/4072*** (2013.01); ***G06F 13/4282*** (2013.01); ***G06F 3/0635*** (2013.01)

(57) **ABSTRACT**

Apparatuses and methods for multi-level communication architectures are disclosed herein. An example apparatus may include a driver circuit configured to convert a plurality of bitstreams into a plurality of multilevel signals. A count of the plurality of bitstreams is greater than count of the plurality of multilevel signals. The driver circuit further configured to drive the plurality of multilevel signals onto a plurality of signal lines using individual drivers. A driver of the individual drivers is configured to drive more than two voltages.



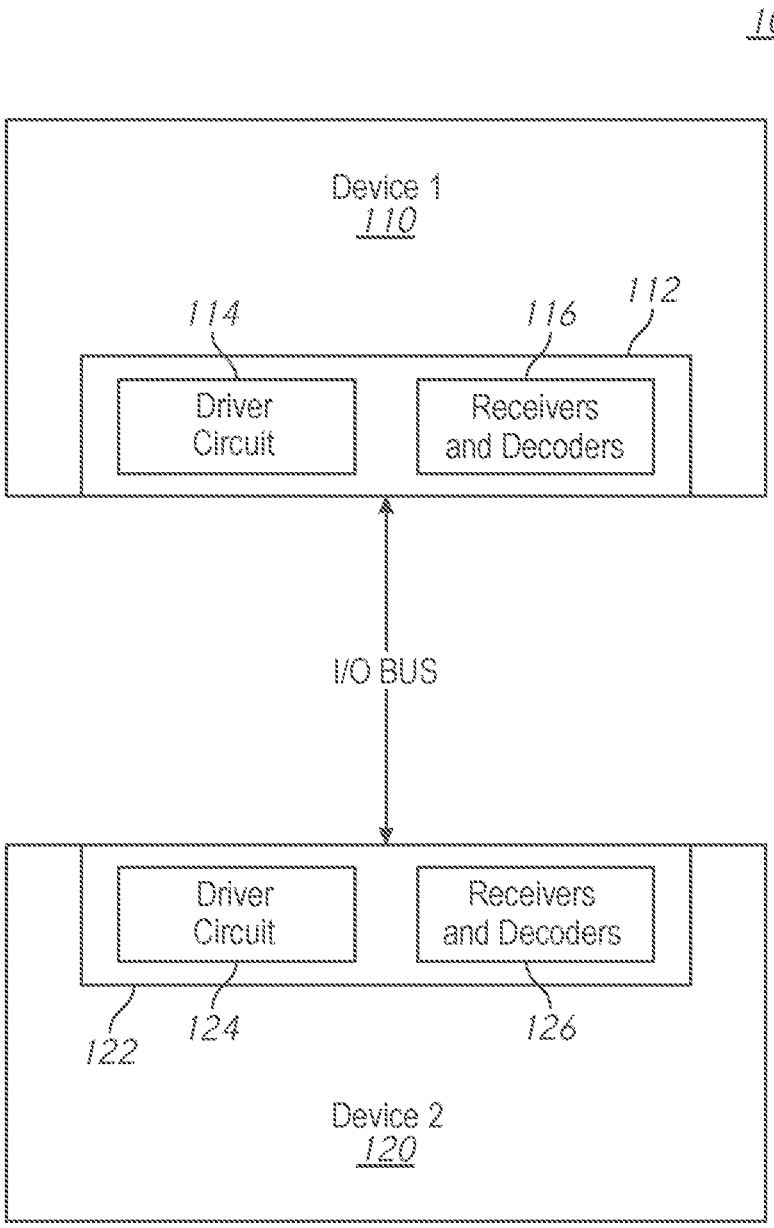

100
Device 1
110
114
116
112
Driver Circuit
Receivers and Decoders
I/O BUS
Driver Circuit
Receivers and Decoders
122
124
126
Device 2
120

FIG. 1

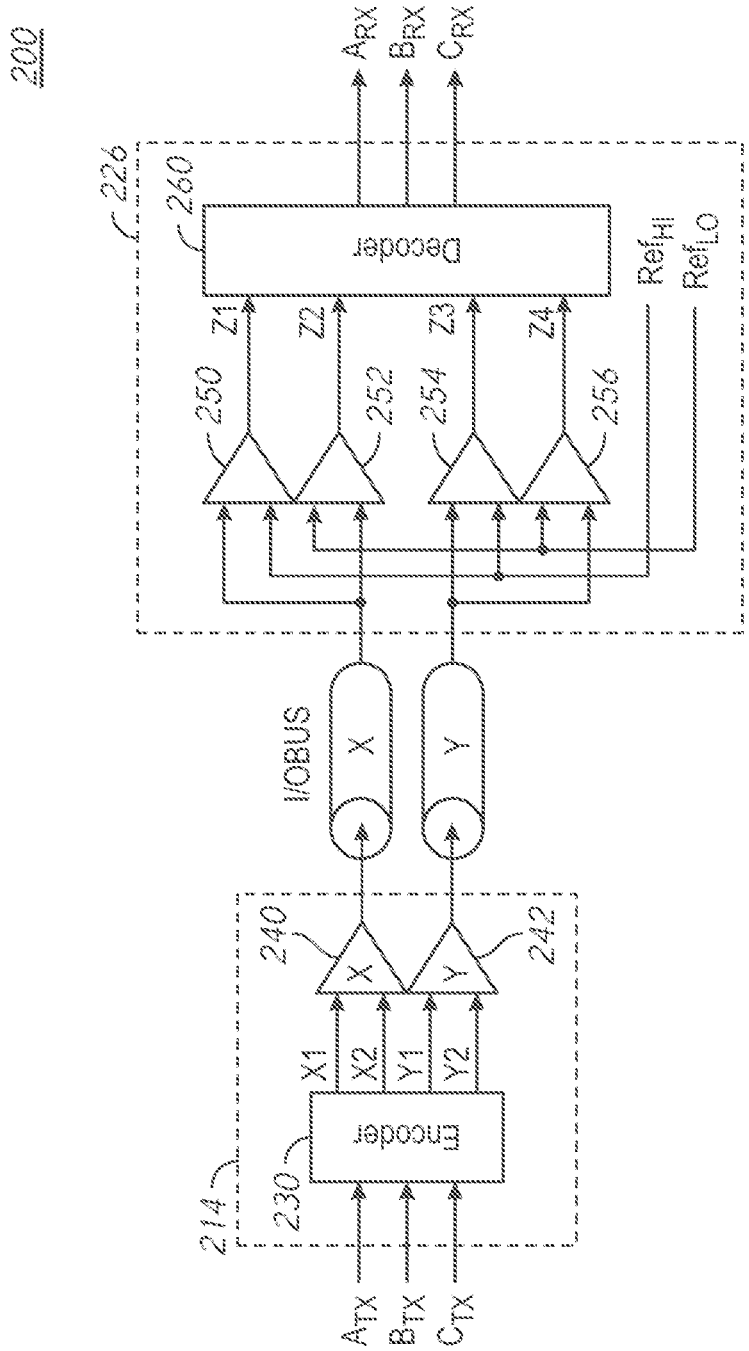

200
A_{RX}
B_{RX}
C_{RX}
226
260
Decoder
Ref_{HI}
Ref_{LO}
Z1
Z2
Z3
Z4
250
252
254
256
I/OBUS
X
Y
240
242
X
Y
X1
X2
Y1
Y2
Encoder
214
230
A_{TX}
B_{TX}
C_{TX}

FIG. 2

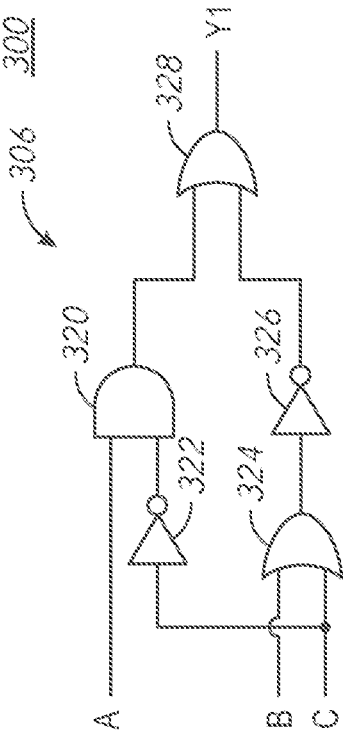


FIG. 3C

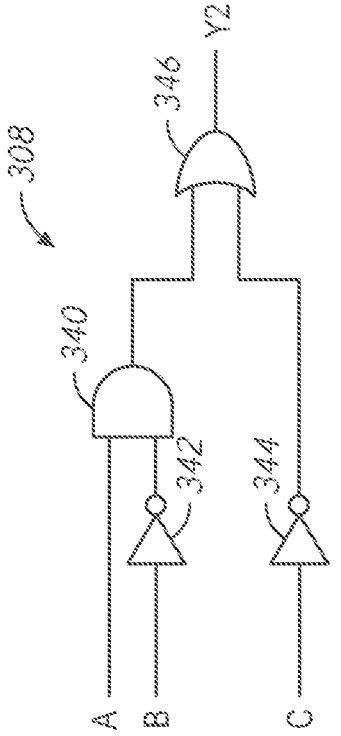


FIG. 3D

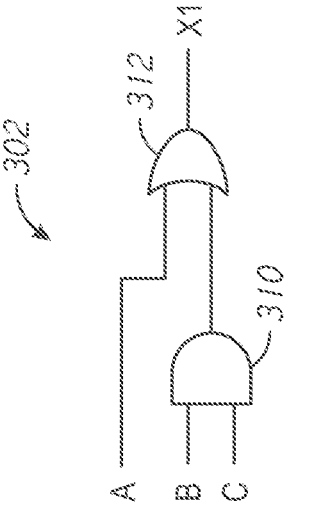


FIG. 3A

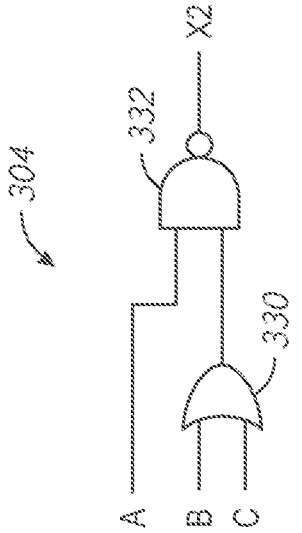


FIG. 3B

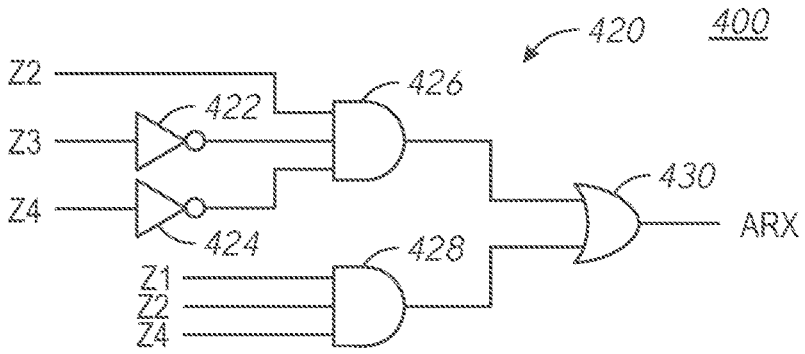


FIG. 4A

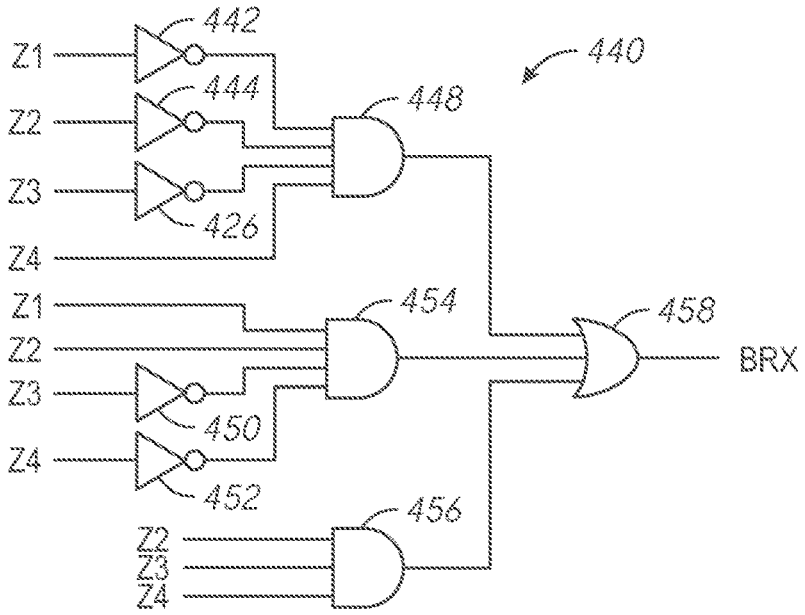


FIG. 4B

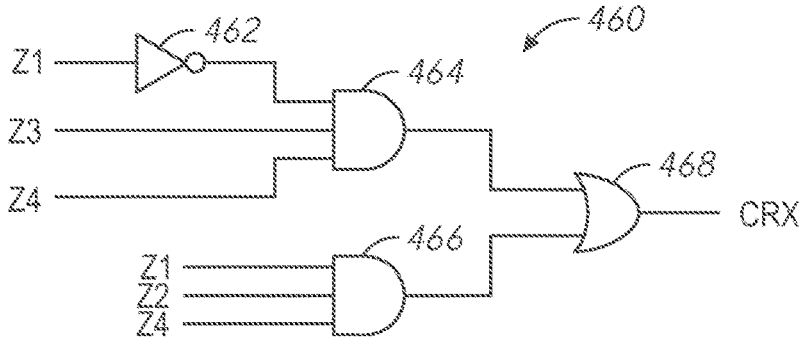


FIG. 4C

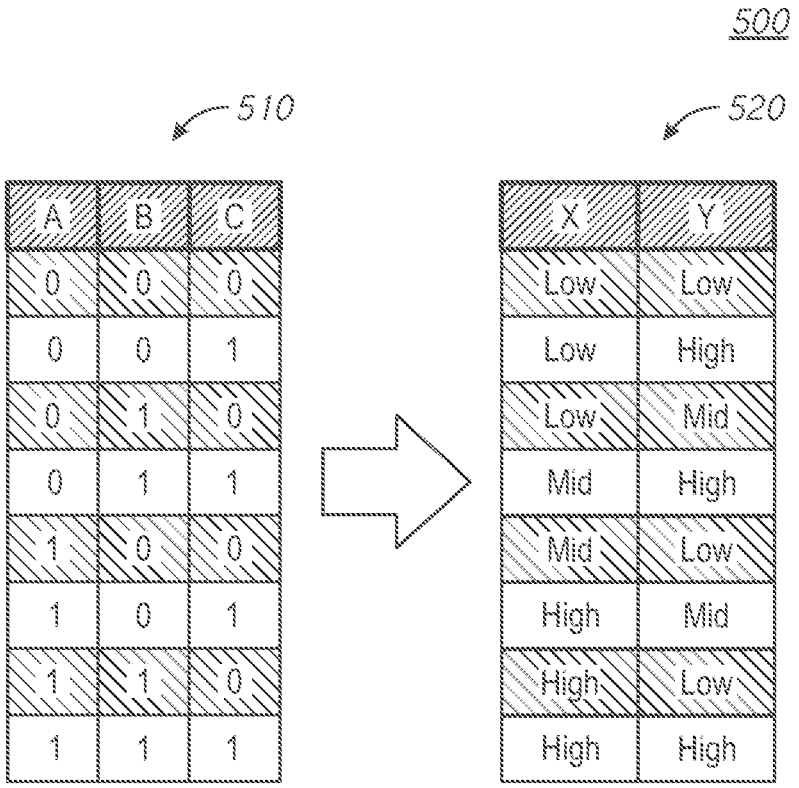

500
510
520
A
B
C
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1
X
Y
Low Low
Low High
Low Mid
Mid High
Mid Low
High Mid
High Low
High High

FIG. 5

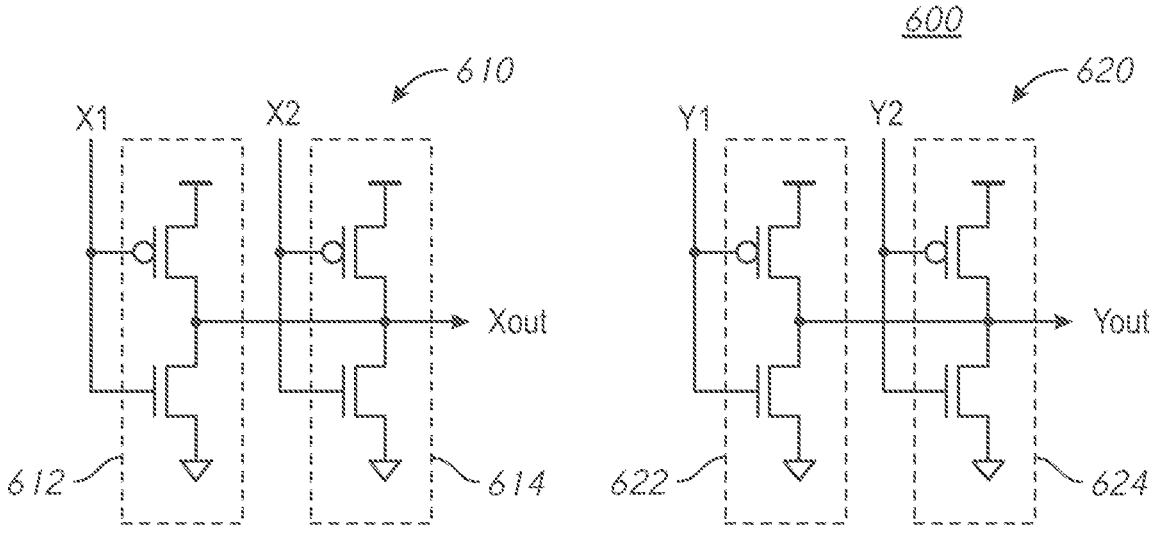

600
610
620
X1
X2
Y1
Y2
Xout
Yout
612
614
622
624

FIG. 6

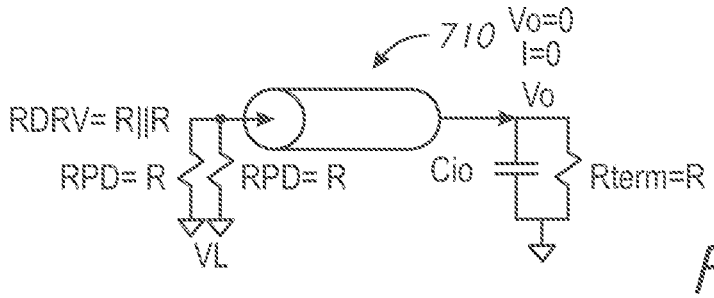


FIG. 7A

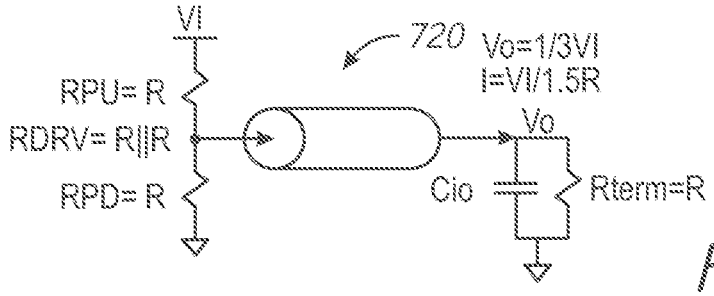


FIG. 7B

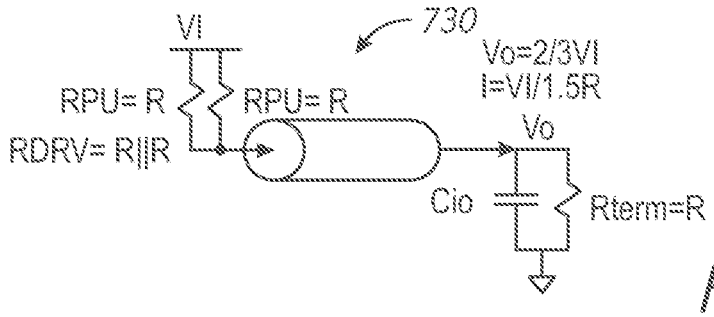


FIG. 7C

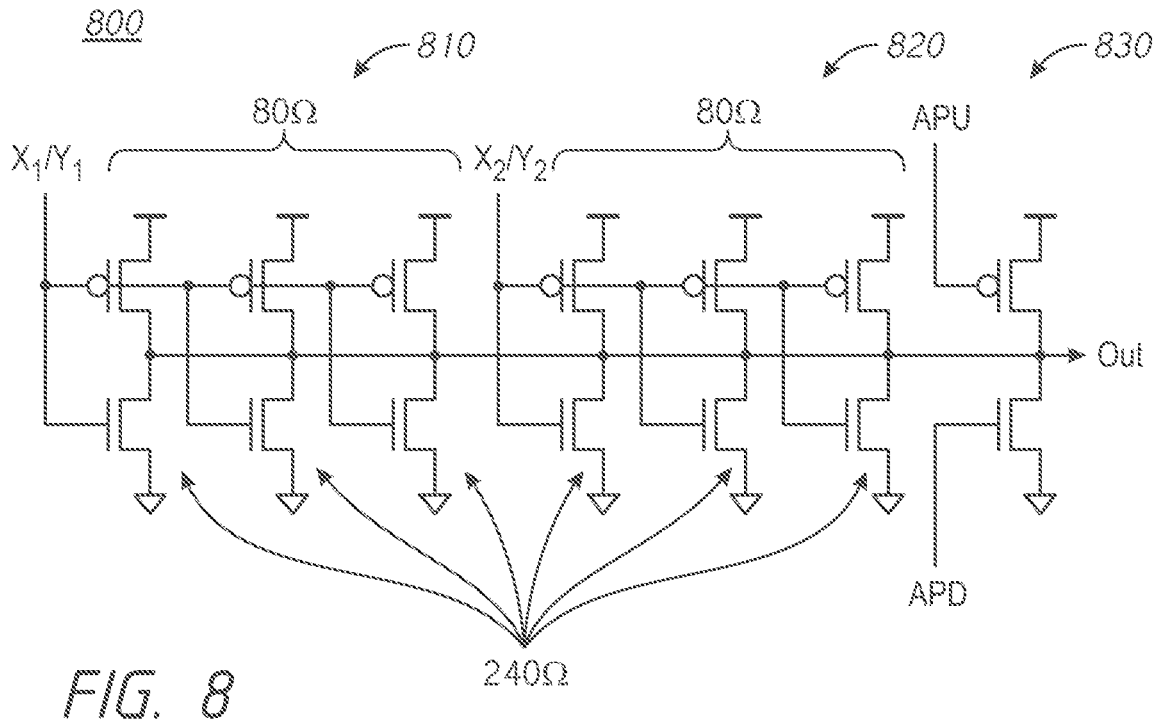


FIG. 8

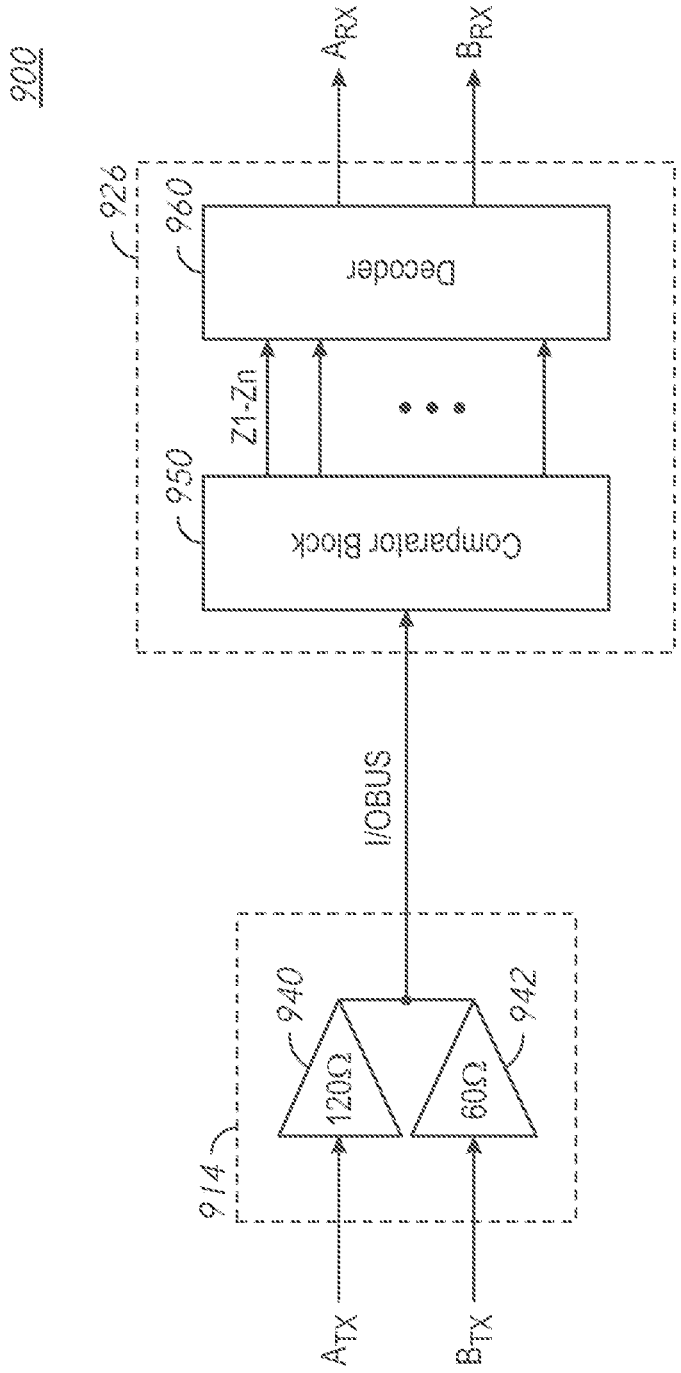

900
926
960
Decoder
Z1-Zn
950
Comparator Block
I/OBUS
940
120Ω
942
60Ω
914
ATX
BTX
ARX
BRX

FIG. 9

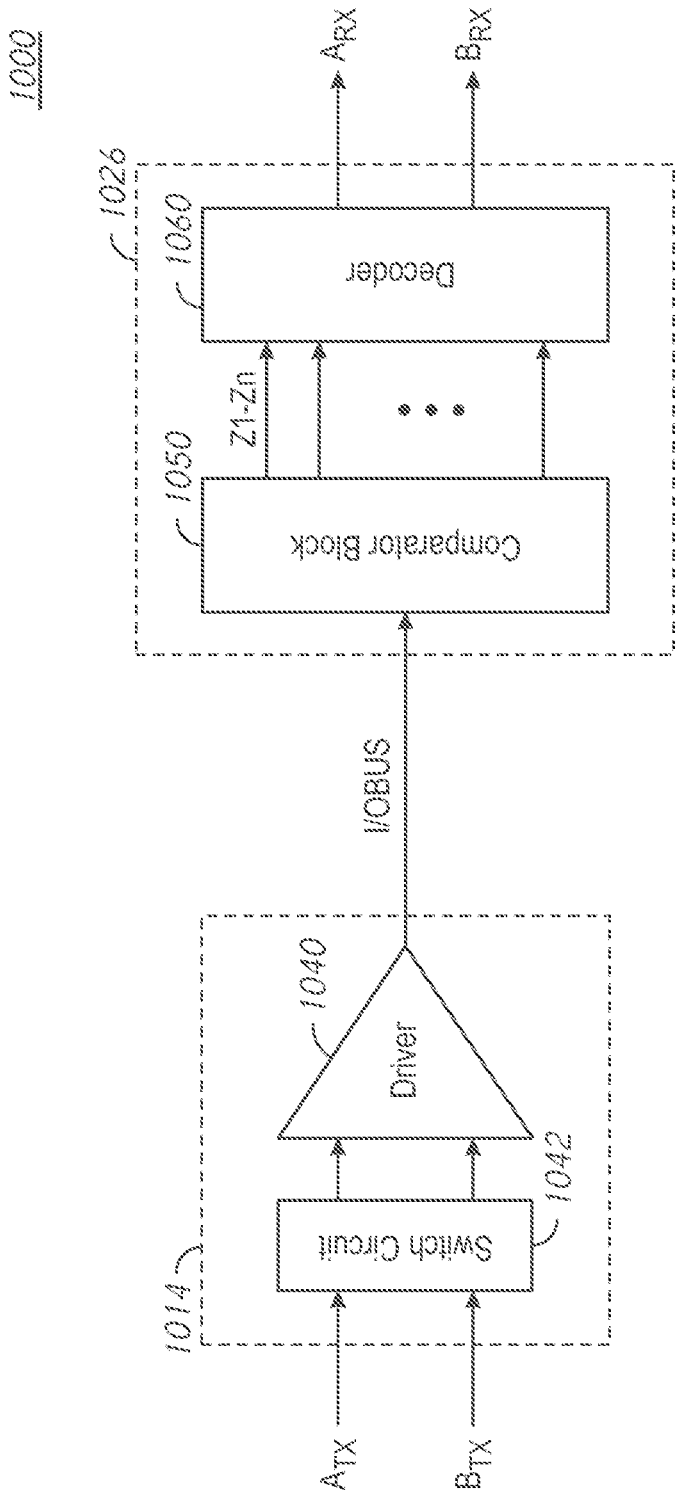

1000
A_{RX}
B_{RX}
1026
1060
Decoder
Z1-Zn
1050
Comparator Block
I/OBUS
1040
Driver
1042
Switch Circuit
1014
A_{TX}
B_{TX}

FIG. 10

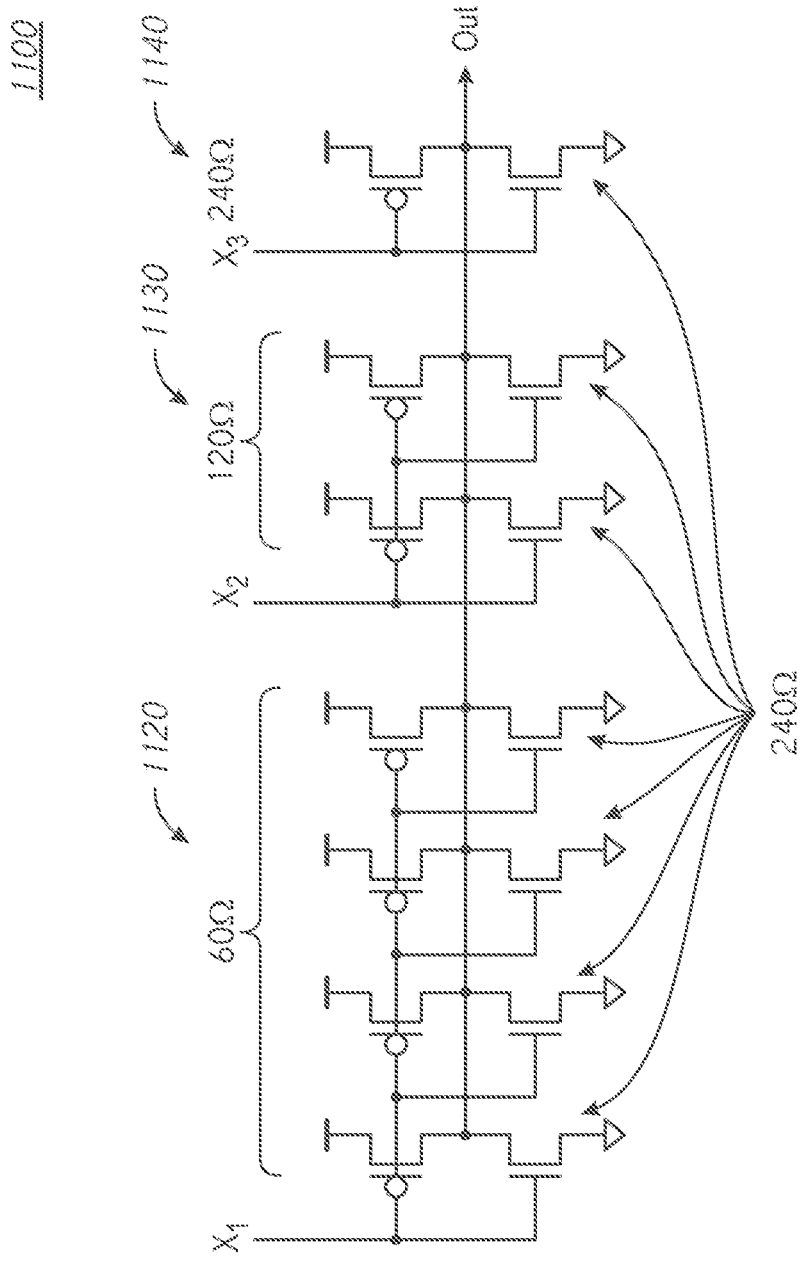


FIG. 11

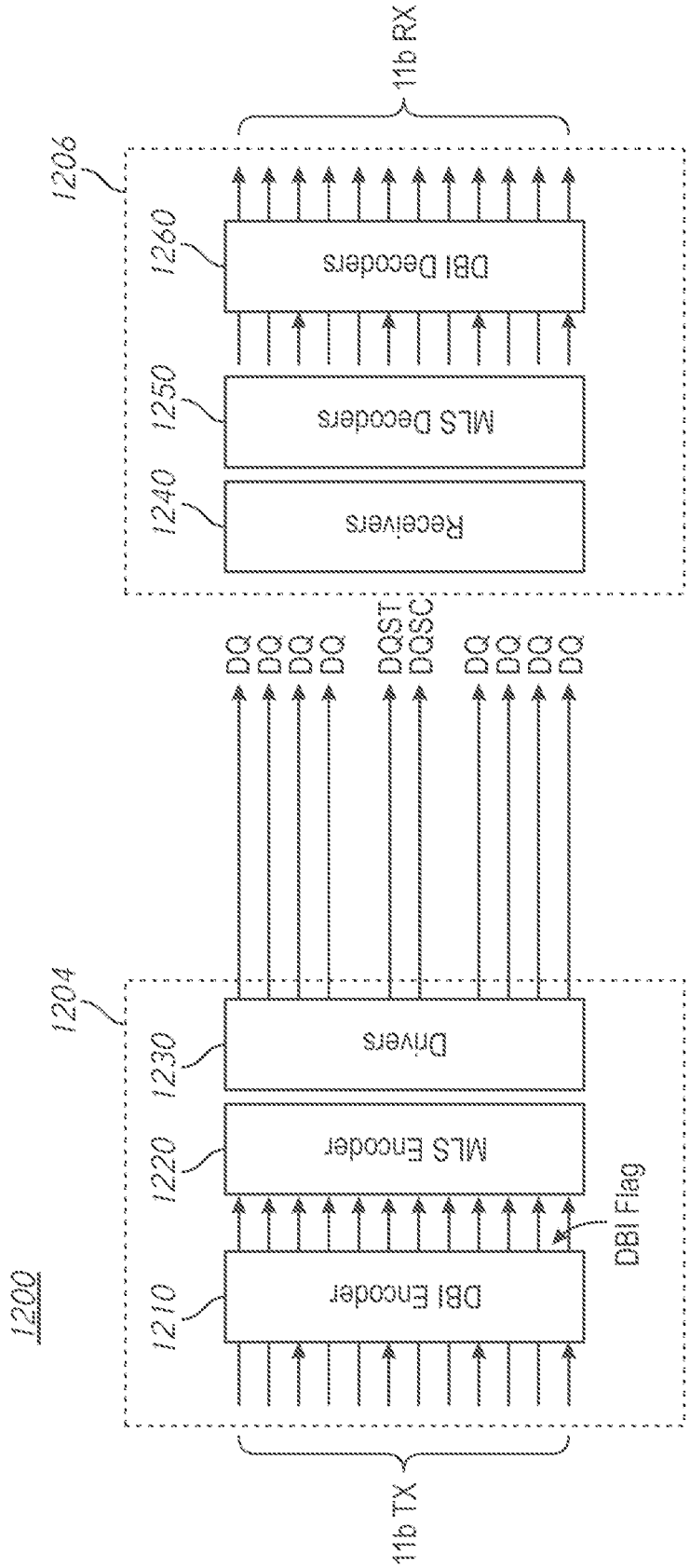

1200
1204
1206
1210
1220
1230
1240
1250
1260
DBI Encoder
MLS Encoder
Drivers
Receivers
MLS Decoders
DBI Decoders
DBI Flag
DQ
DQST
DQSC
11b TX
11b RX

FIG. 12

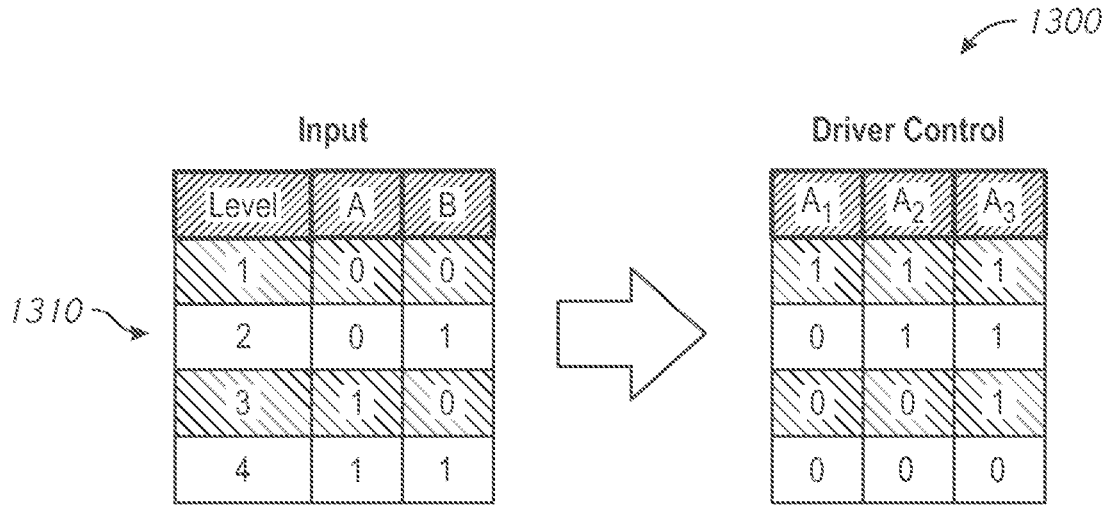


FIG. 13A

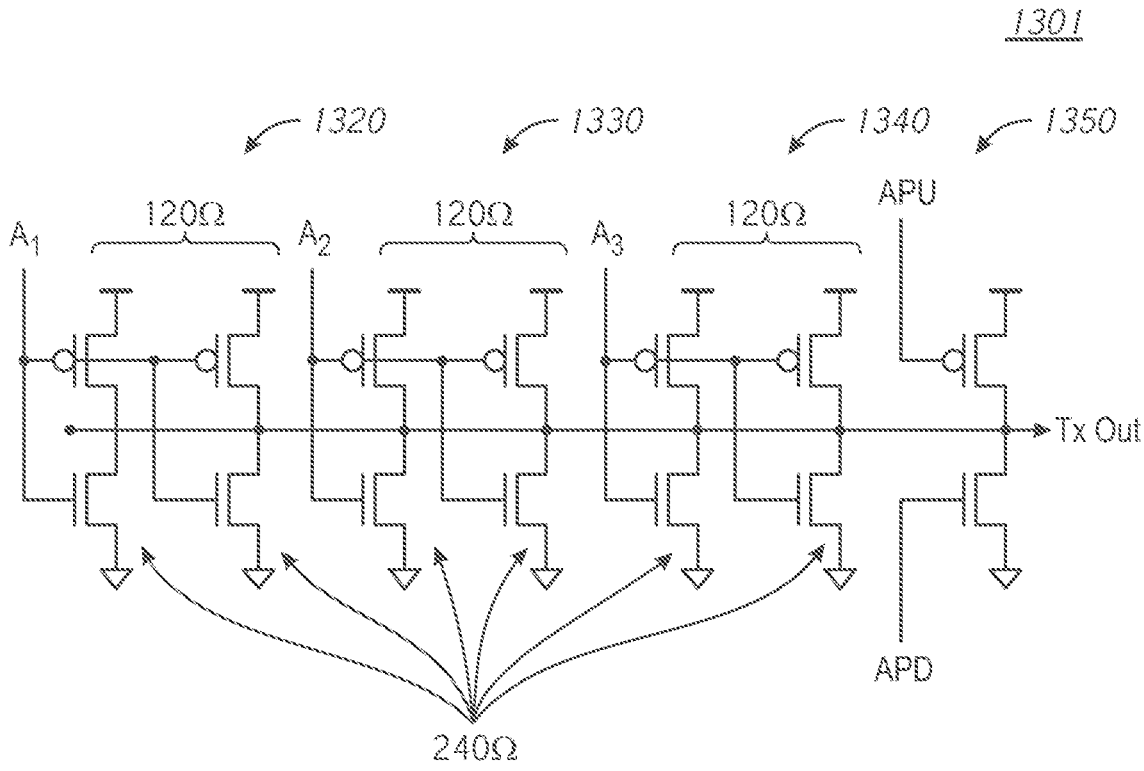


FIG. 13B

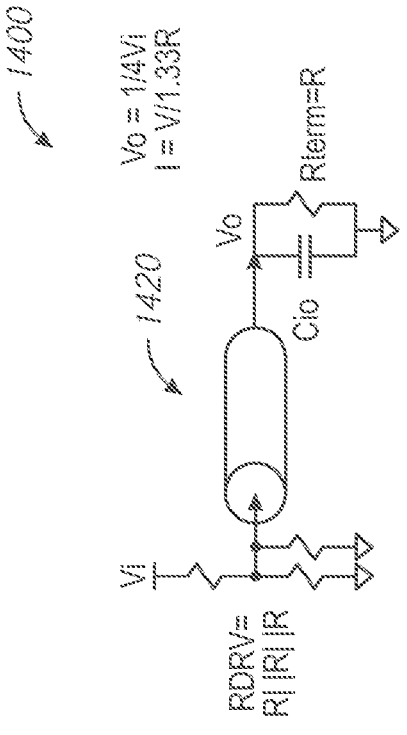


FIG. 14B

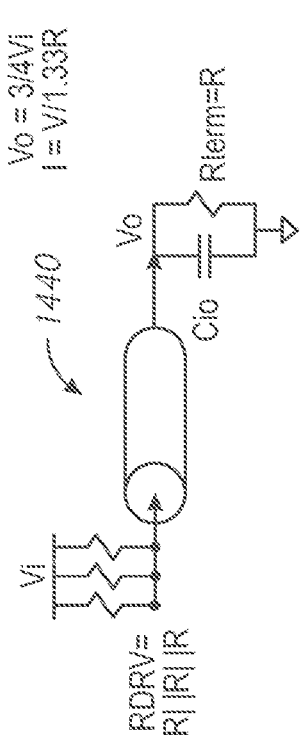


FIG. 14D

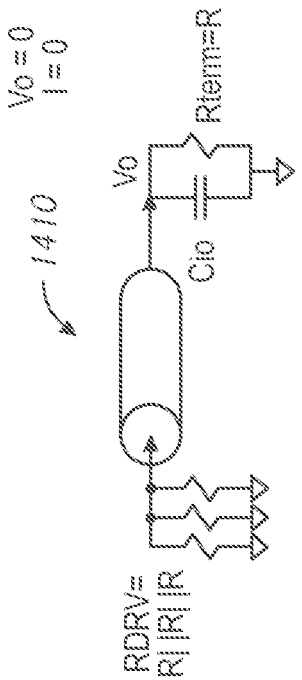


FIG. 14A

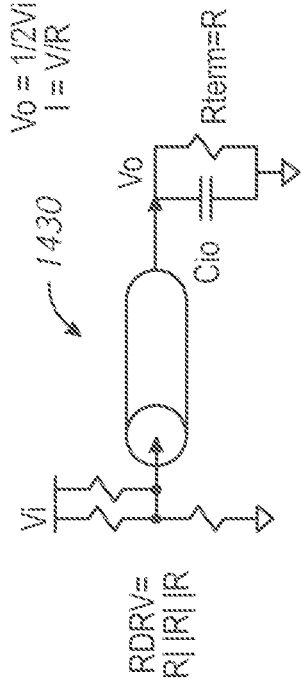


FIG. 14C

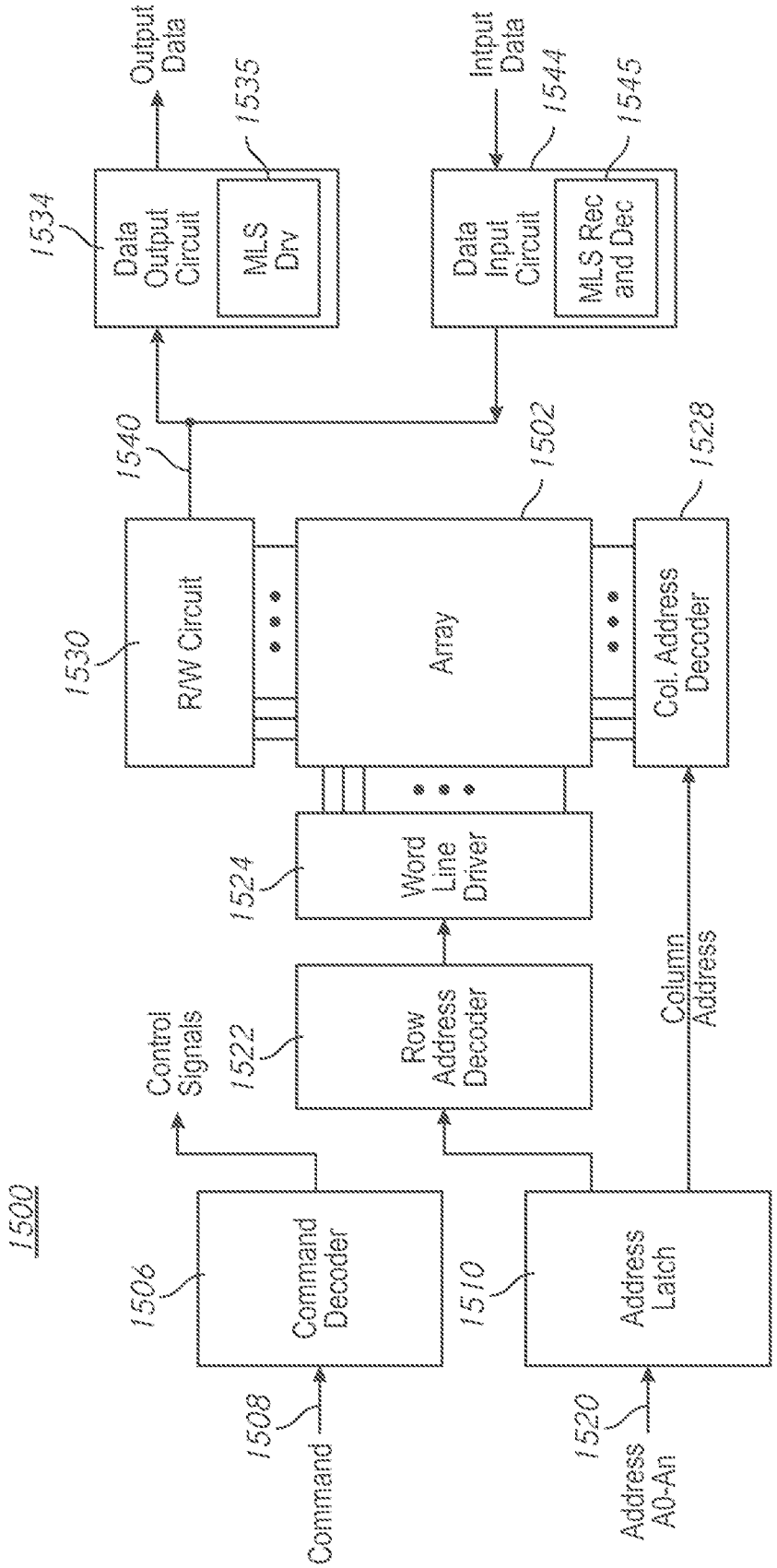

1500
1506
Command Decoder
1508
Command
1510
Address Latch
1520
Address A0-An
Control Signals
1522
Row Address Decoder
1524
Word Line Driver
Column Address
1530
R/W Circuit
Array
1528
Col. Address Decoder
1540
1502
1534
Data Output Circuit
MLS Drv
1535
Output Data
Data Input Circuit
MLS Rec and Dec
1544
1545
Input Data

FIG. 15

APPARATUSES AND METHODS FOR ENCODING AND DECODING OF SIGNAL LINES FOR MULTI-LEVEL COMMUNICATION ARCHITECTURES

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 16/507,292 filed Jul. 10, 2019, which is a continuation of U.S. patent application Ser. No. 15/004,777 filed Jan. 22, 2016 and issued as U.S. Pat. No. 10,365,833 on Jul. 27, 2017. These aforementioned applications and patent are incorporated herein by reference, in their entirety, for any purpose.

BACKGROUND

[0002] The pursuit of making computing systems more powerful and more power efficient has led to advancement in interface communications to improve throughput without increasing, and ideally reducing, energy consumption. Often, as clock speeds increase, a desire to increase data transition times on interface busses to match the faster clock speeds exists. Future double data rate (DDR) dynamic random-access memory (DRAM) performance targets will soon exceed DRAM transistor switching capabilities. Some systems have implemented data encoding and special purpose, multi-level (e.g., more than two levels) bus architectures to increase throughput over an interface bus. However, these special purpose architectures increase cost and complexity, and require additional input/output (I/O) pins.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. **1** is a block diagram of an apparatus according to an embodiment of the present disclosure.

[0004] FIG. **2** is a block diagram of an apparatus for a multilevel communication architecture including a pair of signal lines according to an embodiment of the present disclosure.

[0005] FIGS. **3**A-**3**D are schematic drawings of logic circuits for encoding multilevel signals according to an embodiment of the present disclosure.

[0006] FIGS. **4**A-**4**C are schematic drawings of logic circuits for decoding multilevel signals according to an embodiment of the present disclosure.

[0007] FIG. **5** is an encoding map for encoding three bitstreams on two signal lines that are configured to be driven using a multilevel communication architecture according to an embodiment of the present disclosure.

[0008] FIG. **6** is a schematic diagram of drivers for a multilevel communication architecture according to an embodiment of the present disclosure.

[0009] FIG. **7**A-**7**C are schematic diagrams of an exemplary output of a driver circuit according to an embodiment of the present disclosure.

[0010] FIG. **8** is a schematic diagram of a seven leg driver circuit for a multilevel communication architecture according to an embodiment of the present disclosure.

[0011] FIG. **9** is a block diagram of an apparatus for a multilevel communication architecture according to an embodiment of the present disclosure.

[0012] FIG. **10** is a block diagram of an apparatus for a multilevel communication architecture according to an embodiment of the present disclosure.

[0013] FIG. **11** is a schematic diagram of a seven leg driver circuit for a multilevel communication architecture according to an embodiment of foe present disclosure.

[0014] FIG. **12** is a block diagram of a multilevel communication architecture with data bus inversion system according to an embodiment of the present disclosure.

[0015] FIGS. **13**A and **13**B are an encoding map and a schematic of a seven leg driver circuit for a multilevel communication signal architecture implementing pulse amplitude modulation according to an embodiment of the disclosure.

[0016] FIGS. **14**A-**14**D are schematic diagrams of exemplary outputs of the seven leg driver circuit of FIG. **13**B according to an embodiment of the disclosure.

[0017] FIG. **15** is a block diagram of a portion of a memory according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0018] Certain details are set forth below to provide a sufficient understanding of embodiments of the disclosure. However, it will be clear to one having skill in the art that embodiments of the disclosure may be practiced without these particular details. Moreover, the particular embodiments of the present disclosure described herein are provided by way of example and should not be used to limit the scope of the disclosure to these particular embodiments.

[0019] FIG. **1** is a block diagram of an apparatus **100** according to an embodiment of the present disclosure. The apparatus **100** may include a first device **110** that communicates with a second device **120** over an input/output (I/O) bus. The first device **110** may include an I/O interface circuit **112** that includes driver circuit **114** and receiver and decoder circuit **116** for communication over the I/O bus. The second device **120** may include an I/O interface circuit **122** that includes driver circuit **124** and receiver and decoder circuit **126** for communication over the I/O bus. The I/O bus may support a multi-level communication architecture that includes a plurality of channels. In some embodiments, each channel may be single-ended and may include a single signal line. In other embodiments, each channel may include more than one signal line. In one embodiment, the first device **110**, the second device **120**, and the I/O bus may support a channel that includes conversion of M bitstreams to N multilevel signals, where M is greater than N. A bitstream includes a plurality of bits provided serially, wherein each bit of the bitstream is provided over a period of time. For example, a first bit is provided for a first period, and a second bit is provided for a second period following the first period, and a third bit is provided for a third period following the second period, and so on. The successive bits provided in this serial manner represent a stream of bits. The N multilevel signals may be transmittal over the I/O bus. In one example, 3 bit streams may be converted to 2 tri-level signals. In another example, pulse-amplitude modulation (PAM) may be used to convert 2, 3, or 4 bitstreams into a single multilevel signal having (e.g., 4, 8, 16, etc., levels). In some examples, the first device **110** may include a memory controller or processing system and/or the second device **120** may include a memory, including volatile memory and/or non-volatile memory. In some examples, the second device **120** may include a dynamic random access memory (DRAM), such as a double-data-rate (DDR) DRAM or a low power DDR DRAM. It should be noted, however, that a

memory is not a necessary component of the disclosure. Rather, the disclosure may be applied to any two or more devices, on or off-chip, that communicate with one another using multi-level signaling.

[0020] The driver circuit **114** may include circuitry that applies a bitstream conversion to a set of M bitstreams to generate N multilevel signals and drives the N multilevel signals as channels on the I/O bus. Similarly, the driver circuit **124** may include circuitry that applies a bitstream conversion to a set of M bitstreams to generate N multilevel signals and drives the N multilevel signals as channels on the I/O bus. In some examples, the driver circuit **114** may include modifications to existing DDR drivers to drive the multilevel signals onto the channels of the I/O bus.

[0021] For each channel, the receiver and decoder circuit **116** may include decoders configured to recover the set of M bitstreams by decoding the N multilevel signals received via the channels of the I/O bus as provided by the driver circuit **124**. Further, the receiver and decoder circuit **126** may include decoders configured to recover the set of M bitstreams by decoding the N multilevel signals received via the channels of the I/O bus as provided by the driver circuit **114**. In some embodiments, the receiver and decoder circuit **116** and the receiver and decoder circuit **126** may include comparators and decoding logic to recover the set of M bitstreams.

[0022] In operation, the first device **110** and the second device **120** may communicate over the I/O bus to transfer information, such as data, addresses, commands, etc. While the I/O bus is shown to be bidirectional, the I/O bus may also be a unidirectional bus. The I/O interface circuit **112** and I/O interface circuit **122** may implement a multi-level communication architecture. In a multi-level communication architecture, a symbol is sent over a channel during a symbol period. A symbol may be a single value on a signal line of a channel, or may be a combination of values provided on a plurality of signal lines of a channel. The symbol may represent a channel state. A receiver may determine an output signal value based on the value transmitted on the signal line(s) of a channel. In a single-ended architecture, the signal line value may be compared against one or more reference values to determine the output signal value. A receiver has a time period to determine and latch the output signal value from the time the output signal transitions to the current value to the time the output signal transitions to the next value. The transition time may be determined based on a clock signal, as well as a setup and hold time based on a transition from one value to another. In a multi-level communication architecture with a fixed slew rate or fixed rise/fall times, inherent jitter may occur due to differing magnitude shifts (e.g., from VH to VL vs. from VMID to VH or VL. The amount of jitter may be based on the slew rate, the rise/fall times, the multi-level magnitudes values, or combinations thereof. In some examples, the transition times may also be affected by process, voltage, and temperature variations.

[0023] In an example, the driver circuit **114** may generate a symbol for a channel by converting a bit from each of M bitstreams into N multilevel signals. The symbol may be transmitted to the receiver and decoder circuit **126** via N signal lines of the I/O bus. The receiver and decoder circuit **126** may detect levels on the N signal lines and decode the levels to retrieve the bit from each of the M streams. By using multilevel signal lines, more data can be transmitted during a symbol period as compared with using binary signal line levels. In an example, M is 3 and N is 2, and the signal lines of the I/O bus are capable of being driven to three independent levels. In another example, M is 2 and N is 1, and the signal lines of the I/O bus are capable of being driven to four independent levels (e.g., in a PAM implementation). Communication protocol between the driver circuit **124** and the receiver and decoder circuit **116** maybe similar to the communication protocol between the encoder and driver circuit **114** and the receiver and decoder circuit **126**. The driver circuit **114** may include a DRAM driver that has been segmented to drive multiple (e.g., more than 2) voltage levels on a signal line.

[0024] FIG. **2** is a block diagram of an apparatus **200** for a multilevel communication architecture including a pair of signal lines according to an embodiment of the present disclosure. The apparatus **200** may include a signal driver **214** coupled to a receiver **226** via an I/O bus. The signal driver **214** may be implemented in the driver circuit **114** and/or the driver circuit **124** of FIG. **1** and the receiver **226** may be implemented in the receiver and decoder circuit **116** and/or the receiver and decoder circuit **126** of FIG. **1**.

[0025] The signal driver **214** may include an encoder **230** coupled to a driver **240** and a driver **242**. The encoder **230** may be configured to receive bitstreams ATX, BTX, and CTX. The encoder **230** may encode the ATX, BTX, and CTX to provide X**1**, X**2**, Y**1**, and Y**2** control signals. The driver **240** may receive the X**1** and X**2** control signals and may drive a voltage on an X signal line of the I/O bus based on the X**1** and X**2** control signals. The driver **242** may receive the Y**1** and Y**2** control signals and may drive a voltage on a Y signal line of the I/O bus based on the Y**1** and Y**2** control signals. Thus, the signal driver **214** may convert ATX, BTX, and CTX bitstreams into two multilevel signals to be driven over the I/O bus.

[0026] The receiver **226** may include comparators **250**, **252**, **254**, and **256** coupled to a decoder **260**. The comparators **250** and **252** may be configured to receive the signal from the X signal line of the I/O bus and the comparators **254** and **256** may be configured to receive the signal from the Y signal line of the I/O bus. The comparator **250** may compare the signal of the X signal line to a high reference signal HIREF to provide a Z**1** signal to the decoder **260**. The comparator **252** may compare the signal of the X signal line to a low reference signal LOREF to provide a Z**2** signal to the decoder **260**. The comparator **254** may compare the signal of the Y signal line to the HIREF signal to provide a Z**3** signal to the decoder **260**. The comparator **254** may compare the signal of the Y signal line to the LOREF signal to provide a Z**4** signal to the decoder **260**. The decoder **260** may include logic to generate ARX, BRX, and CRX bitstreams based on the Z**1**, Z**2**, Z**3**, and Z**4** signals from the comparators **250**, **252**, **254**, and **256**, respectively. The ARX, BRX, and CRX signals may be logical equivalents of data transmitted by the ATX, BTX, and CTX signals.

[0027] In operation, the ATX, BTX, and CTX signals may be three bitstreams to be transmitted over the I/O bus. Rather than send each bitstream on a separate signal line, the signal driver **214** may encode the ATX, BTX, and CTX signals to be transmitted over two signal lines using multilevel signals. For example, the encoder **230** may receive the ATX, BTX, and CTX signals, and during each symbol period, may encode a symbol in the form of the X**1**, X**2**, Y**1**, and Y**2** control signals to control the drivers to drive the pair of

signal lines of the I/O bus to respective voltages. While the embodiment illustrated in FIG. **2** is provided the three bitstreams ATX, BTX, and CTX, which are merged through encoding, in other embodiments one bit stream may be provided and three sequential bits may be provided as three bits of data for encoding. For example, every third bit of data from the bitstream may be provided as a first bit of data, every third bit of data of a following bit may be provided as a second bit of data, and every third bit of a yet another following bit may be provided as a third bit of data to provide three bits of data for encoding from one bitstream.

[0028] The encoder **230** may include control logic to provide each of the X**1**, X**2**, Y**1**, and Y**2** control signals. FIG. **3** depicts exemplary logic **300** that may be implemented in the encoder **230** to provide the X**1**, X**2**, Y**1**, and Y**2** control signals. For example, the logic **300** may include an X**1** logic circuit **302** may be used to provide the X**1** control signal. The X**1** logic circuit **302** may include a AND gate **310** that is configured to logically AND together the B and C signals and an OR gate **312** that is configured to logically OR the A signal with the output of the AND gate **310** to provide the X**1** control signal.

[0029] Further, the logic **300** may further include an X**2** logic circuit **304** may be used to provide the X**2** control signal. The X**2** logic circuit **304** may include an OR gate **330** configured to logically OR the B and C signals and a NAND **332** to logically NAND the A signal with the output of the OR gate **330** to provide the X**2** control signal.

[0030] The logic **300** may include a Y**1** logic circuit **306** may be used to provide the Y**1** control signal. The Y**1** logic circuit **306** may include a AND gate **320** configured to logically AND the A signal and an inverted C signal (via an inverter **322**) and an OR gate **324** configured to logically OR the B and C signals. The Y**1** logic circuit **306** may further include an OR gate **328** configured to logically OR the output of the AND gate **320** with an inverted (e.g., via an inverter **326**) output of the OR gate **324** to provide the Y**1** control signal.

[0031] The logic **300** may additionally include a Y**2** logic circuit **308** may be used to provide the Y**2** control signal. The Y**2** logic circuit **308** may include an AND gate **340** that is configured to logically AND together the A signal with an inverted (e.g., via inverter **342**) B signal and a OR gate **346** that is configured to logically OR the output of the AND gate **340** with an inverted (e.g., via inverter **344**) C signal to provide the Y**2** control signal.

[0032] Turning back to FIG. **2**, the driver **240** may drive a voltage on the X signal line of the I/O bus responsive to the X**1** and X**2** control signals. The driver **242** may drive a voltage on the Y signal line of the I/O bus responsive to the Y**1** and Y**2** control signals. The voltages driven by the driver **240** and driver **242** may be one of three levels.

[0033] The comparators **250** and **252** may receive the voltage from the X signal line, and the comparators **254** and **256** may receive the voltage from the Y signal line. The comparator **250** may provide the Z**1** signal based on the comparison between the voltage of the X signal line with the REFHI voltage. The comparator **252** may provide the Z**2** signal based on the comparison between the voltage of the X signal line with the REFLO voltage. The comparator **254** may provide the Z**3** signal based on the comparison between the voltage of the Y signal line with the REFHI voltage. The comparator **256** may provide the Z**4** signal based on the comparison between the voltage of the X signal line with the REFHI voltage. The decoder **260** may include decoding logic to generate ARX, BRX, and CRX signals based on the Z**1**, Z**2**, Z**3**, and Z**4** signals. FIG. **4** depicts exemplary logic **400** that may be implemented in the decoder **260** to provide the ARX, BRX, and CRX control signals. For example, the logic **400** may include an ARX logic circuit **420** that is configured to provide the ARX signal. The ARX logic circuit **420** may include a AND gate **426** and a AND gate **428** coupled in parallel. The AND gate **426** may be configured to logically AND together the Z**2** signal, an inverted (via inverter **422**) Z**3** signal, and an inverted (via inverter **424**) Z**4** signal. The AND gate **428** may be configured to logically AND the Z**1**, Z**2**, and Z**4** signals. The ARX logic circuit **420** may further include an OR gate **430** configured to logically OR the output of the AND gate **426** with the output of the AND gate **428** to provide the ARX signal.

[0034] The logic **400** may further include a BRX logic circuit **440** that is configured to provide the BRX signal. The BRX logic circuit **440** may include a AND gate **448**, a AND gate **454**, and an OR gate **458** coupled in parallel. The AND gate **448** may be configured to logically AND together an inverted (via inverter **442**) Z**1** signal, an inverted (via inverter **444**) Z**2** signal, an inverted (via inverter **4446**) Z**3** signal, and the Z**4** signal. The AND gate **454** may be configured to logically AND the Z**1** signal, the Z**2** signal, an inverted (via inverter **450**) Z**3** signal, and an inverted (via inverter **452**) Z**4** signal. The AND gate **456** may be configured to logically AND the Z**2**, Z**3**, and Z**4** signals. The BRX logic circuit **440** may further include an OR gate **458** configured to logically OR the output of the AND gate **448**, the AND gate **454**, and the AND gate **456** to provide the BRX signal.

[0035] The logic **400** may further include a CRX logic circuit **460** that is configured to provide the CRX signal. The CRX logic circuit **460** may include a AND gate **464** and a AND gate **466** coupled in parallel. The AND gate **464** may be configured to logically AND together an inverted (via inverter **462**) Z**1** signal, the Z**3** signal, and the Z**4** signal. The AND gate **466** may be configured to logically AND the Z**1**, Z**2**, and Z**4** signals. The CRX logic circuit **460** may further include an OR gate **468** configured to logically OR the output of the AND gate **464** with the output of the AND gate **466** to provide the CRX signal.

[0036] Turning back to FIG. **2**, the ARX, BRX, and CRX signals may be provided to downstream circuitry for processing, such as being processed as data to be stored at a memory or as data that has been retrieved from a memory, or as commands or addresses to be decoded and used to perform memory access operations. While FIG. **2** depicts an apparatus **200** that encodes three bitstreams to be transmitted over two multilevel signal lines of an I/O bus, the apparatus **200** may be altered to include additional or less bitstreams, more or less than two signal lines, and an ability to drive more than three voltage levels on each signal line.

[0037] FIG. **5** is an encoding map **500** for encoding three bitstreams on two signal lines that are configured to be driven using a multilevel communication architecture according to an embodiment of the present disclosure. The encoding map **500** maybe used by the encoder **230** of FIG. **2** to encode the ATX, BTX, and CTX bitstreams to multilevel signals to be driven over the X and Y signal lines of the I/O bus via the driver **240** and the driver **242**, respectively. The encoding map **500** includes a first table **510** including possible logical combinations of A, B, and C signals and a

second table **520** that includes exemplary unique multilevel encoding of X and Y signal lines for each logical combination of the A, B, and C signal. For example, when the A, B, and C bitstreams each have a logical value of zero (e.g., line **1** of the first table **510**), the X and Y signals may be driven to a low voltage. In another example, if the A bitstream has a logical value of zero and the B and C bitstreams have a logical value of one, the X signal may be driven to a middle voltage and Y signal may be driven to a high voltage. It will be appreciated that different mapping may be implemented to encode the A, B, and C signals on the X and Y signals, so long as each unique logical combination of the A, B, and C signals maps to a unique voltage combination on the X and Y signals. For example, the A, B, and C bitstreams having logical values of zero may map to the X and Y signals having high voltages, rather than low voltages, and the A, B, and C bitstreams having logical values of one may map to the X and Y signals having low voltages, rather than high voltages.

[0038] FIG. **6** is a schematic diagram of drivers **600** for a multilevel communication architecture according to an embodiment of the present disclosure. The drivers **600** may include an X signal line driver **610** configured to drive an XOUT signal to an X signal line based on X**1** and X**2** control signals and a Y signal line driver **620** configured to drive the YOUT signal to a Y signal line based on Y**1** and Y**2** control signals. The X signal line driver **610** may be implemented in the **114** and/or the **124** of FIG. **1** and/or the driver **240** of FIG. **2**. The Y signal line driver **620** may be implemented in the **114** and/or the **124** of FIG. **1** and/or the driver **242** of FIG. **2**.

[0039] The X signal line driver **610** may include an X**1** signal line driver **612** and an X**2** signal line driver **614** coupled in parallel between a high supply voltage and a low supply voltage. The X**1** signal line driver **612** may be configured to drive a voltage on the XOUT signal responsive to the X**1** control signal. For example, the X**1** signal line driver **612** may drive the XOUT signal to a high voltage responsive via a pull up (e.g., p-type) transistor responsive to the X**1** control signal having a low logical value and may drive the XOUT signal to a low voltage via a pull clown (e.g., n-type) transistor responsive to the X**1** control signal having a high logical value. Likewise, the X**2** signal line driver **614** may be configured to drive the voltage on the XOUT signal responsive to the X**2** control signal. For example, the X**2** signal line driver **614** may drive the XOUT signal to a high voltage via a pull up transistor responsive to the X**2** control signal having a low logical value and may drive the XOUT signal to a low voltage via the pull down transistor responsive to the X**2** control signal having a high logical value. The combination of the X**1** signal line driver **612** and the X**2** signal line driver **614** may drive the XOUT signal to three logical voltage values, e.g., low, mid and high. For example, when both the X**1** signal line driver **612** and the X**2** signal line driver **614** are driving the XOUT to a high voltage, the XOUT signal may have a high voltage. When both the X**1** signal line driver **612** and the X**2** signal line driver **614** are driving the XOUT to a low voltage, the XOUT signal may have a low voltage. When one of the X**1** signal line driver **612** or the X**2** signal line driver **614** am driving the XOUT to a high voltage and the other of the X**1** signal line driver **612** or the X**2** signal line driver **614** are driving the XOUT to a low voltage, the XOUT signal may have a mid voltage level.

[0040] The Y signal line driver **620** may include a Y**1** signal line driver **622** and a Y**2** signal line driver **624** coupled in parallel between the high supply voltage and the low supply voltage. The Y**1** signal line driver **622** may be configured to drive a voltage on the YOUT signal responsive to the Y**1** control signal. For example, the Y**1** signal line driver **622** may drive the YOUT signal to a high voltage via a pull up transistor responsive to the Y**1** control signal having a low logical value and may drive the YOUT signal to a low voltage via a pull down transistor responsive to the Y**1** control signal having a high logical value. Likewise, the Y**2** signal line driver **624** may be configured to drive the voltage on the YOUT signal responsive to the Y**2** control signal. For example, the Y**2** signal line driver **624** may drive the YOUT signal to a high voltage via a pull up transistor responsive to the Y**2** control signal having a low logical value and may drive the YOUT signal to a low voltage via a pull down transistor responsive to the Y**2** control signal having a high logical value. Similar to operation of the X signal line driver **610**, the combination of the Y**1** signal line driver **622** and the Y**2** signal line driver **624** may drive the YOUT signal to three logical voltage values, e.g., low, mid and high.

[0041] In operation, the X signal line driver **610** and the Y signal line driver **620** may drive one of three voltages to the XOUT and YOUT signals, respectively. The X signal line driver **610** may drive the XOUT signal responsive to the X**1** and X**2** control signals, and the Y signal line driver **620** may drive the YOUT signal responsive to the Y**1** and Y**2** control signals. In an example, when the X**1** control signal has a low logical value, the pull up transistor of the X**1** signal line driver **612** is enabled to couple the high supply voltage to the XOUT signal and pull down transistor is disabled. When the X**1** control signal has a high logical value, the pull up transistor of the X**1** signal line driver **612** is disabled and the pull down transistor is enabled to couple the low supply voltage to the XOUT signal. Operation of the X**2** signal line driver **614**, the Y**1** signal line driver **622**, and the Y**2** signal line driver **624** responsive to the X**2**, Y**1**, and Y**2** control signals, respectively, may be similar to the X**1** signal line driver **612** responsive to the X**1** control signal. The XOUT signal may be a combination of the voltages driven by the X**1** signal line driver **612** and the X**2** signal line driver **614**. The YOUT signal may be a combination of the voltages driven by the Y**1** signal line driver **622** and the Y**2** signal line driver **624**. The XOUT and YOUT signals may have a high voltage VH, a low voltage VL, or a middle voltage VMID between the high supply and low supply voltages. The middle voltage may be achieved when the X**1** signal line driver **612** (or the Y**1** signal line driver **622**) and the X**2** signal line driver **614** (or the Y**2** signal line driver **624**) are driving different voltages (e.g., one driving the high supply voltage and the other driving the low supply voltage).

[0042] FIGS. **7**A-**7**C depict schematic diagrams of exemplary output of a driver circuit, such as one of the X signal line driver **610** or the Y signal line driver **620** of FIG. **6**, according to an embodiment of the disclosure. For example, as illustrated in FIG. **7**A, the low voltage signal representation **710** may represent driving the VL voltage (e.g., when both the X**1** signal line driver **612** and the X**2** signal line driver **614** are driving the low supply voltage or when both the Y**1** signal line driver **622** and the Y**2** signal line driver **624** are driving the low supply voltage). In this case, the

output voltage VO received over the signal line maybe a low voltage. The RDRV may represent the inherent resistance of the pull down transistors.

[0043] As illustrated in FIG. **7**B. the mid voltage signal representation **720** may represent driving the middle voltage (e.g., when one of the X**1** signal line driver **612** or the X**2** signal line driver **614** is driving the low supply voltage and the other is driving the high supply voltage or when one of the Y**1** signal line driver **622** and the Y**2** signal line driver **624** is driving the low supply voltage and the other is driving the high supply voltage). In this case, the VO voltage received over the signal fine may be ⅓ of the high supply voltage. The RDRV may represent the inherent resistance of the pull up and pull down transistor.

[0044] The high voltage signal representation **730** of FIG. **7**C may represent driving the VH voltage (e.g., when both the X**1** signal line driver **612** and the X**2** signal line driver **614** are driving the high supply voltage or when both the Y**1** signal line driver **622** and the Y**2** signal line driver **624** are driving the high supply voltage). In this case, the VO voltage received over the signal line may be ⅔ of the high supply voltage. The RDRV may represent the inherent resistance of the pull up transistors. It will be appreciated that, the specific voltage levels described in the previous example are applicable when the pull-up and pull-down and termination resistances are equal. In some embodiments where the termination resistances are not equal, the overall swing will change, but the relative position of the various voltage levels will be maintained. Further, were the termination resistance coupled to a high supply voltage, then the signal levels would be different voltage values, but maintain the same relative positions. Additionally, if the termination resistance were disabled, VH would be equal to the high supply voltage and VL would be equal to the low supply voltage.

[0045] FIG. **8** is a schematic diagram of a seven leg driver circuit **800** for multilevel communication architecture according to an embodiment of the present disclosure. The seven leg driver circuit **800** may be a driver in a DRAM, such as a double data rate (DDR) DRAM driver. The seven leg driver circuit **800** may include seven signal line drivers (e.g., "legs"). In some embodiments, each of the signal line drivers has an impedance of 240 ohms. The seven leg driver circuit **800** may include a first driver section **810** and a second driver section **820** configured to drive an output signal OUT to a signal line based on X**1** and X**2** control signals. The seven leg driver circuit **800** may further include an adjustment driver section **830** that is configured to adjust a voltage of the OUT signal, when, for example, the OUT signal is biased to one voltage or another due to leakage. The adjustment driver section **830** is optional, and is not included in some embodiments. In other embodiments, however, a seventh leg configured as a signal line driver may be included to provide additional signal levels for a multilevel output signal, as will be described in more detail below. The seven leg driver circuit **800** may be implemented in the encoder and driver circuit **114** and/or the encoder and driver circuit **124** of FIG. **1**, the driver **240** of FIG. **2**, and/or the X signal line driver **610** and/or the Y signal line driver **620** of FIG. **6**.

[0046] The first driver section **810** may include three legs, each controlled responsive to the X**1** control signal. Each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor. Similarly, the second driver section **820** may include three legs, each controlled responsive to the X**2** control signal, and each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor. The adjustment driver section **830** may include a single leg with a pull up transistor controlled responsive to an adjust pull up signal APU and a pull down transistor controlled responsive to an adjust pull down signal APD. In an embodiment where each leg has an impedance of 240 ohms, the first driver section **810** has an effective impedance of 80 ohms and the second driver section **820** has an effective impedance of 80 ohms. It should be appreciated that no more than one PU and one PD are required to implement the tri-level signaling scheme. The seven leg embodiment discussed herein is discussed in the context of providing an embodiment for use with common JEDEC DDR architectures. However, driver circuits other than that shown and described with reference to FIG. **8** may be used in alternative embodiments.

[0047] In operation, the seven leg driver circuit **800** may drive the OUT signal responsive to the X**1** and X**2** control signals. In an example, when the X**1** control signal has a low logical value, the pull up transistors of the first driver section **810** are enabled to couple the high supply voltage to the XOUT signal and pull down transistors are disabled. When the X**1** control signal has a high logical value, the pull up transistors of the first driver section **810** are disabled and the pull down transistors are enabled to couple the low supply voltage to the OUT signal. Operation of the second driver section **820** responsive to the X**2** control signal, respectively, may operate similar to the first driver section **810** responsive to the X**1** control signal. The OUT signal may be a combination of the voltages driven by the first driver section **810** and the second driver section **820**. The OUT signal may have a VH voltage, a VL voltage, or a middle voltage between the high supply and low supply voltages. The middle voltage may be achieved when the first driver section **810** and the second driver section **820** are driving different voltages (e.g., one driving the high supply voltage and the other driving the low supply voltage).

[0048] The adjustment driver section **830** may compensate for drive strength differences between the first driver section **810** and the second driver section **820**. For example, the adjustment driver section **830** may pull the voltage of the OUT signal slightly up or down if the combination of the first driver section **810** and the second driver section **820** are not able to drive the OUT signal to a proper voltage. The APU signal may pull the OUT signal slightly up when having an active low value and the APD signal may pull the OUT signal slightly down when having an active high value.

[0049] FIG. **9** is a block diagram of an apparatus **900** for a multilevel communication architecture according to an embodiment of the present disclosure. The apparatus **900** may include a signal driver **914** coupled to a receiver **926** via an I/O bus. The signal driver **914** may be implemented in the driver circuit **114** and/or the driver circuit **124** of FIG. **1** and the receiver **926** may be implemented in the receiver and decoder circuit **116** and/or the receiver and decoder circuit **126** of FIG. **1**.

[0050] The signal driver **914** may include a driver circuit **940** and a driver circuit **942**. In some embodiments, the driver circuit **940** has an impedance that is twice an impedance of the driver circuit **942**. For example, in an embodiment the driver circuit **940** has an impedance of **120** ohms and the driver **942** has an impedance of 60 ohms. The driver circuit **940** may receive bitstream ATX and drive an output

signal in response, and the driver circuit **942** may receive bitstream BTX and drive an output signal in response. The output signal driven by the driver circuit **940** is combined with the output signal driven by the driver circuit **942** to provide a signal to the I/O bus based on the ATX and BTX bitstreams. For example, the signal may be a multilevel signal representing data of the ATX and BTX bitstreams. In some embodiments, the driver circuits **940** and **942** may each be a signal line driver having a pull-up (e.g., p-type) transistor coupled in series with a pull down (e.g., n-type) transistor. A source of the pull-up transistor is coupled to a high supply voltage and the source of the pull-down transistor is coupled to a low supply voltage. Gates of the pull-up and pull-down transistors of the driver circuit **940** are provided with the A TX bitstream and gates of the pull-up and pull-down transistors of the driver circuit **942** are provided with the BTX bitstream. In other embodiments, the driver circuits **940** and **942** may be implemented using other configurations. In contrast to the signal driver **214** of FIG. **2**, the signal driver **914** does not include an encoder. The ATX and BTX signals are provided to the driver circuits **940** and **942** without encoding to provide a signal to the I/O bus.

[0051] The receiver **926** may include comparator block **950** coupled to a decoder **960**. The comparator **950** may be configured to receive the signal from the I/O bus and provide Z**1**-Zn signals (n is a whole number) to the decoder **960**. The comparator block **950** may include circuits (not shown in FIG. **9**) configured to compare the signal from the I/O bus against reference signals to provide the Z**1**-Zn signals. For example, the comparator block **950** may include comparators that compare the signal from the I/O bus against various reference signals to provide the Z**1**-Zn signals. The decoder **260** may include logic to generate the bitstreams ARX and BRX based on the Z**1**-Zn signals from the comparator block **950**. The ARX and BRX signals may be logical equivalents of data transmittal by the ATX and BTX signals.

[0052] In operation, the ATX and BTX signals may be bitstreams to be transmitted over the I/O bus. Rather than send each bitstream on a separate signal line, the signal driver **914** may provide a signal based on the ATX and BTX signals to be transmitted over a signal line using a multilevel signal. For example, the signal driver **914** may receive the ATX and BTX signals, and during each symbol period, the driver circuits **940** and **942** may drive the signal line of the I/O bus with a voltage that will be used by the receiver **926** to provide the ARX and BRX signals. The relative impedances of the driver circuits **940** and **942** result in a combined signal that may be used to represent data of the ATX and BTX bitstreams using fewer signal lines than one signal line per bitstream. For example, as in the embodiment of FIG. **9**, data of the ATX and BTX bitstreams are provided to the receiver **926** on fewer than two signal lines (e.g., one signal on the I/O bus rather than one signal line for the ATX bitstream and another signal line for the BTX bitstream). Although FIG. **9** illustrates operation with bitstreams ATX and BTX for providing bitstreams ARX and BRX, the number of bit streams may be different in other embodiments of the invention. For example, in some embodiments, a bitstream CTX may also be provided to the signal driver **914** in addition to the ATX and BTX bitstreams, a multilevel signal may be provided over the I/O bus representing the data from the ATX, BTX, and CTX bitstreams. Such embodiments are within the scope of the present invention.

[0053] FIG. **10** is a block diagram of an apparatus **1000** for a multilevel communication architecture according to an embodiment of the present disclosure. The apparatus **1000** may include a signal driver **1014** coupled to a receiver **1026** via an I/O bus. The signal driver **1014** may be implemented in the driver circuit **114** and/or the driver circuit **124** of FIG. **1** and the receiver **1026** may be implemented in the receiver and decoder circuit **116** and/or the receiver and decoder circuit **126** of FIG. **1**.

[0054] The signal driver **1014** may include a driver circuit **1040** and a switch circuit **1042**. The switch circuit **1042** may receive bitstream ATX and bitstream BTX and provide the ATX and BTX bitstreams to the driver circuit **1040**. The switch circuit **1042** is provided a control signal SWCTL that controls the routing of the ATX and BTX signals to circuits of the driver circuit **1040**. In some embodiments, the SWCTL signal may be provided by a command decoder. In other embodiments, the SWCTL signal may be provided by programmable elements that are programmed to set the routing of the ATX and BTX signals to the driver circuit **1040**. The switch circuit may include multiplexer circuits in some embodiments that are configured to provide the ATX and BTX bitstreams to the driver circuit **1040**. In response to the ATX and BTX bitstreams, the driver circuit **1040** may drive an output signal to the I/O bus that is based on the ATX and BTX bitstreams. For example, the signal may be a multilevel signal representing data of the ATX and BTX bitstreams. In some embodiments, the driver circuit **1040** may include a plurality of signal line drivers. In contrast to the signal driver **214** of FIG. **2**, the signal driver **1014** does not include an encoder. The ATX and BTX signals are provided to the driver circuit **1040** (through the switch circuit **1042**) without encoding to provide a signal to the I/O bus.

[0055] The receiver **1026** may include comparator block **1050** coupled to a decoder **1060**. The comparator **1050** may be configured to receive the signal from the I/O bus and provide Z**1**-Zn signals to the decoder **1060**. The comparator block **1050** may include circuits (not shown in FIG. **10**) configured to compare the signal from the I/O bus against reference signals to provide the Z**1**-Zn signals. For example, the comparator block **1050** may include comparators that compare the signal from the I/O bus against various reference signals to provide the Z**1**-Zn signals. The decoder **1060** may include logic to generate the bitstreams ARX and BRX based on the Z**1**-Zn signals from the comparator block **1050**. The ARX and BRX signals may be logical equivalents of data transmitted by the ATX and BTX signals.

[0056] In operation, the ATX and BTX signals may be bitstreams to be transmitted over the I/O bus. Rather than send each bitstream on a separate signal line, the signal driver **1014** may provide a signal based on the ATX and BTX signals to be transmitted over a signal line using a multilevel signal. For example, the signal driver **1014** may receive the ATX and BTX signals, and during each symbol period, the driver circuit **1040** may drive the signal line of the I/O bus with a voltage that will be used by the receiver **1026** to provide the ARX and BRX signals. As will be described in more detail below, the signal provided by the signal driver **1014** may be used to represent data of the ATX and BTX bitstreams using fewer signal lines than one signal line per bitstream. For example, as in the embodiment of FIG. **10**, data of the ATX and BTX bitstreams are provided to the receiver **1026** on fewer than two signal lines (e.g., one

signal on the I/O bus rather than one signal line for the ATX bitstream and another signal line for the BTX bitstream). Although FIG. **10** illustrates operation with bitstreams ATX and BTX and tor providing bitstreams ARX and BRX, the number of bit streams may be different in other embodiments of the invention. For example, in some embodiments, a bitstream CTX may also be provided to the signal driver **1014** in addition to the ATX and BTX bitstreams, a multilevel signal may be provided over the I/O bus representing the data of the ATX, BTX, and CTX bitstreams. Such embodiments are within the scope of the present invention.

[0057] FIG. **11** is a schematic drawing of a seven leg driver circuit **1100** for a multilevel signal architecture implementing pulse-amplitude modulation (PAM) according to an embodiment of the disclosure. The seven leg driver circuit **1100** may be a driver in a DRAM, such as a double data rate (DDR) DRAM driver. The seven leg driver circuit **1100** may include seven signal line drivers (e.g., "legs"). In some embodiments, each of the signal line drivers has an impedance of 240 ohms. The seven leg driver circuit **1100** may include a first driver section **1120**, a second driver section **1130**, and a third driver section **1140** configured to drive an output signal OUT to a signal line based on ATX and BTX signals, which may be provided to the legs of the driver circuit **1100** by a switch circuit, for example, the switch circuit **1042** (FIG. **10**). The output signal OUT may be a multilevel signal representing data of the ATX and BTX bitstreams that drives the I/O bus. The seven leg driver circuit **1100** may be implemented in the driver circuit **1040** of FIG. **10**.

[0058] The first driver section **1120** may include four legs, each controlled responsive to the X**1** control signal. Each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor. Similarly, the second driver section **1130** may include two legs, each controlled responsive to the X**2** control signal, and each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor. Lastly, the third driver section **1140** may include one leg, which is controlled responsive to the X**3** control signal, and each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor. In an embodiment when each leg has an impedance of 240 ohms, the first driver section **1120** has an effective impedance of 60 ohms, the second driver section **1130** has an effective impedance of 120 ohms, and the third driver section **1140** has an effective impedance of 240 ohms.

[0059] In operation, the seven leg driver circuit **1100** may drive the OUT signal responsive to the ATX and BTX bitstreams. The ATX and BTX bitstreams are provided to the legs of the driver sections **1120**, **1130**, and/or **1140** to provide an output signal OUT having appropriate voltage tor the multilevel signal, for example, using PAM to convert a plurality of bitstreams into a multilevel signal. The bitstreams may be provided to appropriate legs of the driver circuit **1100**, for example, by a switch circuit that may be controlled or programmed as previously described. The switch circuit may be controlled to effect a PAM conversion by providing the bitstreams to the appropriate legs of the driver circuit **1100**.

[0060] For example, in some embodiments using PAM**4** to convert two bitstreams (e.g., the ATX and BTX bitstreams) into an output signal, the ATX signal may be provided to the legs of the first driver section **1120** as the X**1** control signal and the BTX signals may be provided to the legs of the second driver section **1130** as the X**2** control signal. The resulting output signal will have a voltage representing the data of the ATX and BTX bitstreams. The third driver section **1140** is not needed for the example PAM**4** configuration, and may be omitted or ignored.

[0061] In another example, in some embodiments using PAM**2** to convert a bitstream (e.g., the ATX bitstream or the BTX bitstream) into an output signal, the bitstream may be provided to different combinations of the legs of the seven leg driver circuit **1100** independent of the first, second, and third driver sections. For example, the bitstream may be provided to one leg, which results in a drive based on 240 ohms resistance. The bitstream may be provided to two legs, which results in a drive based on 120 ohms resistance. In another example the bitstream may be provided to three legs, which results in a drive based on 80 ohms resistance. The bitstream may be provided to any combination of the seven legs of the driver circuit **1100** to provide a drive based on a resulting resistance, with the resistance decreasing with each additional leg. In an example where the bitstream is provided to all seven legs of the driver circuit **1100**, the drive is based on 34 ohm resistance. Thus, the number of legs to which the bitstream is provided may provide a desired drive based on the resulting resistance.

[0062] In another example, in some embodiments the seven leg driver circuit **1100** may be used to provide PAM**8** conversion of three bitstreams (e.g., the ATX bitstream, the BTX bitstream, and a CTX bitstream). For example, in some embodiments using PAM**8** to convert three bitstreams into an output signal, the ATX signal may be provided to the legs of the first driver section **1120** as the X**1** control signal, the BTX signals may be provided to the legs of the second driver section **1130** as the X**2** control signal, and the CTX signals may be provided to the legs of the third driver section **1140** as the X**3** control signal. The resulting output signal will have a voltage representing the data of the ATX, BTX, and CTX bitstreams. The order of the bitstream to driver section connection is not important, so long as the receiver is aware for the decoding process.

[0063] FIG. **12** is a block diagram of system that includes a multilevel communication architecture with data bus inversion (DBI) system **1200** according to an embodiment of the present disclosure. The system **1200** may include a multilevel signal driver **1204** configured to transmit to a multilevel signal receiver **1206** via an I/O bus. The multilevel signal driver **1204** may be implemented in the encoder and driver circuit **114** and/or the encoder and driver circuit **124** of FIG. **1** and the multilevel signal receiver **1206** may be implemented in the receiver and decoder circuit **116** and/or the receiver and decoder circuit **126** of FIG. **1**.

[0064] The multilevel signal driver **1204** may include a DBI encoder **1210**, multilevel signal encoder **1220**, and drivers **1230** coupled in series. The DBI encoder **1210** may be configured to perform a DBI operation on 11 data bits to be transmitted to the multilevel signal receiver **1206**. The DBI operation may reduce current consumption during transmission. Typically, in a DBI operation, if more than half of the data bits in a block of data to be sent have the first logical value, the DBI data may be encoded by logically inverting each data bit of the block of data. For example, the data bits in the block of data having the first logic value are inverted to have the second logical value (to be represented by a relatively low voltage), and the data bits in the block of data having the second logical value are inverted to have the

first logical value (to be represented by a relatively high voltage). As a result, more than half of the data bits of the DBI data will have the second logical value, represented by the relatively low voltage. If half or less than half of the data bits in the block of data from have the second logical value, the DBI data may be encoded by providing the block of data in its original state. However, in the case of multilevel signaling, the DBI operation may be dependent on the encoding scheme to generate the transmitted signals. As can be seen in encoding scheme employed in tables **510** and **520** of FIG. **5**, the only scenarios in which both the X and Y signal lines transmit a relatively mid or high voltage (e.g., and thus higher electrical current) is when the C bitstream has a logical 1 value. Thus, the DBI encoder **1210** in a multilevel signal driver **1204** that employs the same encoding scheme depicted in FIG. **5** may invert the C bitstreams for each set of three bits if half or more than half of the C bitstreams have a logical 1 value. In the example depicted in FIG. **12**, this may mean that if two or more of the four C bitstreams have a logical one value, the C bitstream values may be inverted. The multilevel signal driver **1204** may also seta DBI flag to indicate whether the C bitstreams have been inverted.

[0065] The multilevel signal encoder **1220** may be configured to receive the DBI data and the DBI flag and may break the DBI data in to sets of three bitstreams. The multilevel signal encoder **1220** may encode each set of three bitstreams into a two multi-level signals using control signals provided to the multilevel signal driver **1230**. The drivers **1230** may receive the control signals for each pair of signal lines and may drive a voltage on each signal line of the I/O bus based on the respective control signals. Thus, the multilevel signal encoder **1220** and the drivers **1230** may convert each set of three bitstreams into two multilevel signals to be driven over the I/O bus.

[0066] The multilevel signal receiver **1206** may include receivers and latches **1240**, multilevel signal decoders **1250**, and DBI decoders **1260**. The receivers and latches **1240** may include comparators that are configured to determine a signal level of each signal line. The multilevel signal decoders **1250** may include logic to recover each set of three bitstreams of DBI data based on the outputs of the comparators from the receivers and latches **1240**. Each of the recovered sets of three bitstreams of DBI data and DBI flag may be logical equivalents of corresponding sets of three bitstreams encoded by the multilevel signal encoder **1220**. The DBI decoders **1260** may decode each of the recovered sets of three bitstreams of DBI data based on the DBI flag to recover the original eleven bitstreams of data.

[0067] In operation, the multilevel signal driver **1204** may be configured to transmit 11 bitstreams of data along with a DBI flag bit over eight signal lines using multi-level signal encoding, and the multilevel signal receiver **1206** may be configured to receive the multi-level signals over the eight signal lines and recover the 11 bitstreams by decoding received signal levels and decoding DBI data based on the DBI flag. While the multilevel signal driver **1204** is described as encoding each set of three bitstreams over a two signal lines using multilevel signals, other encoding schemes may be implemented, such as transmitting two bitstreams over one signal line. Thus, the multilevel signal driver **1204** may receive the 11 bitstreams, and during each symbol period, may encode a symbol for each set of three bitstreams to be driven on a pair of the eight signal lines using control signals to control the multilevel signal driver **1230**.

[0068] As previously described, the DBI encoder **1210** may perform a DBI operation on 11 bitstreams to generate DBI data and a DBI flag. In the example depicted in FIG. **12** based on the encoding scheme depicted in FIG. **5**, the DBI operation may include dividing the 11 bitstreams into sets of three (e.g., with one of the sets of three including the DBI flag), and determining a count of the third bitstreams of each set that has a logical 1 value. If the count is greater than or equal to two, the DBI encoder **1210** may invert each of the third bitstreams to generate DBI data and set the DBI flag. If the count is less than 2, the DBI encoder **1210** may leave each of the third bitstreams in their original state as the DBI data and may clear the DBI flag. The DBI data and the DBI flag may be provided to the multilevel signal encoder **1220**.

[0069] The multilevel signal encoder **1220** may encode each set of three bitstreams of the DBI data and DBI flag for transmission over a pair multilevel signal lines. The multilevel signal encoder **1220** may include logic that generates respective control signals for each pair of signal lines based on the three bitstreams. The logic of the multilevel signal encoder **1220** may include logic similar to the logic depicted in FIGS. **3**A to **3**D for each set of three bitstreams. The drivers **1230** may include drivers that are configured to drive a multi-level signal on each of pair of the eight signal lines based on the respective control signals provided by the multilevel signal encoder **220**. The drivers **1230** may implement the seven leg driver circuit **800** of FIG. **8** for one or more signal lines.

[0070] The voltages driven on each of the 8 signal lines may be captured by the multilevel signal receiver **1206**. The receivers and latches **1240** of the multilevel signal receiver **1206** may include latches that are configured to capture symbols of each pair of the 8 signal lines responsive to clock and command signals DQST and DQSC. The multilevel signal decoders **1250** may be configured to receive the captured voltages from the receivers and latches **1240**. The multilevel signal decoders **1250** may include comparators and decoding logic to receive and recover the DBI data and the DBI flag by decoding each pair of signal lines to recover a respective set of three bitstreams. The comparators may be configured to provide respective output signals based on a comparison of a voltage of a respective signal line with a reference voltage. The output signals associated with each pair of signal lines may be provided to the decoding logic of the multilevel signal decoders **1250**. The decoding logic of the multilevel signal decoders **1250** may decode output signals for each pair of signal lines to recover each set of three bitstreams of the DBI data and DBI flag. In an embodiment, the decoding logic may include the logic depicted in FIGS. **4**A-**4**C.

[0071] The recovered DBI data and DBI flag may be provided to the DBI decoders **1260**. The DBI decoders **1260** may decode the DBI data based on the DBI flag to recover the logical equivalents of the 11 bitstreams that were provided to the DBI encoder **1210**.

[0072] The encoding scheme employed in the DBI encoder **1210** and the multilevel signal encoder **1220** and the decoding scheme described in the multilevel signal decoders **1250** and multilevel signal decoders **1250** may be based on the multilevel architecture (e.g., the number of independent levels available for each signal over the I/O bus) and the

encoding and decoding implementation (e.g., the mapping of combined bitstreams to the multilevel signal values). One of skill in the art would recognize that other multilevel architectures (e.g., PAM or 4 level signaling) and other encoding and decoding implementations may be implemented in the system **1200**. Thus, while the system **1200** includes converting three bitstreams into two multilevel signals, other implementations may be realized by one of skill in the art.

[0073] FIGS. **13**A and **13**B depict an encoding map **1300** and a schematic of a multi-leg driver circuit **1301** for a multilevel signal architecture implementing PAM according to an embodiment of the disclosure. The multi-leg driver circuit **1301** includes seven legs, and may be referred herein as a seven leg driver circuit. The table **1310** maps bitstream values to control signals A**1**, A**2**, and A**3**. The control signals A**1**, A**2**, and A**3** may be used by the drivers **1230** of FIG. **12** and/or the driver **1301** to drive a voltage on a signal line. The encoding map **1200** may be used by the output encoder and driver circuit **114** and/or **124** of FIG. **1** and/or the multilevel signal encoder **1220** of FIG. **12**. The table **1310** includes possible logical combinations of A and B bitstreams and exemplary unique multilevel encoding of A**1**, A**2**, and A**3** control signals that are used by the driver **1301** to drive a signal line to one of four signal values. For example, when the A and B bitstreams each have a logical value of zero (e.g., line **1** of the table **1310**), the A**1**, A**2**, and A**3** signals may be driven to a logical values of one. In another example, if the A bitstream has a logical value of zero and the B bitstream has a logical value of one, the A**1** signal may be logical value of zero and the A**2** and A**3** signals may be driven to logical values of one. It will be appreciated that different mapping may be employed to encode the A and B, so long as each unique logical combination of the A and B signals maps to a unique combination on the A**1**, A**2**, and A**3** control signals.

[0074] The seven leg driver circuit **1301** may be a driver in a DRAM, such as a double data rate (DDR) DRAM driver. The seven leg driver circuit **1301** may include seven signal line drivers (e.g., "legs"). In some embodiments, each of the signal line drivers have an impedance of 240 ohms. The seven leg driver circuit **1301** may include a first driver section **1320**, a second driver section **1330**, and a third driver section **1340** configured to drive an output signal OUT to a signal line based on A**1**, A**2**, and A**3** control signals. The seven leg driver circuit **1301** may further include an adjustment driver section **1350** that is configured to adjust a voltage of the OUT signal, when, for example, the OUT signal is biased to one voltage or another due to leakage. The seven leg driver circuit **1301** may be implemented in the **114** and/or the **124** of FIG. **1** and/or the drivers **1230** of FIG. **12**.

[0075] The first driver section **1320** may include two legs, each controlled responsive to the A**1** control signal. Each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor. Similarly, the second driver section **1330** may include two legs, each controlled responsive to the A**2** control signal, and each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor, lastly, the third driver section **1340** may include two legs, each controlled responsive to the A**3** control signal, and each leg may include a pull up (e.g., p-type) transistor and a pull down (e.g., n-type) transistor. The adjustment driver section **1350** may include a single leg with a pull up transistor controlled responsive to an adjust pull up signal APU and a pull down transistor controlled responsive to an adjust pull down signal APD. In an embodiment having each leg having an impedance of 240 ohms, the first driver section **1320** has an effective impedance of 120 ohms, the second driver section **1330** has an effective impedance of 120 ohms, and the third driver section **1340** has an effective impedance of 120 ohms.

[0076] In operation, **1301** may drive the OUT signal responsive to the A**1**, A**2**, and A**3** control signals. In an example, when the A**1** control signal has a low logical value, the pull up transistors of the first driver section **1320** are enabled to couple the high supply voltage to the XOUT signal and pull down transistors are disabled. When the A**1** control signal has a high logical value, the pull up transistors of the first driver section **1320** are disabled and the pull down transistors are enabled to couple the low supply voltage to the OUT signal. Operation of the second driver section **1330** responsive to the A**2** control signal and operation of the third driver section **1340** responsive to the A**3** control signal may be similar to operation of the third driver section **1340** responsive to the A**1** control signal. The OUT signal may be a combination of the voltages driven by the first driver section **1320**, the second driver section **1330**, and the third driver section **1340**. The OUT signal may have a VH voltage, a VL voltage, or a high-middle voltage between the high supply and the low supply voltages and a low-middle voltage between the high middle voltage and the low supply voltage. The high-middle voltage may be achieved when the two of the first driver section **1320**, the second driver section **1330**, and the third driver section **1340** are driving the high supply voltage and the other is driving the low supply voltage. The low-middle voltage may be achieved when the two of the first driver section **1320**, the second driver section **1330**, and the third driver section **1340** are driving the low supply voltage and the other is driving the high supply voltage.

[0077] The adjustment driver section **1350** may compensate for drive strength differences between the first driver section **1320**, the second driver section **1330**, and the third driver section **1340**. For example, the adjustment driver section **1350** may pull the voltage of the OUT signal slightly up or down if the combination of the first driver section **1320**, the second driver section **1330**, and the third driver section **1340** are not able to drive the OUT signal to a proper voltage. The APU signal may pull the OUT signal slightly up when having an active low value and the APD signal may pull the OUT signal slightly down when having an active high value.

[0078] FIGS. **14**A-**14**D depict a schematic diagram of exemplary output of the multi-leg driver circuit **1301** of FIG. **13**B according to an embodiment of the disclosure. For example, the low voltage signal representation **1410** may represent driving the VL voltage (e.g., when the first driver section **1320**, the second driver section **1330**, and the third driver section **1340** are driving the low supply voltage). In this case, the output voltage VO received over the signal line may be a low voltage. The RDRV may represent the inherent resistance of the pull down transistors.

[0079] The low-mid voltage signal representation **1420** may represent driving the lower-middle voltage (e.g., when one of the first driver section **1320**, the second driver section **1330**, and the third driver section **1340** is driving the high supply voltage and the others are driving the low supply voltage). In this case, the VO voltage received over the

signal line may be ¼ of the high supply voltage. The RDRV may represent the inherent resistances of the pull up transistor and pull down transfers.

[0080] The high-mid voltage signal representation **1430** may represent driving the upper-middle voltage (e.g., when one of the first driver section **1320**, the second driver section **1330**, and the third driver section **1340** is driving the low supply voltage and the others are driving the high supply voltage). In this case, the VO voltage received over the signal line may be ½ of the high supply voltage. The RDRV may represent the inherent resistances of the pull up transistor and pull down transistors.

[0081] The high voltage signal representation **1440** may represent driving the VH voltage (e.g., when all of the first driver section **1320**, the second driver section **1330**, and the third driver section **1340** are driving the high supply voltage). In this case, the VO voltage received over the signal line may be ¾ of the high supply voltage.

[0082] FIG. **15** illustrates a portion of a memory **1500** according to an embodiment of the present disclosure. The memory **1500** includes an array **1502** of memory cells, which may be, for example, volatile memory cells, non-volatile memory cells, DRAM memory cells, SRAM memory cells, flash memory cells, or some other types of memory cells. The memory **1500** includes a command decoder **1506** that receives memory commands and addresses through an ADDR/CMD bus. The command decoder **1506** provides control signals, based on the commands received through the ADDR/CMD bus. The command decoder **1506** also provides row and column addresses to the memory **1500** through an address bus and an address latch **1510**. The address latch then outputs separate column addresses and separate row addresses.

[0083] The row and column addresses are provided by the address latch **1510** to a row address decoder **1522** and a column address decoder **1528**, respectively. The column address decoder **1528** selects bit lines extending through the array **1502** corresponding to respective column addresses. The row address decoder **1522** is connected to word line driver **1524** that activates respective rows of memory cells in the array **1502** corresponding to received row addresses. The selected data line (e.g., a bit line or bit lines) corresponding to a received column address are coupled to a read/write circuitry **1530** to provide read data to a data output circuit **1534** via an input-output data bus **1540**. The data output circuit **1534** may include multi-level signal encoders and drivers **1535** that are configured to encode and drive multilevel voltages on signal lines on the output data bus. The multi-level signal encoders and drivers **1535** may include the output encoder and driver circuit **114** and/or the output encoder and driver circuit **124** of FIG. **1**, the signal driver **214** of FIG. **2**, the logic circuits **300** of FIGS. **3**A-**3**D, the X signal line driver **610** and the Y signal line driver **620** of FIG. **6**, the seven leg driver circuit **800** of FIG. **8**, the multilevel signal driver **1204** of FIG. **12**, the seven leg driver circuit **1301** of FIG. **13**B, or combinations thereof. The multi-level signal encoders and drivers **1535** may be configured to encode signals based on the encoding implementation **500** described in FIG. **5** and/or the encoding implementation **1300** depicted in FIG. **13**A. Write data are provided to the array **1502** through a data input circuit **1544** and the memory array read/write circuitry **1530**. The data input circuit **1544** may include multi-level signal receivers and decoders **1545** that are configured to receive and decode multilevel voltages on signal lines on the input data bus. The multi-level signal receivers and decoders **1545** may include the receiver and decoder circuit **116** and/or the receiver and decoder circuit **126** of FIG. **1**, the **216** of FIG. **2**, the logic circuits **400** of FIGS. **4**A-**4**C, the multilevel signal receiver **1206** of FIG. **12**, or combinations thereof. The multi-level signal encoders and drivers **1535** may be configured to decode signals based on the encoding implementation **500** described in FIG. **5** and/or the encoding implementation **1300** depicted in FIG. **13**A. The command decoder **1506** responds to memory commands and addresses provided to the ADDR/CMD bus to perform various operations on the array **1502**. In particular, the command decoder **1506** is used to provide control signals to read data from and write data to the array **1502**.

[0084] From the foregoing it will be appreciated that, although specific embodiments of the disclosure have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the disclosure. Accordingly, the disclosure is not limited except as by the appended claims.

What is claimed is:

1. An apparatus, comprising:

a driver circuit configured to convert a plurality of bitstreams into a plurality of multilevel signals,

wherein the driver circuit comprising a plurality of drivers configured to drive the plurality of respective multilevel signals onto a plurality of respective signal lines, and

wherein each driver of the plurality of drivers is configured to drive more than two voltages, and

wherein a number of the plurality of bitstreams is greater than a number of the plurality of multilevel signals.

2. The apparatus of claim **1**, wherein the plurality of drivers comprise:

a first driver configured to receive a first plurality of bitstreams and to drive an output signal in response onto the plurality of respective signal lines; and

a second driver configured to receive a second plurality of bitstreams and to drive an output signal in response onto the plurality of respective signal lines.

3. The apparatus of claim **2**, wherein the first driver and the second driver have different impedances.

4. The apparatus of claim **1**, further comprising a swatch circuit configured to receive a first plurality of bitstreams and a second plurality of bitstreams, and to provide the first and second pluralities of bitstreams to the driver circuit.

5. The apparatus of claim **4**, wherein the switch circuit is configured to receive a control signal that is configured to control routing of the first and second pluralities of bitstreams to circuits of the driver circuit.

6. The apparatus of claim **5**, further comprising a command decoder configured to provide the control signal.

7. The apparatus of claim **5**, further comprising programmable elements programmed to provide the control signal.

8. The apparatus of claim **5**, comprising multiplexer circuits configured to provide the first and second pluralities of bitstreams to the driver circuit.

9. The apparatus of claim **1** wherein the plurality of drivers comprise a plurality of signal line drivers having a same impedance.

10. The apparatus of claim **9**, wherein the driver circuit comprises a first driver section controlled by a first control signal associated with the first plurality of bitstreams and a

second driver section controlled by a second control signal associated with the second plurality of bitstreams.

11. The apparatus of claim **10**, wherein the first driver section comprises a first number of signal line drivers of the plurality of signal line drivers,

wherein the second driver section comprises a second number of the signal line drivers of the plurality of signal line drivers, and

wherein the first number and the second number are different from each other.

12. The apparatus of claim **11**, wherein each signal line driver of the first number of signal line drivers comprises a pull up transistor and a pull down transistor configured to receive the first control signal, and

wherein each signal line driver of the second number of signal line drivers comprises a pull up transistor and a pull down transistor configured to receive the second control signal.

13. A method comprising:

receiving a plurality of multilevel signals including a first multilevel signal and a second multilevel signal;

providing a plurality of output signals based on a first reference voltage and a second reference voltage responsive to any multilevel signal of the plurality of multilevel signals, including:

providing a first output signal and a second output signal based on the first reference voltage and the second reference voltage respectively, responsive to the first multilevel signal;

providing a third output signal and a fourth output signal based on the first reference voltage and the second reference voltage respectively, responsive to the second multilevel signal; and

providing a plurality of bitstreams responsive to the first, second, third and fourth output signals,

wherein the plurality of bitstreams that are greater in number than the plurality of multilevel signals.

14. The method of claim **13**, wherein providing the first output signal and the second output signal based on the first reference voltage and the second reference voltage respectively includes:

comparing the first multilevel signal to the first reference signal;

comparing the first multilevel signal to the second reference signal, and

wherein providing the third output signal and the fourth output signal based on the first reference voltage and the second reference voltage respectively includes:

comparing the second multilevel signal to the first reference signal; and

comparing the second multilevel signal to the second reference signal.

15. The method of claim **13**, further comprising:

receiving the first and second output signals from the first circuit;

receiving the third and fourth output signals from the second circuit; and

providing a first bitstream, a second bitstream and a third bitstream responsive to the first, second, third and fourth output signals.

16. The method of claim **15**, further comprising:

receiving the first, second and third output signals;

providing a first intermediate signal responsive to the first, second and third output signals;

receiving the first, second and fourth output signals;

providing a second intermediate signal responsive to the first, second and fourth output signals;

receiving the first and second intermediate signals; and

providing the first bitstream responsive to the first and second intermediate signals.

17. The method of claim **16**, further comprising:

receiving the first, second, third and fourth output signals;

providing a third intermediate signal responsive to the first, second, third and fourth output signals;

receiving the first, second, third and fourth output signals;

providing a fourth intermediate signal responsive to the first, second, third and fourth output signals;

receiving the first, second and third output signals;

providing a fifth intermediate signal responsive to the first, second and third output signals;

receiving the third, fourth and fifth intermediate signals; and

providing the second bitstream responsive to the third, fourth and fifth intermediate signals.

18. A method, comprising:

converting a plurality of bitstreams into a plurality of multilevel signals by a driver circuit;

driving the plurality of respective multilevel signals onto a plurality of respective signal lines by the driver circuit,

wherein the plurality of multilevel signals have more than two signal levels, and

wherein a number of the plurality of bitstreams is greater than a number of the multilevel signals.

19. The method of claim **18**, further comprising:

driving an output signal onto the plurality of respective signal lines by a first driver responsive to a first plurality of bitstreams of the plurality of bitstreams; and

driving the output signal onto the plurality of respective signal lines by a second driver responsive to a second plurality of bitstreams of the plurality of bitstreams.

20. The method of claim **19**, wherein the first driver and the second driver have different impedances.

21. The method of claim **19**, further comprising:

receiving a control signal indicative of routing of the first and second pluralities of bitstreams to the first and second driver; and

providing either the first plurality of bitstreams or the second plurality of bitstreams responsive to the control signal.

22. The method of claim **21**, comprising

multiplexing the first and second pluralities of bitstreams responsive to the control signal; and

providing the multiplexed first and second pluralities of bitstreams to the driver circuit.

23. The method of claim **21**, further comprising:

controlling a first driver section in the driver circuit by a first control signal associated with the first plurality of bitstreams; and

controlling a second driver section in the driver circuit by a second control signal associated with the second plurality of bitstreams.

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