US 20230389266A1

(19) **United States**
(12) **Patent Application Publication**
WANG et al.
(10) **Pub. No.: US 2023/0389266 A1**
(43) **Pub. Date: Nov. 30, 2023**

(54) **METHOD FOR FORMING CAPACITOR AND SEMICONDUCTOR DEVICE**

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(21) Appl. No.: **18/446,507**

(22) Filed: **Aug. 9, 2023**

Related U.S. Application Data

(63) Continuation of application No. PCT/CN2021/138294, filed on Dec. 15, 2021.

(30) **Foreign Application Priority Data**

Oct. 18, 2021 (CN) 202111208407.X

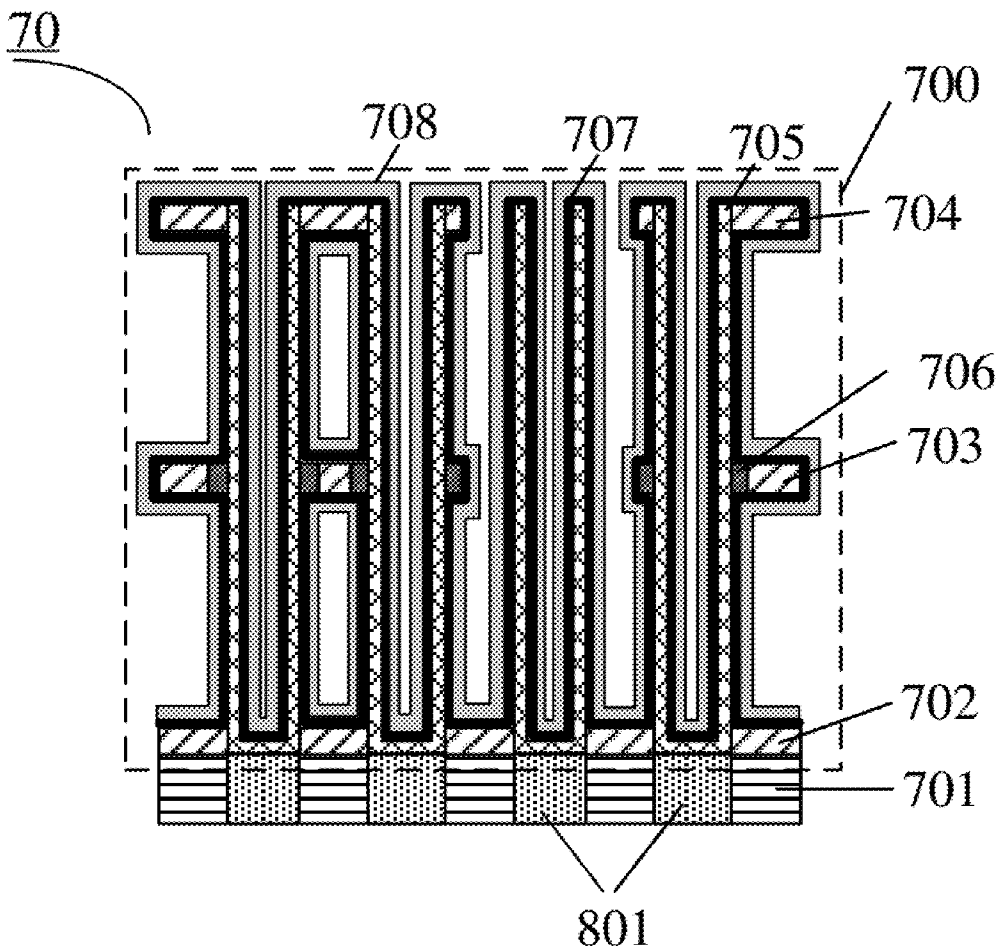
Publication Classification

(51) **Int. Cl.**
H10B 12/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H10B 12/033*** (2023.02); ***H01L 28/91*** (2013.01); ***H01L 28/75*** (2013.01)

(57) **ABSTRACT**

Method for forming a capacitor includes following operations. A base is provided. First supporting layer and first sacrificial layer are formed on the base sequentially. First through holes penetrating first supporting layer and first sacrificial layer are formed to expose the base. First through holes are filled to form first filling structures. Second supporting layer covering remaining first sacrificial layer and first filling structures is formed. Second through holes penetrating second supporting layer are formed. Second sacrificial layer covering remaining second supporting layer and second through holes, and third supporting layer are formed. Third through holes penetrating third supporting layer and second sacrificial layer are formed. First filling structures are removed to communicate each of third through holes and corresponding one of first through holes. First electrode layers, dielectric layer and second electrode layer covering first through holes and third through holes are formed sequentially to form the capacitor.



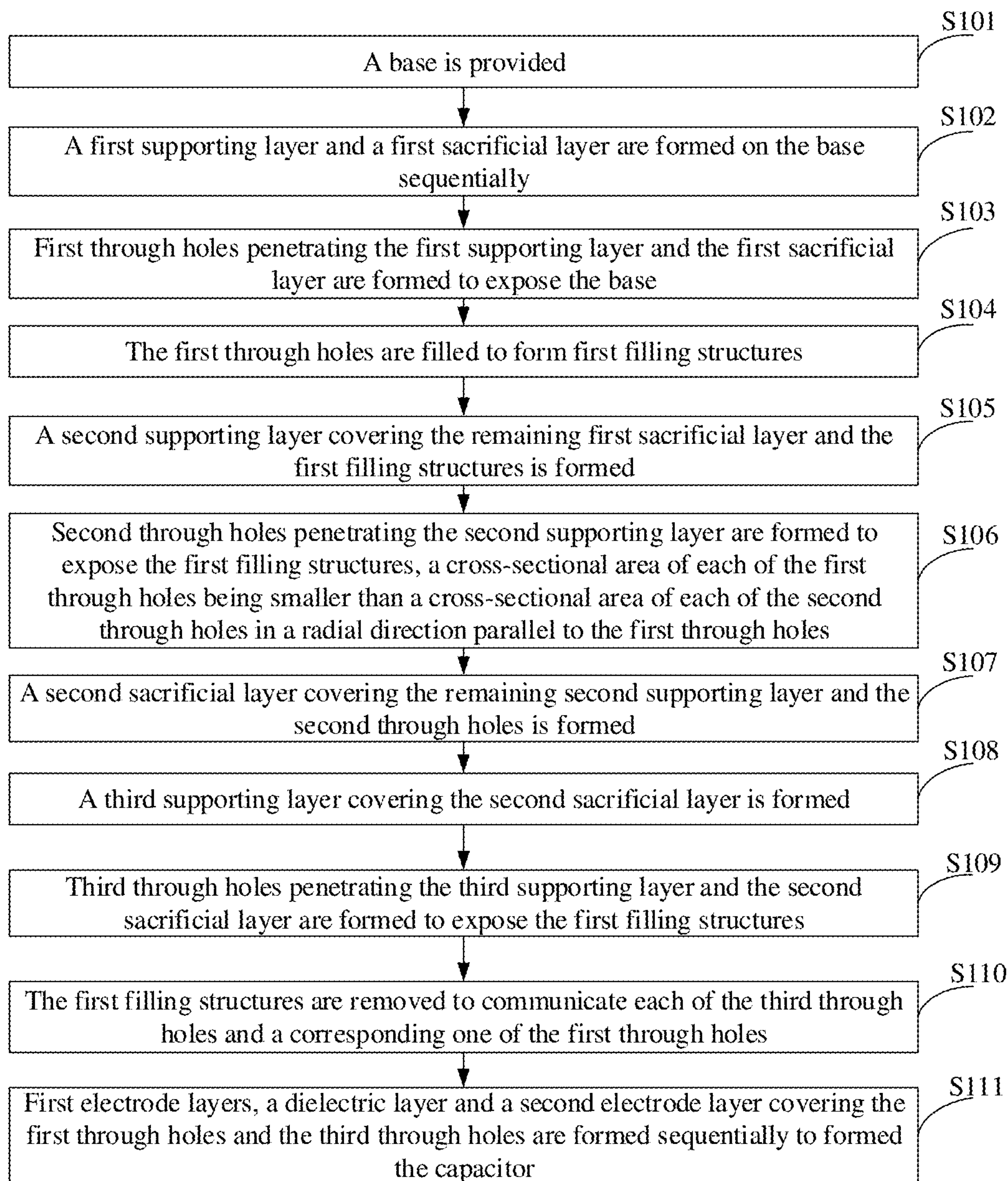


FIG. 1

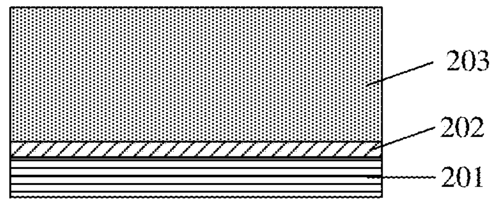


FIG. 2A

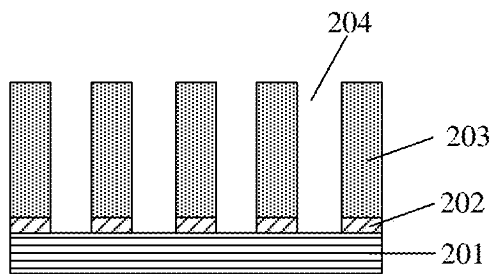


FIG. 2B

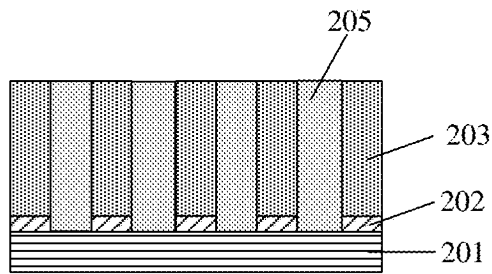


FIG. 2C

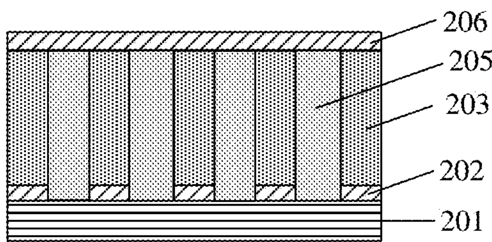


FIG. 2D

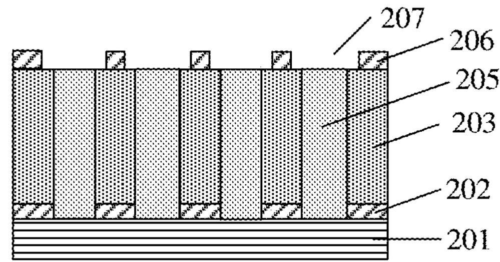


FIG. 2E

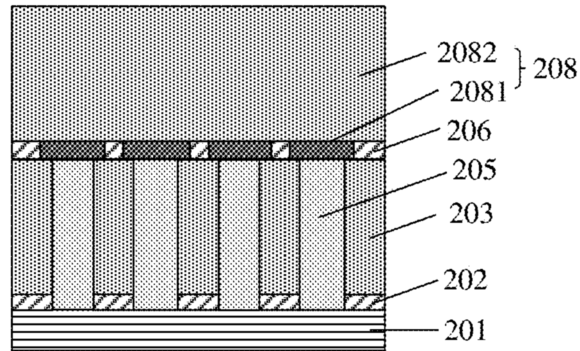


FIG. 2F

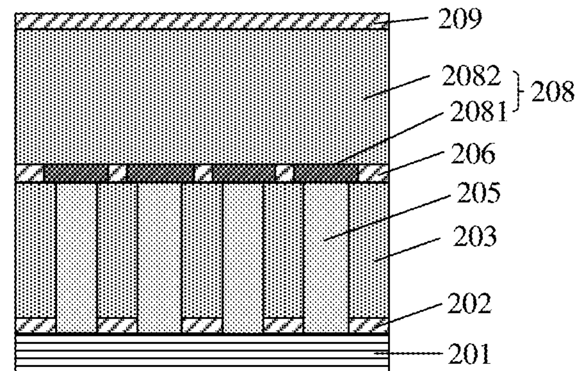


FIG. 2G

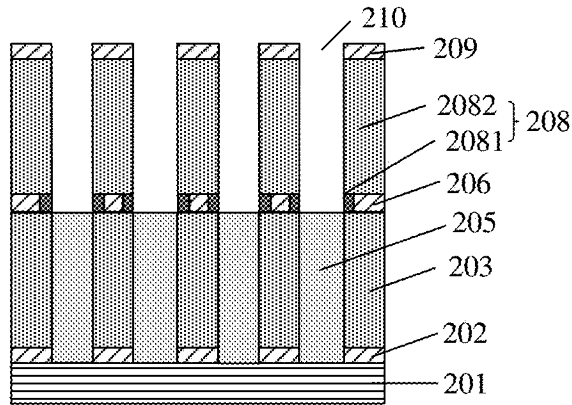


FIG. 2H

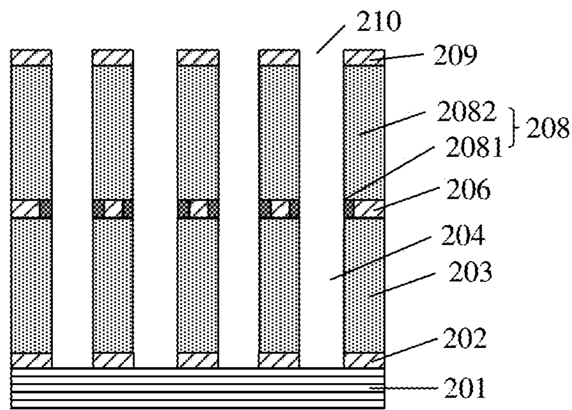


FIG. 2I

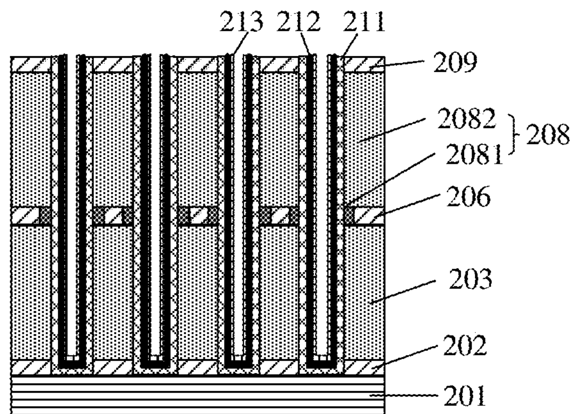


FIG. 2J

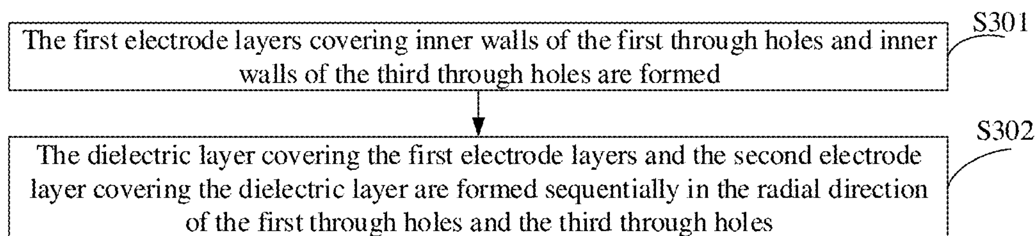


FIG. 3

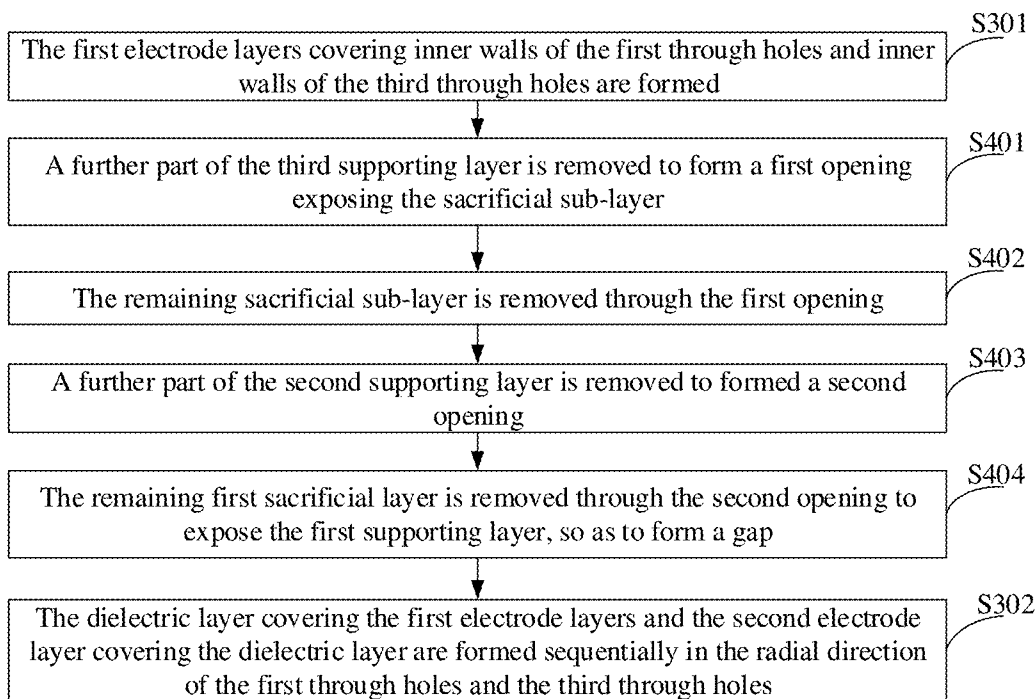


FIG. 4

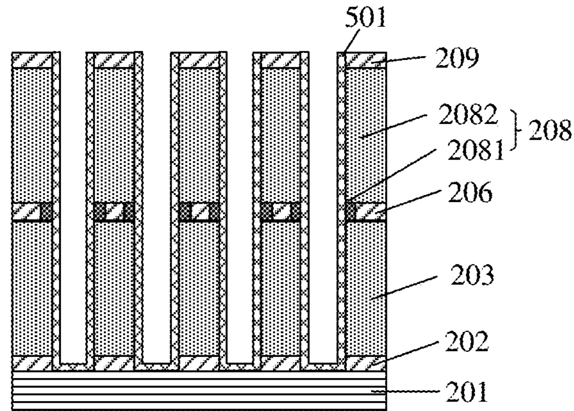


FIG. 5A

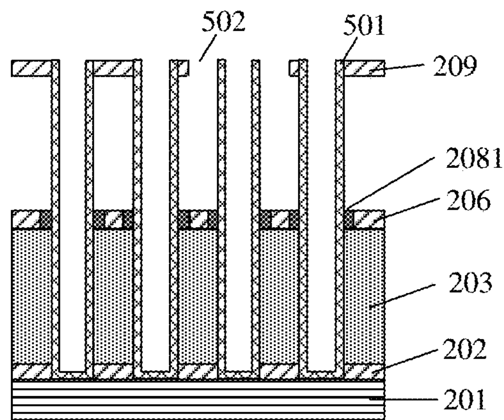


FIG. 5B

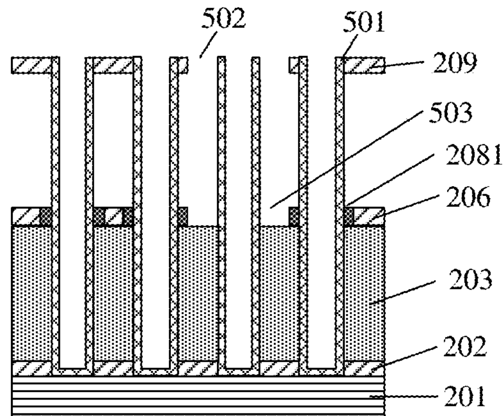


FIG. 5C

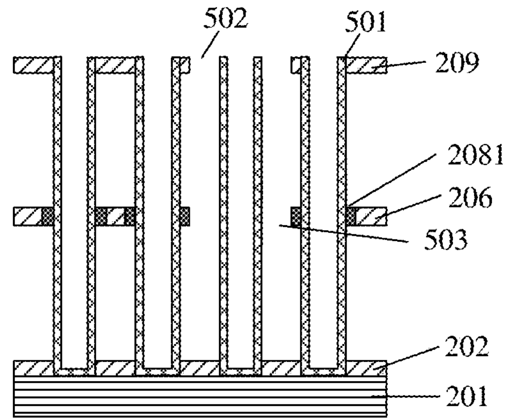


FIG. 5D

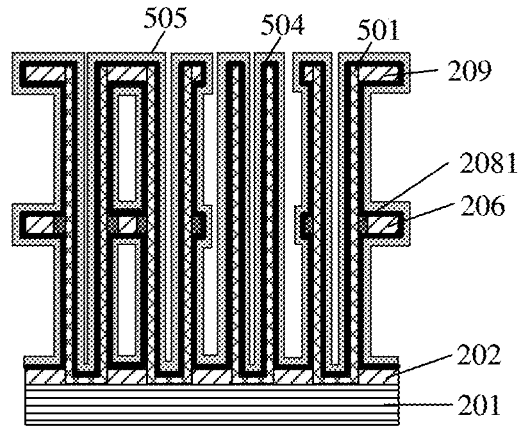


FIG. 5E

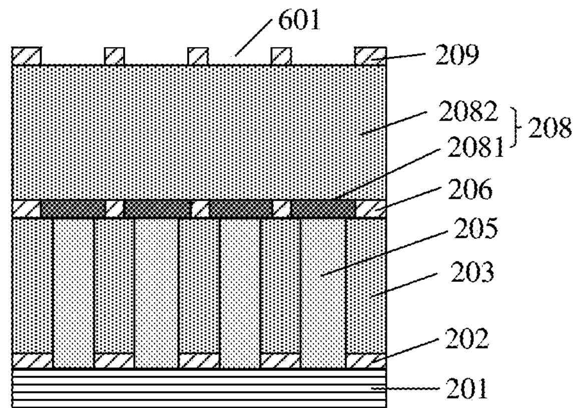


FIG. 6A

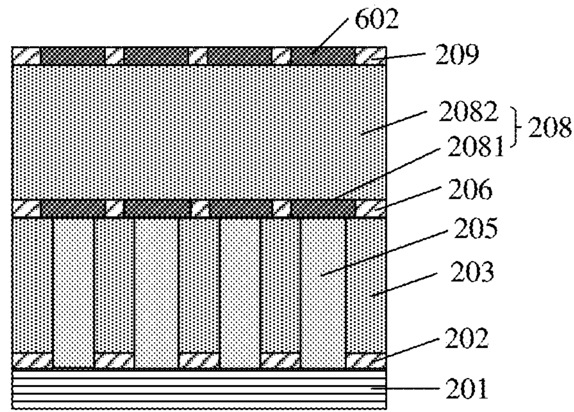


FIG. 6B

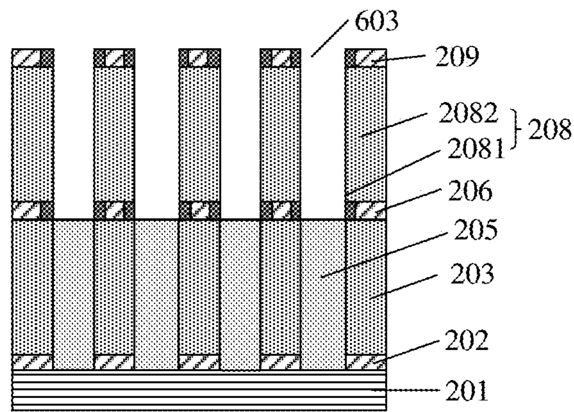


FIG. 6C

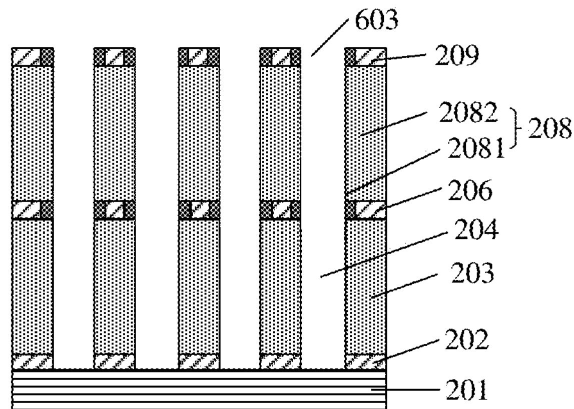


FIG. 6D

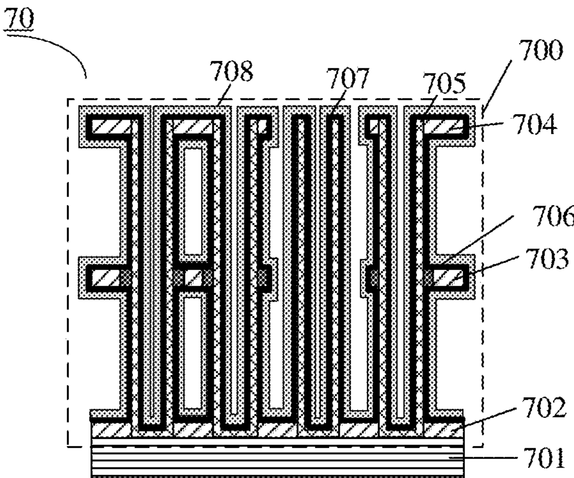


FIG. 7

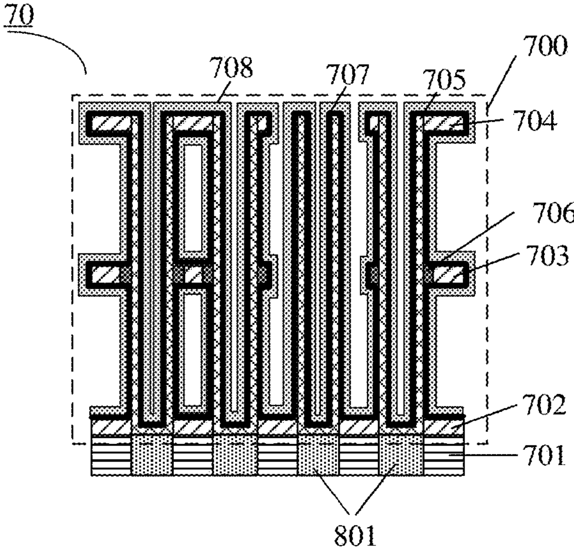


FIG. 8

METHOD FOR FORMING CAPACITOR AND SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a U.S. continuation application of International Application No. PCT/CN2021/138294, filed Dec. 15, 2021, which claims priority to Chinese Patent Application No. 202111208407.X, filed Oct. 18, 2021. International Application No. PCT/CN2021/138294 and Chinese Patent Application No. 202111208407.X are incorporated herein by reference in their entireties.

BACKGROUND

[0002] Dynamic random access memory (DRAM) is a semiconductor memory device commonly used in computers, and is composed of a plurality of repeated storage units. Each of the storage units includes a transistor and a capacitor. The gate of the transistor is connected to a word line, the drain of the transistor is connected to a bit line, and the source of the transistor is connected to the capacitor.

[0003] With the continuous reduction of the manufacturing process dimension of DRAM devices, the height of a capacitor in DRAM is developing towards high aspect ratio, and meanwhile it is also necessary to ensure that there is an enough capacitor storage capacity per unit area of the capacitor, which makes it more difficult to etch a capacitor hole in the capacitor. Therefore, how to provide a method for forming a capacitor which can ensure the perpendicularity of the capacitor hole is an urgent problem to be solved.

SUMMARY

[0004] The disclosure relates to the technical field of semiconductors, and relates to, but is not limited to, a method for forming a capacitor and a semiconductor device.

[0005] In a first aspect, embodiments of the disclosure provide a method for forming a capacitor. The method includes the following operations.

[0006] A base is provided.

[0007] A first supporting layer and a first sacrificial layer are formed on the base sequentially.

[0008] First through holes penetrating the first supporting layer and the first sacrificial layer are formed to expose the base.

[0009] The first through holes are filled to form first filling structures.

[0010] A second supporting layer covering the remaining first sacrificial layer and the first filling structures is formed.

[0011] Second through holes penetrating the second supporting layer are formed to expose the first filling structures. A cross-sectional area of each of the first through holes is smaller than a cross-sectional area of each of the second through holes in a plane parallel to a radial direction of the first through holes.

[0012] A second sacrificial layer covering the remaining second supporting layer and the second through holes is formed.

[0013] A third supporting layer covering the second sacrificial layer is formed.

[0014] Third through holes penetrating the third supporting layer and the second sacrificial layer are formed to expose the first filling structures.

[0015] The first filling structures are removed to communicate each of the third through holes and a corresponding one of the first through holes.

[0016] First electrode layers, a dielectric layer and a second electrode layer covering the first through holes and the third through holes are formed sequentially to form a capacitor.

[0017] In a second aspect, embodiments of the disclosure provide a semiconductor device which at least includes a base and a capacitor. The capacitor includes a first supporting layer, a second supporting layer and a third supporting layer disposed sequentially parallel to the base; first electrode layers disposed perpendicular to the base and penetrating the first supporting layer, the second supporting layer and the third supporting layer, in which the filling sub-layers are disposed between the second supporting layer and the first electrode layers; a dielectric layer covering the surfaces of the first electrode layers, the first supporting layer, the second supporting layer and the third supporting layer; and a second electrode layer covering a surface of the dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] In the accompany drawings (which are not necessarily drawn to scale), similar reference numerals may describe like components in different views. Similar reference numerals with different letter suffixes may denote different examples of similar components. The accompanying drawings generally illustrate the various embodiments discussed herein by way of example, rather than limitation.

[0019] FIG. **1** is a flowchart of a method for forming a capacitor provided by an embodiment of the disclosure.

[0020] FIGS. **2**A to **2**J are schematic diagrams of partial structures corresponding to a method for forming a capacitor provided by an embodiment of the disclosure.

[0021] FIG. **3** is a flowchart of a method for forming a capacitor provided by an embodiment of the disclosure.

[0022] FIG. **4** is a flowchart of a method for forming a capacitor provided by an embodiment of the disclosure.

[0023] FIGS. **5**A to **5**E are schematic diagrams of partial structures corresponding to a method for forming a capacitor provided by an embodiment of the disclosure.

[0024] FIGS. **6**A to **6**D are schematic diagrams of partial structures corresponding to a method for forming a capacitor provided by an embodiment of the disclosure.

[0025] FIG. **7** is a schematic diagram of a partial structure of a semiconductor device provided by an embodiment of the disclosure.

[0026] FIG. **8** is a schematic diagram of a partial structure of a semiconductor device provided by an embodiment of the disclosure.

DESCRIPTION OF REFERENCE NUMERALS

[0027] **201/701**—Base; **202/702**—First supporting layer; **203**—First sacrificial layer; **204**—First through hole; **205**—First filling structure; **206/703**—Second supporting layer; **207**—Second through hole; **208**—Second sacrificial layer; **2081/706**—filling sub-layer; **2082**—sacrificial sub-layer; **209/704**—Third supporting layer; **210**—Third through hole; **211/501/705**—First electrode layer; **212/504/707**—Dielectric layer; **213/505/708**—Second electrode layer; **502**—First opening; **503**—Second opening; **601**—Fourth through hole;

602—Second filling structure; **603**—Third through hole; **70**—Semiconductor device; **801**—Conductive structure.

DETAILED DESCRIPTION

[0028] With reference to accompany drawings of embodiments of the disclosure, a specific technical solution of the disclosure will be further described in detail below. The following embodiments are used to illustrate the disclosure, but are not used to limit the scope of the present disclosure.

[0029] In the following description, numerous specific details are given to provide a more thorough understanding of the disclosure. However, it will be apparent to those skilled in the art that the disclosure may be practiced without one or more of these details. In other examples, some technical features well known in the art are not described in order to avoid confusion with the disclosure. That is, not all features of the actual embodiments are described herein, and well-known functions and structures are not described in detail.

[0030] In the accompany drawings, the dimensions of layers, regions, elements and their relative dimensions may be exaggerated for clarity. The same reference numerals denote the same elements throughout.

[0031] It should be understood that when an element or layer is referred to as being "above", "adjacent to", "connected to" or "coupled to" another element or layer, it may be directly above, adjacent to, connected to, or coupled to the other element or layer, or intervening elements or layers may exist. Conversely, when an element is referred to as being "directly above", "directly adjacent to", "directly connected to" or "directly coupled to" another element or layer, there is no intervening element or layer. It should be understood that, although the terms "first, second, third, etc." may be used to describe various elements, components, regions, layers, and/or portions, the elements, components, regions, layers, and/or portions should not be limited by such terms. These terms are used only to distinguish one element, component, region, layer, or portion from another element, component, region, layer, or portion. Thus, a first element, component, region, layer, or portion discussed below may be represented as a second element, component, region, layer, or portion without departing from the teachings of the disclosure. The discussion of a second element, component, region, layer or portion does not imply that a first element, component, region, layer or portion is necessarily present in the disclosure.

[0032] Spatially relational terms such as "below", "under", "lower", "beneath", "above", and "upper" etc. may be used herein for conveniently describing a relationship between one element or feature and another element or feature illustrated in the figures. It is to be understood that, in addition to the orientations shown in the figures, the spatially relational terms are intended to further include different orientations of a device in use and operation. For example, if the device in the figures is turned over, elements or features described as being "under" or "beneath" or "below" other elements or features will be oriented to be "on" the other elements or features. Therefore, the exemplary terms "under" and "below" may include both upper and lower orientations. The device may be additionally oriented (rotated by 90 degrees or otherwise), and the spatial descriptors used herein are interpreted accordingly.

[0033] The terminology used herein is intended to describe specific embodiments only and is not to be a limitation of the disclosure. As used herein, the singular forms "a", "an" and "said/the" are also intended to include the plural forms, unless the context clearly indicates otherwise. It should also be understood that the terms "compose" and/or "include", when used in this specification, determine the presence of said features, integers, steps, operations, elements and/or components, but do not exclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups. As used herein, the term "and/or" includes any and all combinations of related listed items.

[0034] In the related art, when a capacitor hole of a capacitor is formed by etching, the capacitor hole is usually formed after one etching. However, when a capacitor hole with a high aspect ratio is formed, the etching method of a capacitor hole is easy to cause an etching deflection when etching to form the lower part of the capacitor hole. That is to say, there will be a non-perpendicular etching at the lower part of the capacitor hole with a high aspect ratio formed by one etching, which will reduce the electrical properties of the capacitor and the stability of the capacitor structures.

[0035] Based on the problems existing in the related art, embodiments of the disclosure provide a method for forming a capacitor. Reference is made to FIG. **1**. FIG. **1** is a flowchart of a method for forming a capacitor provided by an embodiment of the disclosure. The capacitor provided by the embodiments of the disclosure may be formed by the following operations.

[0036] In **S101**, a base is provided.

[0037] In **S102**, a first supporting layer and a first sacrificial layer are formed on the base sequentially.

[0038] In **S103**, first through holes penetrating the first supporting layer and the first sacrificial layer are formed to expose the base.

[0039] In **S104**, the first through holes are filled to form first filling structures.

[0040] In **S105**, a second supporting layer covering the remaining first sacrificial layer and the first filling structures is formed.

[0041] In **S106**, second through holes penetrating the second supporting layer are formed to expose the first filling structures. A cross-sectional area of each of the first through holes is smaller than a cross-sectional area of each of the second through holes in a plane parallel to a radial direction of the first through holes.

[0042] In **S107**, a second sacrificial layer covering the remaining second supporting layer and the second through holes is formed.

[0043] In **S108**, a third supporting layer covering the second sacrificial layer is formed.

[0044] In **S109**, third through holes penetrating the third supporting layer and the second sacrificial layer are formed to expose the first filling structures.

[0045] In **S110**, the first filling structures are removed to communicate each of the third through holes and a corresponding one of the first through holes.

[0046] In **S111**, first electrode layers, a dielectric layer and a second electrode layer covering the first through holes and the third through holes are formed sequentially to form the capacitor.

[0047] Referring to FIGS. **2**A to **2**J, the method for forming a capacitor provided by the embodiments of the present disclosure will be described in detail below.

[0048] As shown in FIG. **2**A, S**101** and S**102** are performed. A base **201** is provided, and a first supporting layer **202** and a first sacrificial layer **203** are formed on the base **201** sequentially.

[0049] In some embodiments, the base **201** may be made from a semiconductor material, such as one or more of silicon, germanium, silicon-germanium compounds and silicon-carbon compounds.

[0050] In an embodiment of the disclosure, a first supporting layer **202** and a first sacrificial layer **203** may be formed on the base **201** sequentially by means of a physical vapor deposition (PVD), a chemical vapor deposition (CVD) or an atomic layer deposition process.

[0051] Here, in order to facilitate the etching of the first sacrificial layer **203**, a material for forming the first sacrificial layer **203** may be a soft material such as phosphoro-silicate glass (PSG), boro-phospho-silicate glass (BPSG) or fluoro-silicate glass (FSG). A material for forming the first supporting layer **202** may be a nitride, such as silicon nitride, silicon carbonitride, silicon oxynitride, or silicon boronitride, etc.

[0052] Referring to FIG. **2**B, S**103** is performed. First through holes **204** penetrating the first supporting layer **202** and the first sacrificial layer **203** are formed to expose the base **201**.

[0053] In some embodiments, a patterned mask layer (not shown) covering the first sacrificial layer **203** may be deposited before forming the first through holes **204**. A material of the hard mask may be polysilicon.

[0054] In some embodiments, based on the patterned mask layer, the first through holes **204** are formed by a dry etching process or a wet etching process. The mask layer is removed after forming the first through holes **204**. In the dry etching, the first supporting layer **202** and the first sacrificial layer **203** may be etched with a fluorine-containing gas as an etchant. For example, a gas such as nitrogen trifluoride (NF_3) and carbon tetrafluoride (CF_4) may be used as the etchant to form the first through holes **204**. In the wet etching, a solution such as hydrofluoric acid or phosphoric acid may be used as an etchant to form the first through holes **204**.

[0055] In some embodiments, a thickness range of the first supporting layer **202** may be between 50 nm and 150 nm. A thickness range of the first sacrificial layer **203** may be between 150 nm and 300 nm.

[0056] Referring to FIG. **2**C, S**104** is performed. The first through holes **204** are filled to form first filling structures **205**. Here, the first filling structures **205** may be formed by physical vapor deposition, chemical vapor deposition, atomic layer deposition or spin coating. A material of the first filling structures **205** may be an easily removed material such as a carbon-containing material, spin-on glass, spin-on carbon or a photoresist, so as to facilitate removal of the first filling structures **205** when the capacitor holes are subsequently formed. Top surfaces of the first filling structures **205** may be flush with a top surface of the remaining first sacrificial layer **203** to form a flat surface, thereby providing a flat support surface for subsequent formation of the second supporting layer **206**.

[0057] Referring to FIG. **2**D, S**105** is performed. A second supporting layer **206** covering the remaining first sacrificial layer **203** and the first filling structures **205** is formed.

[0058] Here, the second supporting layer **206** may be formed by physical vapor deposition, chemical vapor deposition or atomic layer deposition. A material of the second supporting layer **206** may be the same as or different from the material of the first supporting layer **202**. The material for forming the second supporting layer **206** may be a nitride, such as silicon nitride, silicon carbonitride, silicon oxynitride, or silicon boronitride, etc.

[0059] Referring to FIG. **2**E, S**106** is performed. Second through holes **207** penetrating the second supporting layer **206** are formed to expose the first filling structures **205**. A cross-sectional area of each of the first through holes **204** is smaller than a cross-sectional area of each of the second through holes **207** in a plane parallel to a radial direction of the first through holes **204**.

[0060] In an embodiment of the disclosure, the second through holes, each with a cross-sectional area larger than that of each of the first through holes, are formed in the second supporting layer, so that in the process of forming the capacitor holes by etching in steps, even if there is a deviation between the positions of the capacitor holes above and below a second through hole, a connection between the capacitor holes formed by etching in steps can be realized through the second through hole with a larger cross-sectional area. Therefore, each layer of through holes of the capacitor (such as the first through holes and the third through holes) are perpendicular through holes, and thus a problem that the capacitor holes collapse due to deflection of the capacitor holes is avoided. In this way, the perpendicularity of the capacitor holes is ensured, improving the performance of the capacitor.

[0061] Referring to FIG. **2**F, S**107** is performed. A second sacrificial layer **208** covering the remaining second supporting layer **206** and the second through holes **207** is formed.

[0062] In some embodiments, a thickness range of the second supporting layer **206** may be the same as or different from a thickness range of the first supporting layer **202**, and a thickness range of the second sacrificial layer **208** may be the same as or different from a thickness range of the first sacrificial layer **203**. The embodiments of the disclosure do not limit them.

[0063] In some embodiments, the second sacrificial layer **208** may include filling sub-layers **2081** and a sacrificial sub-layer **2082**. The filling sub-layers **2081** are used to fill the second through holes **207**.

[0064] In some embodiments, after forming the second through holes **207**, the filling sub-layers **2081** covering the second through holes **207** may be formed by physical vapor deposition, chemical vapor deposition or atomic layer deposition. Surfaces of the filling sub-layers **2081** relatively away from the base **201** are flush with a surface of the second supporting layer **206** relatively away from the base **201**. After forming the filling sub-layers **2081**, the sacrificial sub-layer **2082** covering the remaining second supporting layer **206** and the filling sub-layers **2081** is formed.

[0065] Here, a material of the filling sub-layers **2081** may be the same as or different from that of the sacrificial sub-layer **2082**.

[0066] In some embodiments, when the material of the filling sub-layers **2081** is different from that of the sacrificial sub-layer **2082**, a material hardness of the filling sub-layers **2081** is greater than that of the sacrificial sub-layer **2082**. For example, the material of the sacrificial sub-layer **2082** may be a soft material such as phosphor-silicate glass, boron-phospho-silicate glass or fluoro-silicate glass, while the material of the filling sub-layers **2081** may be a harder

material than the sacrificial sub-layer **2082**, such as silicon oxide, silicon nitride, silicon carbonitride or silicon oxynitride.

[0067] In an embodiment of the disclosure, because the cross-sectional area of each of the second through holes **207** is larger than the cross-sectional area of each of the first through holes **204**, a cross-sectional area of each of the filling sub-layers **2081** filling the second through holes **207** is also larger than a cross-sectional area of each of the first filling structures **205** filling the first through holes **204**. Moreover, in an embodiment of the disclosure, a harder material is used for the filling sub-layers **2081**, so that the unetched filling sub-layers **2081** can fill gaps formed between the first electrode layers and the supporting layer to support the first electrode layers subsequently after forming the third through holes and forming the first electrode layers on the surfaces of the third through holes.

[0068] Referring to FIGS. **2**G to **21**, S**108** to S**110** are performed. A third supporting layer **209** covering the second sacrificial layer **208** is formed. Third through holes **210** penetrating the third supporting layer **209** and the second sacrificial layer **208** are formed to expose the first filling structures **205**. The first filling structures **205** are removed to communicate each of the third through holes **210** and a corresponding one of the first through holes **204**.

[0069] In some embodiments, a thickness of the third supporting layer **209** may be much larger than that of the first supporting layer **202** or the second supporting layer **206**, so that tops of the first electrode layers in the capacitor can be more strongly supported. Therefore, the first electrode layers are not easy to collapse when the first electrode layers are made subsequently, improving the yield and performance of the capacitor.

[0070] In some embodiments, when forming the third through holes **210**, a portion of the third supporting layer **209**, a portion of the sacrificial sub-layer **2082** and a portion of a filling sub-layer **2081** may be removed by an etchant corresponding to dry etching or wet etching until the first filling structures **205** are exposed to form the third through holes **210**. The third through holes **210** communicate with the first through holes **204** to form the capacitor holes of the capacitor.

[0071] In some embodiments, in a dry etching, part of the third supporting layer **209**, the part of the sacrificial sub-layer **2082** and the part of each of the filling sub-layers **2081** may be removed with a fluorine-containing gas as an etchant. For example, a gas such as nitrogen trifluoride (NF_3) and carbon tetrafluoride (CF_4) may be used as the etchant to form the third through holes **210**. In a wet etching, a solution such as hydrofluoric acid or phosphoric acid may be used as an etchant to form the third through holes **210**.

[0072] In some embodiments, a cross-sectional area of each of the third through holes **210** is smaller than the cross-sectional area of each of the second through holes **207** in a plane parallel to a radial direction of the third through holes **210**, and an etching rate of the etchant to the filling sub-layers **2081** is greater than an etching rate of the etchant to the second supporting layer **206**, so that the etchant does not etch the second supporting layer **206** when etching the filling sub-layers **2081** and not result in damage to the support for the capacitor.

[0073] Referring to FIG. **2**J, S**111** is performed. First electrode layers, a dielectric layer and a second electrode layer covering the first through holes and the third through holes are formed sequentially to form a capacitor.

[0074] In the method for forming a capacitor and the semiconductor device provided by the embodiments of the disclosure, the first through holes are formed and filled after the first supporting layer and the first sacrificial layer are formed, followed by forming the second supporting layer. The second through holes, each with a cross-sectional area larger than that of each of the first through holes, are formed in the second support layer by etching. The second sacrificial layer and the third supporting layer are formed sequentially. The third through holes are formed, and the first filling structures are removed. The first electrode layers, the dielectric layer and the second electrode layer are formed sequentially on the surfaces of the first through holes and the third through holes to from the capacitor. In this way, compared with the formation of a whole through hole in the capacitor by one etching, in the embodiments of the disclosure, the through holes in the capacitor are formed by etching in steps, so that the height of the through hole to be etched each time and the etching difficulty are reduced, thereby reducing the probability of etching deflection at a bottom of the capacitor hole in the etching process of the capacitor hole of the capacitor, and thus improving the perpendicularity and quality of the capacitor hole, which is beneficial to enhancing the stability of the capacitor.

[0075] In some embodiments, FIG. **3** is a flowchart of a method for forming a capacitor provided by an embodiment of the disclosure. As shown in FIG. **3**, S**111** may also be performed by the following operations.

[0076] In S**301**, first electrode layers covering inner walls of the first through holes and

[0077] inner walls of the third through holes are formed.

[0078] In S**302**, a dielectric layer covering the first electrode layers and a second electrode layer covering the dielectric layer are formed sequentially in the radial direction of the first through holes and the third through holes.

[0079] In some embodiments, as shown in FIG. **4**, the embodiments of the disclosure may also include the following operations after S**301**.

[0080] In S**401**, a part of the third supporting layer is removed to form a first opening. The first opening exposes the sacrificial sub-layer.

[0081] In S**402**, the remaining sacrificial sub-layer is removed through the first opening.

[0082] In S**403**, a further part of the second supporting layer is removed to form a second opening.

[0083] In S**404**, the remaining first sacrificial layer is removed through the second opening to expose the first supporting layer so as to form a gap.

[0084] Based on the above embodiments, a method for forming a capacitor shown in FIG. **4** will be described in detail below with reference to FIGS. **5**A to **5**E.

[0085] Referring to FIG. **5**A, S**301** is performed. The first electrode layers **501** covering inner walls of the first through holes **204** and inner walls of the third through holes **210** are formed.

[0086] In an embodiment of the disclosure, the first electrode layers **501** may be formed by physical vapor deposition, chemical vapor deposition or atomic layer deposition. A thickness of the first electrode layer may be between 10 nm and 80 nm. A material of the first electrode layers **501** may be metal nitride or metal silicide, for example, titanium nitride or titanium silicide. Here, tops of the first electrode

layers **501** are flush with a top of the third supporting layer **209**, so that a surface area of each of the first electrode layers **501** can be increased, thereby improving the overall capacity of the capacitor and thus the performance of the capacitor.

[0087] Referring to FIG. **5**B, S**401** and S**402** are performed. A further part of the third supporting layer **209** is removed to form a first opening **502**. The first opening **502** exposes the sacrificial sub-layer **2082**. The remaining sacrificial sub-layer **2082** is removed through the first opening **502**.

[0088] In some embodiments, a mask layer (not shown in the figure) covering the third supporting layer **209** may be formed first before the first opening **502** is formed. A material of the hard mask may be polysilicon. The mask layer may have a pattern. The first opening **502** is formed according to the pattern of the mask layer. After the first opening **502** is formed, the mask layer is removed.

[0089] In an embodiment of the disclosure, in a direction perpendicular to the base **201**, one first opening **502** may be formed among every three adjacent first electrode layers **501**, or one first opening **502** may be formed among every four adjacent first electrode layers **501**, or only one first opening **502** may be formed in the third supporting layer **209**. The embodiments of the disclosure do not limit the position and the number of the first opening **502**. FIG. **5**B only shows a cross-sectional view of a mode of the opening exemplarily.

[0090] In some embodiments, the sacrificial sub-layer **2082** may be removed by wet etching, in which the etchant may be a solution such as hydrofluoric acid or phosphoric acid. In this way, even if the third supporting layer **209** has only one first opening **502**, the entire remaining sacrificial sub-layer **2082** can be removed through the first opening **502** using an etchant such as hydrofluoric acid.

[0091] Referring to FIG. **5**C, S**403** is performed. A further part of the second supporting layer **206** is removed to form a second opening **503**. Here, the projection position of the second opening **503** and the projection position of the first opening **502** may be the same or different in the direction perpendicular to the base **201**. In an embodiment of the disclosure, the method for forming a capacitor provided by an embodiment of the disclosure is described in detail by an example where the projection position of the second opening **503** is the same as the projection position of the first opening **502**.

[0092] Referring to FIG. **5**D, S**404** is performed. The remaining first sacrificial layer **203** is removed through the second opening **503** to expose the first supporting layer **202** so as to form a gap. Here, the gap is composed of the first opening **502**, a position of the original sacrificial sub-layer **2082**, the second opening **503** and a position of the original remaining first sacrificial layer **203**, which are communicated sequentially. The remaining first sacrificial layer **203** is removed in the same way as the sacrificial sub-layer **2082**, and the remaining first sacrificial layer **203** may be removed by wet etching.

[0093] After the gap is formed, S**302** is performed. A dielectric layer **504** covering the first electrode layers **501** and a second electrode layer **505** covering the dielectric layer **504** are formed sequentially in the radial direction of the first through holes and the third through holes.

[0094] In some embodiments, as shown in FIG. **5**E, the dielectric layer **504** covering the first electrode layers **501**, the remaining first supporting layer **202**, the further remaining second supporting layer **206**, and the further remaining third supporting layer **209** may be formed in the gap, and then the second electrode layer **505** covering the dielectric layer **504** is formed.

[0095] In some embodiments, the dielectric layer **504** and the second electrode layer **505** may be formed by physical vapor deposition, chemical vapor deposition, or atomic layer deposition.

[0096] In some embodiments, a material of the dielectric layer **504** may include at least one of zirconium oxide, hafnium oxide, zirconium titanium oxide, ruthenium oxide, antimony oxide, or aluminum oxide. A material of the second electrode layer **505** may include at least one of metal nitride or metal silicide, for example, titanium nitride or titanium silicide.

[0097] Based on the above embodiments, in some embodiments, after forming the third supporting layer **209**, fourth through holes **601** penetrating the third supporting layer **209** may also be formed as shown in FIGS. **6**A to **6**C. The fourth through holes **601** are filled to form second filling structures **602**. A part of a second filling structure **602** and a part of the second sacrificial layer **208** are finally removed to form the third through holes **603**. A cross-sectional area of each of the third through holes **603** is smaller than a cross-sectional area of each of the fourth through holes **601** in a plane parallel to a radial direction of the third through holes **603**.

[0098] In some embodiments, a material of the second filling structures **602** may be the same as or different from that of the filling sub-layers **2081**.

[0099] In an embodiment of the disclosure, by forming the through holes, each with a larger cross-sectional area than the capacitor holes (such as the first through holes and the third through holes) in the third support layer, the method for forming a capacitor provided by an embodiment of the disclosure can be applied to an etching alignment of more than two layers of through holes of the capacitor.

[0100] In some embodiments, after forming the third through holes **603**, the first filling structures **205** are removed by dry etching or wet etching to expose the first through holes **204**, so that the third through holes **603** are communicated with the first through holes **204**. After that, in an embodiment of the disclosure, surfaces of the third through holes **603** and surfaces of the first through holes **204** may also be cleaned by a cleaning agent, for example, by diluted hydrofluoric acid. A drying gas may then be introduced into the cleaned surfaces of the third through holes **603** and the cleaned surfaces of the first through holes **204** to dry the surfaces of the third through holes **603** and the surfaces of the first through holes **204**. Here, the drying gas may be hydrogen or nitrogen.

[0101] In an embodiment of the disclosure, after the capacitor holes of the capacitor are formed, residues on the surfaces of the capacitor holes are cleaned, so that the capacitor will not fail because of the residues, improving the service life and performance of the capacitor.

[0102] Based on the above method for forming a capacitor, embodiments of the disclosure provide a semiconductor device **70**. As shown in FIG. **7**, the semiconductor device **70** includes at least a capacitor **700** and a base **701**. The capacitor **700** include a first supporting layer **702**, a second supporting layer **703**, and a third supporting layer **704** disposed sequentially parallel to the base **701**; first electrode layers **705** disposed perpendicular to the base **701** and penetrating the first supporting layer **702**, the second sup-

porting layers **703**, and the third supporting layers **704**, in which the filling sub-layers **706** are disposed between the second supporting layer **703** and the first electrode layers **705**; a dielectric layer **707** covering the surfaces of the first electrode layers **705**, the first supporting layer **702**, the second supporting layer **703**, and the third supporting layer **704**; and a second electrode layer **708** covering the surface of the dielectric layer **707**.

[0103] In the capacitor in the semiconductor device provided by embodiments of the disclosure, the filling sub-layers are disposed between the second supporting layer and the first electrode layers, and the filling sub-layers are in contact with the first electrode layers, so that the filling sub-layers can form support for the first electrode layers, avoiding a problem of capacitor failure caused by collapse of the first electrode layers due to insufficient support for the capacitor, and thus improving the performance of the capacitor.

[0104] In some embodiments, as shown in FIG. **8**, the semiconductor device **70** further includes conductive structures **801** located in the base **701**. The conductive structures **801** are connected with the first electrode layers **705**. Here, the conductive structures **801** are used to connect the capacitor provided by the embodiments of the disclosure with a lower circuit. In a dynamic random access memory, the conductive structures **801** are used to connect the capacitor with a source or a drain of a lower transistor.

[0105] In some embodiments, materials of the first supporting layer **702**, the second supporting layer **703**, and the third supporting layer **704** include at least one of silicon oxide, silicon nitride, silicon carbonitride, or silicon oxynitride. Materials of the first electrode layers **705** and the second electrode layer **708** include metal nitride and/or metal silicide. A material of the dielectric layer **707** includes at least one of zirconium oxide, hafnium oxide, zirconium titanium oxide, ruthenium oxide, antimony oxide, or aluminum oxide.

[0106] In the embodiments provided by the disclosure, it is to be understood that the disclosed device and method may be implemented in a non-target way. The device embodiments described above are only schematic. For example, the division of the unit is only a logical function division, and there may be another division mode in actual implementation, for example, multiple units or components can be combined, or integrated into another system, or some features can be ignored or not executed. In addition, the components shown or discussed are coupled with each other, or directly coupled.

[0107] The units described above as separate parts may or may not be physically separated, and the parts shown as units may or may not be physical units, i.e. may be located in one place or may be distributed over multiple network units. According to the actual needs, some or all of the units can be selected to achieve the purpose of the solutions of the embodiments.

[0108] The features disclosed in the several method or device embodiments provided by the disclosure can be arbitrarily combined without conflict, in order to obtain a new method embodiment or device embodiment.

[0109] The above-mentioned are only some implementations of the disclosure, and the protection scope of the disclosure is not limited thereto. Any changes or substitutions that can be readily conceived by a person skilled in the art within the technical scope disclosed the disclosure shall be covered within the protection scope of the disclosure. Therefore, the protection scope of the disclosure shall be subject to the protection scope of the claims.

INDUSTRIAL PRACTICALITY

[0110] In the method for forming a capacitor and the semiconductor device provided by the embodiments of the disclosure, the first through holes are formed and filled after the first supporting layer and the first sacrificial layer are formed, followed by forming the second supporting layer. The second through holes, each with a cross-sectional area larger than that of each of the first through holes, are formed in the second support layer by etching. The second sacrificial layer and third supporting layer are formed sequentially. The third through holes are formed, and the first filling structures are removed. The first electrode layers, the dielectric layer and the second electrode layer are formed sequentially on the surfaces of the first through holes and the third through holes to form the capacitor. In this way, compared with the formation of a whole through hole in the capacitor by one etching, in the embodiments of the disclosure, the through holes in the capacitor are formed by etching in steps, so that the height of the through hole to be etched each time and the etching difficulty are reduced, thereby reducing the probability of etching deflection at a bottom of the capacitor hole in the etching process of the capacitor hole of the capacitor, and thus improving the perpendicularity and quality of the capacitor hole, which is beneficial to enhancing the stability of the capacitor.

1. A method for forming a capacitor, comprising:

providing a base;

forming a first supporting layer and a first sacrificial layer on the base sequentially;

forming first through holes penetrating the first supporting layer and the first sacrificial layer to expose the base;

filling the first through holes to form first filling structures;

forming a second supporting layer covering remaining first sacrificial layer and the first filling structures;

forming second through holes penetrating the second supporting layer to expose the first filling structures, wherein a cross-sectional area of each of the first through holes is smaller than a cross-sectional area of each of the second through holes in a plane parallel to a radial direction of the first through holes;

forming a second sacrificial layer covering remaining second supporting layer and the second through holes;

forming a third supporting layer covering the second sacrificial layer;

forming third through holes penetrating the third supporting layer and the second sacrificial layer to expose the first filling structures;

removing the first filling structures to communicate each of the third through holes and a corresponding one of the first through holes; and

forming first electrode layers, a dielectric layer and a second electrode layer sequentially covering the first through holes and the third through holes to form the capacitor.

2. The method of claim **1**, wherein the second sacrificial layer comprises filling sub-layers and a sacrificial sub-layer; and

the forming a second sacrificial layer covering remaining second supporting layer and the second through holes comprises:

forming the filling sub-layers covering the second through holes, wherein surfaces of the filling sub-layers relatively away from the base are flush with a surface of the second supporting layer relatively away from the base; and

forming the sacrificial sub-layer covering the remaining second supporting layer and the filling sub-layers.

3. The method of claim **2**, wherein the forming third through holes penetrating the third supporting layer and the second sacrificial layer comprises:

removing a part of the third supporting layer, a part of the sacrificial sub-layer and a part of a filling sub-layer by an etchant until the first filling structures are exposed, so as to form the third through holes, wherein a cross-sectional area of each of the third through holes is smaller than a cross-sectional area of each of the second through holes in a plane parallel to a radial direction of the third through holes, and an etching rate of the etchant to the filling sub-layers is greater than an etching rate of the etchant to the second supporting layer.

4. The method of claim **2**, wherein the forming first electrode layers, a dielectric layer and a second electrode layer sequentially covering the first through holes and the third through holes comprises:

forming the first electrode layers covering inner walls of the first through holes and inner walls of the third through holes; and

forming the dielectric layer covering the first electrode layers and the second electrode layer sequentially covering the dielectric layer in a radial direction of the first through holes and the third through holes.

5. The method of claim **4**, further comprising: after forming the first electrode layers,

removing a further part of the third supporting layer to form a first opening, wherein the first opening exposes the sacrificial sub-layer;

removing remaining sacrificial sub-layer through the first opening;

removing a further part of the second supporting layer to form a second opening; and

removing the remaining first sacrificial layer through the second opening to expose the first supporting layer so as to form a gap.

6. The method of claim **5**, wherein the forming the dielectric layer covering the first electrode layers and the second electrode layer sequentially covering the dielectric layer comprises:

forming, in the gap, the dielectric layer covering the first electrode layers, remaining first supporting layer, further remaining second supporting layer and further remaining third supporting layer; and

forming the second electrode layer covering the dielectric layer.

7. The method of claim **1**, further comprising: after forming the third supporting layer,

forming fourth through holes penetrating the third supporting layer; and

filling the fourth through holes to form second filling structures;

wherein the forming third through holes penetrating the third supporting layer and the second sacrificial layer comprises:

removing a part of a second filling structure and a part of the second sacrificial layer to form the third through holes, wherein a cross-sectional area of each of the third through holes is smaller than a cross-sectional area of each of the fourth through holes in a plane parallel to a radial direction of the third through holes.

8. The method of claim **1**, further comprising: after communicating each of the third through holes and a corresponding one of the first through holes,

cleaning surfaces of the third through holes and surfaces of the first through holes by a cleaning agent; and

introducing a drying gas into cleaned surfaces of the third through holes and cleaned surfaces of the first through holes to dry the surfaces of the third through holes and the surfaces of the first through holes.

9. The method of claim **1**, wherein a material of the first filling structures comprises at least one of spin-on glass or spin-on carbon.

10. The method of claim **1**, wherein a material of the first sacrificial layer or the second sacrificial layer comprises at least one of phosphor-silicate glass, boro-phospho-silicate glass, fluoro-silicate glass, silicon oxide, hafnium oxide or tantalum oxide.

11. A semiconductor device manufactured by the method of claim **1**, comprising at least: a base and a capacitor; wherein the capacitor comprises:

a first supporting layer, a second supporting layer and a third supporting layer disposed sequentially parallel to the base;

first electrode layers disposed perpendicular to the base and penetrating the first supporting layer, the second supporting layer and the third supporting layer, wherein filling sub-layers are disposed between the second supporting layer and the first electrode layers;

a dielectric layer covering surfaces of the first electrode layers, the first supporting layer, the second supporting layer and the third supporting layer; and

a second electrode layer covering a surface of the dielectric layer.

12. The semiconductor device of claim **11**, further comprising conductive structures located in the base and connected with the first electrode layers.

13. The semiconductor device of claim **11**, wherein a material of the first supporting layer, the second supporting layer, or the third supporting layer comprises at least one of silicon oxide, silicon nitride, silicon carbonitride, or silicon oxynitride.

14. The semiconductor device of claim **11**, wherein a material of the first electrode layers or the second electrode layer comprises at least one of metal nitride or metal silicide.

15. The semiconductor device of claim **11**, wherein a material of the dielectric layer comprises at least one of zirconium oxide, hafnium oxide, zirconium titanium oxide, ruthenium oxide, antimony oxide, or aluminum oxide.

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