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(54) **SEMICONDUCTOR MEMORY DEVICE AND ITS MANUFACTURING METHOD**

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H01L 27/108 (2006.01)

(52) **U.S. Cl.** **257/57**; 257/71; 257/E27.084

(57) **ABSTRACT**

A semiconductor memory device has a plurality of word line provided on a semiconductor region, extending in a row direction, a plurality of bit lines provided in the semiconductor region, extending in a column direction, and a plurality of memory elements provided at intersections between the plurality of word lines and the plurality of bit lines. Each word line provides a first gate electrode in the corresponding memory element. A lower portion of a side surface of each word line in a direction parallel to an extending direction of the word line is perpendicular to a main surface of the semiconductor region. An upper portion of the side surface is inclined so that a width thereof becomes smaller toward a top thereof.

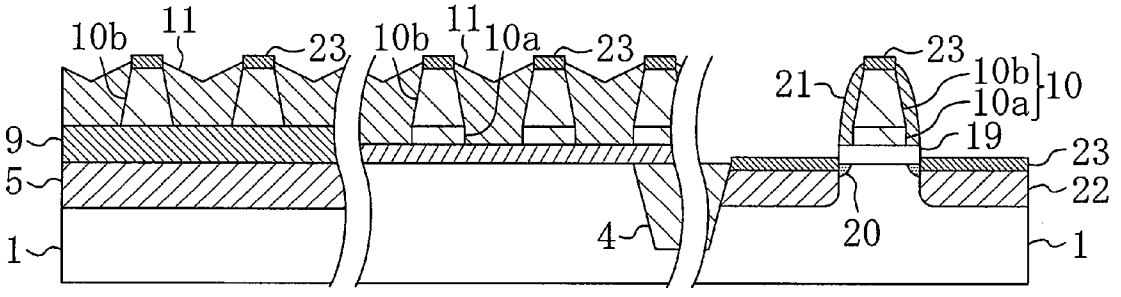


FIG. 1

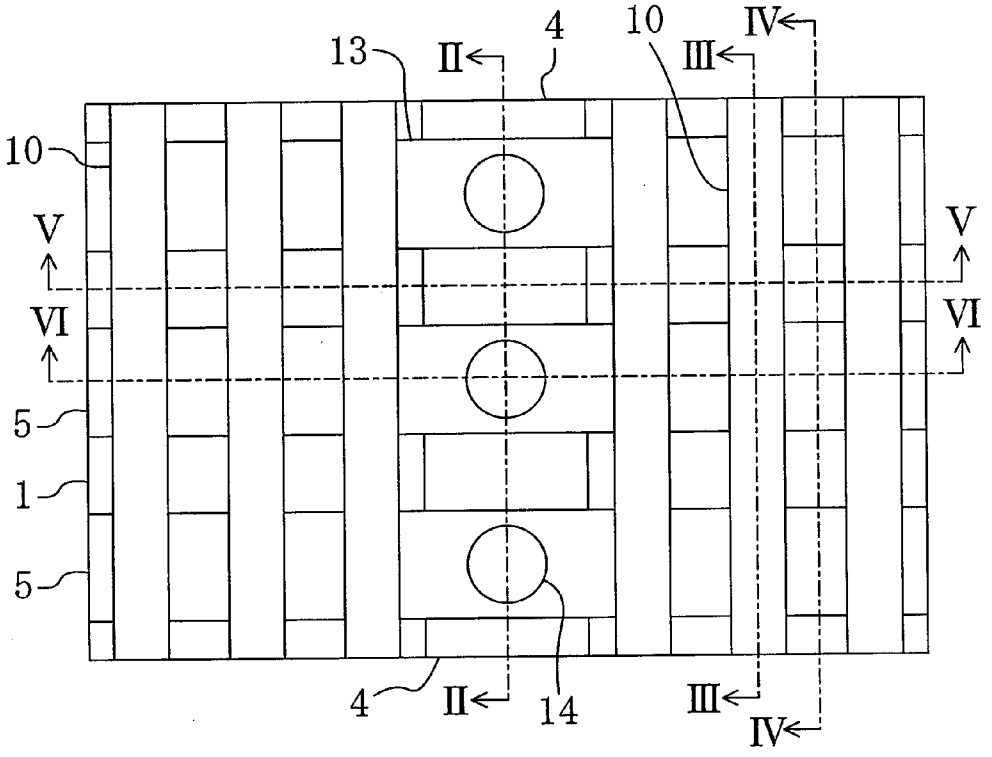


FIG. 2

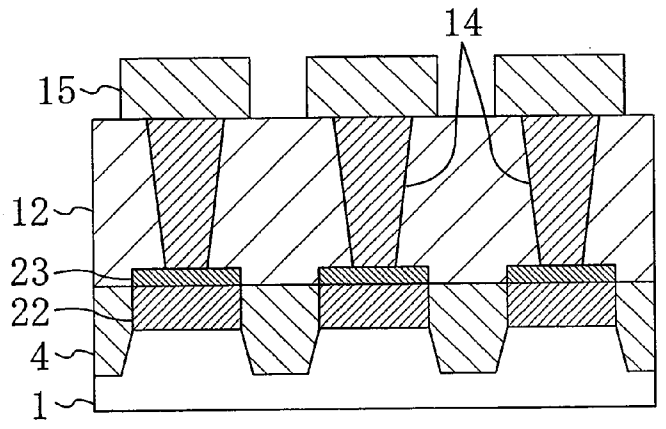


FIG. 3

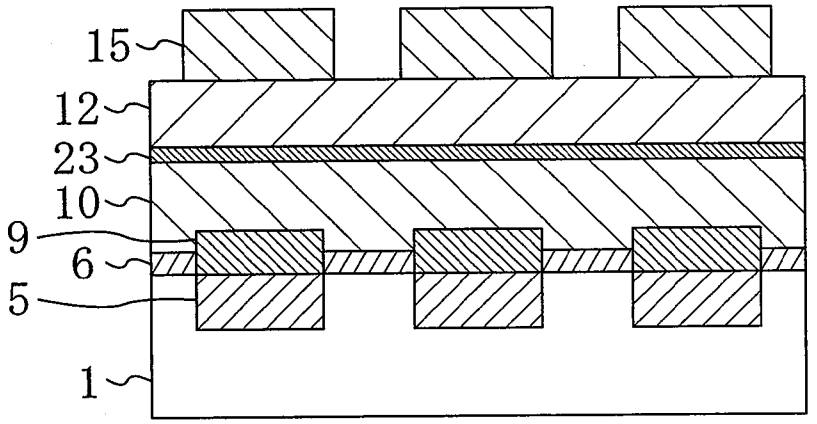


FIG. 4

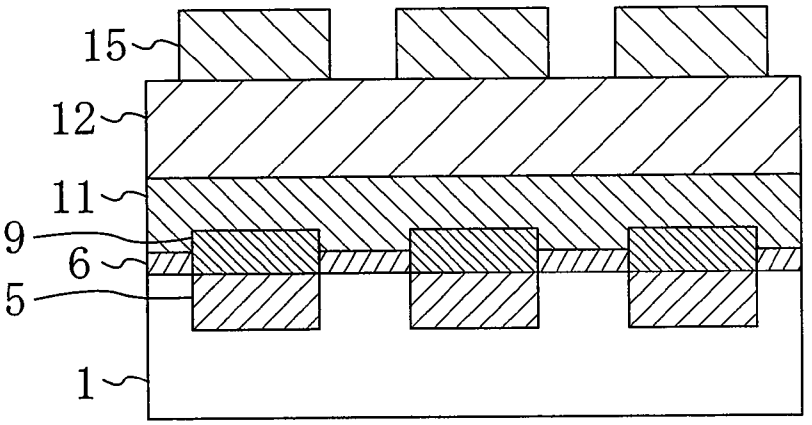


FIG. 5

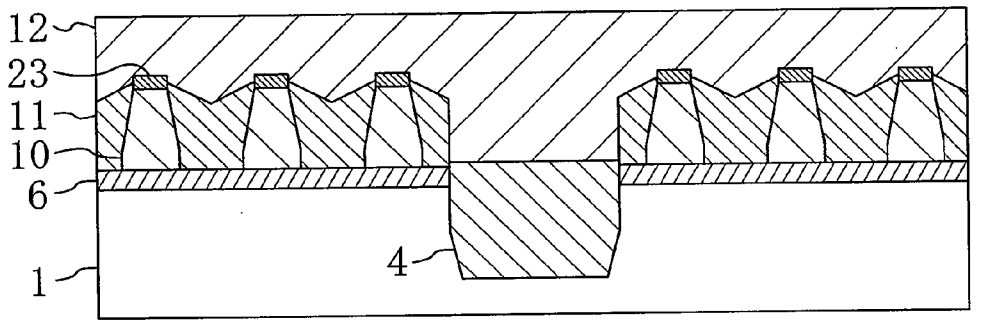


FIG. 6

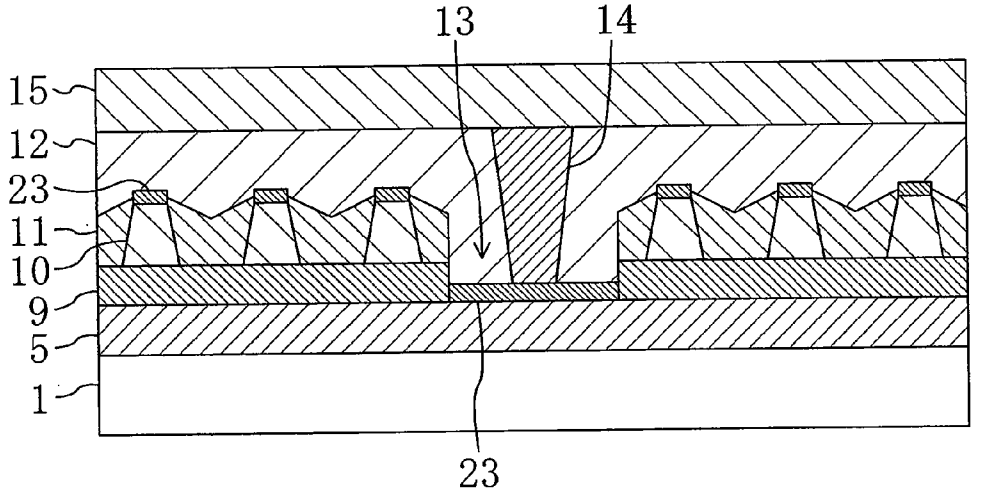


FIG. 7A

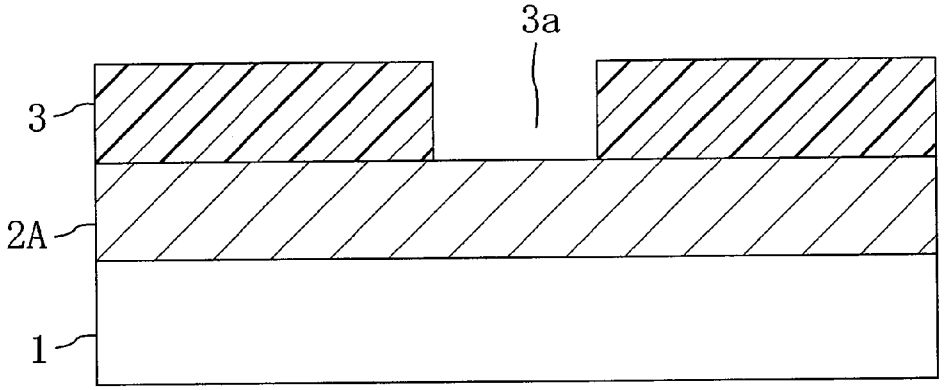


FIG. 7B

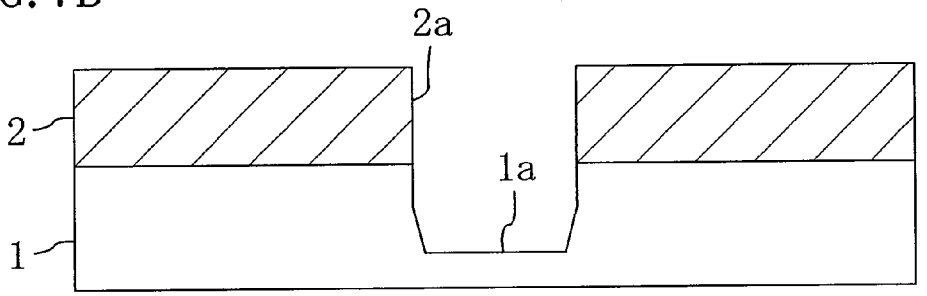


FIG. 7C

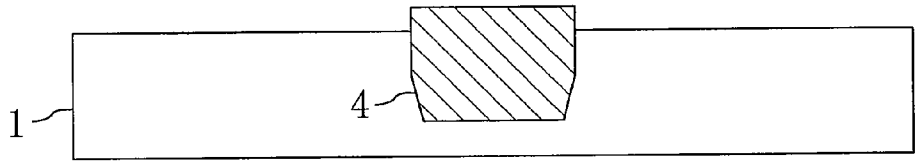


FIG. 8A

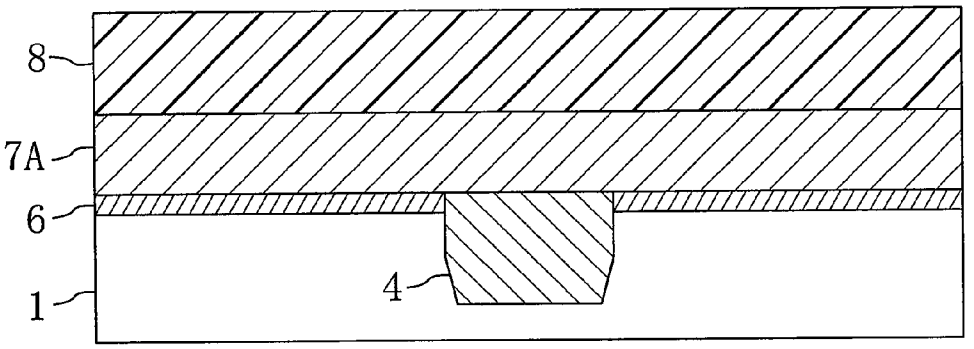


FIG. 8B

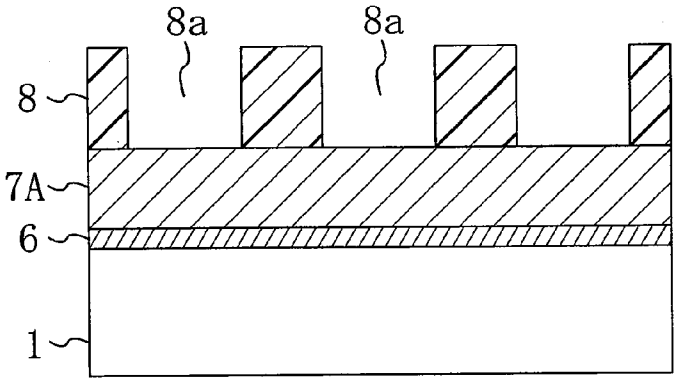


FIG. 8C

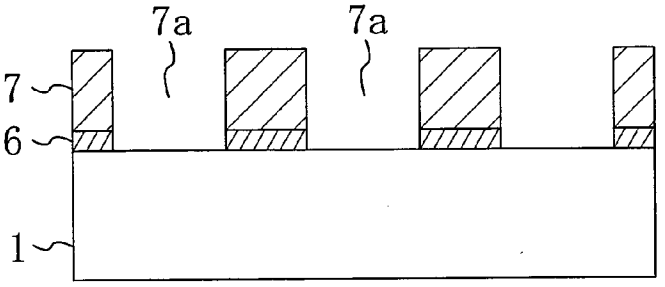


FIG. 9A

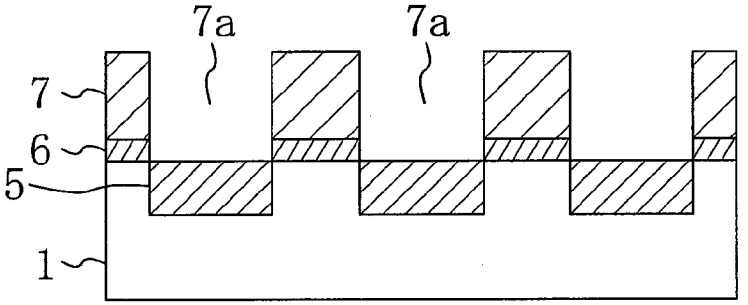


FIG. 9B

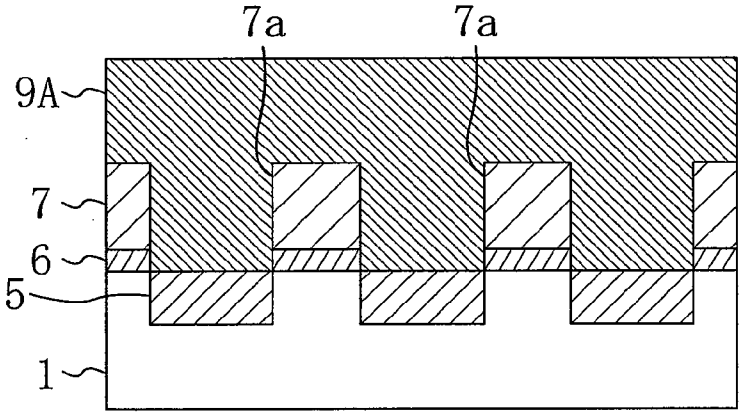


FIG. 9C

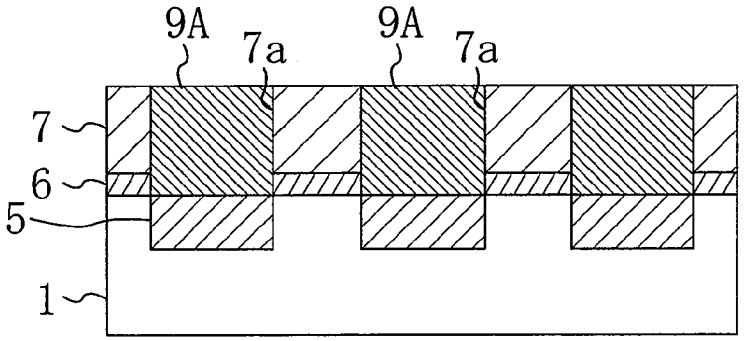


FIG. 10A

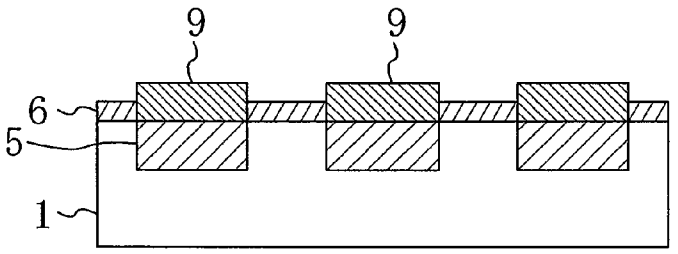


FIG. 10B

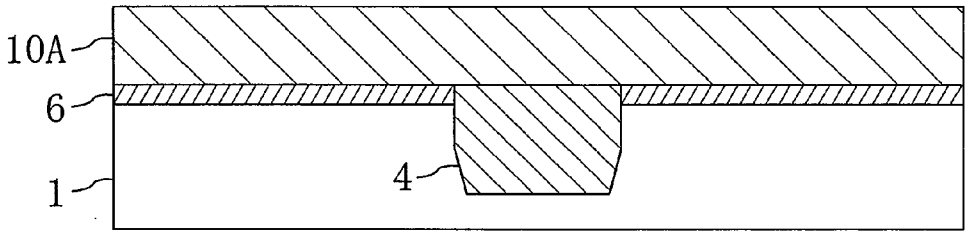


FIG. 10C

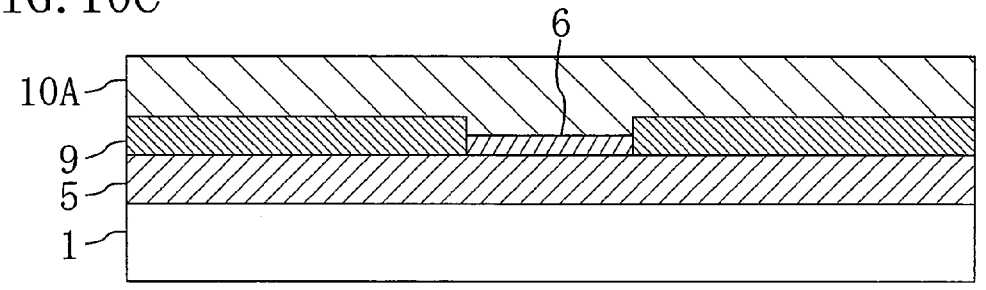


FIG. 11A

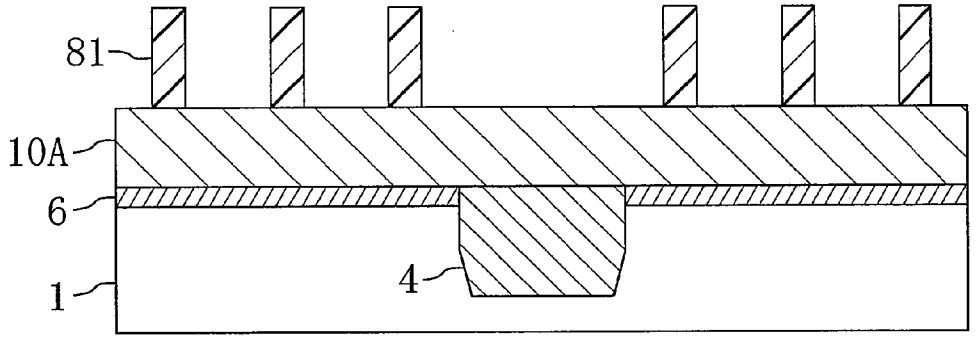


FIG. 11B

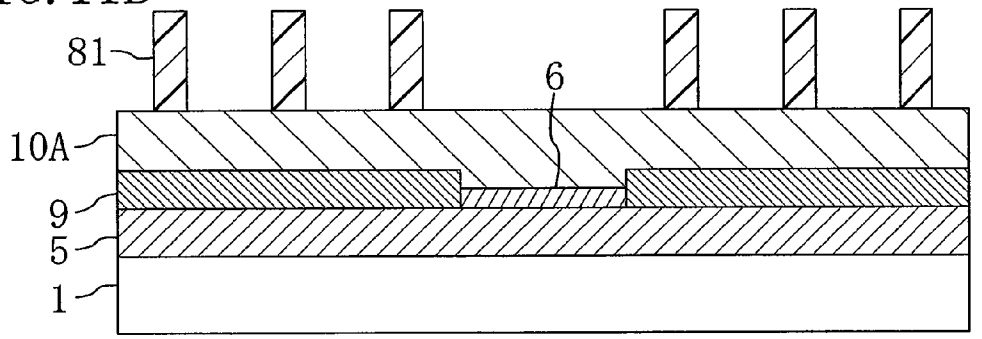


FIG. 12A

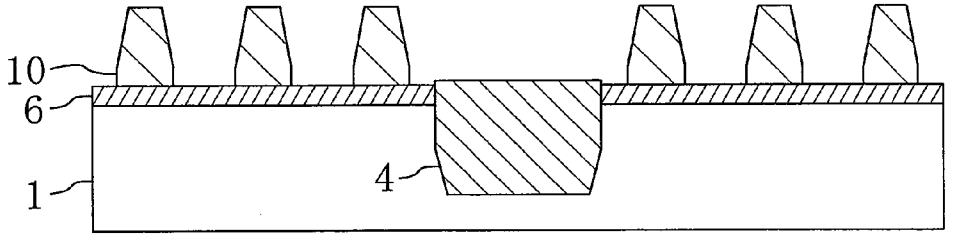


FIG. 12B

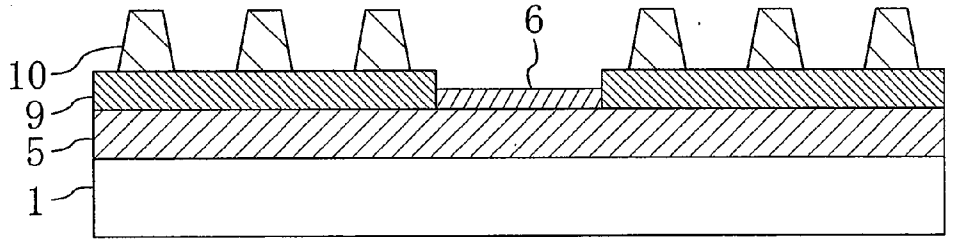


FIG. 13A

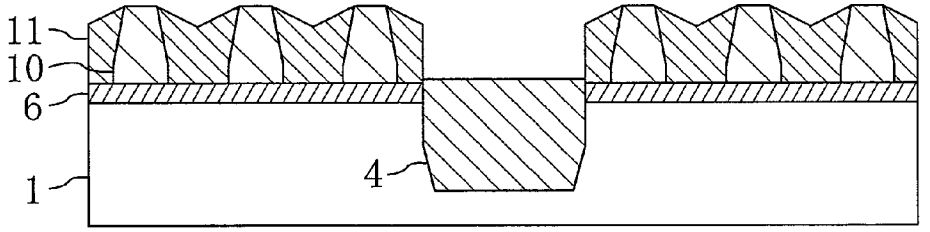


FIG. 13B

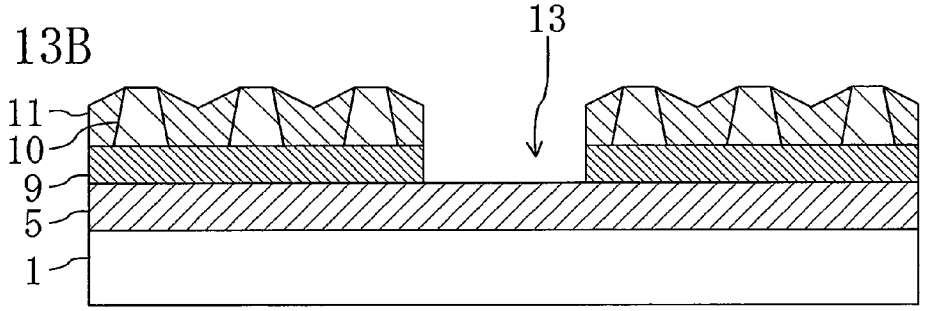


FIG. 14A

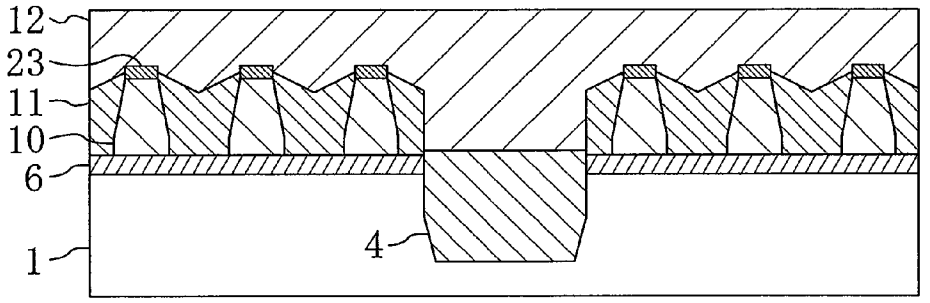


FIG. 14B

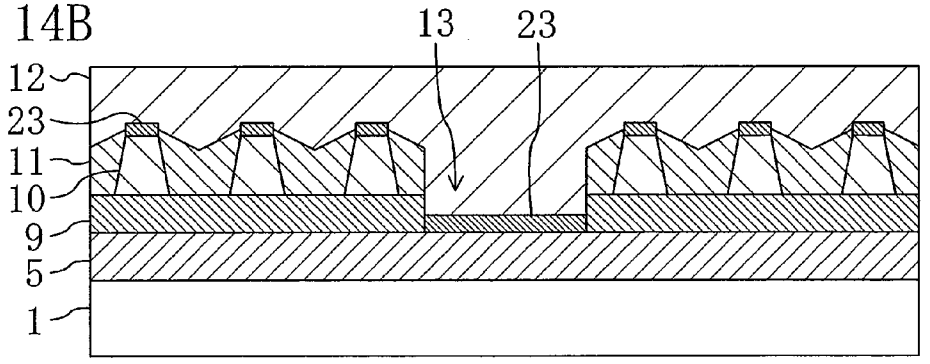


FIG. 15

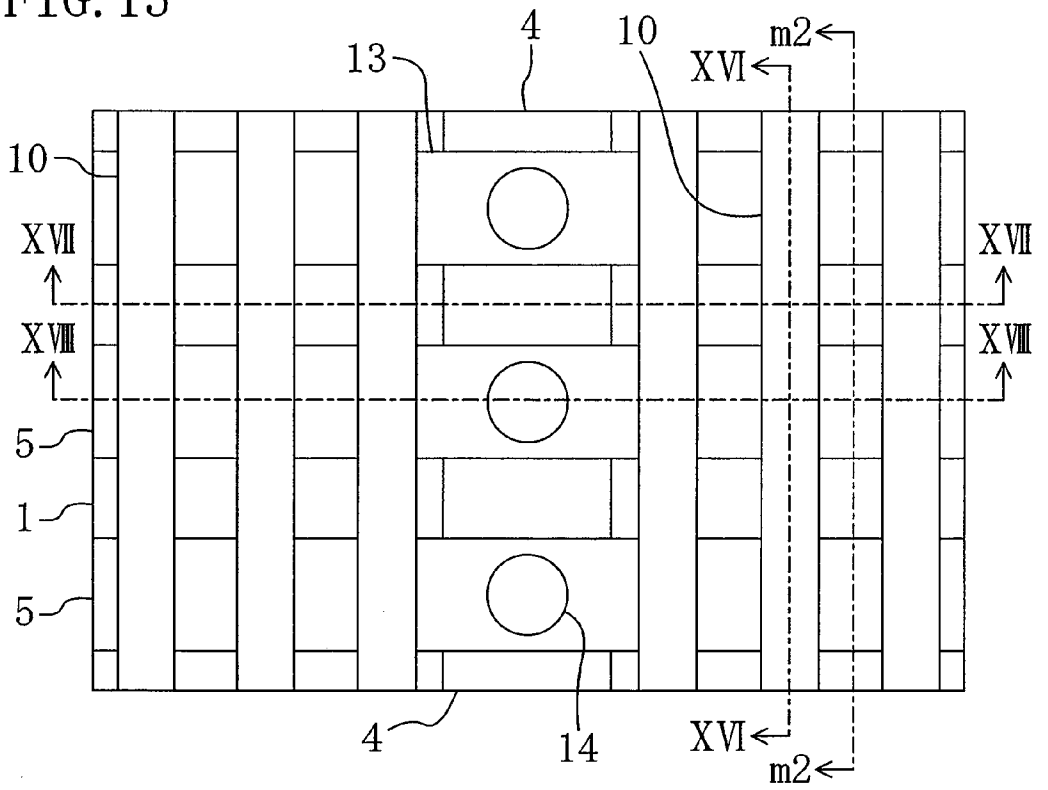

4
10
m2
13
XVI
10
XVII
XVII
XVIII
XVIII
5
1
5
4
14
XVI
m2

FIG. 16

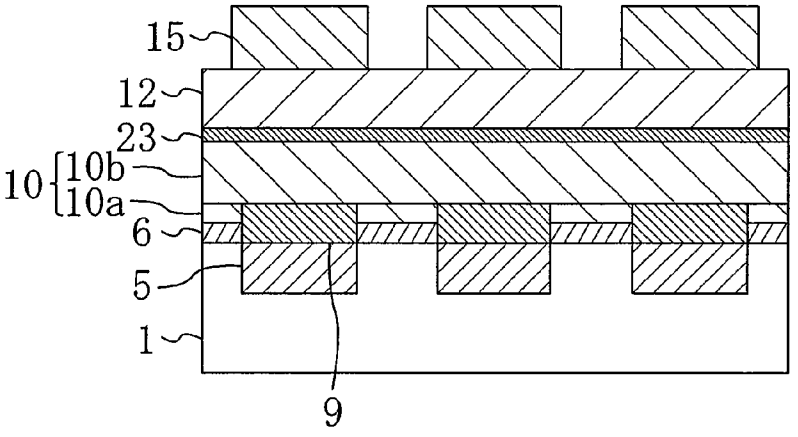

15
12
23
10
10b
10a
6
5
1
9

FIG. 17

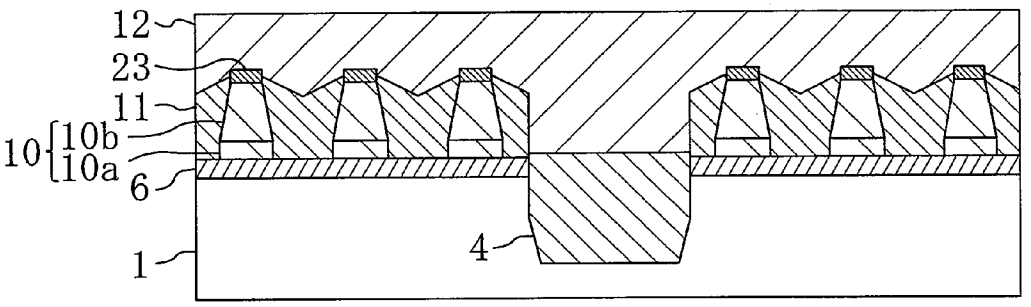


FIG. 18

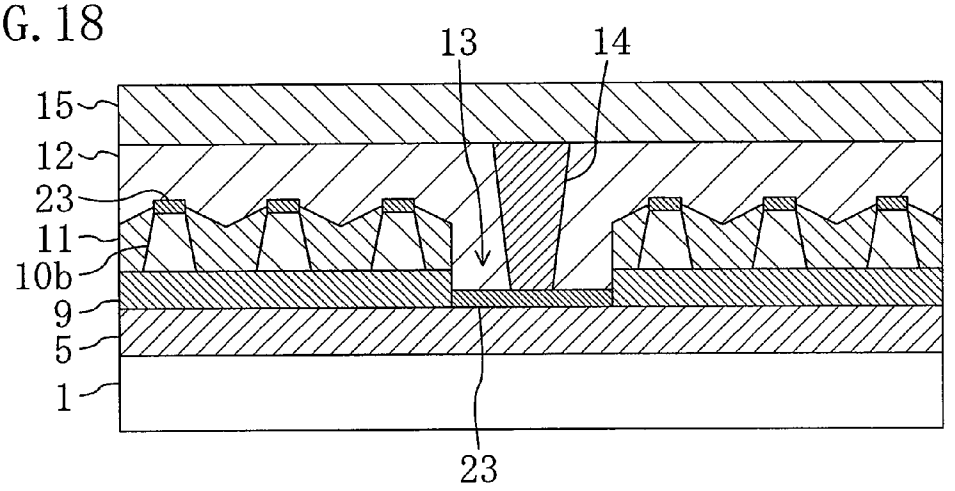


FIG. 19A

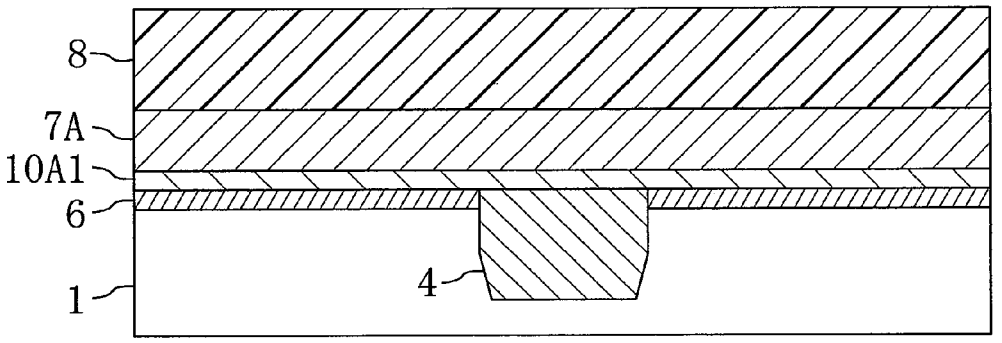


FIG. 19B

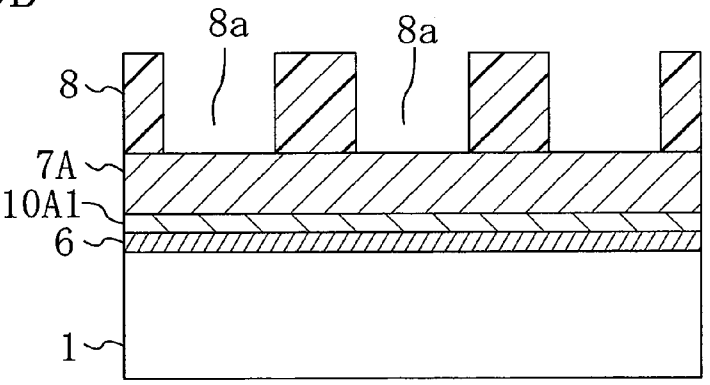


FIG. 19C

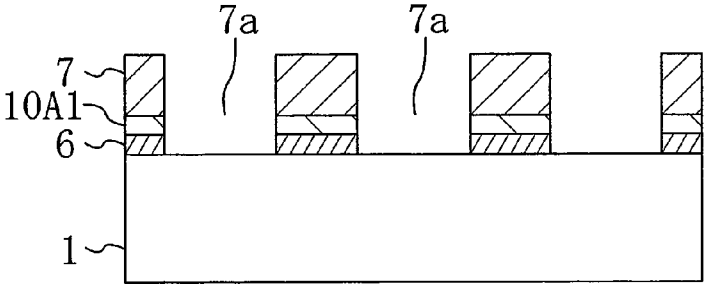


FIG. 20A

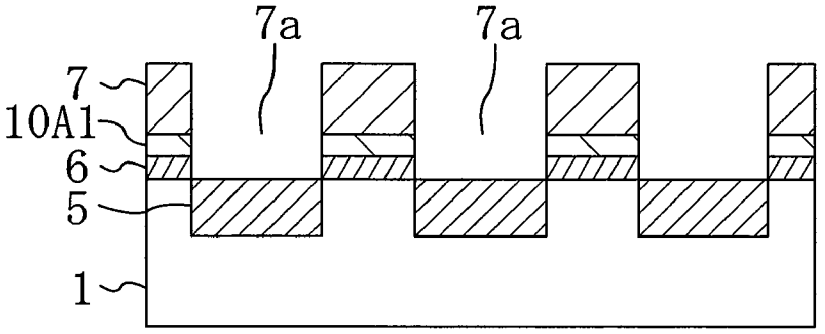


FIG. 20B

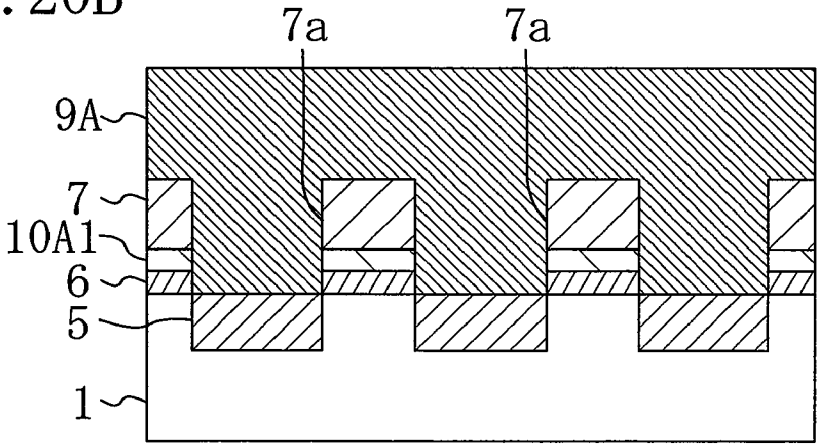


FIG. 20C

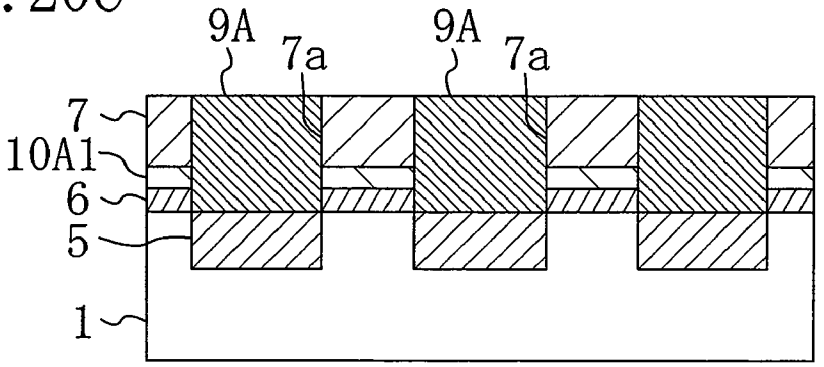


FIG. 21A

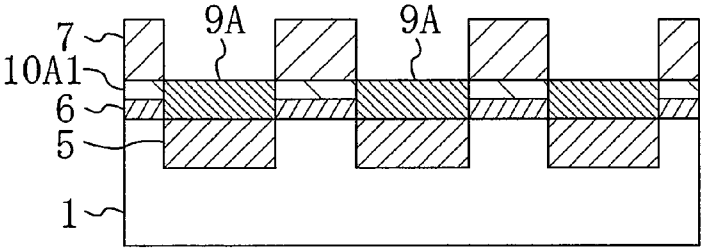


FIG. 21B

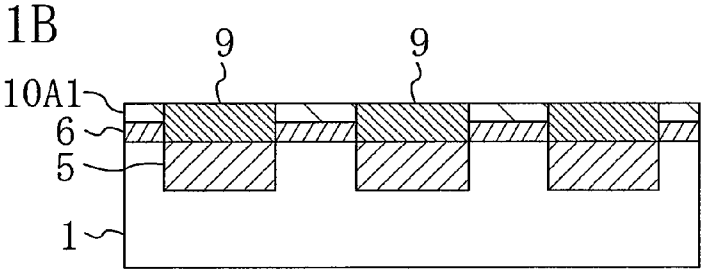


FIG. 22A

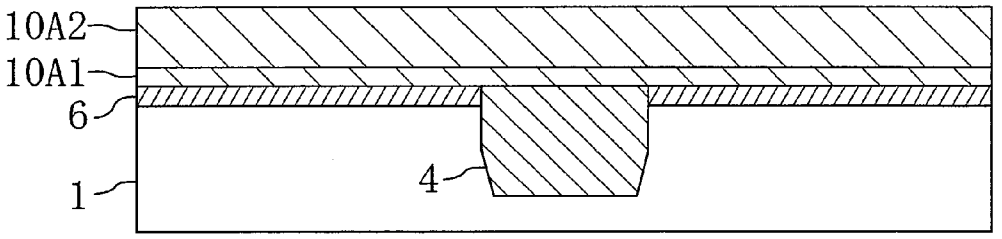


FIG. 22B

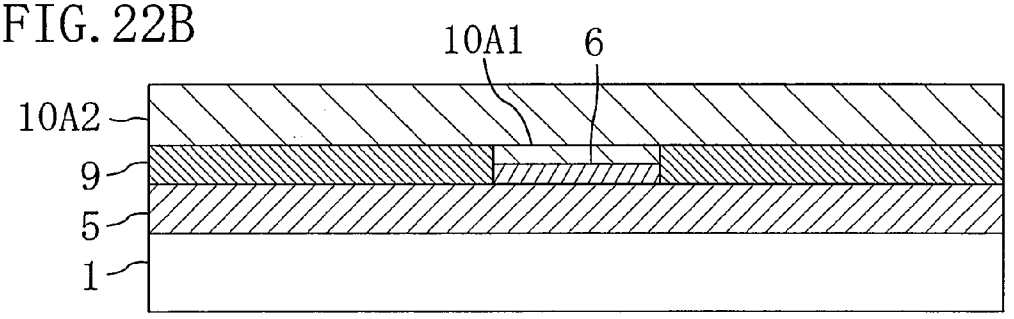


FIG. 23A

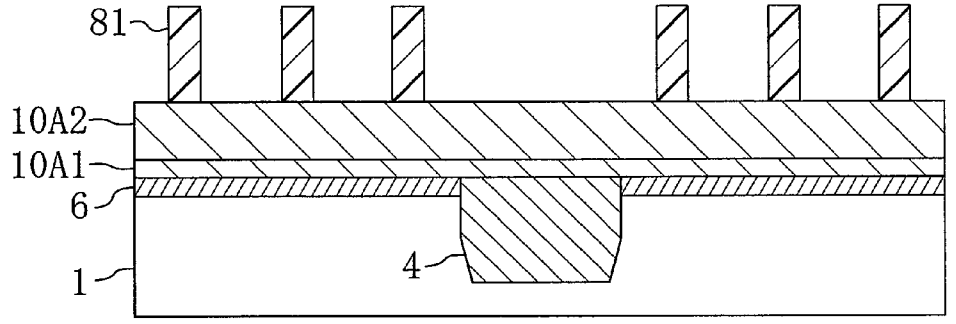


FIG. 23B

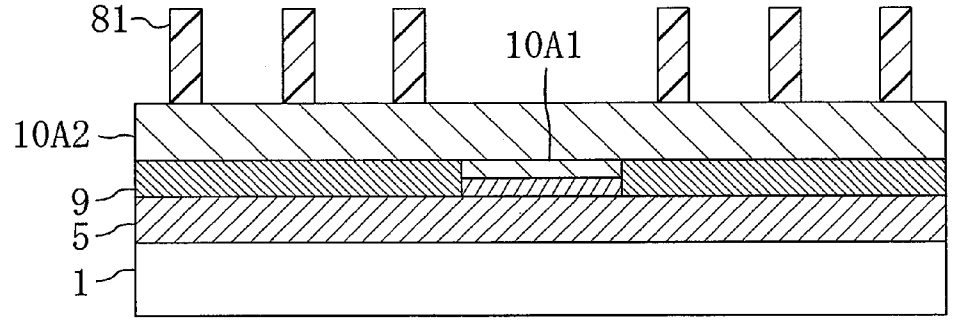


FIG. 24A

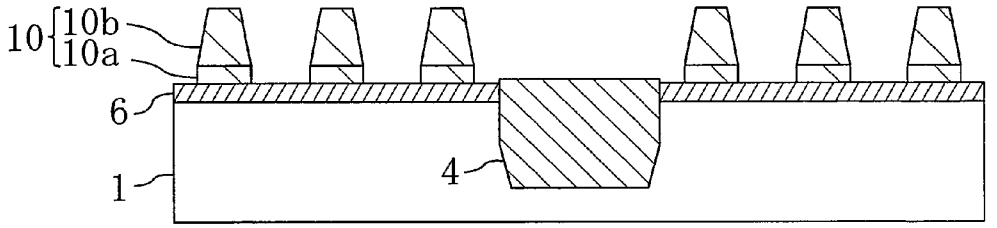


FIG. 24B

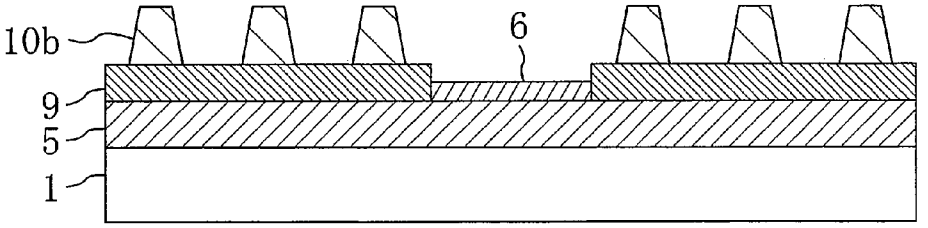


FIG. 25A

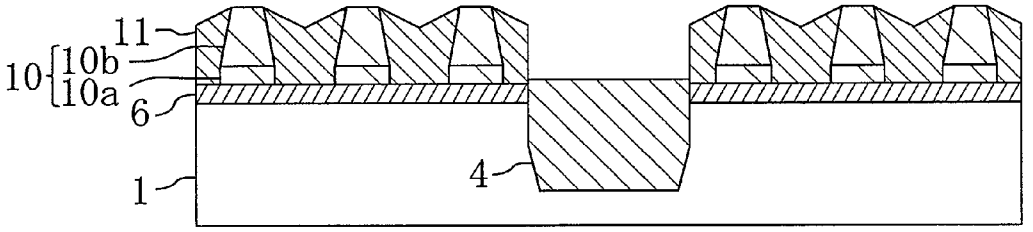


FIG. 25B

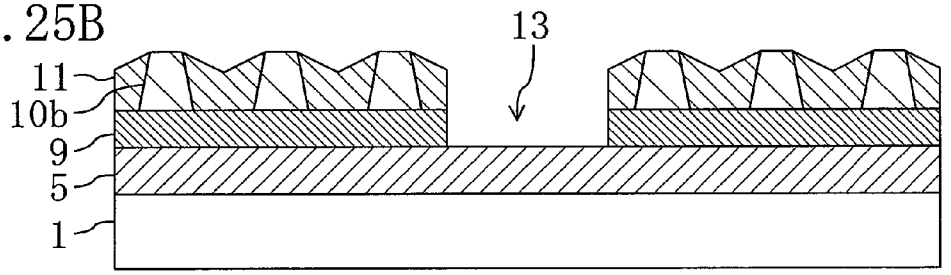


FIG. 26A

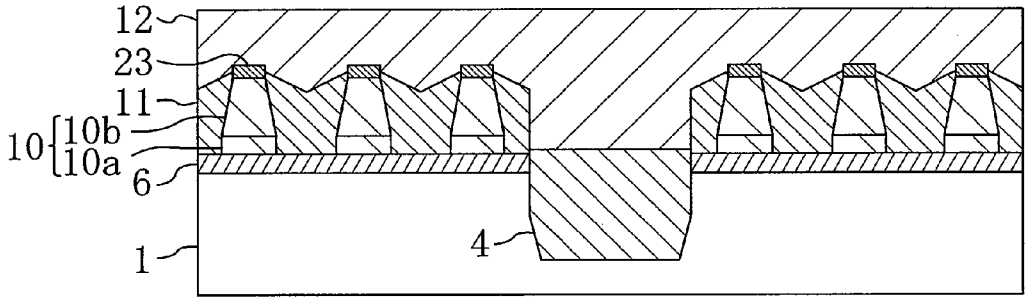


FIG. 26B

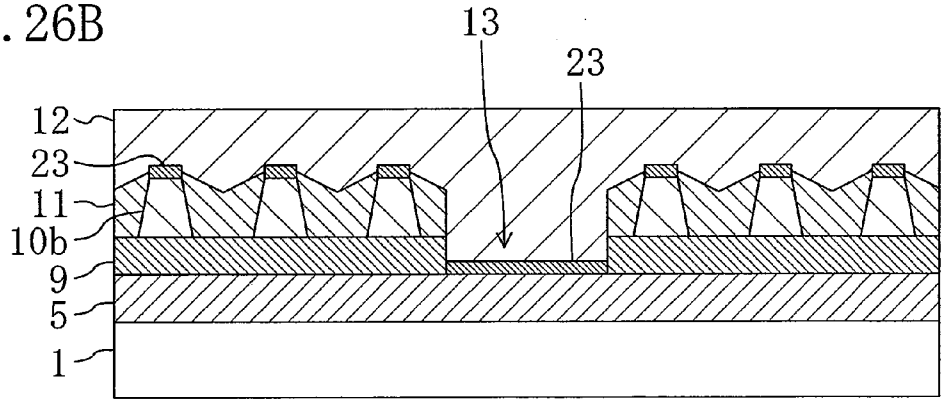


FIG. 27

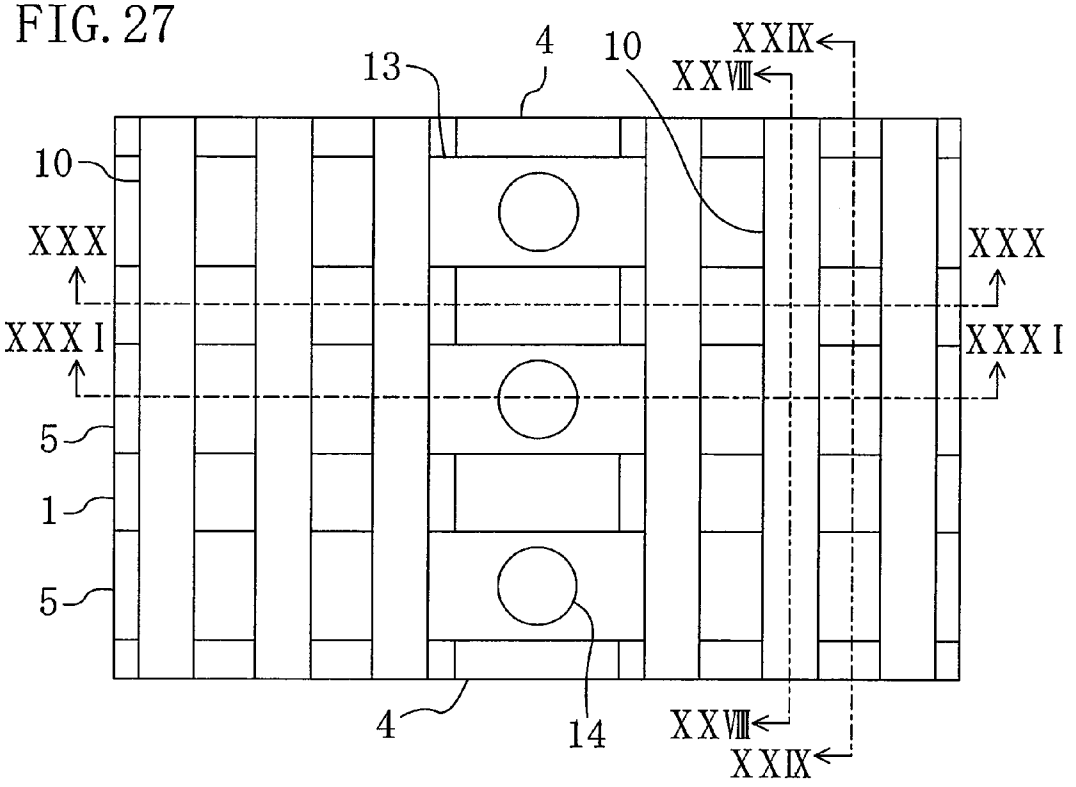

13
4
10
XXIX
XXVIII
10
XXX
XXXI
5
1
5
XXX
XXXI
4
14
XXVIII
XXIX

FIG. 28

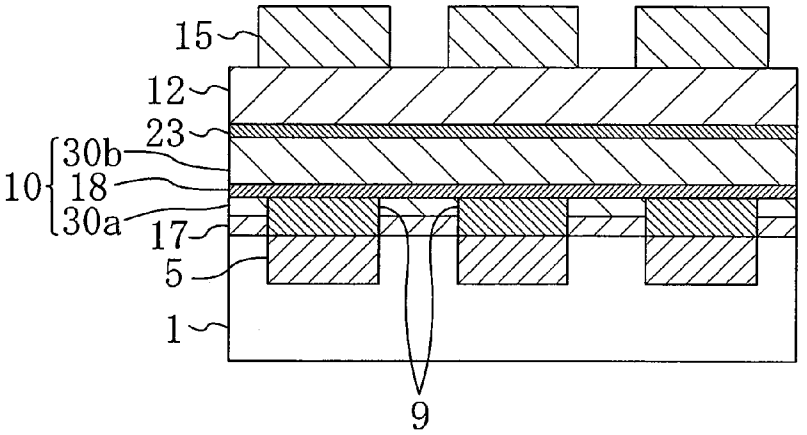

15
12
23
30b
10
18
30a
17
5
1
9

FIG. 29

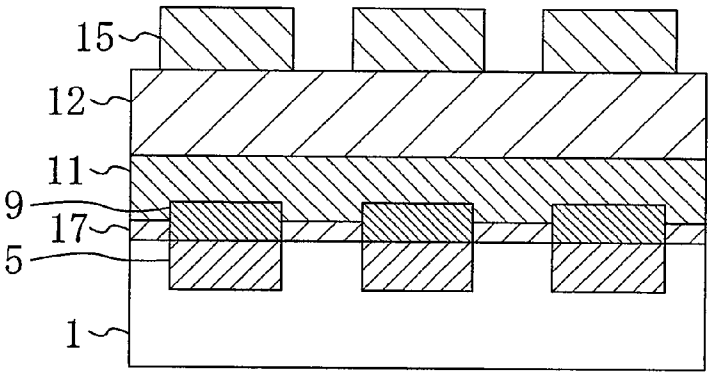


FIG. 30

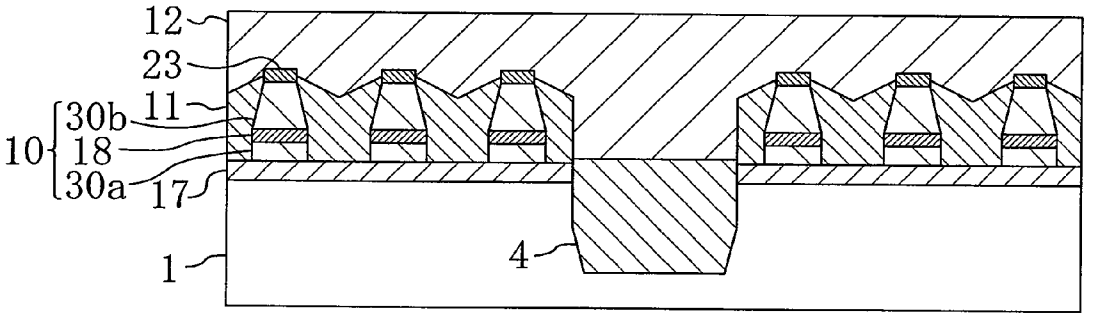


FIG. 31

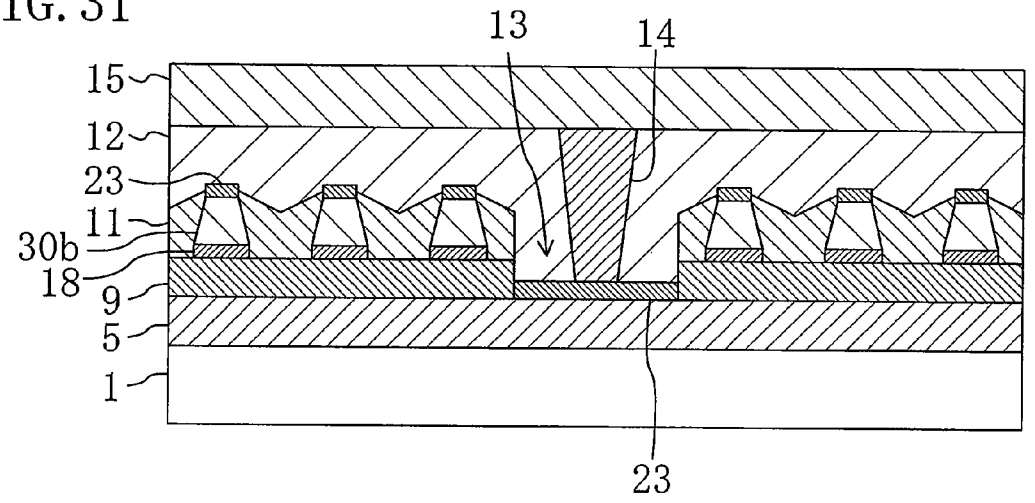


FIG. 32A

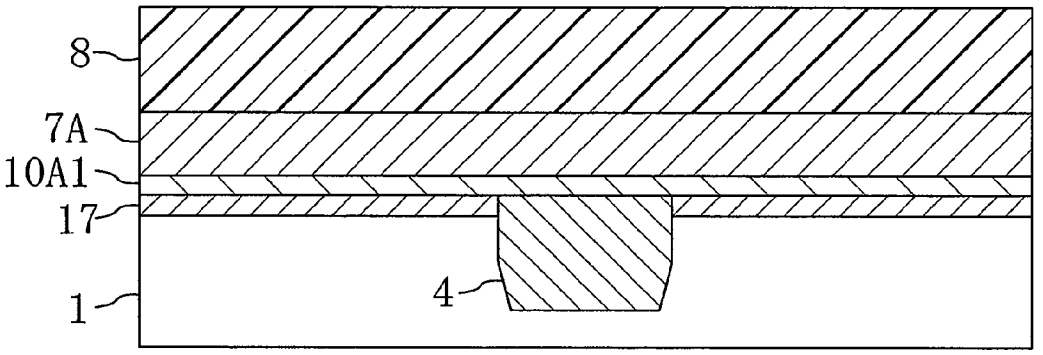


FIG. 32B

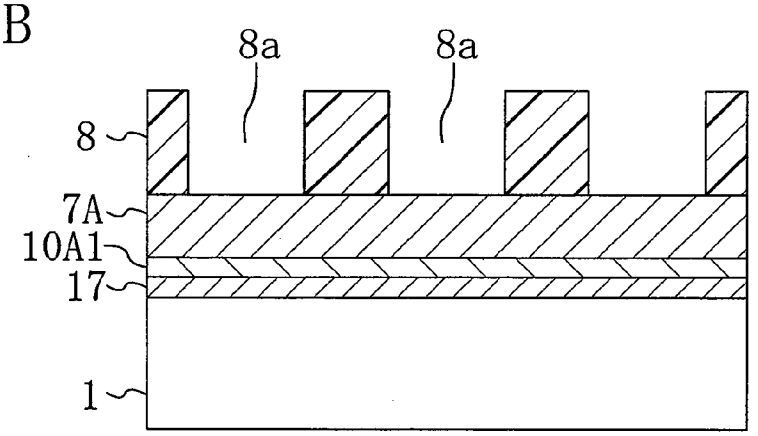


FIG. 32C

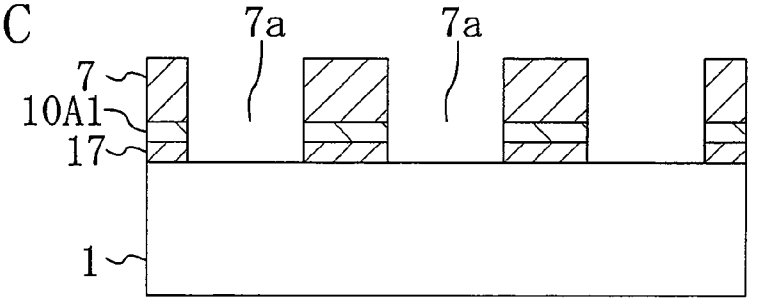


FIG. 33A

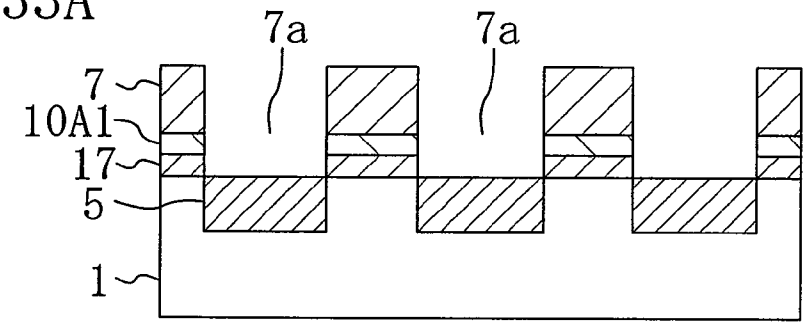


FIG. 33B

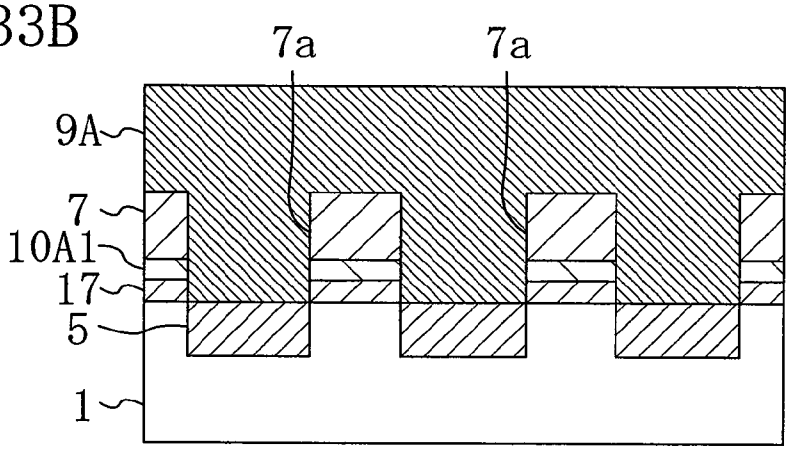


FIG. 33C

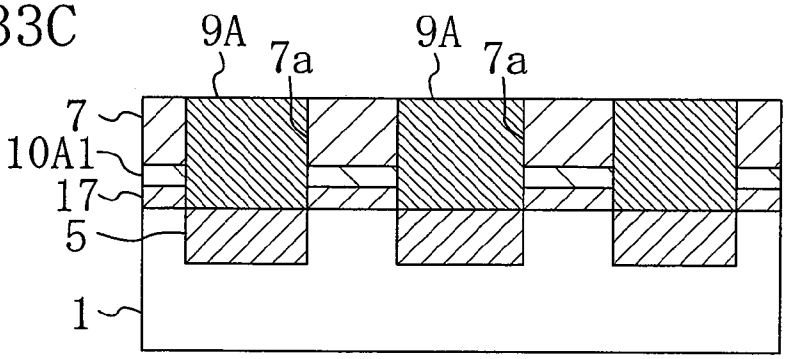


FIG. 34A

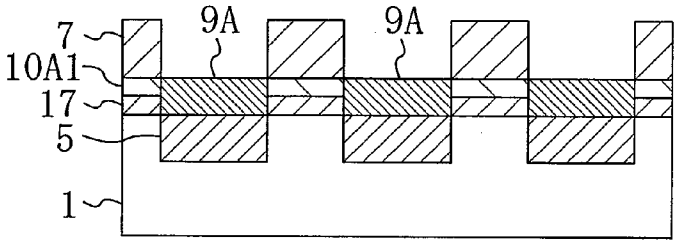


FIG. 34B

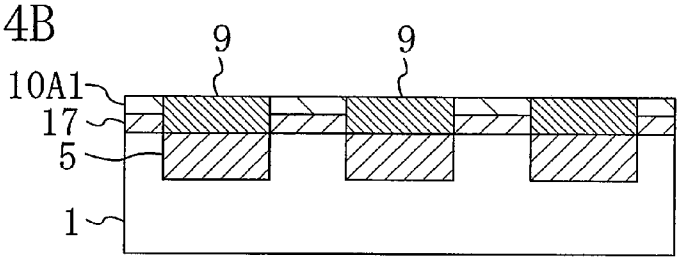


FIG. 35A

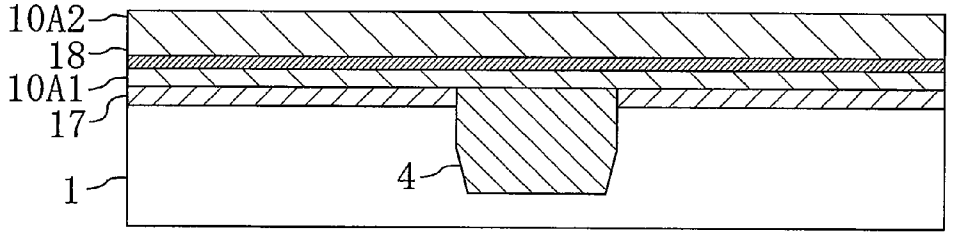


FIG. 35B

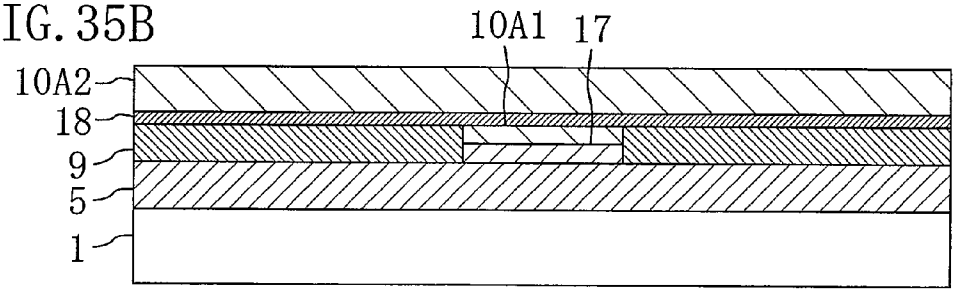


FIG. 36A

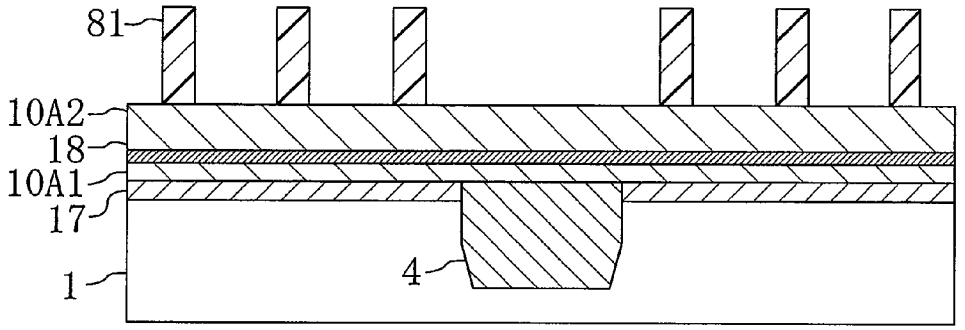


FIG. 36B

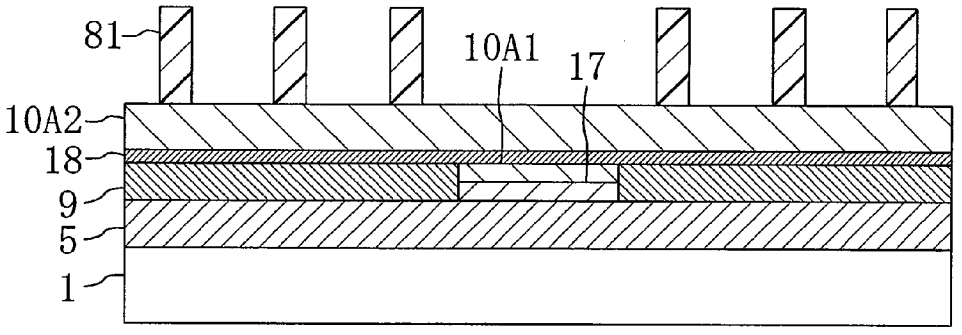


FIG. 37A

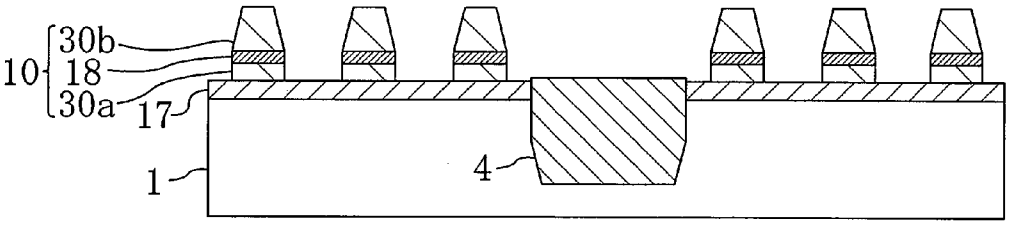


FIG. 37B

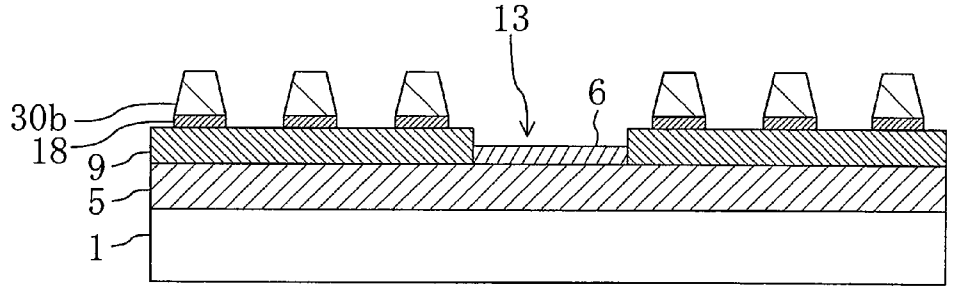


FIG. 38A

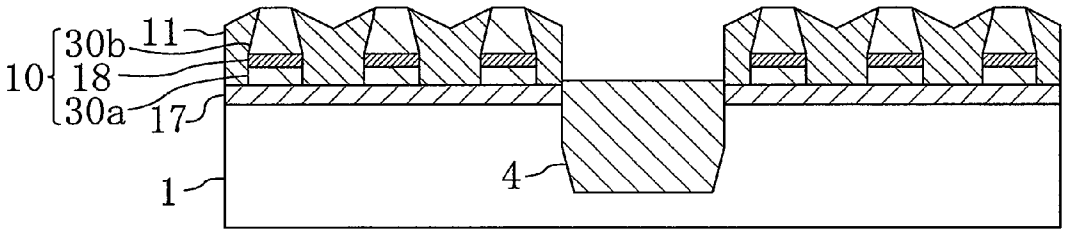


FIG. 38B

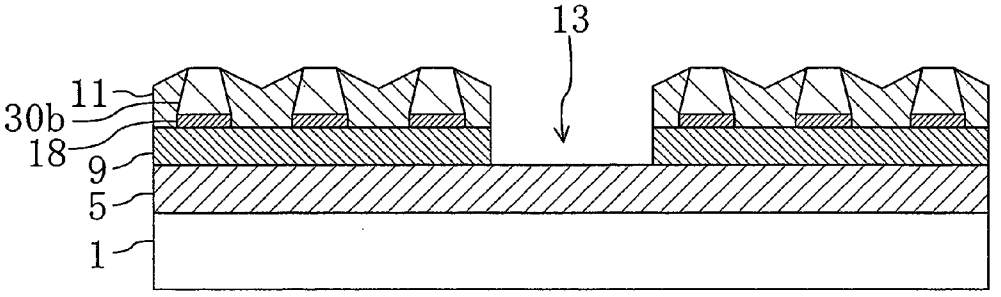


FIG. 39A

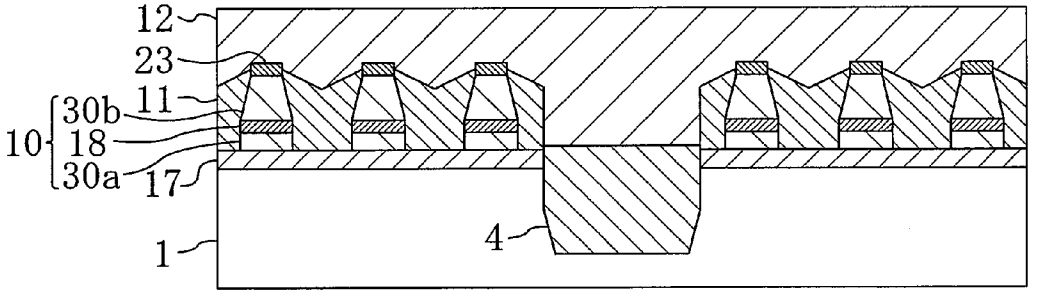
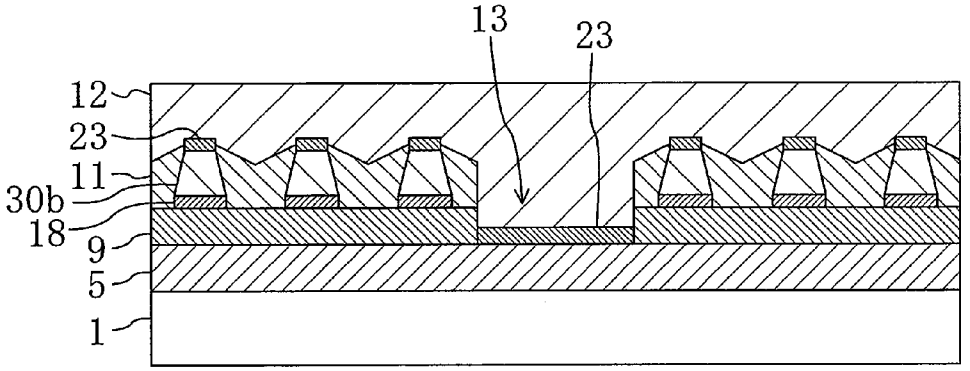


FIG. 39B



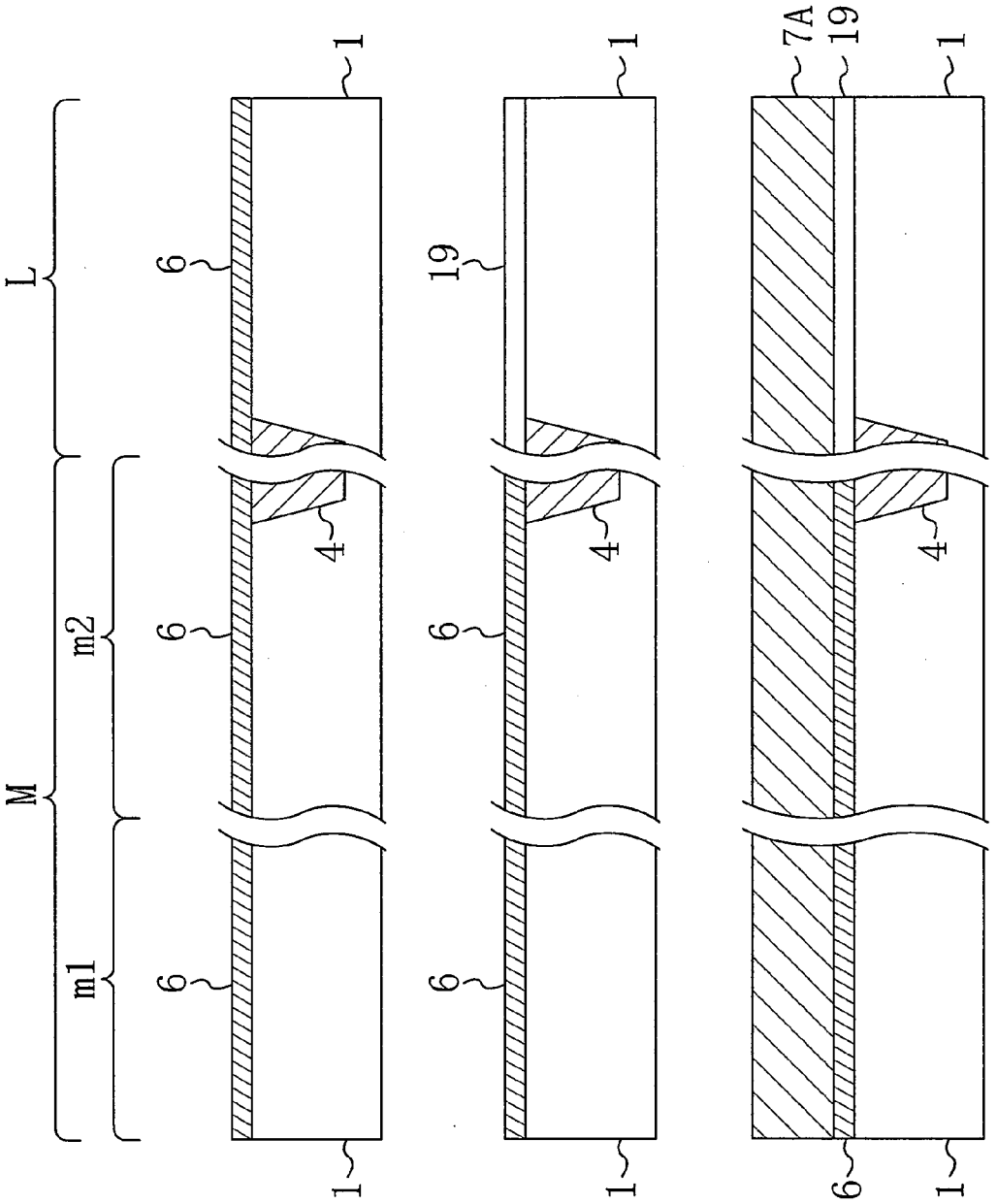


FIG. 40A

FIG. 40B

FIG. 40C

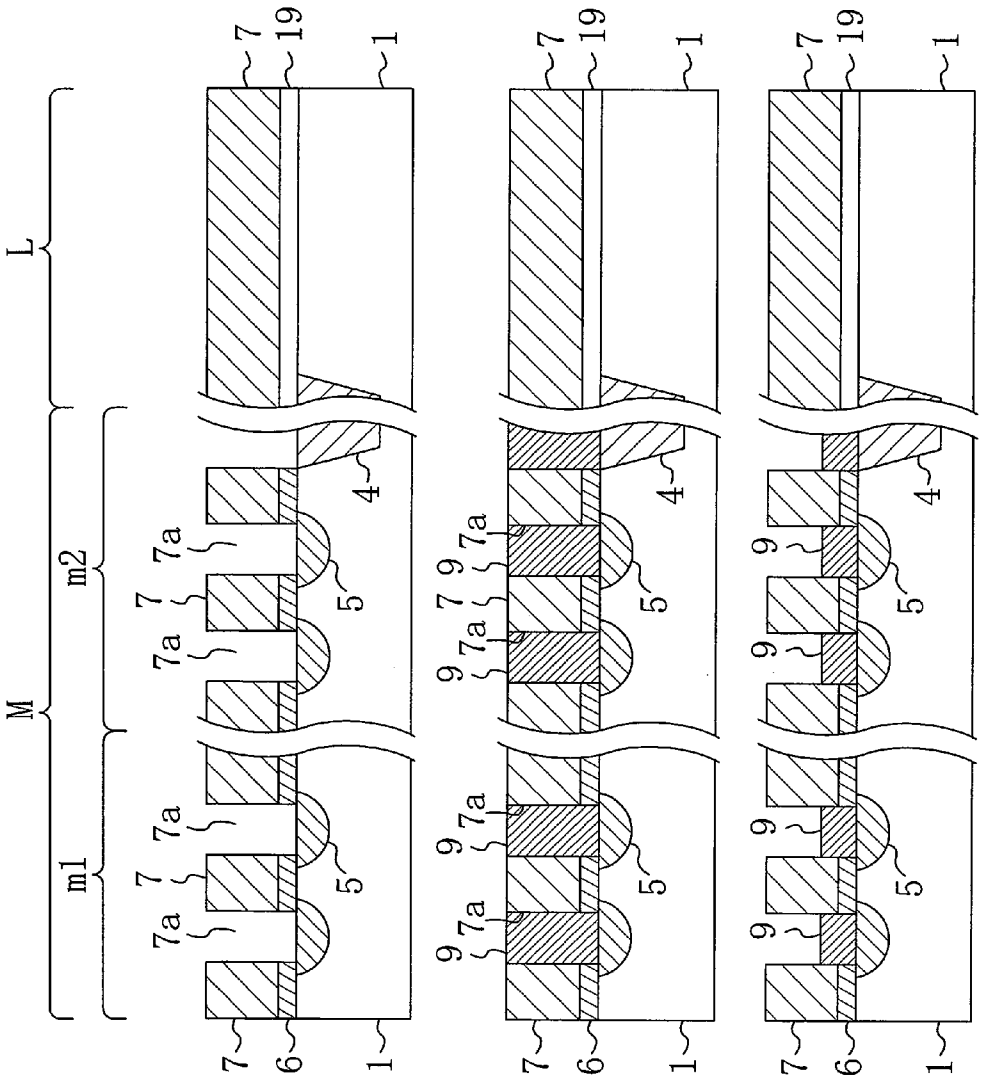


FIG. 41A

FIG. 41B

FIG. 41C

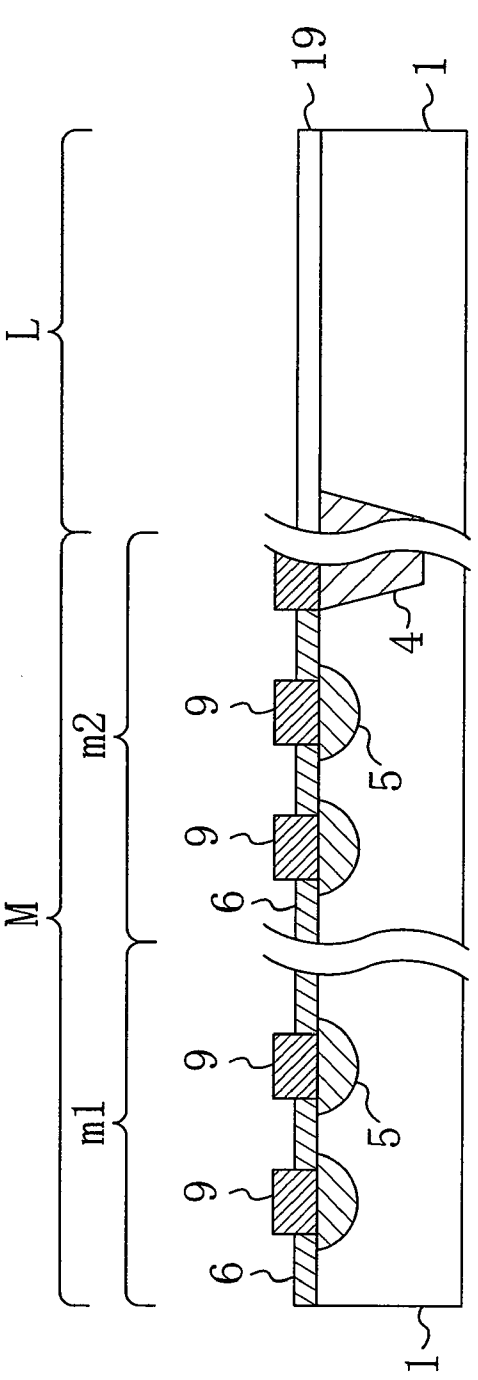


FIG. 42A

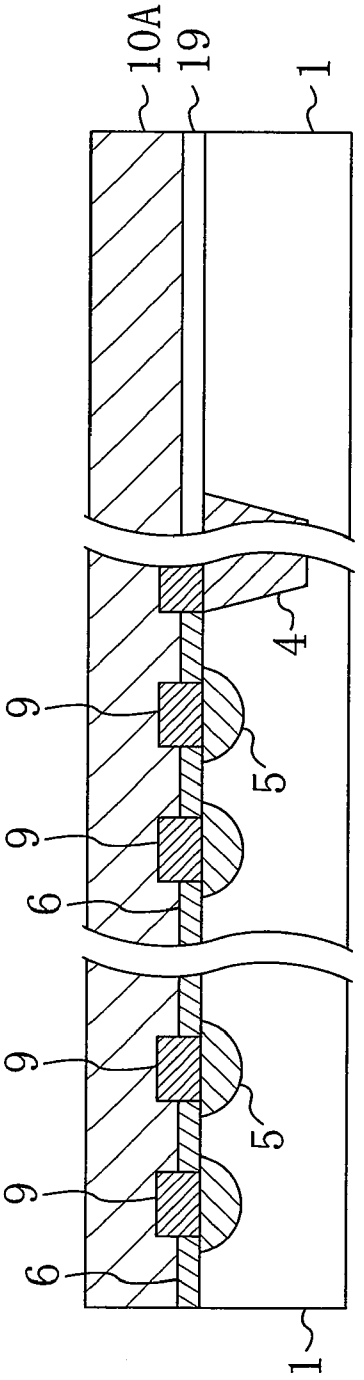


FIG. 42B

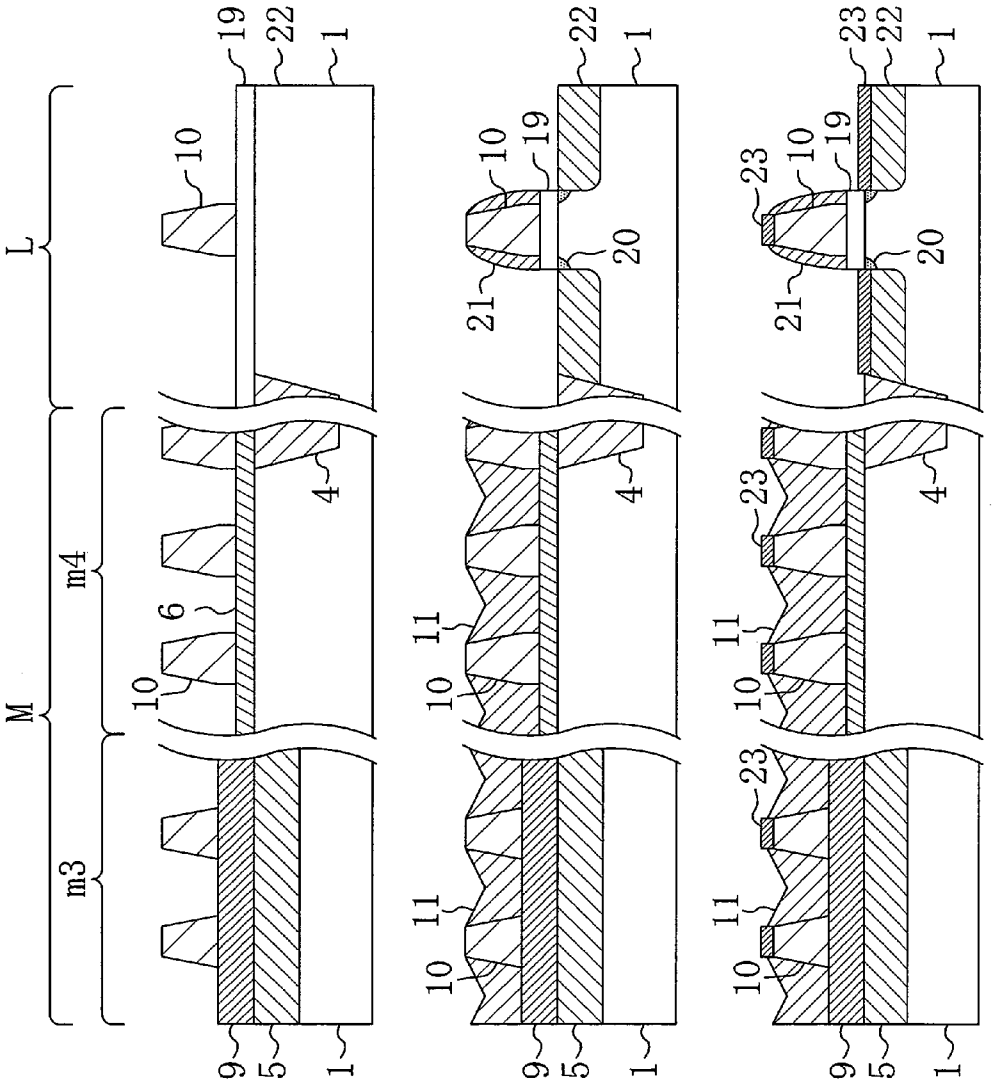


FIG. 43A

FIG. 43B

FIG. 43C

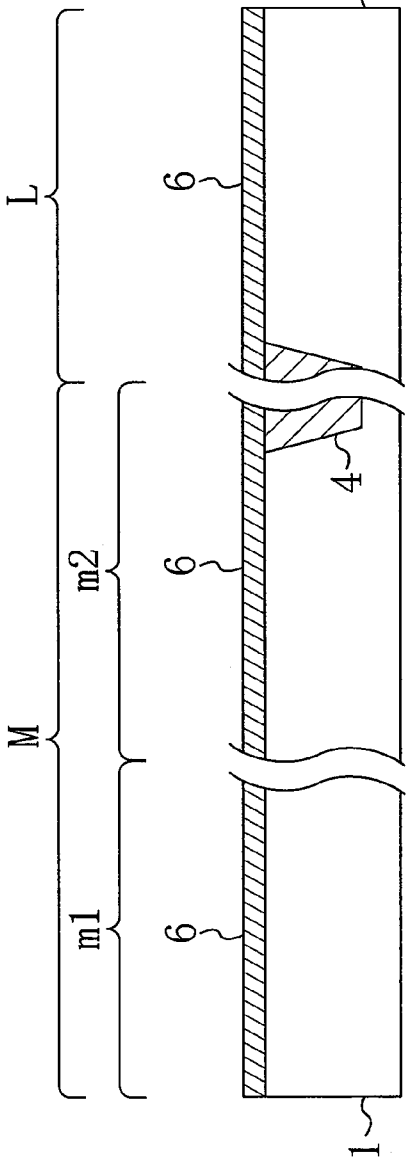


FIG. 44A

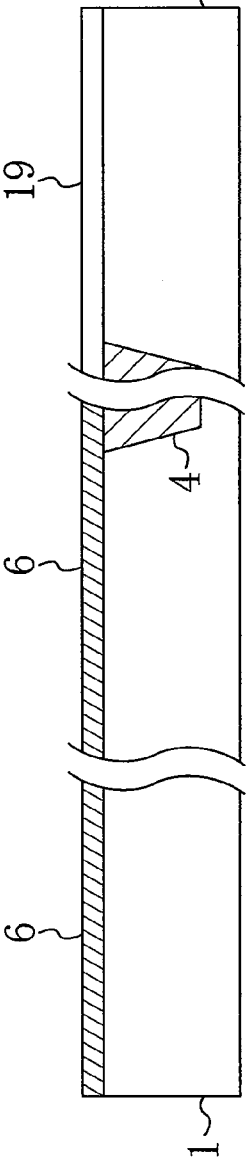


FIG. 44B

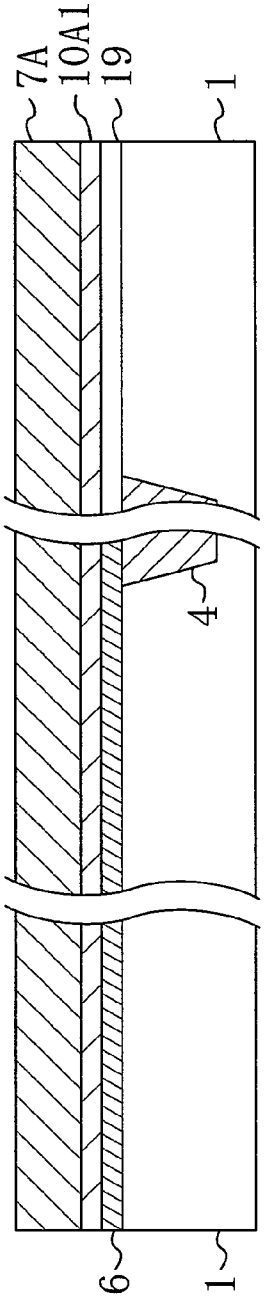


FIG. 44C

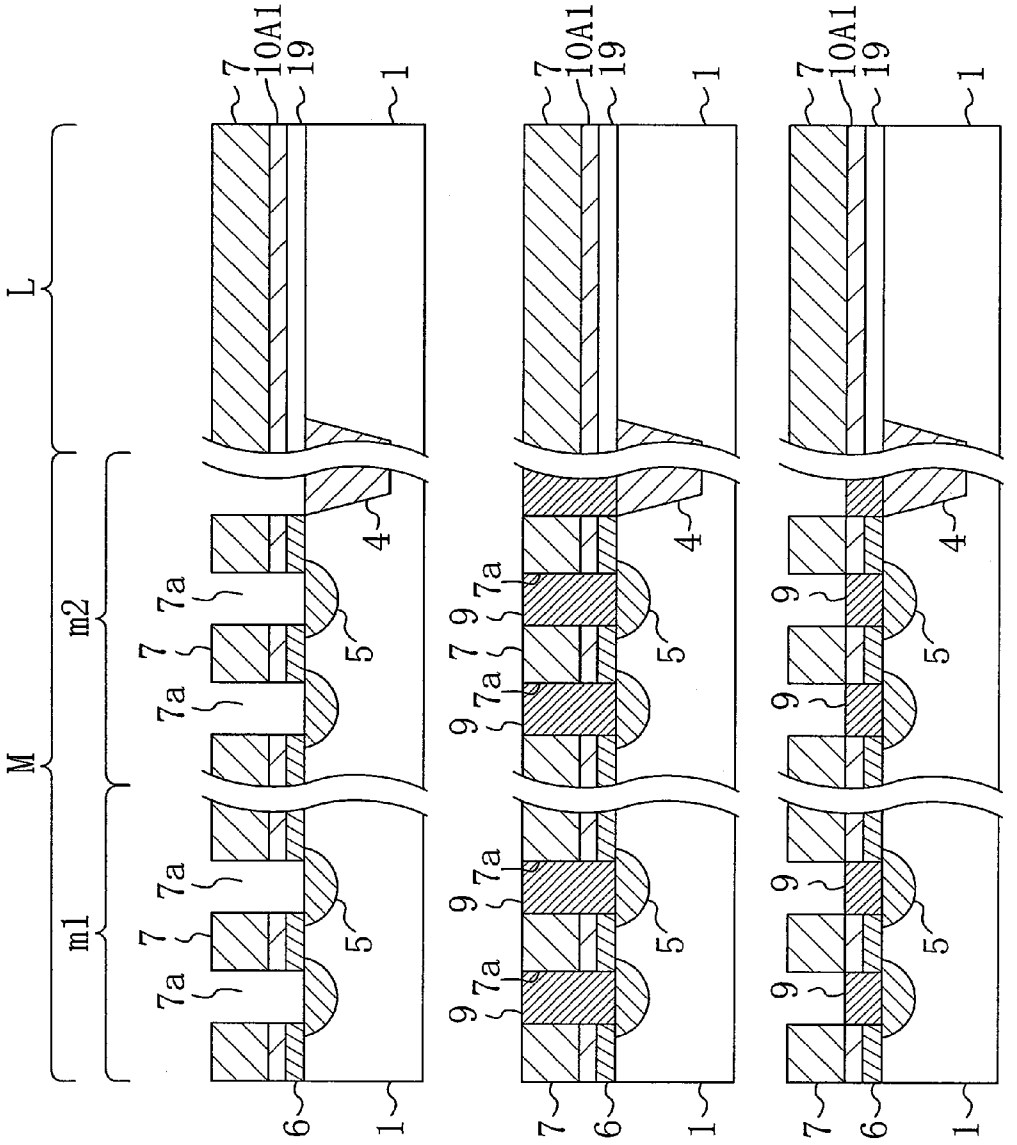


FIG. 45A

FIG. 45B

FIG. 45C

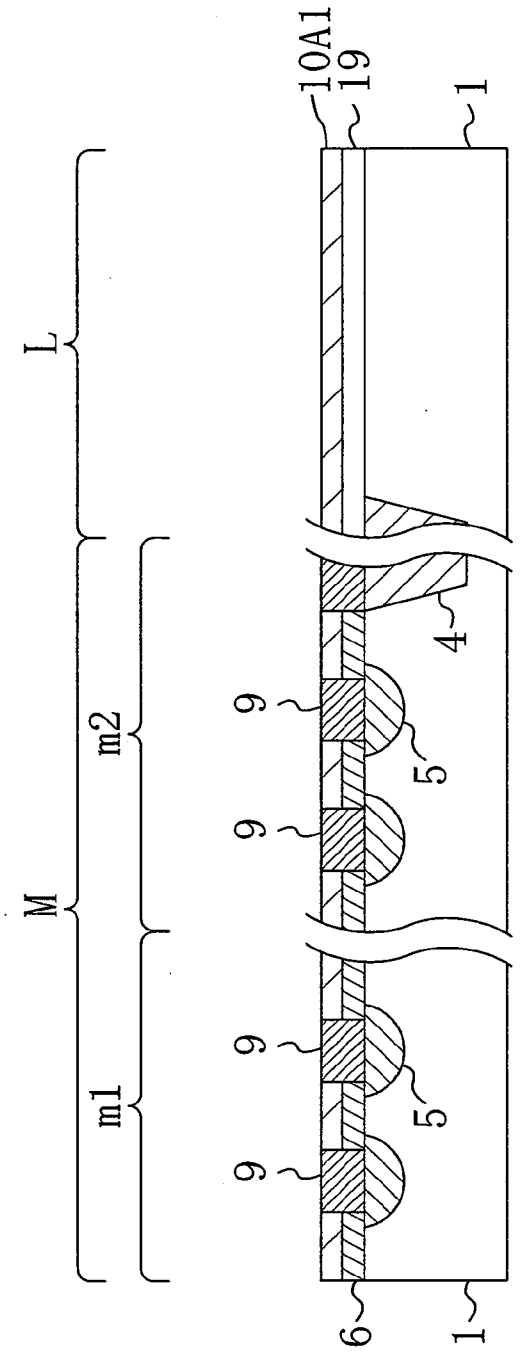


FIG. 46A

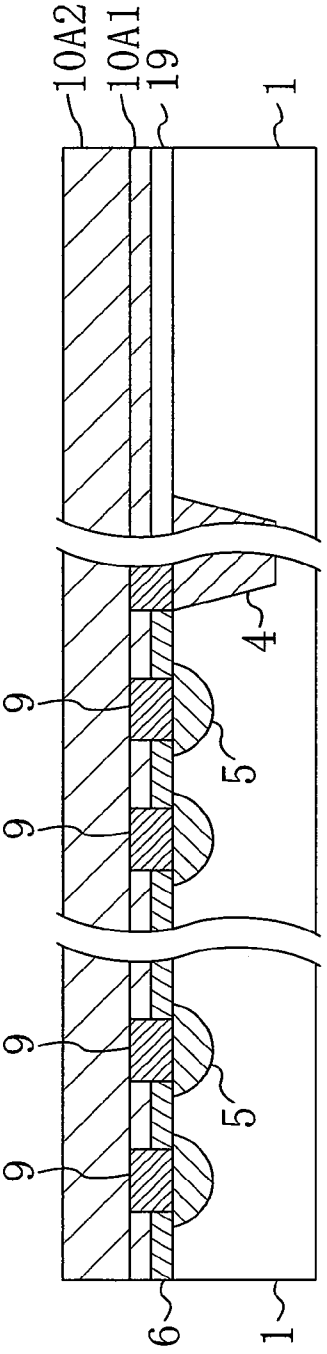


FIG. 46B

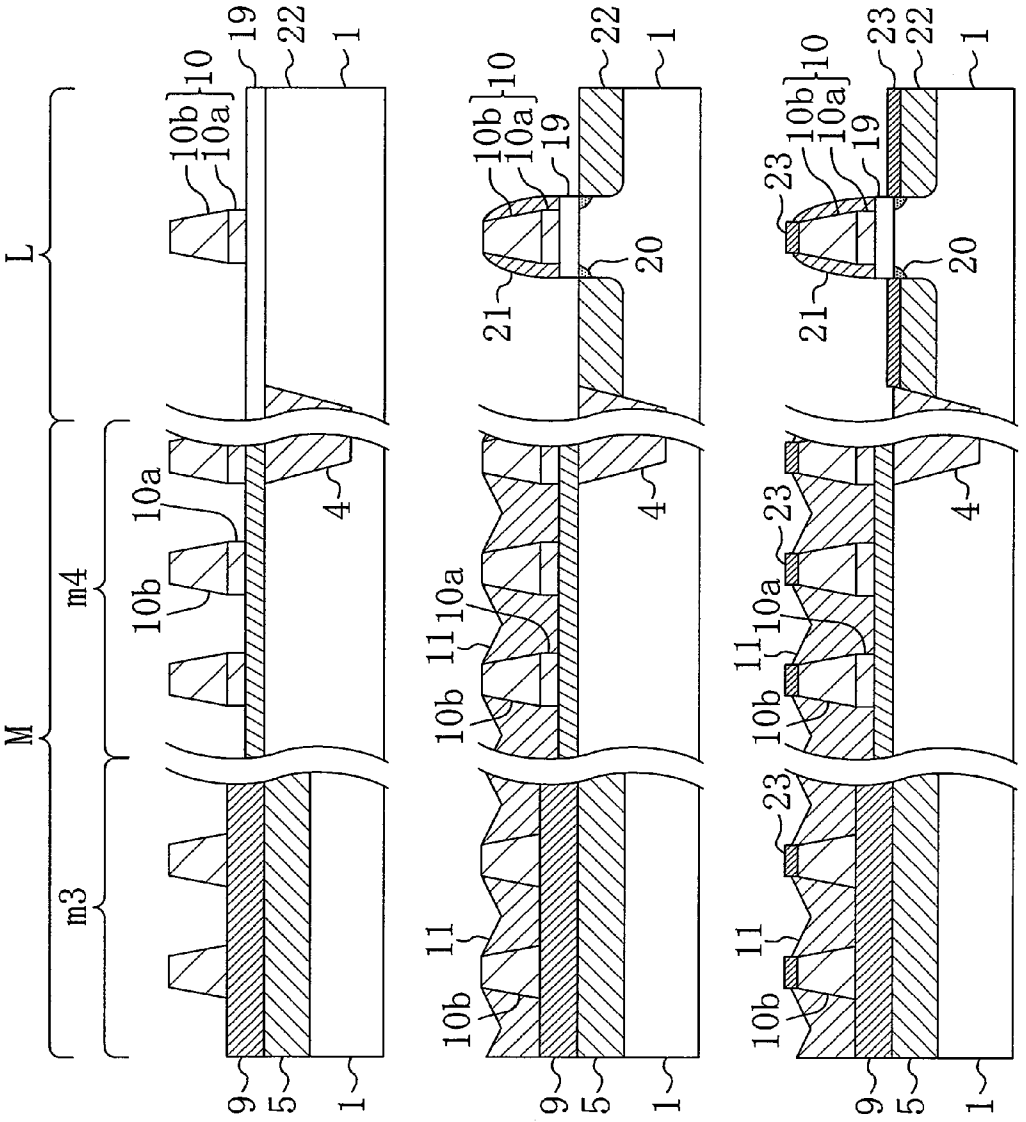


FIG. 47A

FIG. 47B

FIG. 47C

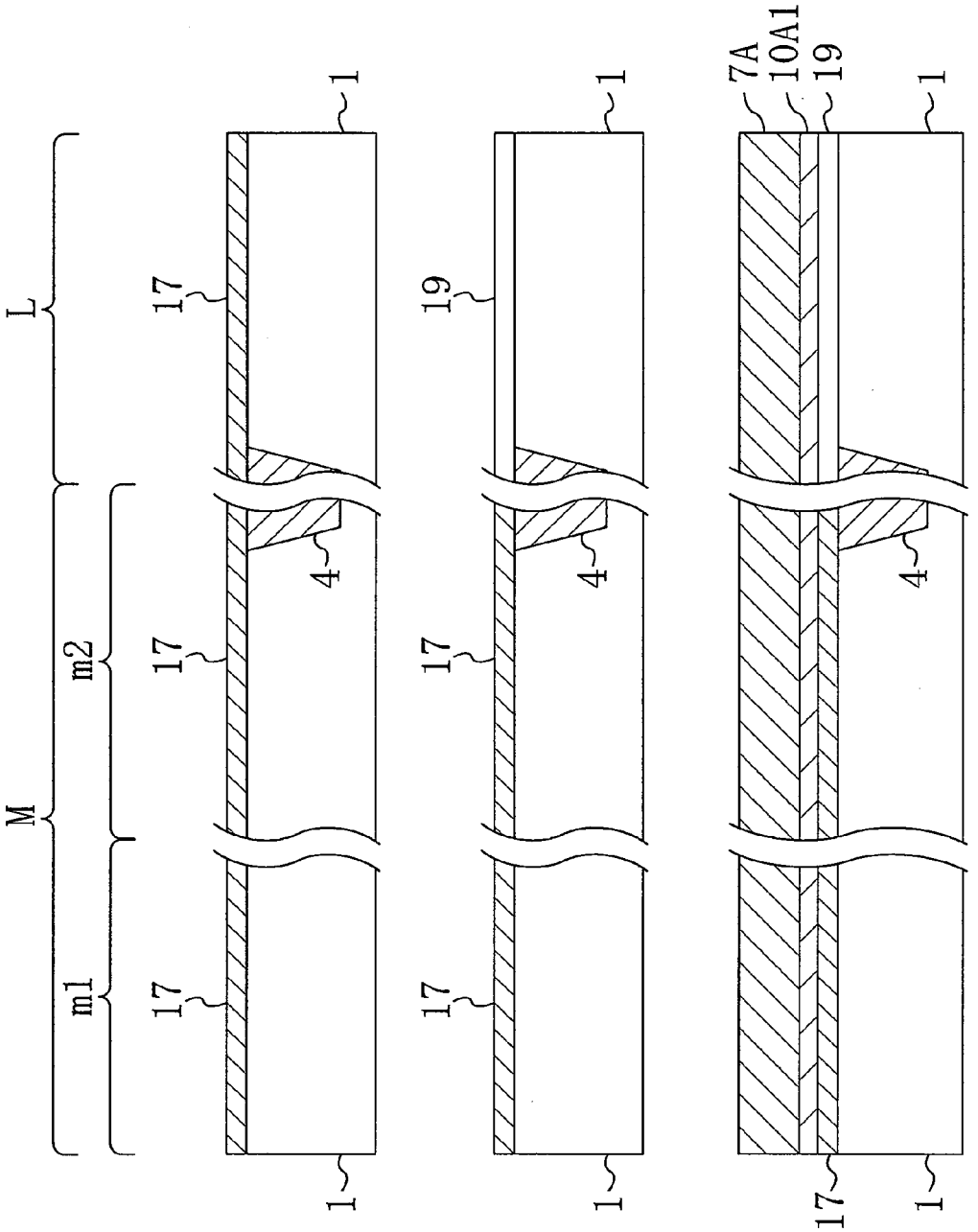


FIG. 48A

FIG. 48B

FIG. 48C

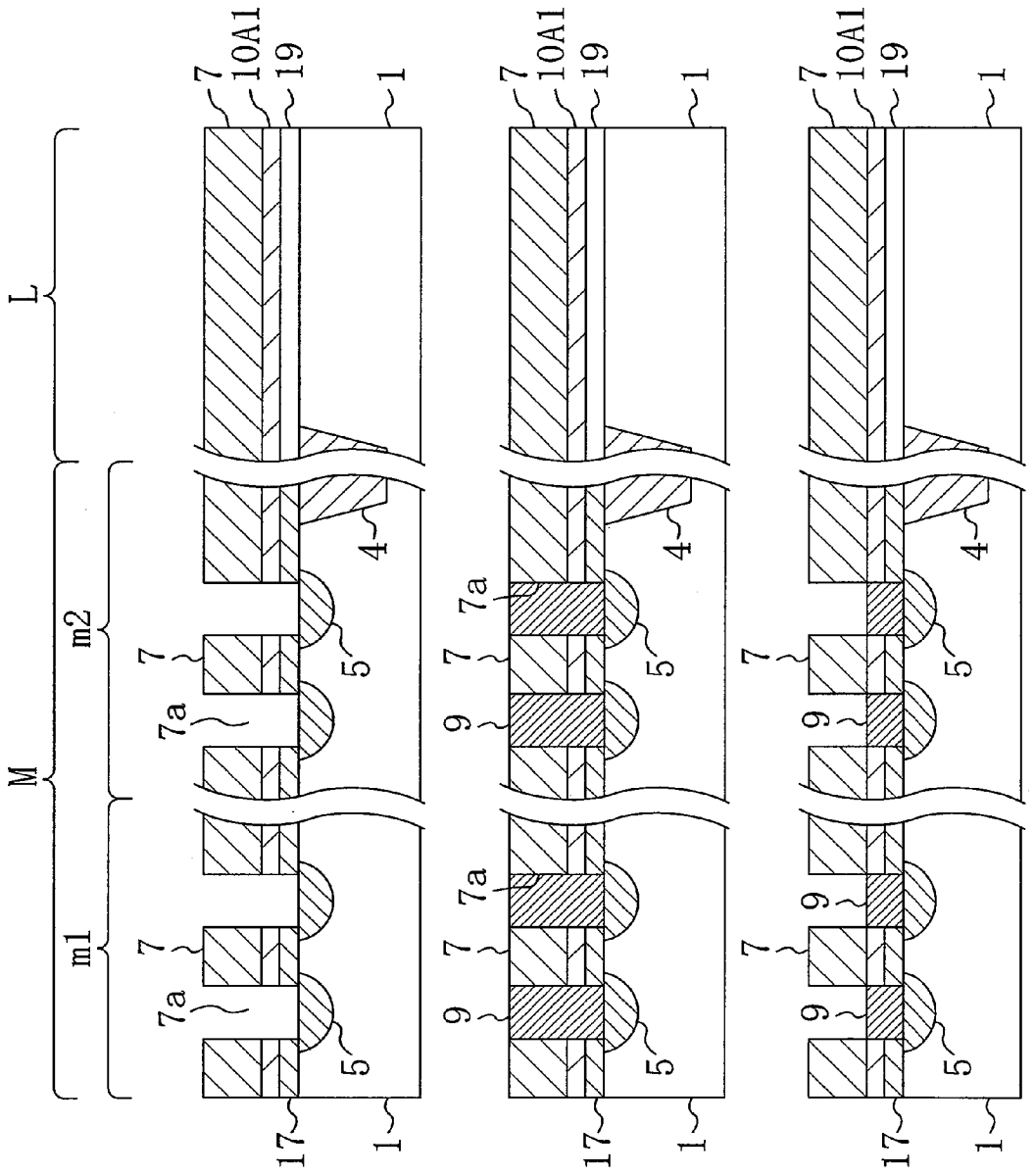


FIG. 49A

FIG. 49B

FIG. 49C

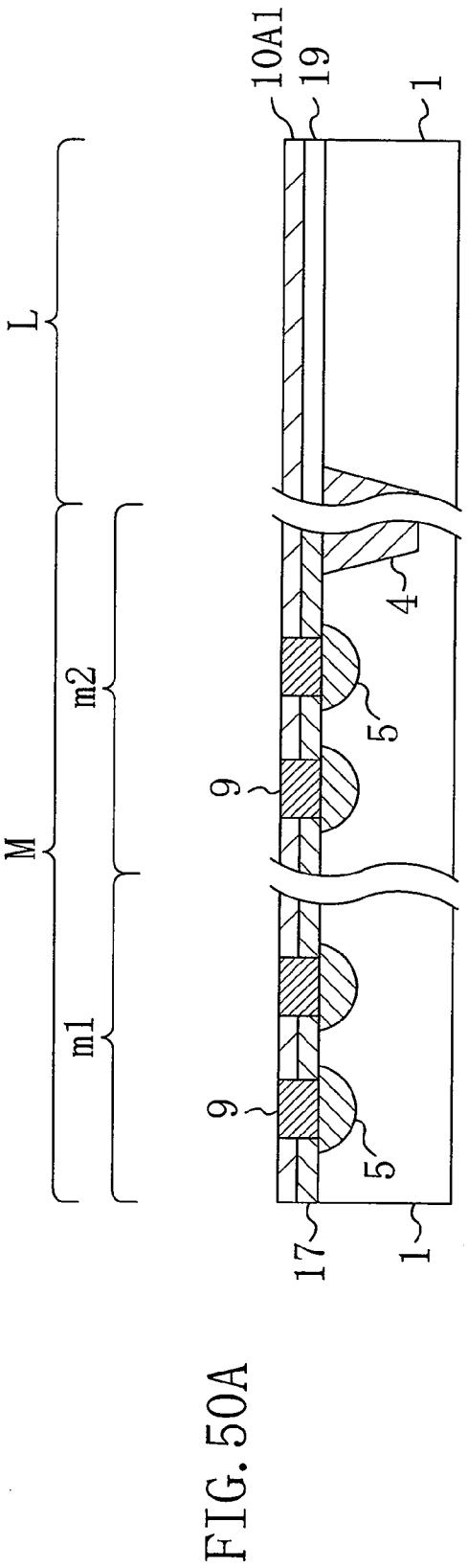


FIG. 50A

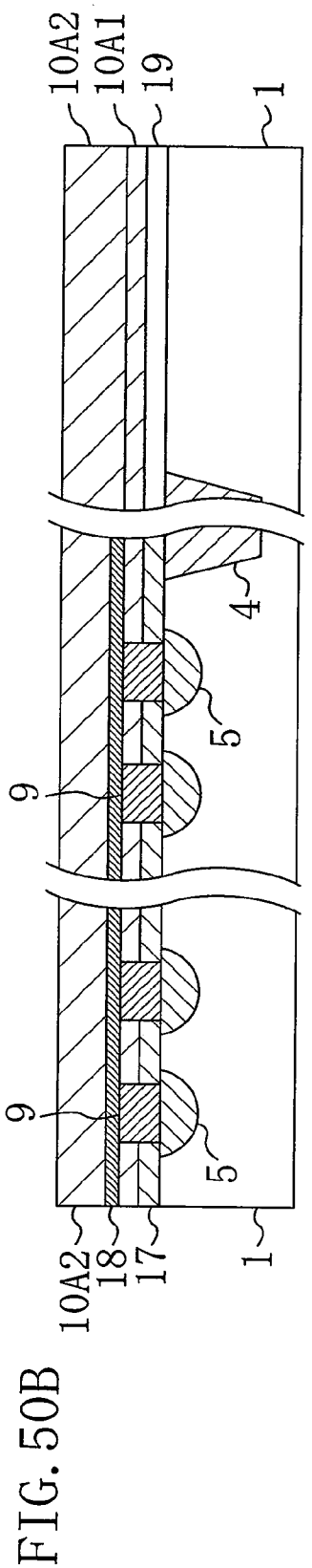


FIG. 50B

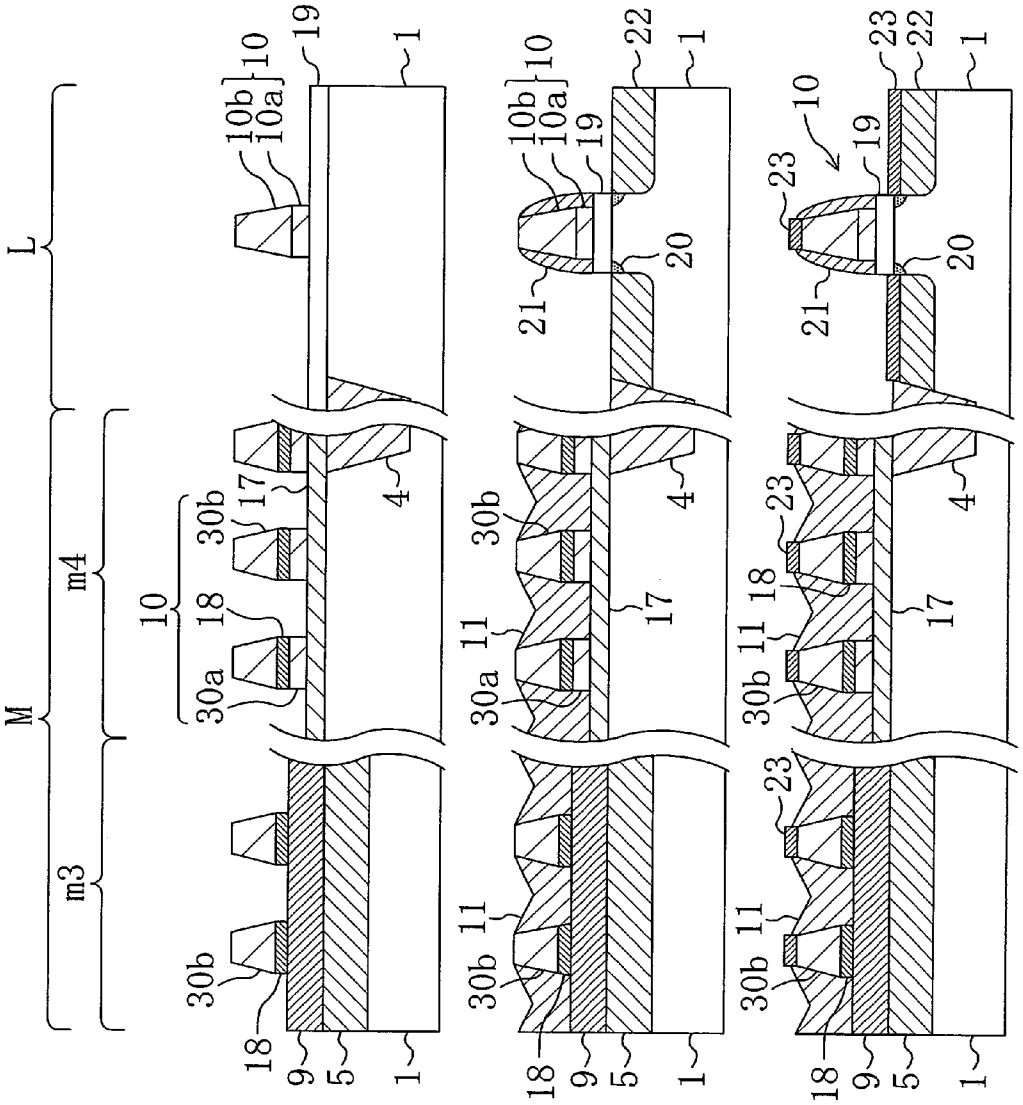


FIG. 51A

FIG. 51B

FIG. 51C

FIG. 52
PRIOR ART

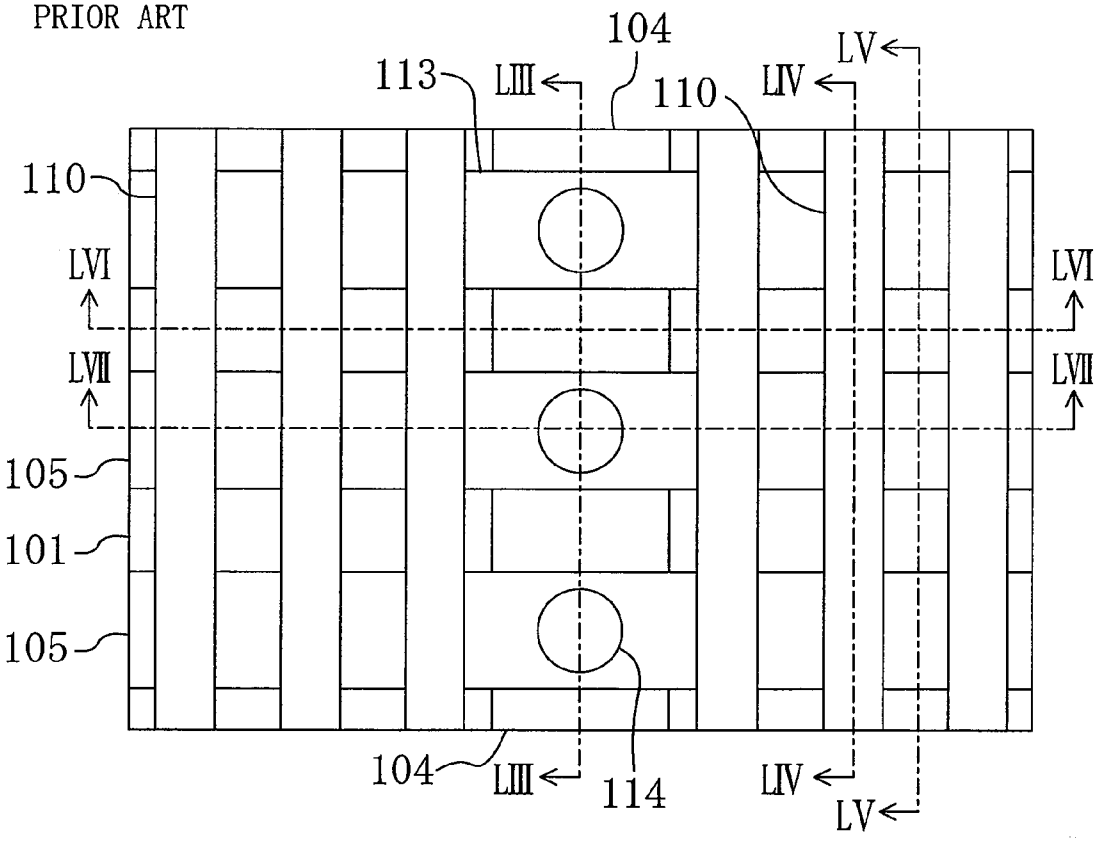


FIG. 53
PRIOR ART

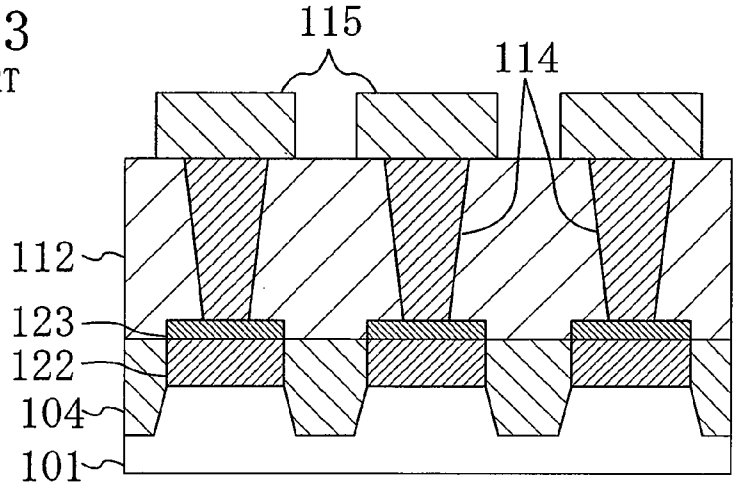


FIG. 54
PRIOR ART

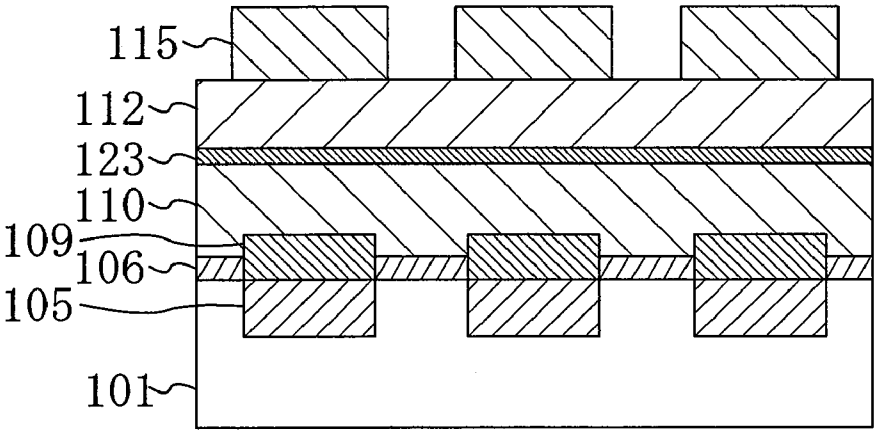


FIG. 55
PRIOR ART

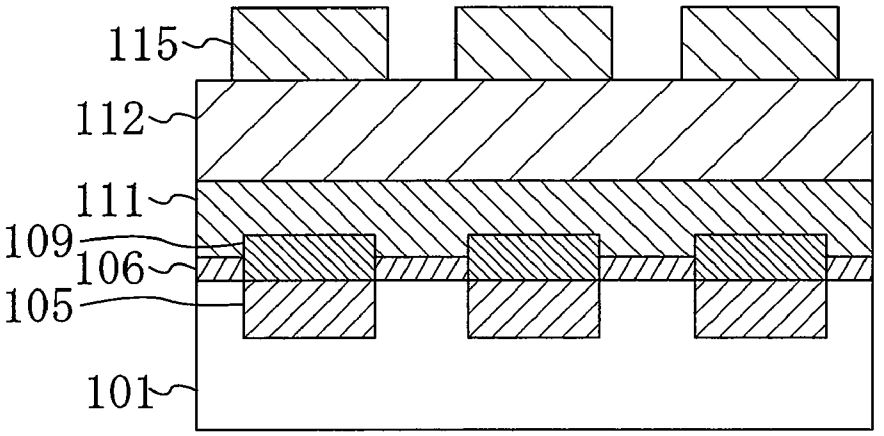


FIG. 56A
PRIOR ART

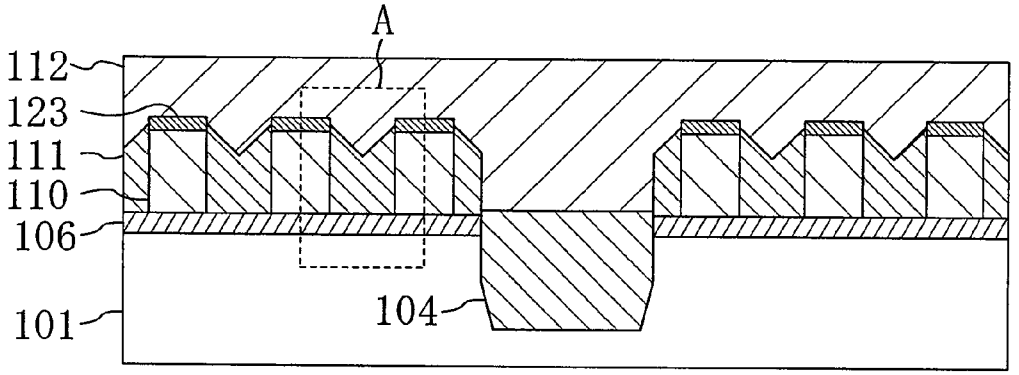


FIG. 56B
PRIOR ART

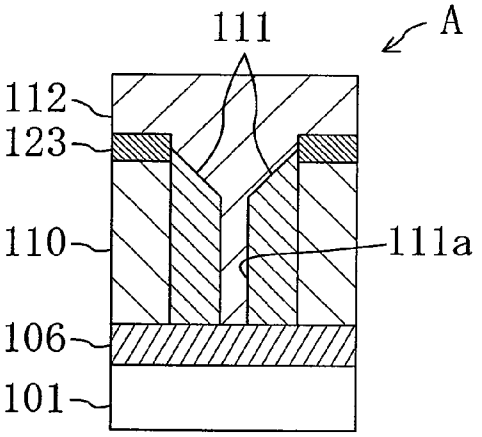


FIG. 57
PRIOR ART

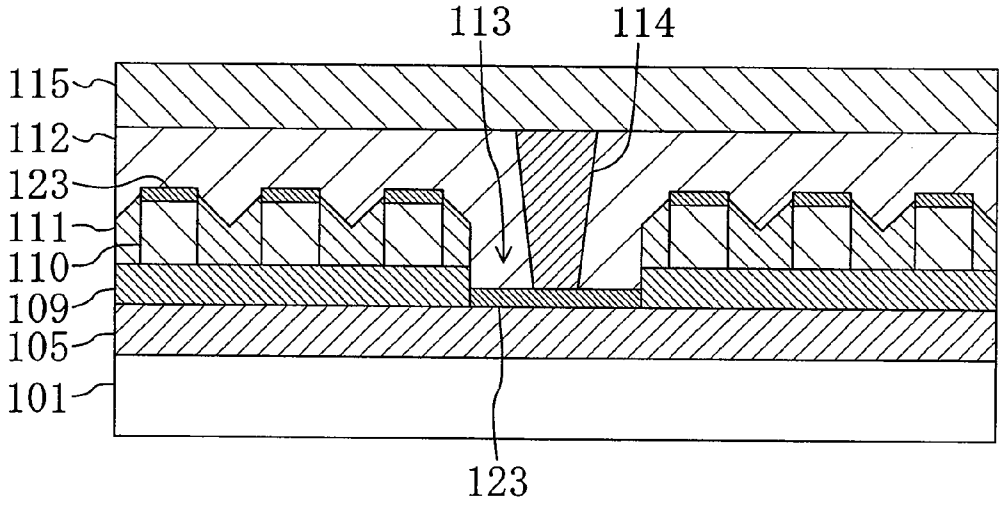


FIG. 58A
PRIOR ART

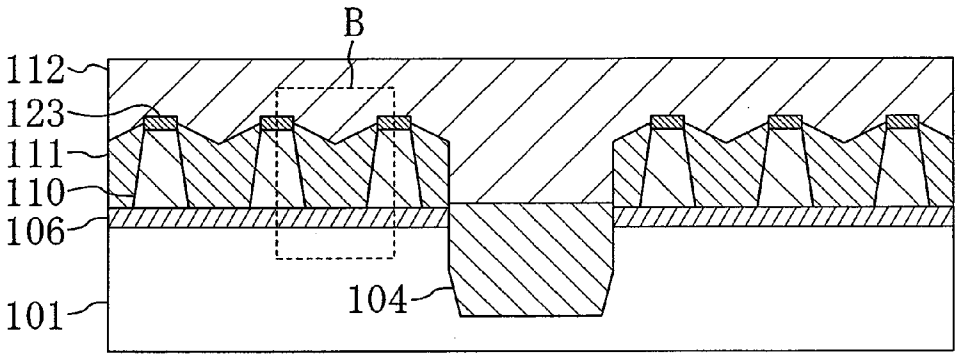


FIG. 58B
PRIOR ART

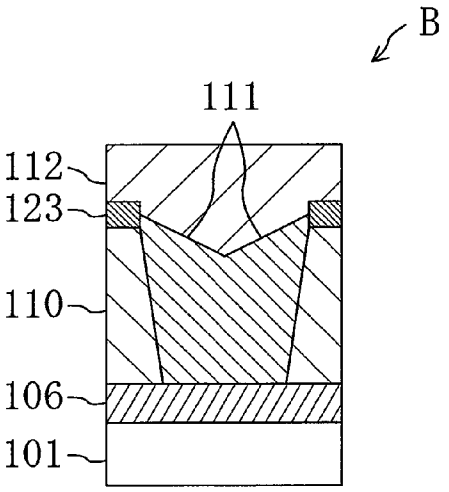


FIG. 59A
PRIOR ART

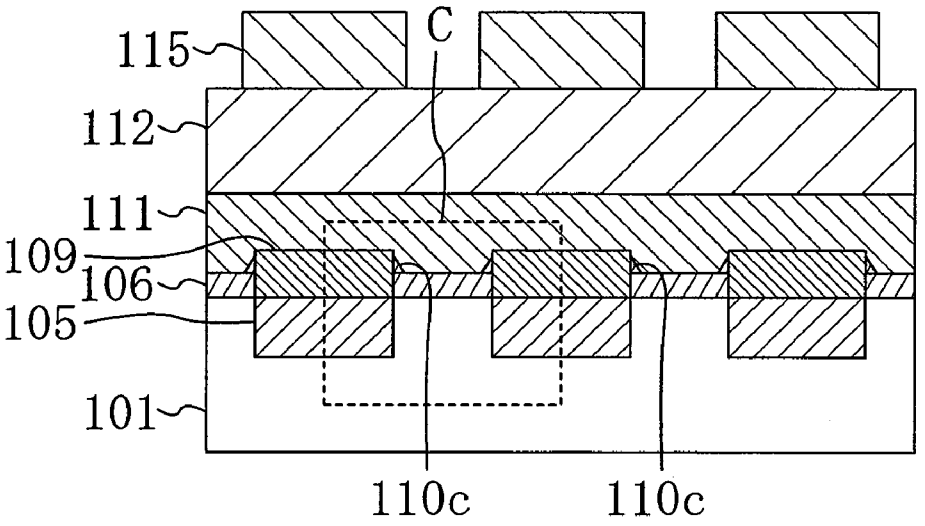
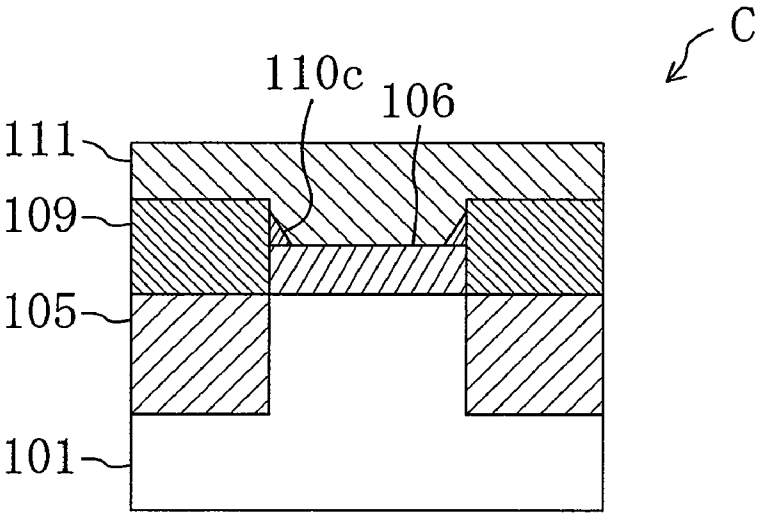


FIG. 59B
PRIOR ART



SEMICONDUCTOR MEMORY DEVICE AND ITS MANUFACTURING METHOD

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This Non-provisional application claims priority under 35 U.S.C. §119(a) on Patent Application No. 2007-214575 filed in Japan on Aug. 21, 2007, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor memory device and its manufacturing method, and more particularly, to a non-volatile semiconductor memory device and its manufacturing method.

[0004] 2. Description of the Related Art

[0005] In recent years, various forms of semiconductor memory devices have been proposed. For example, attention has been attracted by a non-volatile semiconductor memory element in which bit lines made of a diffusion layer and word lines made of a conductive layer made of polysilicon or the like are arranged to intersect and electric charges are accumulated in a trap film, since the scale of integration thereof can be easily increased (see, for example, U.S. Pat. No. 6,803,284 and US Published Application No. 2006/0214218).

[0006] Hereinafter, a semiconductor memory device according to a first conventional example will be described with reference to the accompanying drawings. FIG. **52** shows a plan view of a memory cell formation region of the conventional semiconductor memory device. FIGS. **53** to **57** show cross-sectional views taken along lines LIII-LIII, LIV-LIV, LV-LV, LVI-LVI and LVII-LVII of FIG. **52**, respectively. Note that FIG. **56**B is an expanded view of a portion indicated by a reference letter A of FIG. **56**A.

[0007] As shown in FIGS. **52** and **53**, a plurality of isolation regions **104** made of a buried oxide film are formed in an upper portion of a semiconductor substrate **101** made of, for example, silicon. A plurality of source/drain regions (diffusion bit lines) **105** made of an n-type impurity diffusion layer are spaced from each other in one direction. Bit line contact portions **113** connected to the source/drain regions **105** are separated by the isolation regions **104**.

[0008] As shown in FIGS. **54** and **55**, a bit line buried oxide film **109** is formed on each source/drain region **105**. A trap film **106** is formed on an active region formed between each source/drain region **105**. The trap film **106** is made of a stack of, for example, silicon oxide, silicon nitride and silicon oxide films (so-called ONO film), and has a site where electric charges are trapped.

[0009] A word line **110** which provides a gate electrode of each memory cell is formed on each trap film **106**. The word line **110** is made of polycrystal silicon into which an n-type impurity (e.g., phosphorus) is introduced, and is formed in a direction that intersects the bit line buried oxide film **109**.

[0010] As shown in FIG. **56**A, a buried insulating film **111** is buried between adjacent word lines **110** formed on the trap film **106**. A metal silicide layer **123** is formed on an upper surface of each word line **110** that is exposed from the buried insulating film **111**. An interlayer insulating film **112** is formed on each word line **110** in which the metal silicide layer **123** is formed, and each buried insulating film **111**.

[0011] As shown in FIG. **57**, in the bit line contact portion **113**, the source/drain region **105** is connected to a contact **114** that penetrates through the interlayer insulating film **112**, and is also connected to a bit interconnect **115** made of a metal formed on the interlayer insulating film **112**. Note that the bit line contact portion **113** connected to the source/drain region **105** forms the high-concentration impurity diffusion layer **122**, and the metal silicide layer **123** is also formed in an upper portion of the high-concentration impurity diffusion layer **122**.

[0012] Note that, in FIG. **52**, the buried insulating film **111**, the interlayer insulating film **112**, the bit line buried oxide film **109**, and the trap film **106** and bit interconnect **115** are not shown.

[0013] In the semiconductor memory device of the first conventional example, when the pitch of the word lines **110** is reduced as the level of microfabrication and the scale of integration are enhanced, it is difficult to reduce the height of the word line **110** since electrical characteristics thereof need to be secured, so that the aspect ratio of an interval between adjacent word lines **110** is inevitably increased. Therefore, the following problems arise when the buried insulating film **111** is buried between each word line **110** for electrical separation, and when the metal silicide layer **123** is subsequently formed.

[0014] Firstly, as shown in FIG. **56**B, when the buried insulating film **111** is buried between each word line **110**, a slit-like void **111***a* occurs between each word line **110**, depending on the step coverage property of a material for the buried insulating film **111**.

[0015] Secondly, when the buried insulating film **111** is etched (etch back) to expose an upper surface of the word line **110**, etching proceeds along the slit-like void **111***a*, so that the void **111***a* reaches the trap film **106** or the active region below the trap film **106**. When the void **111***a* thus reaches the trap film **106** and further the active region, charge-up or the like occurs in or an unexpected ion injection species reaches the trap film **106** or the active region, so that memory retention characteristics are adversely affected.

[0016] In contrast, a semiconductor memory device according to a second conventional example has been proposed in which the occurrence of the void **111***a* can be suppressed by providing a structure in which, for example, a side surface of the word line (gate electrode) **110** is inclined (see, for example, US Published Application No. 2007/0048993 and R. Koval et al. "Flash ETOX Virtual Ground Architecture: A Future Scaling Direction", 2005 Symposium on VLSI Technology 11B-1).

[0017] In these documents, as shown in FIG. **58**A, a side surface of the word line **110** is inclined so that a width thereof becomes narrower toward the top, so that the value of an aspect ratio that is the ratio of the height of the word line **110** to the interval between each word line **110** apparently becomes smaller. Therefore, as shown in FIG. **58**B that shows an expanded view of a region B of FIG. **58**A, when the buried insulating film **111** is buried between each word line **110**, a satisfactory step coverage property is obtained, so that the occurrence of the void **111***a* is suppressed.

[0018] However, the second conventional example has the following problem. Specifically, as shown in FIG. **59**A, and FIG. **59**B that shows an expanded view of a region C of FIG. **59**A, when the word line **110** is subjected to patterning by dry etching or the like, then if the bit line buried oxide film **109** or the isolation region **104** (shallow trench isolation (STI), etc.))

is provided below the word line **110**, an etching residue **110***c* occurs on a sidewall thereof. If the residue **110***c* short-circuits the word lines **110**, the yield significantly decreases.

[0019] To solve this problem, etching conditions may be modified so that, for example, etching time is extended, which is a well-known technique. In this case, however, an extraordinary shape, such as a notch or the like, often occurs in a lower portion of the word line (gate electrode) **110**. If the buried insulating film **111** is buried in a portion where a notch occurs, a void occurs. Thus, the occurrence of a void is often not suppressed.

[0020] Therefore, the method of adjusting etching conditions for the semiconductor memory device of the second conventional example requires formation conditions that need to be highly accurately controlled.

SUMMARY OF THE INVENTION

[0021] In view of the above-described problems, the present invention has been achieved. An object of the present invention is to suppress the occurrence of a void that occurs in an insulating film buried between word lines (gate electrodes) and suppress the occurrence of an etching residue when the word line is fabricated.

[0022] To achieve the object, the present invention provides a semiconductor memory device in which an upper portion of a side surface in an extending direction of a word line (gate electrode) is inclined so that a width between each side surface becomes narrower toward the top, while a lower portion of the side surface is formed perpendicular to a bottom surface thereof.

[0023] Specifically, a semiconductor memory device according to an aspect of the present invention includes a plurality of word line provided on a semiconductor region, extending in a row direction, a plurality of bit lines provided in the semiconductor region, extending in a column direction, and a plurality of memory elements provided at intersections between the plurality of word lines and the plurality of bit lines. Each of the plurality of word lines provides a first gate electrode in the corresponding one of the plurality of memory elements. A lower portion of a side surface of each word line in a direction parallel to an extending direction of the word line is perpendicular to a main surface of the semiconductor region. An upper portion of the side surface is inclined so that a width thereof becomes smaller toward a top thereof.

[0024] According to the semiconductor memory device of the aspect of the present invention, the upper portion of the side surface of each word line in the direction parallel to the extending direction of the word line is inclined so that the width becomes smaller toward the top. Therefore, the value of an aspect ratio of a height of the word line and an interval between each word line is substantially small. Therefore, when a buried material is buried for insulation and separation between each word line, a step coverage property with respect to the word line is satisfactory, so that the occurrence of a void can be suppressed. In addition, since the lower portion of the side surface of each word line is formed perpendicular to the main surface of the semiconductor region, an etching residue due to a material for word line is less likely to occur on a side wall of a bit line buried insulating film made of an impurity diffusion layer or an isolation region (STI, etc.).

[0025] In the semiconductor memory device of the aspect of the present invention, each word line preferably includes a multilayer film including a lower-layer film and an upper-layer film provided on the lower-layer film. A side surface of the lower-layer film in the direction parallel to the extending direction of the word line is preferably perpendicular to the main surface of the semiconductor region. A side surface of the upper-layer film in the direction parallel to the extending direction of the word line is preferably inclined so that a width thereof becomes smaller toward a top thereof.

[0026] In the semiconductor memory device of the aspect of the present invention, each memory element preferably has a trap film for accumulating electric charges. The trap film serves as a gate insulating film.

[0027] In this case, the gate insulating film is preferably a multilayer film that is a stack of a lower-layer silicon oxide film, a charge-accumulating silicon nitride film and an upper-layer silicon oxide film that are successively formed, the lower-layer silicon oxide film being closest to the semiconductor region.

[0028] In the semiconductor memory device of the aspect of the present invention, when each word line includes a multilayer film including a lower-layer film and an upper-layer film, the lower-layer film is preferably a floating gate electrode for accumulating electric charges, the upper-layer film is preferably a control gate electrode, and an interelectrode insulating film is preferably provided between the floating gate electrode and the control gate electrode, in the first gate electrode.

[0029] In the semiconductor memory device of the aspect of the present invention, each bit line preferably includes an impurity diffusion layer that is selectively provided in an upper portion of the semiconductor region.

[0030] In this case, the impurity diffusion layer preferably includes a first impurity diffusion layer, and a second impurity diffusion layer provided around the first impurity diffusion layer.

[0031] In this case, an impurity concentration of the first impurity diffusion layer is preferably higher than an impurity concentration of the second impurity diffusion layer.

[0032] The semiconductor memory device of the aspect of the present invention preferably further includes a plurality of bit line buried insulating films covering upper portions of the plurality of bit lines. A height of the bit line buried insulating film is preferably the same as a height of the lower portion of the side surface of the word line.

[0033] In the semiconductor memory device of the aspect of the present invention, when each word line includes a multilayer film including a lower-layer film and an upper-layer film, the lower-layer film and the upper-layer film are preferably made of polycrystal silicon or amorphous silicon.

[0034] In this case, a metal silicide layer is preferably provided in an upper portion of the upper-layer film.

[0035] In the semiconductor memory device of the aspect of the present invention, at least the upper-layer film of the word line is preferably a metal film.

[0036] The semiconductor memory device of the aspect of the present invention preferably further includes a plurality of bit interconnects provided above the semiconductor region, each bit interconnect being electrically connected to the corresponding bit line via a corresponding contact. A metal silicide layer is preferably provided in a region where the bit line is connected to the contact.

[0037] Also, the semiconductor memory device of the aspect of the present invention preferably further includes a logic circuit portion provided in a region excluding the memory elements of the semiconductor region, the logic circuit portion including a transistor having a second gate elec-

trode. The second gate electrode preferably includes a multilayer film having the same configuration as that of the word line including the lower-layer film and the upper-layer film.

[0038] A first method for manufacturing a semiconductor memory device according to an aspect of the present invention includes the steps of (a) forming a trap film for holding electric charges on a semiconductor region, (b) forming a first mask film on the trap film, the first mask film having a plurality of opening portions spaced from each other and extending in a column direction, (c) forming a plurality of bit lines in an upper portion of the semiconductor region by introducing an impurity into the semiconductor region using the first mask film, the bit lines extending in a column direction and each including an impurity diffusion layer, (d) burying a first buried insulating film in each opening portion of the first mask film, (e) after the step (d), removing the first mask film, and thereafter, forming a first conductive film on the semiconductor region, (f) forming a second mask film having a plurality of opening portions on the first conductive film, the opening portions being spaced from each other and extending in a row direction, and (g) subjecting the first conductive film to patterning by etching using the second mask film to form a plurality of word lines from the first conductive film, and exposing the first buried insulating film. The step (g) includes a first step of performing etching until an upper surface of the first buried insulating film is exposed, so that a width of an upper portion of a side surface in a direction parallel to an extending direction of each word line becomes larger toward a bottom thereof as the etching proceeds, and a second step of performing patterning by the etching after an upper surface of the first buried insulating film is exposed and until the trap film is exposed, so that a lower portion of the side surface of each word line is perpendicular to a main surface of the semiconductor region.

[0039] In the first method, preferably, in the step (b), a portion of the trap film exposed from each opening portion of the first mask film is left, and in the step (c), the impurity is introduced via the trap film into the semiconductor region.

[0040] Also, in the first method, preferably, in the step (b), a portion of the trap film exposed from each opening portion of the first mask film is also removed, and in the step (c), the impurity is directly introduced into the semiconductor region.

[0041] In the first method, preferably, in the step (e), the first conductive film is a polycrystal silicon film, an amorphous silicon film, a metal film, a multilayer film including a polycrystal silicon film and a silicide film, or a multilayer film including an amorphous silicon film and a silicide film.

[0042] The first method preferably further includes (h) after the step (g), forming a second buried insulating film between adjacent ones of the word lines while exposing an upper surface of each word line, and (i) causing the exposed upper surface of each word line to be silicide.

[0043] A second method for manufacturing a semiconductor memory device according to an aspect of the present invention includes the steps of (a) forming a trap film for holding electric charges on a semiconductor region, (b) forming a first conductive film on the trap film, (c) forming a first mask film on the first conductive film, the first mask film having a plurality of opening portions spaced from each other and extending in a column direction, (d) selectively removing at least the first conductive film using the first mask film, and thereafter, forming a plurality of bit lines in an upper portion of the semiconductor region by introducing an impurity into the semiconductor region through each opening portion formed in the first mask film and the first conductive film, the bit lines extending in a column direction and each including an impurity diffusion layer, (e) forming a first buried insulating film in each opening portion formed in the first mask film and the first conductive film while exposing the first mask film, (f) after the step (e), removing the first mask film, and thereafter, forming a second conductive film on the first conductive film and the first buried insulating film, (g) forming a second mask film having a plurality of opening portions on the second conductive film, the opening portions being spaced from each other and extending in a row direction, and (h) subjecting the second conductive film and the first conductive film to patterning by etching using the second mask film to form a plurality of word lines from the first conductive film and the second conductive film, and exposing the first buried insulating film. The step (h) includes a first step of etching the second conductive film so that a width of a side surface in a direction parallel to an extending direction of each word line becomes larger toward a bottom thereof as the etching proceeds, and a second step of subjecting the first conductive film to patterning by the etching so that a side surface of each word line is perpendicular to a main surface of the semiconductor region.

[0044] In the second method, preferably, in the step (c), a portion of the trap film exposed from each opening portion of the first mask film is left, and in the step (d), the impurity is introduced via the trap film into the semiconductor region.

[0045] In the second method, preferably, in the step (c), a portion of the trap film exposed from each opening portion of the first mask film is also removed, and in the step (d), the impurity is directly introduced into the semiconductor region.

[0046] In the second method, preferably, in the step (f), the second conductive film is a polycrystal silicon film, an amorphous silicon film, a metal film, a multilayer film including a polycrystal silicon film and a silicide film, or a multilayer film including an amorphous silicon film and a silicide film.

[0047] The second method preferably further includes (i) after the step (h), forming a second buried insulating film between adjacent word lines while exposing an upper surface of each word line, and (j) causing the exposed upper surface of each word line to be silicide.

[0048] A third method for manufacturing a semiconductor memory device according to an aspect of the present invention includes the steps of (a) forming a tunnel film on a semiconductor region, (b) forming a first conductive film on the tunnel film, (c) forming a first mask film on the first conductive film, the first mask film having a plurality of opening portions spaced from each other and extending in a column direction, (d) selectively removing at least the first conductive film using the first mask film, and thereafter, forming a plurality of bit lines in an upper portion of the semiconductor region by introducing an impurity into the semiconductor region through each opening portion formed in the first mask film and the first conductive film, the bit lines extending in a column direction and each including an impurity diffusion layer, (e) forming a first buried insulating film in each of the plurality of opening portions formed in the first mask film and the first conductive film while exposing the first mask film, (f) after the step (e), removing the first mask film, and thereafter, forming an interelectrode insulating film on the first conductive film and the first buried insulating film, (g) forming a second conductive film on the interelectrode insulating film, (h) forming a second mask film having a plurality of opening portions on the second conductive film, the open-

ing portions being spaced from each other and extending in a row direction, and (i) subjecting the second conductive film, the interelectrode insulating film and the first conductive film to patterning by etching using the second mask film to form a plurality of word lines from the first conductive film, the interelectrode insulating film and the second conductive film, and exposing the first buried insulating film. The step (i) includes a first step of etching the second conductive film so that a width of a side surface in a direction parallel to an extending direction of each word line becomes larger toward a bottom thereof as the etching proceeds, and a second step of subjecting the first conductive film to patterning by the etching so that a side surface of each word line is perpendicular to a main surface of the semiconductor region.

[0049] In the third method, preferably, in the step (c), a portion of the tunnel film exposed from each of the plurality of opening portions of the first mask film is left, and in the step (d), the impurity is introduced via the tunnel film into the semiconductor region.

[0050] Also, in the third method, preferably, in the step (c), a portion of the tunnel film exposed from each of the plurality of opening portions of the first mask film is also removed, and in the step (d), the impurity is directly introduced into the semiconductor region.

[0051] In the third method, preferably, in the step (g), the second conductive film is a polycrystal silicon film, an amorphous silicon film, a metal film, a multilayer film including a polycrystal silicon film and a silicide film, or a multilayer film including an amorphous silicon film and a silicide film.

[0052] The third method preferably further includes (j) after the step (i), forming a second buried insulating film between adjacent word lines while exposing an upper surface of each word line, and (k) causing the exposed upper surface of each word line to be silicide.

[0053] In the first method, the semiconductor region preferably has a logic circuit formation region. The method preferably further includes, between the steps (a) and (e), (j) selectively forming a gate insulating film on the logic circuit formation region of the semiconductor region. In the step (e), the first conductive film is also preferably formed on the gate insulating film in the logic circuit formation region. In the step (f), a pattern for forming a gate electrode of a transistor is preferably formed from a portion covering the logic circuit formation region of the second mask film. The step (g) preferably includes forming the gate electrode of the transistor in the logic circuit formation region from a portion included in the logic circuit formation region of the first conductive film.

[0054] Also, in the second method, the semiconductor region preferably has a logic circuit formation region. The method preferably further includes, between the steps (a) and (b), (k) selectively forming a gate insulating film on the logic circuit formation region of the semiconductor region. In the step (b), the first conductive film is also preferably formed on the gate insulating film in the logic circuit formation region. In the step (f), the second conductive film is also preferably formed on the first conductive film in the logic circuit formation region. In the step (g), a pattern for forming a gate electrode of a transistor is preferably formed from a portion covering the logic circuit formation region of the second mask film. The step (h) preferably includes forming the gate electrode of the transistor in the logic circuit formation region from portions included in the logic circuit formation region of the first conductive film and the second conductive film.

[0055] In the third method, the semiconductor region preferably has a logic circuit formation region. The method preferably further includes, between the steps (a) and (b), (l) selectively forming a gate insulating film on the logic circuit formation region of the semiconductor region. In the step (b), the first conductive film is also preferably formed on the gate insulating film in the logic circuit formation region. In the step (g), the second conductive film is also preferably formed on the first conductive film in the logic circuit formation region. In the step (h), a pattern for forming a gate electrode of a transistor is preferably formed from a portion covering the logic circuit formation region of the second mask film. The step (i) preferably includes forming the gate electrode of the transistor in the logic circuit formation region from portions included in the logic circuit formation region of the first conductive film and the second conductive film.

[0056] As described above, according to the semiconductor memory device of the present invention and its manufacturing method, bit lines made of a diffusion layer are formed and spaced from each other in a semiconductor region, and word lines (gate electrode) are formed and spaced from each other, intersecting the bit lines. In the semiconductor memory device, a void is suppressed from occurring in an insulating film between each word line, and etching residue due to the word line is suppressed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0057] FIG. **1** is a plan view showing a memory cell region in a semiconductor memory device according to a first embodiment of the present invention.

[0058] FIG. **2** is a cross-sectional view taken along line II-II of FIG. **1**.

[0059] FIG. **3** is a cross-sectional view taken along line of FIG. **1**.

[0060] FIG. **4** is a cross-sectional view taken along line IV-IV of FIG. **1**.

[0061] FIG. **5** is a cross-sectional view taken along line V-V of FIG. **1**.

[0062] FIG. **6** is a cross-sectional view taken along line VI-VI of FIG. **1**.

[0063] FIGS. **7**A to **7**C are cross-sectional views showing a method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0064] FIGS. **8**A to **8**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0065] FIGS. **9**A to **9**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0066] FIGS. **10**A to **10**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0067] FIGS. **11**A and **11**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0068] FIGS. **12**A and **12**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0069] FIGS. **13**A and **13**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0070] FIGS. **14**A and **14**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the first embodiment of the present invention in the order in which the device is manufactured.

[0071] FIG. **15** is a plan view showing a memory cell region in a semiconductor memory device according to a second embodiment of the present invention.

[0072] FIG. **16** is a cross-sectional view taken along line XVI-XVI of FIG. **15**.

[0073] FIG. **17** is a cross-sectional view taken along line XVII-XVII of FIG. **15**.

[0074] FIG. **18** is a cross-sectional view taken along line XVIII-XVIII of FIG. **15**.

[0075] FIGS. **19**A to **19**C are cross-sectional views showing a method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0076] FIGS. **20**A to **20**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0077] FIGS. **21**A and **21**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0078] FIGS. **22**A and **22**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0079] FIGS. **23**A and **23**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0080] FIGS. **24**A and **24**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0081] FIGS. **25**A and **25**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0082] FIGS. **26**A and **26**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the second embodiment of the present invention in the order in which the device is manufactured.

[0083] FIG. **27** is a plan view showing a memory cell region in a semiconductor memory device according to a third embodiment of the present invention.

[0084] FIG. **28** is a cross-sectional view taken along line XXVIII-XXVIII of FIG. **27**.

[0085] FIG. **29** is a cross-sectional view taken along line XXIX-XXIX of FIG. **27**.

[0086] FIG. **30** is a cross-sectional view taken along line XXX-XXX of FIG. **27**.

[0087] FIG. **31** is a cross-sectional view taken along line XXXI-XXXI of FIG. **27**.

[0088] FIGS. **32**A to **32**C are cross-sectional views showing a method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0089] FIGS. **33**A to **33**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0090] FIGS. **34**A and **34**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0091] FIGS. **35**A and **35**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0092] FIGS. **36**A and **36**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0093] FIGS. **37**A and **37**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0094] FIGS. **38**A and **38**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0095] FIGS. **39**A and **39**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the third embodiment of the present invention in the order in which the device is manufactured.

[0096] FIGS. **40**A to **40**C are cross-sectional views showing a method for manufacturing a semiconductor memory according to a fourth embodiment of the present invention in the order in which the device is manufactured.

[0097] FIGS. **41**A to **41**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the fourth embodiment of the present invention in the order in which the device is manufactured.

[0098] FIGS. **42**A and **42**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the fourth embodiment of the present invention in the order in which the device is manufactured.

[0099] FIGS. **43**A to **43**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the fourth embodiment of the present invention in the order in which the device is manufactured.

[0100] FIGS. **44**A to **44**C are cross-sectional views showing a method for manufacturing a semiconductor memory according to a fifth embodiment of the present invention in the order in which the device is manufactured.

[0101] FIGS. **45**A to **45**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the fifth embodiment of the present invention in the order in which the device is manufactured.

[0102] FIGS. **46**A and **46**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the fifth embodiment of the present invention in the order in which the device is manufactured.

[0103] FIGS. **47**A to **47**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the fifth embodiment of the present invention in the order in which the device is manufactured.

[0104] FIGS. **48**A to **48**C are cross-sectional views showing a method for manufacturing a semiconductor memory according to a sixth embodiment of the present invention in the order in which the device is manufactured.

[0105] FIGS. **49**A to **49**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the sixth embodiment of the present invention in the order in which the device is manufactured.

[0106] FIGS. **50**A and **50**B are cross-sectional views showing the method for manufacturing the semiconductor memory of the sixth embodiment of the present invention in the order in which the device is manufactured.

[0107] FIGS. **51**A to **51**C are cross-sectional views showing the method for manufacturing the semiconductor memory of the sixth embodiment of the present invention in the order in which the device is manufactured.

[0108] FIG. **52** is a plan view showing a memory cell region in a semiconductor memory device according to a first conventional example.

[0109] FIG. **53** is a cross-sectional view taken along line LIII-LIII of FIG. **52**.

[0110] FIG. **54** is a cross-sectional view taken along line LIV-LIV of FIG. **52**.

[0111] FIG. **55** is a cross-sectional view taken along line LV-LV of FIG. **52**.

[0112] FIG. **56**A is a cross-sectional view taken along line LVI-LVI of FIG. **52**.

[0113] FIG. **56**B is an expanded cross-sectional view of a region A of FIG. **56**A.

[0114] FIG. **57** is a cross-sectional view taken along line LVII-LVII of FIG. **52**.

[0115] FIGS. **58**A and **58**B show a memory cell region in a semiconductor memory device according to a second conventional example, FIG. **58**A being a cross-sectional view corresponding to LVI-LVI of FIG. **52**, and FIG. **58**B being an expanded cross-sectional view of a region B of FIG. **58**A.

[0116] FIGS. **59**A and **59**B show the memory cell region in the semiconductor memory device of the second conventional example, FIG. **59**A being a cross-sectional view corresponding to LV-LV of FIG. **52**, and FIG. **59**B being an expanded cross-sectional view of a region C of FIG. **59**A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0117] A first embodiment of the present invention will be described with reference to the accompanying drawings.

[0118] FIG. **1** shows a plan view of a memory cell region in a semiconductor memory device according to a first embodiment of the present invention. FIGS. **2** to **6** show cross-sectional views taken along lines II-II, III-III, IV-IV, V-V and VI-VI of FIG. **1**, respectively.

[0119] As shown in FIGS. **1** and **2**, a plurality of isolation regions **4** (e.g., STI) made of a buried oxide film are formed in an upper portion of a semiconductor substrate **1** made of, for example, silicon (Si). A plurality of source/drain regions **5** made of an n-type impurity diffusion layer that function as diffusion bit lines are formed in one direction in an upper portion of the semiconductor substrate **1**. Bit line contact portions **13** connected to the source/drain regions **5** are separated from each other by the isolation regions **4**.

[0120] As shown in FIGS. **3** and **4**, a bit line buried oxide film **9** is formed on each source/drain region **5**. A trap film **6** is formed on an active region formed between each source/drain region **5**. The trap film **6** is made of a stack of, for example, silicon oxide, silicon nitride and silicon oxide films (so-called ONO film), and has a site where electric charges are trapped.

[0121] A word line **10** which constitutes a gate electrode of each memory cell is formed on each trap film **6**. The word line **110** is made of polycrystal silicon into which an n-type impurity (e.g., phosphorus (P)) is introduced, and is formed in a direction that intersects the bit line buried oxide film **9**.

[0122] As shown in FIGS. **5** and **6**, the word line (gate electrode) **10** of the first embodiment has a side surface in a direction (perpendicular to the surface of the drawing paper) parallel to a direction along which the word line **10** extends. A lower portion of the side surface is perpendicular to a main surface of the semiconductor substrate **1**, and an upper portion of the side surface is inclined so that the word line **10** becomes narrower toward the top (e.g., a forward taper shape). Here, as can be seen from FIGS. **5** and **6**, up to the height of the bit line buried oxide film **9** corresponds to the lower portion of the word line **10**.

[0123] As shown in FIG. **5**, a buried insulating film **11** is buried between adjacent word lines **10** formed on the trap film **6**. A metal silicide layer **23** made of, for example, cobalt (Co), nickel (Ni) or the like is formed on an upper surface of each word line **10** that is exposed from the buried insulating film **11**. An interlayer insulating film **12** is formed on each word line **10** in which the metal silicide layer **23** is formed, and each buried insulating film **11**.

[0124] As shown in FIG. **6**, in the bit line contact portion **13**, the source/drain region **5** that is a diffusion bit line is connected to a contact **14** that penetrates through the interlayer insulating film **12**, and a bit interconnect **15** that is made of a metal including, for example, aluminum (Al) or copper (Cu) as a major component and is formed on the interlayer insulating film **12**. Note that a reason why the bit interconnect **15** made of the metal is provided in parallel with the source/drain region **5** is that the bit interconnect **15** having a lower resistance can enable faster access to the source/drain region **5** made of the impurity diffusion layer and hence the memory cell.

[0125] The bit line contact portion **13** connected to the source/drain region **5** is made of a high-concentration impurity diffusion layer **22**. The metal silicide layer **23** is also formed in an upper portion of the high-concentration impurity diffusion layer **22**.

[0126] Note that the buried insulating film **11**, the interlayer insulating film **12**, the bit line buried oxide film **9**, the trap film **6**, and the bit interconnect **15** are not shown in FIG. **1**.

[0127] Hereinafter, a method for manufacturing the thus-configured semiconductor memory device will be described with reference to FIGS. **7** to **14**. Note that FIGS. **7**A to **14**B show cross-sectional views each taken along any one of lines of FIG. **1**. Specifically, FIGS. **7**A to **8**A, **10**B, **11**A, **12**A, **13**A and **14**A show cross-sectional views taken along line V-V of FIG. **1**. FIGS. **8**B to **10**A show cross-sectional views taken along line III-III of FIG. **1**, and FIGS. **10**C, **11**B, **12**B, **13**B and **14**B show cross-sectional views taken along line VI-VI of FIG. **1**.

[0128] Initially, as shown in FIG. **7**A, a first mask formation film **2**A made of, for example, silicon nitride having a thickness of about 80 nm to 300 nm is formed on a main surface of the semiconductor substrate **1**. Next, a first resist film **3** is applied on the first mask formation film **2**A. Thereafter, an opening portion **3***a* for formation of an isolation region is formed in the first resist film **3** by lithography.

[0129] Next, as shown in FIG. **7**B, the first mask formation film **2**A is etched by dry etching or the like using the first resist film **3** to form, from the first mask formation film **2**A, a first mask film **2** having an opening portion **2***a* to which the opening portion **3***a* of the first resist film **3** is transferred. Next, the first resist film **3** is removed before the semiconductor substrate **1** is etched by dry etching or the like using the first mask film **2** to form a groove portion **1***a* in an upper portion of the semiconductor substrate **1**.

[0130] Next, as shown in FIG. **7**C, the groove portion **1***a* of the semiconductor substrate **1** is filled with an insulating film made of, for example, silicon oxide. An upper surface of the filling silicon oxide is planarized by chemical mechanical polishing to form the isolation region **4** made of STI or the like.

[0131] Next, as shown in FIG. **8**A, the trap film **6**, which is an ONO film having a film thickness of 20 nm and has a site where electric charges are trapped, is deposited on an entire surface including the isolation regions **4** of the semiconductor substrate **1**. Next, a second mask formation film **7**A made of silicon nitride having a film thickness of about 50 nm to 200 nm is deposited by, for example, chemical vapor deposition (CVD). Further, a second resist film **8** is applied on the second mask formation film **7**A.

[0132] Next, as shown in FIG. **8**B, opening patterns **8***a* each having an opening for a source/drain formation region is formed in the second resist film **8** by lithography. Here, the opening has a width of 100 nm, which is a width of the source/drain region **5**, i.e., a width of the diffusion bit line. On the other hand, the second resist film **8** has a line width of 150 nm, and this line width corresponds to a channel width of a memory cell transistor.

[0133] Next, as shown in FIG. **8**C, the second mask formation film **7**A is etched by dry etching or the like using the second resist film **8** to form, from the second mask formation film **7**A, a second mask film **7** having opening portions **7***a* to which the opening patterns **8***a* of the second resist film **8** are transferred. Next, the trap film **6** that is exposed from the opening portion **7***a* of the second mask film **7** is removed. Note that since the trap film **6** has a film thickness of as small as 20 nm, the trap film **6** may not be removed and may be used as a protection film for the semiconductor substrate **1** during ion implantation.

[0134] Next, as shown in FIG. **9**A, ion implantation is performed once or twice or more using the second mask film **7** under conditions such that, for example, arsenic (As), which is an n-type impurity, is used, the acceleration energy is 5 keV to 200 keV, and the dose is 1×10^{14} cm^{-2} to 1×10^{17} cm^{-2}, so that the source/drain regions **5** each made of an n-type impurity diffusion layer are formed.

[0135] Next, as shown in FIG. **9**B, a silicon oxide film **9**A is deposited by, for example, high-density plasma chemical vapor deposition (HDP-CVD), low-pressure chemical vapor deposition (LP-CVD) or the like, so that at least each opening portion **7***a* of the second mask film **7** is buried.

[0136] Next, as shown in FIG. **9**C, the silicon oxide film **9**A is removed by, for example, CMP, etch back, or the like, leaving portions thereof buried in the opening portions **7***a* of the second mask film **7**.

[0137] Next, as shown in FIG. **10**A, only the second mask film **7** is selectively removed by wet etching, etch back, or the like. Thereby, the trap film **6** is exposed while the bit line buried oxide film **9** is formed of the silicon oxide film **9**A. Here, a height of the bit line buried oxide film **9** is adjusted to, for example, 50 nm by wet etching, etch back or the like before or after the removal of the second mask film **7**.

[0138] Next, as shown in FIGS. **10**B and **10**C, a polycrystal silicon film **10**A that is doped with phosphorus (P), which is an n-type impurity, to about 1×10^{18} cm^{-3} to 1×10^{22} cm^{-3}, is deposited on the trap film **6** and the bit line buried oxide film **9** by, for example, LP-CVD.

[0139] Next, as shown in FIGS. **11**A and **11**B, a third resist film **81** having a wiring pattern for forming a plurality of word lines is formed in a direction that intersects the source/drain formation region, on the polycrystal silicon film **10**A by lithography.

[0140] Next, as shown in FIGS. **12**A and **12**B, the word lines (gate electrodes) **10** made of the polycrystal silicon film **10**A are formed by subjecting the polycrystal silicon film **10**A to patterning by dry etching using the third resist film **81**.

[0141] In this case, dry etching is performed so that the side surface in the direction parallel to the extending direction of each word line **10** has an angle of, for example, about 84°±4°, that is smaller than 90°, with respect to the semiconductor substrate **1** (first step). Next, when a height of a lower end portion (deepest portion) of the etched polycrystal silicon film **10**A reaches substantially the same height of the bit line buried oxide film **9**, dry etching is performed so that the side surface in the direction parallel to the extending direction of each word line **10** has an angle of, for example, about 90°±1° with respect to the semiconductor substrate **1**, thereby exposing the trap film **6** between each word line **10** (second step). Note that it is known that etching conditions are modified or switched while monitoring a film thickness during etching (see, for example, Japanese Unexamined Patent Application Publication No. H05-259127).

[0142] The method for inclining the side surface of the polycrystal silicon film **10**A can be modified by adjusting a pressure or a gas composition during etching, the amount or depth of ions implanted into the polycrystal silicon film **10**A, or an annealing time during which ions are diffused in the polycrystal silicon film **10**A.

[0143] More specifically, the etching conditions for inclining the side surface of the polycrystal silicon film **10**A are specifically determined by changing the set values of etching parameters, depending on the required final angle of the side surface. Here, for example, conditions for setting the angle of the side surface of the word line **10** to be 84° are such that, in an inductively coupled high-density plasma etching apparatus, the etching gas species are chloride (Cl_2), hydrogen bromide (HBr), chloride tetrafluoride (CF_4), and oxygen (O_2), and their flow rates are 50 ml/min, 175 ml/min, 35 ml/min, and 3.5 ml/min, respectively. In addition, the pressure is 5×133.3 mPa (=5 mTorr), the RF power of the upper electrode is set to be 600 W, the RF power of the lower electrode is set to be 125 V, and the temperature of the lower electrode is set to be 45° C.

[0144] Also, for example, in order to adjust the angle of the side surface of the word line 10 to 88°, the pressure is set to be 10×133.3 mPa (=10 mTorr) and the overall flow rate of the etching gas is set to be double.

[0145] The implantation amount and implantation energy of an impurity ion and annealing conditions are set so that the word line **10** finally has an appropriate resistance value. The angle of the side surface can also be adjusted by setting each parameter so that the profile of an ion implantation species becomes nonuniform when etching is performed. In this case, the final profile of the implantation species is caused to

become uniform by annealing after implantation to the source/drain, and therefore, the profile of the implantation species does not need to be uniform during etching.

[0146] For example, conditions for causing the side surface of the word line **10** to have an angle of 86° are such that phosphorus (P) ions are implanted at an acceleration energy of 15 keV and in a dose of 1×10^{14} cm^{-2}, followed by rapid thermal annealing (RTA) at 700° C. for 30 seconds. Also, for example, conditions for causing the side surface of the word line **10** to have an angle of 88° are such that RTA is performed at 850° C. for 30 seconds. Alternatively, the profile of the ion implantation species may be changed by setting implantation energy to be 35 keV.

[0147] Next, as shown in FIGS. **13**A and **13**B, the third resist film **81** is removed before the buried insulating film **11** made of silicon oxide or silicon nitride is deposited by, for example, LP-CVD to fill an interstice between each word line **10**. In this case, the upper portions of the side surfaces of adjacent word lines **10** become wider toward the top as described above. Therefore, substantially no void occurs in the buried insulating film **11**. Next, the buried insulating film **11** on the upper surfaces of the word lines **10** and the bit line contact portion **13** is removed by etch back, leaving the buried insulating film **11** on the side surfaces of the word lines **10**.

[0148] Next, as shown in FIGS. **14**A and **14**B, a metal film made of cobalt, nickel or the like is deposited on an entire surface of the semiconductor substrate **1** by, for example, vacuum vapor deposition or the like. Thereafter, a heat treatment is performed to form the metal silicide layer **23** in upper portions of each word line **10** and each bit line contact portion **13**. Next, the interlayer insulating film **12** made of silicon oxide is deposited on an entire surface of the semiconductor substrate **1** by, for example, HDP-CVD, atmospheric pressure chemical vapor deposition (AP-CVD), plasma enhanced chemical vapor deposition (PE-CVD), or the like. Thereafter, an upper surface of the interlayer insulating film **12** is planarized by, for example, CMP, dry etch back or the like.

[0149] Subsequently, as shown in FIGS. **2** and **6**, a connection hole is formed so as to expose the bit line contact portion **13** of each source/drain region **5** formed in the upper portion of the semiconductor substrate **1**. A metal monolayer film or a metal multilayer film made of, for example, tungsten (W), a tungsten compound, titanium (Ti), a titanium compound (titanium nitride (TiN), etc.) or the like is deposited on an entire surface of the interlayer insulating film **12**, burying each connection hole, so that each contact **14** is formed. Next, a conductive film for formation of a bit interconnect is deposited on the interlayer insulating film **12**, and the deposited conductive film is subjected to patterning so as to be electrically connected to each contact **14**. Each bit interconnect **15** is thus formed from the conductive film.

[0150] According to the first embodiment, the side surface of each word line (gate electrode) **10** in a direction parallel to the extending direction of the word line **10** has the upper and lower portions having different angles. Specifically, the lower portion of the side surface of the word line **10** is perpendicular to the main surface of the semiconductor substrate **1**, so that the side surface of the bit line buried oxide film **9** having substantially the same height as that of the lower portion having the perpendicular side surface of the word line **10** is also perpendicular to the main surface of the semiconductor substrate **1**. Therefore, an etching residue does not occur on the side surface of the bit line buried oxide film **9**. In contrast, the upper portion of the side surface of each word line **10** is inclined so that an interval between adjacent side surfaces becomes wider toward the top. Therefore, a void is unlikely to occur when the buried insulating film **11** is formed and buried between each word line **10**.

[0151] Thus, in the first embodiment, as is different from the conventional art, a void does not occur in the buried insulating film **11** that is formed between each word line (gate electrode) **10** to insulate and separate the word lines **10**, and also, an etching residue does not occur on the side surface of the bit line buried oxide film **9**. Therefore, microfabrication of the semiconductor memory device can be achieved with a satisfactory yield.

[0152] Although it has been assumed in the first embodiment that the second mask film **7** for formation of the source/drain region **5** is made of silicon nitride, the second mask film **7** may be an insulating film made of a silicon compound, such as silicon oxide or the like, instead of silicon nitride. Also, when the source/drain region **5** is formed, a resist material may be used as a mask instead of a mask film made of a silicon compound.

[0153] It has also been assumed in the first embodiment that the trap film **6** having a site where electric charges are trapped is a multilayer film made of three films, i.e., silicon oxide, silicon nitride and silicon oxide films. Instead of this, a monolayer film made of silicon oxynitride, a monolayer film made of silicon nitride, a two-layer film including silicon oxide and silicon nitride films successively formed (i.e., the silicon oxide film closer to the semiconductor substrate **1**), or a five-layer film including silicon oxide, silicon nitride, silicon oxide, silicon nitride and silicon oxide films successively deposited may be used.

[0154] Although it has also been assumed as an example in the first embodiment that the trap film **6** has a film thickness of 20 nm, the film thickness may be adjusted within 10 nm to 30 nm as appropriate so that transistor characteristics are optimized.

[0155] Although it has also been assumed as an example in the first embodiment that the bit line buried oxide film **9** has a height of 50 nm, the height may be adjusted within 20 nm to 100 nm as appropriate so that a leakage current between the word line **10** and the source/drain region **5** is optimized.

[0156] Although it has also been assumed as an example in the first embodiment that the n-type impurity diffusion layer included in the source/drain region **5** has a width of 100 nm, the width may be adjusted within 50 nm to 300 nm as appropriate by optimizing transistor characteristics.

[0157] It has been assumed in the first embodiment that a resist material (third resist film **81**) is used as a mask for dry etching with respect to the polycrystal silicon film **10**A included in the word line **10**. For a high scale of integration, a high etching selectivity is assumed to be required. In such a case, a mask film made of silicon oxide or silicon nitride may be used, or alternatively, a multilayer mask including these films and a resist material may be used.

[0158] Although it has also been assumed in the first embodiment that the step of performing dry etching with respect to the polycrystal silicon film **10**A includes switching the step when the height of the side surface to be inclined of each word line **10** becomes the same as the height of the bit line buried oxide film **9**, the present invention is not limited to this. Specifically, even if etching may be switched within about ±30 nm from the height of the bit line buried oxide film **9**, it is possible to remove etching residue.

[0159] Although it has also been assumed in the first embodiment that the polycrystal silicon film **10**A included in the word line **10** is formed by depositing doped polysilicon, non-doped polycrystal silicon that is not doped with an impurity may be deposited before being doped by impurity implantation.

[0160] Also, the polycrystal silicon film **10**A included in the word line **10** is only for illustrative purposes. Instead of polycrystal silicon, a monolayer film made of amorphous silicon, a high-melting point metal having a melting point of 600° C. or more (tantalum (Ta), titanium (Ti), etc.), a metal compound, or a metal silicide, or a multilayer film thereof may be used. Alternatively, the polycrystal silicon film **10**A of the word line **10** may be changed to silicide using a metal.

[0161] Although it has also been assumed as an example in the first embodiment that the buried insulating film **11** buried between each word line **10** is a silicon oxide film or a silicon nitride film formed by LP-CVD, the present invention is not limited to this. Specifically, any insulating film that has a satisfactory step coverage property and can be formed by a method without plasma may be used. Note that an insulating film that is formed by AP-CVD and hence needs to be subsequently baked at high temperature is difficult to handle and requires highly precise conditions for film formation and baking.

[0162] Although it has also been assumed in the first embodiment that a memory element whose source/drain region **5** is of n type is used, a p-type memory element may be used.

[0163] Also, in the first embodiment, a side surface and a bottom surface of the n-type impurity diffusion layer included in each source/drain region **5** may be covered by a p-type impurity diffusion layer having a lower impurity concentration than that of the n-type impurity diffusion layer. With this structure, the p-type impurity diffusion layer can suppress a short channel effect that is caused by diffusion of an impurity of the n-type impurity diffusion layer. Therefore, an interval between a pair of source/drain regions **5** can be reduced, i.e., the gate length can be reduced, so that the scale of integration of the semiconductor memory device can be further increased.

Second Embodiment

[0164] Hereinafter, a second embodiment of the present invention will be described with reference to the drawings. Here, only a difference(s) from the semiconductor memory device of the first embodiment of the present invention will be described. Therefore, the same constituents as those of FIGS. **1** to **6** are indicated by the same reference numerals.

[0165] FIG. **15** shows a plan view of a memory cell region in the semiconductor memory device of the second embodiment of the present invention. FIGS. **16** to **18** show cross-sectional views taken along lines XVI-XVI, XVII-XVII and XVIII-XVIII of FIG. **15**, respectively.

[0166] As shown in FIGS. **16** and **17**, a word line (gate electrode) **10** of the semiconductor memory device of the second embodiment includes a lower word line **10***a* and an upper word line **10***b*. The lower word line **10***a* has a side surface in a direction parallel to an extending direction of the word line **10**, the side surface being perpendicular to a main surface of a semiconductor substrate **1**. The upper word line **10***b* is formed on the lower word line **10***a*, and has a side surface in the direction parallel to the extending direction of the word line **10**, the side surface being inclined so that a width of the upper word line **10***b* becomes narrower toward the top (e.g., a forward taper shape). Here, as can be seen from FIGS. **17** and **18**, up to a height of a bit line buried oxide film **9** corresponds to the lower word line **10***a*.

[0167] Note that, in FIG. **15**, a buried insulating film **11**, an interlayer insulating film **12**, the bit line buried oxide film **9**, a trap film **6**, and a bit interconnect **15** are not shown.

[0168] Hereinafter, a method for manufacturing the thus-configured semiconductor memory device will be described with reference to FIGS. **19**A to **26**B. Note that FIGS. **19**A to **26**B each correspond to a cross-section taken along any one of lines of FIG. **15**. Specifically, FIGS. **19**A, **22**A, **23**A, **24**A, **25**A and **26**A correspond to a cross-section taken along line XVII-XVII of FIG. **15**, FIGS. **19**B to **21**B correspond to a cross-section taken along line XVI-XVI of FIG. **15**, and FIGS. **22**B, **23**B, **24**B, **25**B and **26**B correspond to a cross-section taken along line XVIII-XVIII of FIG. **15**.

[0169] Initially, as shown in FIG. **19**A, an isolation region **4** (STI, etc.) made of silicon oxide is selectively formed on the semiconductor substrate **1** made of Si as in the first embodiment. Next, a trap film **6** that is an ONO film having a film thickness of 20 nm and has a site where electric charges are trapped is deposited on an entire surface of the semiconductor substrate **1** including the isolation region **4**. Next, a first polycrystal silicon film **10A1** having a thickness of about 20 nm to 80 nm (e.g., 50 nm) is deposited by, for example, CVD, and a silicon oxide film (not shown) having a thin film thickness of about 10 nm is then deposited on the first polycrystal silicon film **10A1**. Here, the first polycrystal silicon film **10A1** is doped with an n-type impurity during or after the deposition. Thereafter, a second mask formation film **7**A made of silicon nitride having a film thickness of about 50 nm to 200 nm is deposited. Note that the silicon oxide film (not shown) is formed so as to protect the first polycrystal silicon film **10A1** when the second mask formation film **7**A is subsequently selectively removed, and therefore, the silicon oxide film may not be used if the process of removing the second mask formation film **7**A can be made more precise. Also, if the silicon oxide film (not shown) is removed, following the adjustment of the height of the bit line buried oxide film **9**, the silicon oxide film does not have an influence on the subsequent word line formation step. Thereafter, a second resist film **8** is applied on the second mask formation film **7**A.

[0170] Next, as shown in FIG. **19**B, opening patterns **8***a* each having an opening for a source/drain formation region is formed in the second resist film **8** by lithography. Here, the opening has a width of 100 nm, which is a width of the source/drain region **5**, i.e., a width of a diffusion bit line. On the other hand, the second resist film **8** has a line width of 150 nm, and this line width corresponds to a channel width of a memory cell transistor.

[0171] Next, as shown in FIG. **19**C, the second mask formation film **7**A is etched by dry etching or the like using the second resist film **8** to form, from the second mask formation film **7**A, a second mask film **7** having opening portions **7***a* to which the opening patterns **8***a* of the second resist film **8** are transferred. Next, the silicon oxide film (not shown), the first polycrystal silicon film **10A1** and the trap film **6** that are exposed from the opening portion **7***a* of the second mask film **7** are removed. Note that since the trap film **6** has a film thickness of as small as 20 nm, the trap film **6** may not be removed and may be used as a protection film for the semiconductor substrate **1** during ion implantation.

[0172] Next, as shown in FIG. **20**A, ion implantation is performed once or twice or more using the second mask film **7** under conditions such that, for example, arsenic, which is an n-type impurity, is used, the acceleration energy is 5 keV to 200 keV, and the dose is 1×10^{14} cm^{-2} to 1×10^{17} cm^{-2}, so that the source/drain regions **5** each made of an n-type impurity diffusion layer are formed.

[0173] Next, as shown in FIG. **20**B, a silicon oxide film **9**A is deposited by, for example, HDP-CVD, LP-CVD or the like, so that at least each opening portion **7***a* of the second mask film **7** is buried.

[0174] Next, as shown in FIG. **20**C, the silicon oxide film **9**A is removed by, for example, CMP, etch back or the like, leaving portions thereof buried in the opening portions **7***a* of the second mask film **7**.

[0175] Next, as shown in FIG. **21**A, a height of the buried silicon oxide film **9**A is adjusted to substantially the same height of the first polycrystal silicon film **10A1** by wet etching or etch back.

[0176] Next, as shown in FIG. **21**B, only the second mask film **7** is selectively removed by wet etching, etch back or the like. Next, the silicon oxide film (not shown) on the first polycrystal silicon film **10A1** is removed to form a bit line buried oxide film **9** from the silicon oxide film **9**A. Thereby, a height of the bit line buried oxide film **9** is adjusted to substantially the same height as that of the first polycrystal silicon film **10A1**. This height adjusting step is performed before the removal of the second mask film **7**. In order to achieve the same height more precisely, the height adjusting step is preferably performed both before and after the removal of the second mask film **7**.

[0177] Next, as shown in FIGS. **22**A and **22**B, a second polycrystal silicon film **10A2** that is doped with phosphorus (P), which is an n-type impurity, to about 1×10^{18} cm^{-3} to 1×10^{22} cm^{-3}, is deposited on the first polycrystal silicon film **10A1** and the bit line buried oxide film **9** by, for example, LP-CVD. In this case, a very thin native oxide film having a film thickness of about 1 nm may be formed at an interface between the first polycrystal silicon film **10A1** and the second polycrystal silicon film **10A2**. However, since the first polycrystal silicon film **10A1** and the second polycrystal silicon film **10A2** are electrically connected, such a native oxide film does not cause a problem when they are used as the word line (gate electrode).

[0178] Next, as shown in FIGS. **23**A and **23**B, a third resist film **81** having a wiring pattern for forming a plurality of word lines is formed in a direction that intersects the source/drain formation region, on the second polycrystal silicon film **10A2** by lithography.

[0179] Next, as shown in FIGS. **24**A and **24**B, the word lines (gate electrodes) **10** including the lower word line **10***a* and the upper word line **10***b* thereon made of the first polycrystal silicon film **10**A and the second polycrystal silicon film **10**B, respectively, are formed by subjecting the second polycrystal silicon film **10**B and the first polycrystal silicon film **10**A to patterning by dry etching using the third resist film **81**.

[0180] In this case, dry etching is performed with respect to the second polycrystal silicon film **10A2** so that the side surface in the direction parallel to the extending direction of each word line **10** has an angle of, for example, about 84°±4°, that is smaller than 90°, with respect to the semiconductor substrate **1** (first step). Next, when the etching of the second polycrystal silicon film **10A2** is ended, the interface oxide film (not shown) is removed by dry etching (second step). Thereafter, dry etching is performed with respect to the first polycrystal silicon film **10A1** so that the side surface in the direction parallel to the extending direction of each word line **10** has an angle of, for example, about 90°±1° with respect to the semiconductor substrate **1**, thereby exposing the trap film **6** between each word line **10** (third step). Note that the switching of etching steps may include switching etching conditions while monitoring the film thickness during etching as in the first embodiment. Alternatively, a change in intensity of plasma light emission may be detected while the interface oxide film remains interposed, which is a known method.

[0181] The method for inclining the side surface of the second polycrystal silicon film **10A2** can be modified by adjusting a pressure or a gas composition during etching, the amount or depth of ions implanted into the second polycrystal silicon film **10A2**, or an annealing time during which ions are diffused in the second polycrystal silicon film **10A2**.

[0182] More specifically, the etching conditions for inclining the side surface of the second polycrystal silicon film **10A2** are specifically determined by changing the set values of etching parameters, depending on the required final angle of the side surface. Here, for example, conditions for setting the angle of the side surface of the upper word line **10***b* to be 84° are such that, in an inductively coupled high-density plasma etching apparatus, the etching gas species are chloride (Cl_2), hydrogen bromide (HBr), chloride tetrafluoride (CFO, and oxygen (O_2), and their flow rates are 50 ml/min, 175 ml/min, 35 ml/min, and 3.5 ml/min, respectively. In addition, the pressure is 5×133.3 mPa (=5 mTorr), the RF power of the upper electrode is set to be 600 W, the RF power of the lower electrode is set to be 125 V, and the temperature of the lower electrode is set to be 45° C.

[0183] Also, for example, in order to adjust the angle of the side surface of the upper word line **10***b* to 88°, the pressure is set to be 10×133.3 mPa (=10 mTorr) and the overall flow rate of the etching gas is set to be double.

[0184] The implantation amount and implantation energy of an impurity ion and annealing conditions are set so that the word line **10** finally has an appropriate resistance value. The angle of the side surface can also be adjusted by setting each parameter so that the profile of an ion implantation species becomes nonuniform when etching is performed. In this case, the final profile of the implantation species is caused to become uniform by annealing after implantation to the source/drain, and therefore, the profile of the implantation species does not need to be uniform during etching.

[0185] For example, conditions for causing the side surface of the word line **10** to have an angle of 86° are such that phosphorus ions are implanted at an acceleration energy of 15 keV and in a dose of 1×10^{14} cm^2, followed by RTA at 700° C. for 30 seconds. Also, for example, conditions for causing the side surface of the word line **10** to have an angle of 88° are such that RTA is performed at 850° C. for 30 seconds. Alternatively, the profile of the ion implantation species may be changed by setting implantation energy to be 35 keV.

[0186] Next, as shown in FIGS. **25**A and **25**B, the third resist film **81** is removed before a buried insulating film **11** made of silicon oxide or silicon nitride is deposited by, for example, LP-CVD to fill an interstice between each word line **10**. In this case, the upper portions of the side surfaces of adjacent upper word lines **10***b* become wider toward the top as described above. Therefore, substantially no void occurs in the buried insulating film **11**. Next, the buried insulating film

11 on the upper surfaces of the word lines **10** and the bit line contact portion **13** is removed by etch back, leaving the buried insulating film **11** on the side surfaces of the word lines **10**.

[0187] Next, as shown in FIGS. **26**A and **26**B, a metal film made of cobalt, nickel or the like is deposited on an entire surface of the semiconductor substrate **1** by, for example, vacuum vapor deposition or the like. Thereafter, a heat treatment is performed to form a metal silicide layer **23** in upper portions of each word line **10** and each bit line contact portion **13**. Next, an interlayer insulating film **12** made of silicon oxide is deposited on an entire surface of the semiconductor substrate **1** by, for example, HDP-CVD, AP-CVD, PE-CVD or the like. Thereafter, an upper surface of the interlayer insulating film **12** is planarized by, for example, CMP, dry etch back or the like.

[0188] Subsequently, as shown in FIG. **18**, a connection hole is formed so as to expose the bit line contact portion **13** of each source/drain region **5** formed in the upper portion of the semiconductor substrate **1**. A metal monolayer film or a metal multilayer film made of, for example, tungsten, a tungsten compound, titanium, a titanium compound (titanium nitride (TiN), etc.) or the like is deposited on an entire surface of the interlayer insulating film **12**, burying each connection hole, so that each contact **14** is formed. Next, a conductive film for formation of a bit interconnect is deposited on the interlayer insulating film **12**, and the deposited conductive film is subjected to patterning so as to be electrically connected to each contact **14**. Each bit interconnect **15** is thus formed from the conductive film.

[0189] According to the second embodiment, the side surface of each word line (gate electrode) **10** in a direction parallel to the extending direction of the word line **10** has the upper and lower portions having different angles. Specifically, the side surface of the lower word line **10***a* is perpendicular to the main surface of the semiconductor substrate **1**, so that the side surface of the bit line buried oxide film **9** having substantially the same height as that of the lower word line **10***a* is also perpendicular to the main surface of the semiconductor substrate **1**. Therefore, an etching residue does not occur on the side surface of the bit line buried oxide film **9**. In contrast, the side surface of the upper word line **10***b* is inclined so that an interval between adjacent side surfaces becomes wider toward the top. Therefore, a void is unlikely to occur when the buried insulating film **11** is formed and buried between each word line **10**.

[0190] Thus, also in the second embodiment, as is different from the conventional art, a void does not occur in the buried insulating film **11** that is formed between each word line (gate electrode) **10** to insulate and separate the word lines **10**, and also, an etching residue does not occur on the side surface of the bit line buried oxide film **9**. Therefore, microfabrication of the semiconductor memory device can be achieved with a satisfactory yield.

[0191] In addition, the lower word line **10***a* having a perpendicular side surface and the upper word line **10***b* having an inclined side surface that constitue each word line **10** are separately formed in the second embodiment. Therefore, the bit line buried oxide film **9** is formed while the first polycrystal silicon film **10**A**1** of the lower word line **10***a* has been formed. Therefore, it is easy to cause the first polycrystal silicon film **10**A**1** and the bit line buried oxide film **9** to have substantially the same height, thereby making it possible to control the yield more reliably.

[0192] Although it has been assumed in the second embodiment that the second mask film **7** for formation of the source/drain region **5** is made of silicon nitride, the second mask film **7** may be an insulating film made of a silicon compound, such as silicon oxide or the like, instead of silicon nitride. Also, when the source/drain region **5** is formed, a resist material may be used as a mask instead of a mask film made of a silicon compound.

[0193] It has also been assumed in the second embodiment that the trap film **6** having a site where electric charges are trapped is a multilayer film made of three films, i.e., silicon oxide, silicon nitride and silicon oxide films. Instead of this, a monolayer film made of silicon oxynitride, a monolayer film made of silicon nitride, a two-layer film including silicon oxide and silicon nitride films successively formed (i.e., the silicon oxide film closer to the semiconductor substrate **1**), or a five-layer film including silicon oxide, silicon nitride, silicon oxide, silicon nitride and silicon oxide films successively deposited may be used.

[0194] Although it has also been assumed as an example in the second embodiment that the trap film **6** has a film thickness of 20 nm, the film thickness may be adjusted within 10 nm to 30 nm as appropriate so that transistor characteristics are optimized.

[0195] Although it has also been assumed as an example in the second embodiment that the first polycrystal silicon film **10**A**1** and the bit line buried oxide film **9** have a height of 50 nm, the height may be adjusted within 20 nm to 100 nm as appropriate so that a leakage current between the word line **10** and the source/drain region **5** is optimized.

[0196] Although it has also been assumed as an example in the second embodiment that the n-type impurity diffusion layer included in the source/drain region **5** has a width of 100 nm, the width may be adjusted within 50 nm to 300 nm as appropriate by optimizing transistor characteristics.

[0197] It has been assumed in the second embodiment that a resist material (third resist film **81**) is used as a mask for dry etching with respect to the second polycrystal silicon film **10**A**2** and the first polycrystal silicon film **10**A**1** included in the word line **10**. For a high scale of integration, a high etching selectivity is assumed to be required. In such a case, a mask film made of silicon oxide or silicon nitride may be used, or alternatively, a multilayer mask including these films and a resist material may be used.

[0198] Although it has also been assumed in the second embodiment that the step of performing dry etching with respect to the polycrystal silicon films **10**A**1** and **10**A**2** includes switching the step when etching with respect to the second polycrystal silicon film **10**A**2** reaches the height of the bit line buried oxide film **9**, the present invention is not limited to this. Specifically, even if etching may be switched within about ±30 nm from the height of the bit line buried oxide film **9**, it is possible to remove etching residue.

[0199] Although it has also been assumed in the second embodiment that the second polycrystal silicon film **10**A**2** included in the upper word line **10***b* is formed by depositing doped polysilicon, non-doped polycrystal silicon that is not doped with an impurity may be deposited before being doped by impurity implantation.

[0200] Also, the polycrystal silicon films **10**A**1** and **10**A**2** included in the word line **10** are only for illustrative purposes. Instead of polycrystal silicon, a monolayer film made of amorphous silicon, a high-melting point metal having a melting point of 600° C. or more (tantalum (Ta), titanium (Ti),

etc.), a metal compound, or a metal silicide, or a multilayer film thereof may be used. Alternatively, the second polycrystal silicon film **10**A**2** of the upper word line **10***b* may be changed to silicide using a metal.

[0201] Although it has also been assumed as an example in the second embodiment that the buried insulating film **11** buried between each word line **10** is a silicon oxide film or a silicon nitride film formed by LP-CVD, the present invention is not limited to this. Specifically, any insulating film that has a satisfactory step coverage property and can be formed by a method without plasma may be used. Note that an insulating film that is formed by AP-CVD and hence needs to be subsequently baked at high temperature is difficult to handle and requires highly precise conditions for film formation and baking.

[0202] Although it has also been assumed in the second embodiment that a memory element whose source/drain region **5** is of n type is used, a p-type memory element may be used.

[0203] Also, in the second embodiment, a side surface and a bottom surface of the n-type impurity diffusion layer included in each source/drain region **5** may be covered by a p-type impurity diffusion layer having a lower impurity concentration than that of the n-type impurity diffusion layer. With this structure, the p-type impurity diffusion layer can suppress a short channel effect that is caused by diffusion of an impurity of the n-type impurity diffusion layer. Therefore, an interval between a pair of source/drain regions **5** can be reduced, i.e., the gate length can be reduced, so that the scale of integration of the semiconductor memory device can be further increased.

Third Embodiment

[0204] Hereinafter, a third embodiment of the present invention will be described with reference to the drawings. Here, only a difference(s) from the semiconductor memory device of the first embodiment of the present invention will be described. Therefore, the same constituents as those of FIGS. **1** to **6** are indicated by the same reference numerals.

[0205] FIG. **27** shows a plan view of a memory cell region in the semiconductor memory device of the third embodiment of the present invention. FIGS. **28** to **31** show cross-sectional views taken along lines XXVIII-XXVIII, XXIX-XXIX, XXX-XXX and XXXI-XXXI of FIG. **27**, respectively.

[0206] As shown in FIGS. **28**, **29** and **30**, a word line (gate electrode) **10** of the semiconductor memory device of the third embodiment includes a floating gate electrode **30***a*, an interelectrode insulating film **18** and a control gate electrode **30***b* that are formed via a tunnel film **17** made of silicon oxide on a main surface of a semiconductor substrate **1**.

[0207] The floating gate electrode **30***a* and the control gate electrode **30***b* are each made of polycrystal silicon to which an n-type impurity (e.g., phosphorus (P), etc.) is introduced. The interelectrode insulating film **18** is an ONO film that is a stack of silicon oxide, silicon nitride and silicon oxide films.

[0208] The floating gate electrode **30***a* included in the word line **10** has a side surface in a direction parallel to an extending direction of the word line **10**, the side surface being perpendicular to the main surface of the semiconductor substrate **1**. The control gate electrode **30***b* has a side surface in the direction parallel to the extending direction of the word line **10**, the side surface being inclined so that a width of the control gate electrode **30***b* becomes narrower toward the top (e.g., a forward taper shape). Here, as can be seen from FIGS. **30** and **31**, up to a height of a bit line buried oxide film **9** corresponds to the floating gate electrode **30***a*.

[0209] Note that, in FIG. **27**, a buried insulating film **11**, an interlayer insulating film **12**, the bit line buried oxide film **9**, the tunnel film **17**, and a bit interconnect **15** are not shown.

[0210] Hereinafter, a method for manufacturing the thus-configured semiconductor memory device will be described with reference to FIGS. **32**A to **39**B. Note that FIGS. **32**A to **39**B each correspond to a cross-section taken along any one of lines of FIG. **27**. Specifically, FIGS. **32**A, **35**A, **36**A, **37**A, **38**A and **39**A correspond to a cross-section taken along line XXX-XXX of FIG. **27**, FIGS. **32**B to **34**B correspond to a cross-section taken along line XXVIII-XXVIII of FIG. **27**, and FIGS. **35**B, **36**B, **37**B, **38**B and **39**B correspond to a cross-section taken along line XXXI-XXXI of FIG. **27**.

[0211] Initially, as shown in FIG. **32**A, an isolation region **4** (STI, etc.) made of silicon oxide is selectively formed on the semiconductor substrate **1** made of Si as in the first embodiment. Next, the tunnel film **17** made of silicon oxide having a film thickness of 10 nm is deposited on an entire surface of the semiconductor substrate **1** including the isolation region **4**. Next, a first polycrystal silicon film **10**A**1** having a thickness of about 20 nm to 80 nm (e.g., 50 nm) and having an n-type conductivity is deposited by, for example, CVD, and a silicon oxide film (not shown) having a thin film thickness of about 10 nm is then deposited on the first polycrystal silicon film **10**A**1**. Thereafter, a second mask formation film **7**A made of silicon nitride having a film thickness of about 50 nm to 200 nm is deposited. Note that the silicon oxide film (not shown) is formed so as to protect the first polycrystal silicon film **10**A**1** when the second mask formation film **7**A is subsequently selectively removed as in the second embodiment. Therefore, a second resist film **8** is applied on the second mask formation film **7**A.

[0212] Next, as shown in FIG. **32**B, opening patterns **8***a* each having an opening for a source/drain formation region is formed in the second resist film **8** by lithography. Here, the opening has a width of 100 nm, which is a width of the source/drain region **5**, i.e., a width of a diffusion bit line. On the other hand, the second resist film **8** has a line width of 150 nm, and this line width corresponds to a channel width of a memory cell transistor.

[0213] Next, as shown in FIG. **32**C, the second mask formation film **7**A is etched by dry etching or the like using the second resist film **8** to form, from the second mask formation film **7**A, a second mask film **7** having opening portions **7***a* to which the opening patterns **8***a* of the second resist film **8** are transferred. Next, the silicon oxide film (not shown), the first polycrystal silicon film **10**A**1** and the tunnel film **17** that are exposed from the opening portion **7***a* of the second mask film **7** are removed. Note that since the tunnel film **17** has a film thickness of as small as 10 nm, the tunnel film **17** may not be removed and may be used as a protection film during ion implantation.

[0214] Next, as shown in FIG. **33**A, ion implantation is performed once or twice or more using the second mask film **7** under conditions such that, for example, arsenic, which is an n-type impurity, is used, the acceleration energy is 5 keV to 200 keV, and the dose is 1×10^{14} cm^{-2} to 1×10^{17} cm^{-2}, so that the source/drain regions **5** each made of an n-type impurity diffusion layer are formed.

[0215] Next, as shown in FIG. **33**B, a silicon oxide film **9**A is deposited by, for example, HDP-CVD, LP-CVD or the like, so that at least each opening portion **7***a* of the second mask film **7** is buried.

[0216] Next, as shown in FIG. **33**C, the silicon oxide film **9**A is removed by, for example, CMP, etch back or the like, leaving portions thereof buried in the opening portions **7***a* of the second mask film **7**.

[0217] Next, as shown in FIG. **34**A, a height of the buried silicon oxide film **9**A is adjusted to substantially the same height of the first polycrystal silicon film **10**A**1** by wet etching or etch back.

[0218] Next, as shown in FIG. **34**B, only the second mask film **7** is selectively removed by wet etching, etch back or the like. Next, the silicon oxide film (not shown) on the first polycrystal silicon film **10**A**1** is removed to form, from the silicon oxide film **9**A, a bit line buried oxide film **9**. Thereby, a height of the bit line buried oxide film **9** is adjusted to substantially the same height as that of the first polycrystal silicon film **10**A**1**. This height adjusting step is performed before the removal of the second mask film **7**. In order to achieve the same height more precisely, the height adjusting step is preferably performed both before and after the removal of the second mask film **7**.

[0219] Next, as shown in FIGS. **35**A and **35**B, the interelectrode insulating film **18** made of a multilayer film of silicon oxide, silicon nitride and silicon oxide and having a film thickness of about 20 nm is formed on the first polycrystal silicon film **10**A**1** and the bit line buried oxide film **9** by, for example, LP-CVD. Next, a second polycrystal silicon film **10**A**2** that is doped with phosphorus, which is an n-type impurity, to about 1×10^{18} cm^{-3} to 1×10^{22} cm^{-3}, is deposited on the interelectrode insulating film **18** by, for example, LP-CVD.

[0220] Next, as shown in FIGS. **36**A and **36**B, a third resist film **81** having a wiring pattern for forming a plurality of word lines is formed in a direction that intersects the source/drain formation region, on the second polycrystal silicon film **10**A**2** by lithography.

[0221] Next, as shown in FIGS. **37**A and **37**B, the word lines **10** including the floating gate electrode **30***a*, the interelectrode insulating film **18** and the control gate electrode **30***b* made of the first polycrystal silicon film **10**A, the interelectrode insulating film **18** and the second polycrystal silicon film **10**A**2**, respectively, are formed by subjecting the second polycrystal silicon film **10**A**2**, the interelectrode insulating film **18** and the first polycrystal silicon film **10**A**1** to patterning by dry etching using the third resist film **81**.

[0222] In this case, dry etching is performed with respect to the second polycrystal silicon film **10**A**2** so that the side surface in the direction parallel to the extending direction of each word line **10** has an angle of, for example, about 84°±4°, that is smaller than 90°, with respect to the semiconductor substrate **1** (first step). Next, when the etching of the second polycrystal silicon film **10**A**2** is ended, so that the interelectrode insulating film **18** is exposed, the interelectrode insulating film **18** is removed by dry etching (second step). Thereafter, dry etching is performed with respect to the first polycrystal silicon film **10**A**1** so that the side surface in the direction parallel to the extending direction of each word line **10** has an angle of, for example, about 90°±1° with respect to the semiconductor substrate **1**, thereby exposing the tunnel film **17** between each word line **10** (third step). Note that the switching of etching steps may include switching etching conditions while monitoring the film thickness during etching as in the first embodiment. Alternatively, a change in intensity of plasma light emission may be detected while a known interface oxide film remains interposed.

[0223] The method for inclining the side surface of the second polycrystal silicon film **10**A**2** can be modified by adjusting a pressure or a gas composition during etching, the amount or depth of ions implanted into the second polycrystal silicon film **10**A**2**, or an annealing time during which ions are diffused in the second polycrystal silicon film **10**A**2**.

[0224] More specifically, the etching conditions for inclining the side surface of the second polycrystal silicon film **10**A**2** are specifically determined by changing the set values of etching parameters, depending on the required final angle of the side surface. Here, for example, conditions for setting the angle of the side surface of the control gate electrode **30***b* to be 84° are such that, in an inductively coupled high-density plasma etching apparatus, the etching gas species are chloride (Cl_2), hydrogen bromide (HBr), chloride tetrafluoride (CF_4), and oxygen (O_2), and their flow rates are 50 ml/min, 175 ml/min, 35 ml/min, and 3.5 ml/min, respectively. In addition, the pressure is 5×133.3 mPa (=5 mTorr), the RF power of the upper electrode is set to be 600 W, the RF power of the lower electrode is set to be 125 V, and the temperature of the lower electrode is set to be 45° C.

[0225] Also, for example, in order to adjust the angle of the side surface of the control gate electrode **30***b* to 88°, the pressure is set to be 10×133.3 mPa (=10 mTorr) and the overall flow rate of the etching gas is set to be double.

[0226] The implantation amount and implantation energy of an impurity ion and annealing conditions are set so that the word line **10** finally has an appropriate resistance value. The angle of the side surface can also be adjusted by setting each parameter so that the profile of an ion implantation species becomes nonuniform when etching is performed. In this case, the final profile of the implantation species is caused to become uniform by annealing after implantation to the source/drain, and therefore, the profile of the implantation species does not need to be uniform during etching.

[0227] For example, conditions for causing the side surface of the word line **10** to have an angle of 86° are such that phosphorus ions are implanted at an acceleration energy of 15 keV and in a dose of 1×10^{14} cm^{-2}, followed by RTA at 700° C. for 30 seconds. Also, for example, conditions for causing the side surface of the word line **10** to have an angle of 88° are such that RTA is performed at 850° C. for 30 seconds. Alternatively, the profile of the ion implantation species may be changed by setting implantation energy to be 35 keV.

[0228] Next, as shown in FIGS. **38**A and **38**B, the third resist film **81** is removed before a buried insulating film **11** made of silicon oxide or silicon nitride is deposited by, for example, LP-CVD to fill an interstice between each word line **10**. In this case, the upper portions of the side surfaces of adjacent control gate electrodes **30***b* become wider toward the top as described above. Therefore, substantially no void occurs in the buried insulating film **11**. Next, the buried insulating film **11** on the upper surfaces of the word lines **10** and the bit line contact portion **13** is removed by etch back, leaving the buried insulating film **11** on the side surfaces of the word lines **10**.

[0229] Next, as shown in FIGS. **39**A and **39**B, a metal film made of cobalt, nickel or the like is deposited on an entire surface of the semiconductor substrate **1** by, for example, vacuum vapor deposition or the like. Thereafter, a heat treat-

ment is performed to form a metal silicide layer **23** in upper portions of each word line **10** (control gate electrode **30***b*) and each bit line contact portion **13**. Next, an interlayer insulating film **12** made of silicon oxide is deposited on an entire surface of the semiconductor substrate **1** by, for example, HDP-CVD, AP-CVD, PE-CVD or the like. Thereafter, an upper surface of the interlayer insulating film **12** is planarized by, for example, CMP, dry etch back or the like.

[0230] Subsequently, as shown in FIG. **31**, a connection hole is formed so as to expose the bit line contact portion **13** of each source/drain region **5** formed in the upper portion of the semiconductor substrate **1**. A metal monolayer film or a metal multilayer film made of, for example, tungsten, a tungsten compound, titanium, a titanium compound (titanium nitride (TiN), etc.) or the like is deposited on an entire surface of the interlayer insulating film **12**, burying each connection hole, so that each contact **14** is formed. Next, a conductive film for formation of a bit interconnect is deposited on the interlayer insulating film **12**, and the deposited conductive film is subjected to patterning so as to be electrically connected to each contact **14**. Each bit interconnect **15** is thus formed from the conductive film.

[0231] According to the third embodiment, the floating gate electrode **30***a* and the control gate electrode **30***b* formed thereon via the interelectrode insulating film **18** that are included in each word line (gate electrode) **10** have their side surfaces in the direction parallel to the extending direction of the word line **10**, the side surfaces having different angles. Specifically, the side surface of the floating gate electrode **30***a* is perpendicular to the main surface of the semiconductor substrate **1**, so that the side surface of the bit line buried oxide film **9** having substantially the same height as that of the floating gate electrode **30***a* is also perpendicular to the main surface of the semiconductor substrate **1**. Therefore, an etching residue does not occur on the side surface of the bit line buried oxide film **9**. In contrast, the side surface of the control gate electrode **30***b* is inclined so that an interval between adjacent side surfaces becomes wider toward the top. Therefore, a void is unlikely to occur when the buried insulating film **11** is formed and buried between each word line **10**.

[0232] Thus, also in the third embodiment, as is different from the conventional art, a void does not occur in the buried insulating film **11** that is formed between each word line (gate electrode) **10** to insulate and separate the word lines **10**, and also, an etching residue does not occur on the side surface of the bit line buried oxide film **9**. Therefore, microfabrication of the semiconductor memory device can be achieved with a satisfactory yield.

[0233] Also, in the third embodiment, the floating gate electrode **30***a* and the control gate electrode **30***b* can be formed in a self-aligning manner and are therefore more easily formed than when they are separately formed. Therefore, a higher scale of integration can be easily achieved by this embodiment.

[0234] In addition, the bit line buried oxide film **9** is formed while the first polycrystal silicon film **10A1** of the floating gate electrode **30***a* has been formed. Therefore, it is easy to cause the first polycrystal silicon film **10A1** and the bit line buried oxide film **9** to have substantially the same height, thereby making it possible to control the yield more reliably.

[0235] Although it has been assumed in the third embodiment that the second mask film **7** for formation of the source/drain region **5** is made of silicon nitride, the second mask film **7** may be an insulating film made of a silicon compound, such as silicon oxide or the like, instead of silicon nitride. Also, when the source/drain region **5** is formed, a resist material may be used as a mask instead of a mask film made of a silicon compound.

[0236] It has also been assumed in the third embodiment that the tunnel film **17** has a film thickness of 10 nm, the film thickness may be adjusted within 5 nm to 30 nm as appropriate so that transistor characteristics are optimized.

[0237] Although it has also been assumed as an example in the third embodiment that the first polycrystal silicon film **10A1** and the bit line buried oxide film **9** have a height of 50 nm, the height may be adjusted within 20 nm to 100 nm as appropriate so that a leakage current between the word line **10** and the source/drain region **5** is optimized.

[0238] Although it has also been assumed as an example in the third embodiment that the n-type impurity diffusion layer included in the source/drain region **5** has a width of 100 nm, the width may be adjusted within 50 nm to 300 nm as appropriate by optimizing transistor characteristics.

[0239] It has been assumed in the third embodiment that a resist material (third resist film **81**) is used as a mask for dry etching with respect to the second polycrystal silicon film **10A2** and the first polycrystal silicon film **10A1** included in the word line **10**. For a high scale of integration, a high etching selectivity is assumed to be required. In such a case, a mask film made of silicon oxide or silicon nitride may be used, or alternatively, a multilayer mask including these films and a resist material may be used.

[0240] Although it has also been assumed in the third embodiment that the step of performing dry etching with respect to the polycrystal silicon films **10A1** and **10A2** includes switching the step at the interelectrode insulating film **18**, the present invention is not limited to this. Specifically, even if etching may be switched within about ±30 nm from the height of the bit line buried oxide film **9**, it is possible to remove etching residue.

[0241] Although it has also been assumed in the third embodiment that the first polycrystal silicon film **10A1** and the second polycrystal silicon film **10A2** are formed by depositing doped polysilicon, non-doped polycrystal silicon that is not doped with an impurity may be deposited before being doped by impurity implantation.

[0242] Also, the polycrystal silicon films **10A1** and **10A2** are only for illustrative purposes. Instead of polycrystal silicon, a monolayer film made of amorphous silicon, a high-melting point metal having a melting point of 600° C. or more (tantalum (Ta), titanium (Ti), etc.), a metal compound, or a metal silicide, or a multilayer film thereof may be used. Alternatively, the second polycrystal silicon film **10A2** may be changed to silicide using a metal.

[0243] Although it has also been assumed as an example in the third embodiment that the buried insulating film **11** buried between each word line **10** is a silicon oxide film or a silicon nitride film formed by LP-CVD, the present invention is not limited to this. Specifically, any insulating film that has a satisfactory step coverage property may be used. Note that if a memory element includes the floating gate electrode **30***a*, then the scale of integration is high, a capacitance between each floating gate electrode **30***a* increases, leading to a significant deterioration in characteristics. In such a case, therefore, the buried insulating film **11** needs to be made of a low-k dielectric material.

[0244] Although it has also been assumed in the third embodiment that a memory element whose source/drain region **5** is of n type is used, a p-type memory element may be used.

[0245] Also, in the third embodiment, a side surface and a bottom surface of the n-type impurity diffusion layer included in each source/drain region **5** may be covered by a p-type impurity diffusion layer having a lower impurity concentration than that of the n-type impurity diffusion layer. With this structure, the p-type impurity diffusion layer can suppress a short channel effect that is caused by diffusion of an impurity of the n-type impurity diffusion layer. Therefore, an interval between a pair of source/drain regions **5** can be reduced, i.e., the gate length can be reduced, so that the scale of integration of the semiconductor memory device can be further increased.

Fourth Embodiment

[0246] Hereinafter, a semiconductor memory device according to a fourth embodiment of the present invention and its manufacturing method will be described with reference to FIGS. **40**A to **43**C.

[0247] The semiconductor memory device of the fourth embodiment includes a memory element portion having a memory cell according to the first embodiment, and a logic circuit portion including a peripheral circuit or the like. Here, a method for manufacturing the semiconductor memory device of this embodiment will be described. Therefore, the memory element portion of the fourth embodiment can be manufactured by a method similar to that of the first embodiment.

[0248] Initially, as shown in FIG. **40**A, a main surface of a semiconductor substrate **1** made of silicon is divided into a memory element portion M and a logic circuit portion L by an isolation region **4** (e.g., STI, etc.). Note that the memory element portion M includes a region m**1** corresponding to a cross-section taken along line of FIG. **1** and a region m**2** corresponding to a cross-section taken along line IV-IV of FIG. **1**. The logic circuit portion L typically includes an n-channel transistor and a p-channel transistor. Since both transistors are different only in that they include impurity ions of different conductive types. Therefore, as an example, only the n-channel transistor is here shown.

[0249] Next, a trap film **6** that is an ONO film having a film thickness of 20 nm is deposited on an entire surface of the main surface of the semiconductor substrate **1** including the isolation region **4**. In this case, the trap film **6** may be formed thinner by a film thickness of a gate insulating film that will be formed in the logic circuit portion L in a subsequent step.

[0250] Next, as shown in FIG. **40**B, a portion of the trap film **6** that is deposited in the logic circuit portion L is removed, and thereafter, a gate insulating film **19** that is made of silicon oxide (e.g., a thermal oxide film) and has a film thickness of 3 nm is selectively formed on an entire surface of the logic circuit portion L of the main surface of the semiconductor substrate **1**.

[0251] Next, as shown in FIG. **40**C, a second mask formation film **7**A made of silicon nitride having a film thickness of about 50 nm to 200 nm is formed on the trap film **6** and the gate insulating film **19**.

[0252] Next, as shown in FIG. **41**A, stripe-shaped opening portions **7***a* having openings for source/drain formation regions of the memory element portion M are formed in the second mask formation film **7**A by lithography and dry etching, and a second mask film **7** is obtained from the second mask formation film **7**A. Further, the trap film **6** that is exposed from each opening portion **7***a* of the second mask film **7** is removed by etching. Here, the opening portion **7***a* of the second mask film **7** has an opening width of 100 nm, which is a width of the source/drain region. On the other hand, each line width of the second mask film **7** is 150 nm, which is a channel width of a memory cell transistor. Note that, as described in the first embodiment, the trap film **6** that is exposed from each opening portion **7***a* of the second mask film **7** may not be necessarily removed. Next, ion implantation is performed with respect to the memory element portion M of the semiconductor substrate **1** once or twice or more using the second mask film **7** under conditions such that, for example, arsenic, which is an n-type impurity, is used, the acceleration energy is 5 keV to 200 keV, and the dose is 1×10^{14} cm^{-2} to 1×10^{17} cm^{-2}, so that source/drain regions **5** each made of an n-type impurity diffusion layer are formed.

[0253] Next, as shown in FIG. **41**B, a bit line buried oxide film **9** made of silicon oxide is deposited, burying each opening portion **7***a* of the second mask film **7**, and thereafter, an upper surface of the bit line buried oxide film **9** is planarized.

[0254] Next, as shown in FIG. **41**C, a height of the bit line buried oxide film **9** is adjusted to 50 nm by wet etching or dry etch back.

[0255] Next, as shown in FIG. **42**A, only the second mask film **7** is selectively removed by wet etching or etch back. Thereby, in the memory element portion M, the trap film **6** is exposed while the bit line buried oxide film **9** is formed. At the same time, the gate insulating film **19** is exposed in the logic circuit portion L.

[0256] Next, as shown in FIG. **42**B, a polycrystal silicon film **10**A that is doped with phosphorus (n type) to about 1×10^{18} cm^{-3} to 1×10^{22} cm^{-3} is deposited on the trap film **6** and the bit line buried oxide film **9** in the memory element portion M, and on the gate insulating film **19** in the logic circuit portion L.

[0257] Next, as shown in FIG. **43**A, the deposited polycrystal silicon film **10**A is selectively subjected to the following two-step dry etching, thereby forming, from the polycrystal silicon film **10**A, word lines **10** that interest the source/drain regions **5** in the memory element portion M. Also, a word line (gate electrode) **10** of a transistor is formed in the logic circuit portion L. Here, a region m**3** corresponds to a cross-section taken along line VI-VI of FIG. **1** and the region m**4** corresponds to a cross-section taken along line V-V of FIG. **1**.

[0258] Specifically, etching is performed with respect to the polycrystal silicon film **10**A so that a width of an upper portion of both side surfaces in a direction parallel to an extending direction of the word line **10** becomes narrower toward the top (forward taper shape) (first step). Next, when a height of a lower end portion of etching becomes substantially equal to a height of the bit line buried oxide film **9**, etching is performed with respect to a lower portion of the polycrystal silicon film **10**A so that a side surface thereof is substantially perpendicular to the main surface of the semiconductor substrate **1** (second step). As an example, the upper portion of the side surface of the word line **10** is caused to have an angle of about 84°±4° in the first step. Etching is performed so that the lower portion of the side surface of the word line **10** has an angle of about 90°±1° in the second step. Thereby, the trap film **6** is exposed between each word line **10** in the region m**4** of the memory element portion M, and the gate insulating film **19** is exposed in the logic circuit portion

L. Note that specific process conditions under which the upper portion of both side surfaces of the word line **10** is caused to have a forward taper shape and a method for switching etching steps while monitoring a film thickness during etching have been described above.

[0259] Next, as shown in FIG. **43**B, an n-type impurity ion is implanted into the logic circuit portion L of the semiconductor substrate **1** using the word line (gate electrode) **10** as a mask, thereby forming a low-concentration impurity diffusion layer **20** in regions on both sides of the gate electrode **10** of the semiconductor substrate **1**. Next, for example, a silicon oxide film having a film thickness of about 5 nm to 100 nm and a silicon nitride film having a film thickness of about 30 nm to 100 nm are deposited on an entire surface of the semiconductor substrate **1** by CVD, and thereafter, the deposited silicon oxide film and silicon nitride film are etched back, so that a side-wall insulating film **21** is formed on both side surfaces of the gate electrode **10** in the logic circuit portion L, and a buried insulating film **11** is formed between adjacent word lines **10** in the memory element portion M.

[0260] Next, a resist film (not shown) is formed, covering the memory element portion M. Using the formed resist film, and the gate electrode **10** and the side-wall insulating film **21** in the logic circuit portion L as a mask, an n-type impurity ion is selectively implanted into the semiconductor substrate **1** so that a high-concentration impurity diffusion layer **22** that will become a drain region or a source region is formed. In this case, an n-type impurity ion is selectively implanted into bit line contact portions (not shown) of the source/drain regions **5** in the memory element portion M so that a high-concentration impurity diffusion layer is formed. Here, an order in which the high-concentration impurity diffusion layer (not shown) included in the bit line contact portion of the source/drain region **5** in the memory element portion M and the high-concentration impurity diffusion layer **22** in the logic circuit portion L are formed is not particularly limited.

[0261] Next, as shown in FIG. **43**C, a metal film of cobalt, nickel or the like is deposited on an entire surface of the semiconductor substrate **1** by, for example, vacuum vapor deposition or the like. Next, a heat treatment is performed with respect to the deposited metal film so that a metal silicide layer **23** is formed in upper portions of the word line **10** and the bit line contact portion in the memory element portion M, and the metal silicide layer **23** is also formed in upper portions of the gate electrode **10** and the high-concentration impurity diffusion layer **22** in the logic circuit portion L.

[0262] Subsequently, though not shown, as described in the first embodiment, an interlayer insulating film made of silicon oxide is deposited on an entire surface of the semiconductor substrate **1** by, for example, CVD. Thereafter, a plurality of connection holes for exposing the metal silicide layer on each bit line contact portion are selectively formed in the interlayer insulating film by lithography or etching. Next, a conductive film including a metal monolayer film or a metal multilayer film made of tungsten, a tungsten compound, titanium, a titanium compound (titanium nitride, etc.) or the like is deposited on an entire surface of the interlayer insulating film, burying each connection hole. Next, the deposited conductive film is subjected to patterning so that the source/drain regions **5** are connected to the deposited conductive film. Bit interconnects are thus formed from the conductive film.

[0263] Thereby, the semiconductor memory device including the logic circuit portion L in addition to the memory element portion M having a structure similar to that of the first embodiment can be obtained.

[0264] Thus, according to the fourth embodiment, an effect similar to that of the semiconductor memory device of the first embodiment can be obtained in the memory element portion M. In addition, the word line (gate electrode) **10** included in the memory element portion M and the word line (gate electrode) **10** of the transistor included in the logic circuit portion L can be formed in the same step, thereby making it possible to reduce the number of steps.

[0265] Note that, also in the fourth embodiment, the constituent materials and their film thicknesses can be changed and modified as in the first embodiment.

Fifth Embodiment

[0266] Hereinafter, a semiconductor memory device according to a fifth embodiment of the present invention and its manufacturing method will be described with reference to FIGS. **44**A to **47**C.

[0267] The semiconductor memory device of the fifth embodiment includes a memory element portion having a memory cell according to the second embodiment, and a logic circuit portion including a peripheral circuit or the like. Here, a method for manufacturing the semiconductor memory device of this embodiment will be described. Therefore, the memory element portion of the fifth embodiment can be manufactured by a method similar to that of the second embodiment.

[0268] Initially, as shown in FIG. **44**A, a main surface of a semiconductor substrate **1** made of silicon is divided into a memory element portion M and a logic circuit portion L by an isolation region **4** (e.g., STI, etc.). Note that the memory element portion M includes a region m**1** corresponding to a cross-section taken along line XVI-XVI of FIG. **15** and a region m**2** corresponding to a cross-section taken along line m**2**-m**2** of FIG. **15**. The logic circuit portion L typically includes an n-channel transistor and a p-channel transistor. Since both transistors are different only in that they include impurity ions of different conductive types. Therefore, as an example, only the n-channel transistor is here shown.

[0269] Next, a trap film **6** that is an ONO film having a film thickness of 20 nm is deposited on an entire surface of the main surface of the semiconductor substrate **1** including the isolation region **4**. In this case, the trap film **6** may be formed thinner by a film thickness of a gate insulating film that will be formed in the logic circuit portion L in a subsequent step.

[0270] Next, as shown in FIG. **44**B, a portion of the trap film **6** that is deposited in the logic circuit portion L is removed, and thereafter, a gate insulating film **19** is made of silicon oxide (e.g., a thermal oxide film) and has a film thickness of 3 nm is selectively formed on an entire surface of the logic circuit portion L of the main surface of the semiconductor substrate **1**.

[0271] Next, as shown in FIG. **44**C, a first polysilicon film **10A1** having a film thickness of about 20 nm to 80 nm and a thin silicon oxide film (not shown) having a film thickness of about 10 nm are deposited on the trap film **6** and the gate insulating film **19**. Next, a second mask formation film **7**A made of silicon nitride having a film thickness of about 50 nm to 200 nm is formed.

[0272] Next, as shown in FIG. **45**A, stripe-shaped opening portions **7***a* having openings for source/drain formation

regions of the memory element portion M are formed in the second mask formation film **7**A by lithography and dry etching, and a second mask film **7** is obtained from the second mask formation film **7**A. Further, the silicon oxide film (not shown), the first polysilicon film **10A1** and the trap film **6** that are exposed from each opening portion **7***a* of the second mask film **7** are successively removed by etching. Here, the opening portion **7***a* of the second mask film **7** has an opening width of 100 nm, which is a width of the source/drain region. On the other hand, each line width of the second mask film **7** is 150 nm, which is a channel width of a memory cell transistor. Note that, as described in the second embodiment, the trap film **6** that is exposed from each opening portion **7***a* of the second mask film **7** may not be necessarily removed. Next, ion implantation is performed with respect to the memory element portion M of the semiconductor substrate **1** once or twice or more using the second mask film **7** under conditions such that, for example, arsenic, which is an n-type impurity, is used, the acceleration energy is 5 keV to 200 keV, and the dose is 1×10^{14} cm^{-2} to 1×10^{17} cm^{-2}, so that source/drain regions **5** each made of an n-type impurity diffusion layer are formed.

[0273] Next, as shown in FIG. **45**B, a bit line buried oxide film **9** made of silicon oxide is deposited, burying each opening portion **7***a* of the second mask film **7**, and thereafter, an upper surface of the bit line buried oxide film **9** is planarized.

[0274] Next, as shown in FIG. **45**C, a height of the bit line buried oxide film **9** is adjusted to substantially the same height as that of the first polycrystal silicon film **10A1** by wet etching or dry etch back.

[0275] Next, as shown in FIG. **46**A, only the second mask film **7** is selectively removed by wet etching or etch back, and further, the silicon oxide film (not shown) on the first polycrystal silicon film **10A1** is removed to form a bit line buried oxide film **9**. Thereby, a height of the bit line buried oxide film **9** is adjusted to substantially the same height as that of the first polycrystal silicon film **10A1**. This height adjusting step is performed before the removal of the second mask film **7**. In order to achieve the same height more precisely, the height adjusting step is preferably performed both before and after the removal of the second mask film **7**.

[0276] Next, as shown in FIG. **46**B, a second polycrystal silicon film **10A2** that is doped with phosphorus, which is an n-type impurity, to about 1×10^{18} cm^{-3} to 1×10^{22} cm^{-3}, is deposited on the bit line buried oxide film **9** and the first polycrystal silicon film **10A1**. In this case, a very thin native oxide film having a film thickness of about 1 nm may be formed at an interface between the first polycrystal silicon film **10A1** and the second polycrystal silicon film **10A2**. However, since the first polycrystal silicon film **10A1** and the second polycrystal silicon film **10A2** are electrically connected, such a native oxide film does not cause a problem when they are used as the gate electrode.

[0277] Next, as shown in FIG. **47**A, the following three-step dry etching is selectively performed with respect to the deposited second polycrystal silicon film **10A2** and first polycrystal silicon film **10A1**. Thereby, in the memory element portion M, word lines **10** that include the lower word lines **10***a* and the upper word lines **10***b* and intersect the source/drain regions **5** are formed from the first polycrystal silicon film **10A1** and the second polycrystal silicon film **10A2**. Also, in the logic circuit portion L, a word line (gate electrode) **10** that includes the lower word line **10***a* and the upper word line **10***b* is formed from the first polycrystal silicon film **10A1** and the second polycrystal silicon film **10A2**. Here, the region m**3** corresponds to a cross-section taken along line XVIII-XVIII of FIG. **15**, and the region m**4** corresponds to a cross-section taken along line XVII-XVII of FIG. **15**.

[0278] Specifically, etching is performed with respect to the second polycrystal silicon film **10A2** so that a width of both side surfaces in a direction parallel to an extending direction of the word line **10** becomes narrower toward the top (forward taper shape) (first step). Next, when a height of a lower end portion of etching becomes substantially equal to a height of the bit line buried oxide film **9**, an interface oxide film (not shown) between the first polysilicon film **10A1** and the second polysilicon film **10A2** is removed (second step). Next, etching is performed with respect to the first polysilicon film **10A1** so as to obtain a side surface that is substantially perpendicular to the main surface of the semiconductor substrate **1**. As an example, the side surface of the upper word line **10***b* is caused to have an angle of about 84°±4° in the first step. Also, the side surface of the lower word line **10***a* is caused to have an angle of about 90°±1° in the third step. Thereby, the trap film **6** is exposed between each word line **10** in the region m**4** of the memory element portion M, and the gate insulating film **19** is exposed in the logic circuit portion L. Note that specific process conditions under which both side surfaces of the upper word line **10***b* is caused to have a forward taper shape and a method for switching etching steps while monitoring a film thickness during etching have been described above.

[0279] Next, as shown in FIG. **47**B, an n-type impurity ion is implanted into the logic circuit portion L of the semiconductor substrate **1** using the word line (gate electrode) **10** as a mask, thereby forming a low-concentration impurity diffusion layer **20** in regions on both sides of the gate electrode **10** of the semiconductor substrate **1**. Next, for example, a silicon oxide film having a film thickness of about 5 nm to 100 nm and a silicon nitride film having a film thickness of about 30 nm to 100 nm are deposited on an entire surface of the semiconductor substrate **1** by CVD, and thereafter, the deposited silicon oxide film and silicon nitride film are etched back, so that a side-wall insulating film **21** is formed on both side surfaces of the gate electrode **10** in the logic circuit portion L, and a buried insulating film **11** is formed between adjacent word lines **10** in the memory element portion M.

[0280] Next, a resist film (not shown) is formed, covering the memory element portion M. Using the formed resist film, and the gate electrode **10** and the side-wall insulating film **21** in the logic circuit portion L as a mask, an n-type impurity ion is selectively implanted into the semiconductor substrate **1** so that a high-concentration impurity diffusion layer **22** that will become a drain region or a source region is formed. In this case, an n-type impurity ion is selectively implanted into bit line contact portions (not shown) of the source/drain regions **5** in the memory element portion M so that a high-concentration impurity diffusion layer is formed. Here, an order in which the high-concentration impurity diffusion layer (not shown) included in the bit line contact portion of the source/drain region **5** in the memory element portion M and the high-concentration impurity diffusion layer **22** in the logic circuit portion L are formed is not particularly limited.

[0281] Next, as shown in FIG. **47**C, a metal film of cobalt, nickel or the like is deposited on an entire surface of the semiconductor substrate **1** by, for example, vacuum vapor deposition or the like. Next, a heat treatment is performed with respect to the deposited metal film so that a metal silicide

layer **23** is formed in upper portions of the upper word line **10***b* and the bit line contact portion in the memory element portion M, and the metal silicide layer **23** is also formed in upper portions of the upper word line **10***b* and the high-concentration impurity diffusion layer **22** in the logic circuit portion L.

[0282] Subsequently, though not shown, as described in the second embodiment, an interlayer insulating film made of silicon oxide is deposited on an entire surface of the semiconductor substrate **1** by, for example, CVD. Thereafter, a plurality of connection holes for exposing the metal silicide layer on each bit line contact portion are selectively formed in the interlayer insulating film by lithography or etching. Next, a conductive film including a metal monolayer film or a metal multilayer film made of tungsten, a tungsten compound, titanium, a titanium compound (titanium nitride, etc.) or the like is deposited on an entire surface of the interlayer insulating film, burying each connection hole. Next, the deposited conductive film is subjected to patterning so that the source/drain regions **5** are connected to the deposited conductive film. Bit interconnects are thus formed from the conductive film.

[0283] Thereby, the semiconductor memory device including the logic circuit portion L in addition to the memory element portion M having a structure similar to that of the second embodiment can be obtained.

[0284] Thus, according to the fifth embodiment, an effect similar to that of the semiconductor memory device of the second embodiment can be obtained in the memory element portion M. In addition, the word line (gate electrode) **10** included in the memory element portion M and the word line (gate electrode) **10** of the transistor included in the logic circuit portion L can be formed in the same step, thereby making it possible to reduce the number of steps.

[0285] Note that, also in the fifth embodiment, the constituent materials and their film thicknesses can be changed and modified as in the second embodiment.

Sixth Embodiment

[0286] Hereinafter, a semiconductor memory device according to a sixth embodiment of the present invention and its manufacturing method will be described with reference to FIGS. **48**A to **51**C.

[0287] The semiconductor memory device of the sixth embodiment includes a memory element portion having a memory cell according to the third embodiment, and a logic circuit portion including a peripheral circuit or the like. Here, a method for manufacturing the semiconductor memory device of this embodiment will be described. Therefore, the memory element portion of the sixth embodiment can be manufactured by a method similar to that of the third embodiment.

[0288] Initially, as shown in FIG. **48**A, a main surface of a semiconductor substrate **1** made of silicon is divided into a memory element portion M and a logic circuit portion L by an isolation region **4** (e.g., STI, etc.). Note that the memory element portion M includes a region nil corresponding to a cross-section taken along line XXVIII-XXVIII of FIG. **27** and a region m**2** corresponding to a cross-section taken along line XXIX-XXIX of FIG. **27**. The logic circuit portion L typically includes an n-channel transistor and a p-channel transistor. Since both transistors are different only in that they include impurity ions of different conductive types. Therefore, as an example, only the n-channel transistor is here shown.

[0289] Next, a tunnel film **17** that is made of silicon oxide and has a film thickness of 10 nm is deposited on an entire surface of the main surface of the semiconductor substrate **1** including the isolation region **4**. In this case, the tunnel film **17** may be formed thinner by a film thickness of a gate insulating film that will be formed in the logic circuit portion L in a subsequent step.

[0290] Next, as shown in FIG. **48**B, a portion of the tunnel film **17** that is deposited in the logic circuit portion L is removed, and thereafter, a gate insulating film **19** is made of silicon oxide (e.g., a thermal oxide film) and has a film thickness of 3 nm is selectively formed on an entire surface of the logic circuit portion L of the main surface of the semiconductor substrate **1**.

[0291] Next, as shown in FIG. **48**C, a n-type conductivity first polysilicon film **10A1** having a film thickness of about 20 nm to 80 nm and a thin silicon oxide film (not shown) having a film thickness of about 10 nm are successively deposited on the tunnel film **17** and the gate insulating film **19**. Next, a second mask formation film **7**A made of silicon nitride having a film thickness of about 50 nm to 200 nm is formed.

[0292] Next, as shown in FIG. **49**A, stripe-shaped opening portions **7***a* having openings for source/drain formation regions of the memory element portion M are formed in the second mask formation film **7**A by lithography and dry etching, and a second mask film **7** is obtained from the second mask formation film **7**A. Further, the silicon oxide film (not shown), the first polysilicon film **10A1** and the tunnel film **17** that are exposed from each opening portion **7***a* of the second mask film **7** are successively removed by etching. Here, the opening portion **7***a* of the second mask film **7** has an opening width of 100 nm, which is a width of the source/drain region. On the other hand, each line width of the second mask film **7** is 150 nm, which is a channel width of a memory cell transistor. Note that, as described in the third embodiment, the tunnel film **17** that is exposed from each opening portion **7***a* of the second mask film **7** may not be necessarily removed. Next, ion implantation is performed with respect to the memory element portion M of the semiconductor substrate **1** once or twice or more using the second mask film **7** under conditions such that, for example, arsenic, which is an n-type impurity, is used, the acceleration energy is 5 keV to 200 keV, and the dose is 1×10^{14} cm^{-2} to 1×10^{17} cm^{-2}, so that source/drain regions **5** each made of an n-type impurity diffusion layer are formed.

[0293] Next, as shown in FIG. **49**B, a bit line buried oxide film **9** made of silicon oxide is deposited, burying each opening portion **7***a* of the second mask film **7**, and thereafter, an upper surface of the bit line buried oxide film **9** is planarized.

[0294] Next, as shown in FIG. **49**C, a height of the bit line buried oxide film **9** is adjusted to substantially the same height as that of the first polycrystal silicon film **10A1** by wet etching or dry etch back.

[0295] Next, as shown in FIG. **50**A, only the second mask film **7** is selectively removed by wet etching or etch back, and further, the silicon oxide film (not shown) on the first polycrystal silicon film **10A1** is removed to form a bit line buried oxide film **9**. Thereby, a height of the bit line buried oxide film **9** is adjusted to substantially the same height as that of the first polycrystal silicon film **10A1**. This height adjusting step is performed before the removal of the second mask film **7**. In order to achieve the same height more precisely, the height adjusting step is preferably performed both before and after the removal of the second mask film **7**.

[0296] Next, as shown in FIG. **50**B, an interelectrode insulating film **18** that is a multilayer film made of silicon oxide, silicon nitride and silicon oxide is deposited on the first polycrystal silicon film **10**A**1** and the bit line buried oxide film **9**. Thereafter, the deposited interelectrode insulating film **18** is selectively removed from the logic circuit portion L. Next, a second polycrystal silicon film **10**A**2** that is doped with phosphorus, which is an n-type impurity, to about 1×10^{18} cm^{-3} to 1×10^{22} cm^{-3}, is deposited on an entire surface of the memory element portion M and the logic circuit portion L of the semiconductor substrate **1**.

[0297] Next, as shown in FIG. **51**A, the following three-step dry etching is selectively performed with respect to the deposited second polycrystal silicon film **10**A**2**, interelectrode insulating film **18** and first polycrystal silicon film **10**A**1**. Thereby, in the memory element portion M, word lines **10** that include a floating gate electrode **30***a*, the interelectrode insulating film **18** and a control gate electrode **30***b* and intersect the source/drain regions **5** are formed from the first polycrystal silicon film **10**A**1**, the interelectrode insulating film **18** and the second polycrystal silicon film **10**A**2**. Also, in the logic circuit portion L, a word line (gate electrode) **10** that includes a lower word line **10***a* and an upper word line **10***b* is formed from the first polycrystal silicon film **10**A**1** and the second polycrystal silicon film **10**A**2**. Here, the region m**3** corresponds to a cross-section taken along line XXXI-XXXI of FIG. **27**, and the region m**4** corresponds to a cross-section taken along line XXX-XXX of FIG. **27**.

[0298] Specifically, etching is performed with respect to the second polycrystal silicon film **10**A**2** so that a width of both side surfaces in a direction parallel to an extending direction of the word line **10** becomes narrower toward the top (forward taper shape) (first step). Next, when a height of a lower end portion of etching becomes substantially equal to a height of the interelectrode insulating film **18**, the interelectrode insulating film **18** is removed (second step). Next, etching is performed with respect to the first polysilicon film **10**A**1** so as to obtain a side surface that is substantially perpendicular to the main surface of the semiconductor substrate **1**. As an example, the side surface of the control gate electrode **30***b* is caused to have an angle of about 84°±4° in the first step. Also, the side surface of the floating gate electrode **30***a* is caused to have an angle of about 90°±1° in the third step. Thereby, the tunnel film **17** is exposed between each word line **10** in the region m**4** of the memory element portion M, and the gate insulating film **19** is exposed in the logic circuit portion L. Note that specific process conditions under which both side surfaces of the floating gate electrode **30***b* is caused to have a forward taper shape and a method for switching etching steps while monitoring a film thickness during etching have been described above. Specifically, the switching of etching steps may include switching etching conditions while monitoring the film thickness during etching as in the first embodiment. Alternatively, a change in intensity of plasma light emission may be detected while the interface oxide film remains interposed, as in the third embodiment.

[0299] Next, as shown in FIG. **51**B, an n-type impurity ion is implanted into the logic circuit portion L of the semiconductor substrate **1** using the word line (gate electrode) **10** as a mask, thereby forming a low-concentration impurity diffusion layer **20** in regions on both sides of the gate electrode **10** of the semiconductor substrate **1**. Next, for example, a silicon oxide film having a film thickness of about 5 nm to 100 nm and a silicon nitride film having a film thickness of about 30 nm to 100 nm are deposited on an entire surface of the semiconductor substrate **1** by CVD, and thereafter, the deposited silicon oxide film and silicon nitride film are etched back, so that a side-wall insulating film **21** is formed on both side surfaces of the gate electrode **10** in the logic circuit portion L, and a buried insulating film **11** is formed between adjacent word lines **10** in the memory element portion M.

[0300] Next, a resist film (not shown) is formed, covering the memory element portion M. Using the formed resist film, and the gate electrode **10** and the side-wall insulating film **21** in the logic circuit portion L as a mask, an n-type impurity ion is selectively implanted into the semiconductor substrate **1** so that a high-concentration impurity diffusion layer **22** that will become a drain region or a source region is formed. In this case, an n-type impurity ion is selectively implanted into bit line contact portions (not shown) of the source/drain regions **5** in the memory element portion M so that a high-concentration impurity diffusion layer is formed. Here, an order in which the high-concentration impurity diffusion layer (not shown) included in the bit line contact portion of the source/drain region **5** in the memory element portion M and the high-concentration impurity diffusion layer **22** in the logic circuit portion L are formed is not particularly limited.

[0301] Next, as shown in FIG. **51**C, a metal film of cobalt, nickel or the like is deposited on an entire surface of the semiconductor substrate **1** by, for example, vacuum vapor deposition or the like. Next, a heat treatment is performed with respect to the deposited metal film so that a metal silicide layer **23** is formed in upper portions of the control gate electrode **30***b* and the bit line contact portion in the memory element portion M, and the metal silicide layer **23** is also formed in upper portions of the upper word line **10***b* and the high-concentration impurity diffusion layer **22** in the logic circuit portion L.

[0302] Subsequently, though not shown, as described in the third embodiment, an interlayer insulating film made of silicon oxide is deposited on an entire surface of the semiconductor substrate **1** by, for example, CVD. Thereafter, a plurality of connection holes for exposing the metal silicide layer on each bit line contact portion are selectively formed in the interlayer insulating film by lithography or etching. Next, a conductive film including a metal monolayer film or a metal multilayer film made of tungsten, a tungsten compound, titanium, a titanium compound (titanium nitride, etc.) or the like is deposited on an entire surface of the interlayer insulating film, burying each connection hole. Next, the deposited conductive film is subjected to patterning so that the source/drain regions **5** are connected to the deposited conductive film. Bit interconnects are thus formed from the conductive film.

[0303] Thereby, the semiconductor memory device including the logic circuit portion L in addition to the memory element portion M having a structure similar to that of the third embodiment can be obtained.

[0304] Thus, according to the sixth embodiment, an effect similar to that of the semiconductor memory device of the third embodiment can be obtained in the memory element portion M. In addition, the word line (gate electrode) **10** that includes the floating gate electrode **30***a*, the interelectrode insulating film **18** and the control gate electrode **30***b* and is included in the memory element portion M, and the word line (gate electrode) **10** of the transistor included in the logic circuit portion L can be formed in the same step, thereby making it possible to reduce the number of steps.

[0305] Note that, also in the sixth embodiment, the constituent materials and their film thicknesses can be changed and modified as in the third embodiment.

[0306] Each of the above-described first to sixth embodiments is not limited to a non-volatile semiconductor memory device called a flash memory device, and is applicable to a semiconductor memory device in which bit lines and word line intersecting each other are integrated in a high packing density, as in the non-volatile semiconductor memory device. As an example, the present invention is also applicable to a non-volatile semiconductor memory device, such as a dynamic random access memory (DRAM) or the like, a magnetic random access memory (MRAM), a resistive random access memory (RRAM), a ferroelectric random access memory (FRAM), or the like.

[0307] As described above, the semiconductor memory device of the present invention and its manufacturing method provides a semiconductor memory device that has bit lines made of a diffusion layer formed in a semiconductor region, the bit lines being spaced from each other, and word lines intersecting the bit lines, the word lines being spaced from each other, and in which a void is suppressed from occurring in an insulating film between each word line, and a etching residue caused by patterning of the word lines is also suppressed, and are particularly useful as a non-volatile semiconductor memory device and its manufacturing method, or the like.

1. A semiconductor memory device comprising:

a plurality of word line provided on a semiconductor region, extending in a row direction;

a plurality of bit lines provided in the semiconductor region, extending in a column direction,

a plurality of memory elements provided at intersections between the plurality of word lines and the plurality of bit lines; and

a plurality of bit line buried insulating films covering upper portions of the plurality of bit lines,

wherein each of the plurality of word lines provides a first electrically single gate electrode with an equipotential structure in the corresponding one of the plurality of memory elements,

a lower portion of a side surface of each of the plurality of word lines in a direction parallel to an extending direction of the word line is perpendicular to a main surface of the semiconductor region, and an upper portion of the side surface is inclined so that a width thereof becomes smaller toward a top thereof, and

a height of the bit line buried insulating films is substantially the same as a height of the lower portion of the side surface of each of the plurality of word lines.

2. The semiconductor memory device of claim **1**, wherein each of the plurality of word lines includes a multilayer film including a lower-layer film and an upper-layer film provided on the lower-layer film,

a side surface of the lower-layer film in the direction parallel to the extending direction of the word line is perpendicular to the main surface of the semiconductor region, and

a side surface of the upper-layer film in the direction parallel to the extending direction of the word line is inclined so that a width of a cross-section thereof becomes smaller toward a top thereof.

3. The semiconductor memory device of claim **1**, wherein each of the plurality of memory elements has a trap film for accumulating electric charges, wherein the trap film serves as a gate insulating film.

4. The semiconductor memory device of claim **3**, wherein the gate insulating film is a multilayer film that is a stack of a lower-layer silicon oxide film, a charge-accumulating silicon nitride film and an upper-layer silicon oxide film that are successively formed, the lower-layer silicon oxide film being closest to the semiconductor region.

5. (canceled)

6. The semiconductor memory device of claim **1**, wherein each of the plurality of bit lines includes an impurity diffusion layer that is selectively provided in an upper portion of the semiconductor region.

7. The semiconductor memory device of claim **6**, wherein the impurity diffusion layer includes a first impurity diffusion layer, and a second impurity diffusion layer provided around the first impurity diffusion layer.

8. The semiconductor memory device of claim **7**, wherein an impurity concentration of the first impurity diffusion layer is higher than an impurity concentration of the second impurity diffusion layer.

9. The semiconductor memory device of claim **1**, further comprising:

a plurality of bit line buried insulating films covering upper portions of the plurality of bit lines,

wherein a height of the bit line buried insulating film is substantially the same as a height of the lower portion of the side surface of the word line.

10. The semiconductor memory device of claim **2**, wherein the lower-layer film and the upper-layer film are made of polycrystal silicon or amorphous silicon.

11. The semiconductor memory device of claim **10**, wherein

a metal silicide layer is provided in an upper portion of the upper-layer film.

12. The semiconductor memory device of claim **2**, wherein at least the upper-layer film of the word line is a metal film.

13. The semiconductor memory device of claim **6**, further comprising:

a plurality of bit interconnects provided above the semiconductor region, each of the plurality of bit interconnects being electrically connected to the corresponding one of the bit lines via a corresponding contact,

wherein a metal silicide layer is provided in a region where the bit line is connected to the contact.

14. The semiconductor memory device of claim **2**, further comprising:

a logic circuit portion provided in a region excluding the plurality of memory elements of the semiconductor region, the logic circuit portion including a transistor having a second gate electrode,

wherein the second gate electrode includes a multilayer film having the same configuration as that of the word line including the lower-layer film and the upper-layer film.

15-32. (canceled)

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