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(54) **ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE**

Publication Classification

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(57) **ABSTRACT**

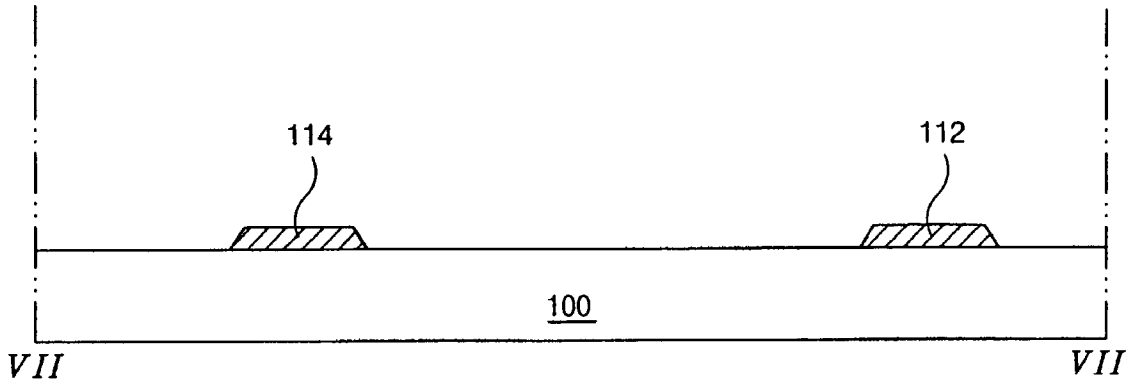
An array substrate of the present invention includes a storage capacitor that has a storage-on-gate structure. The storage capacitor includes a gate line as a first electrode and a capacitor electrode as a second electrode. The capacitor electrode particularly has an extension that protruding from the capacitor electrode into a pixel region. Thus, when connecting a pixel electrode to the storage capacitor, the pixel electrode contacts the extension of the capacitor electrode. Since a storage contact hole through which the pixel electrode contacts the extension, a short between the pixel electrode and the gate line in the storage capacitor is prevented.

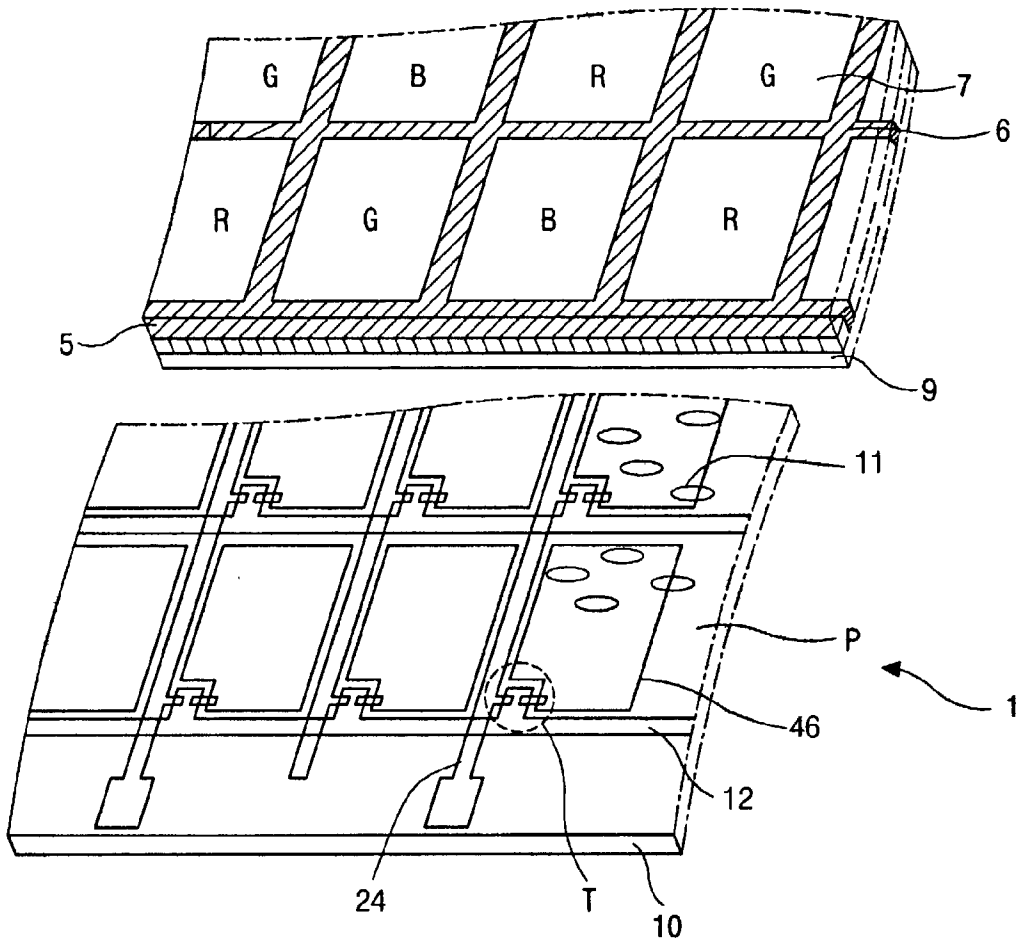
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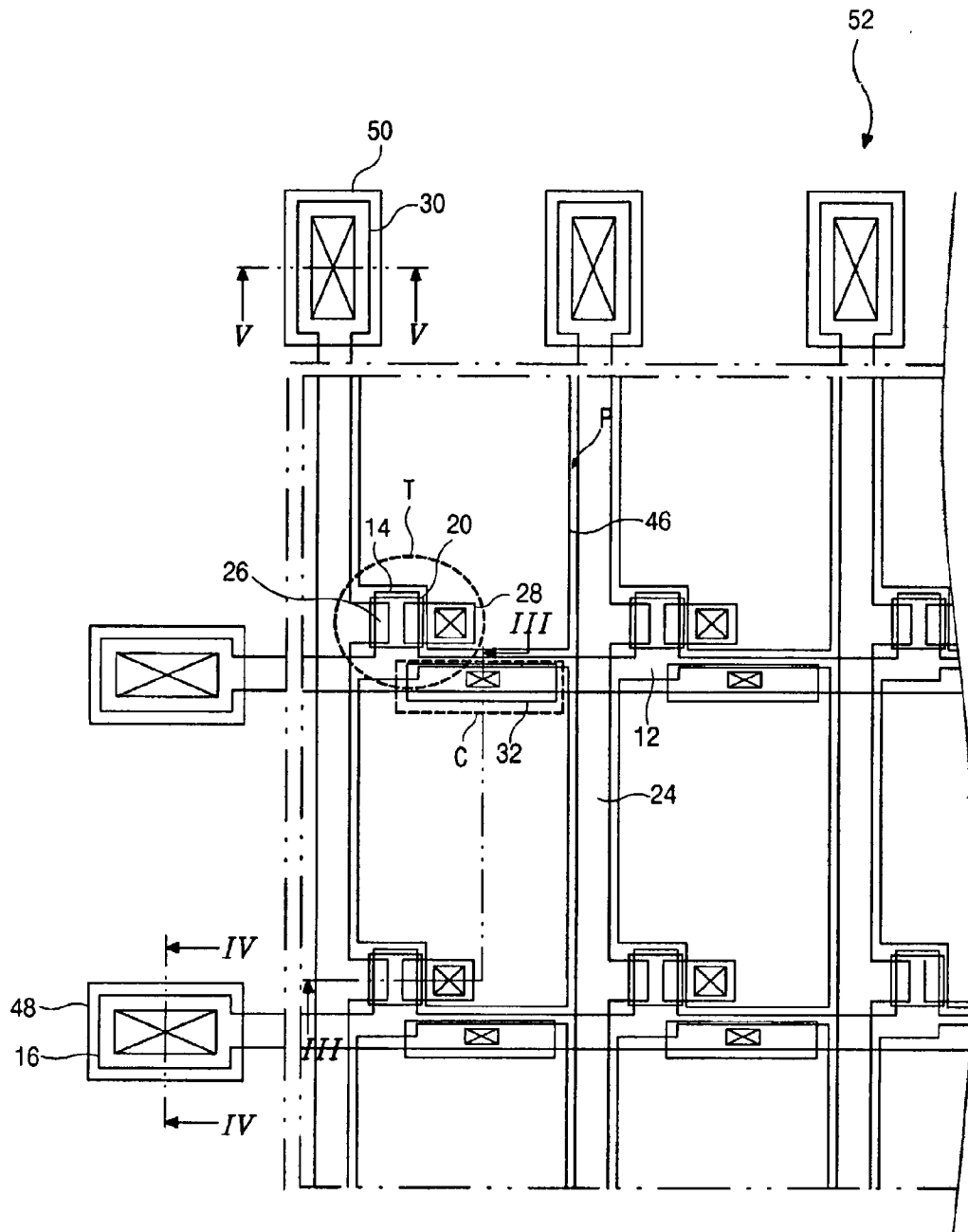
(30) **Foreign Application Priority Data**

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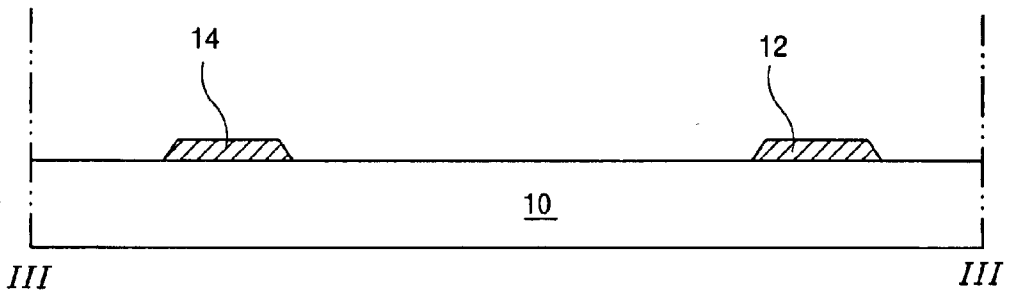




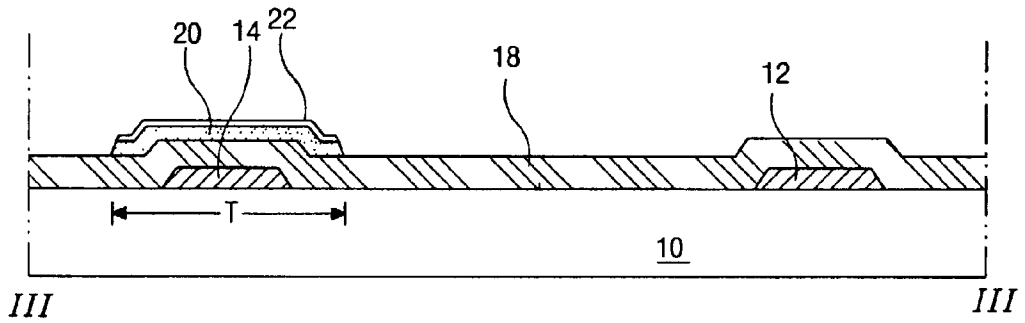
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FIG. 1



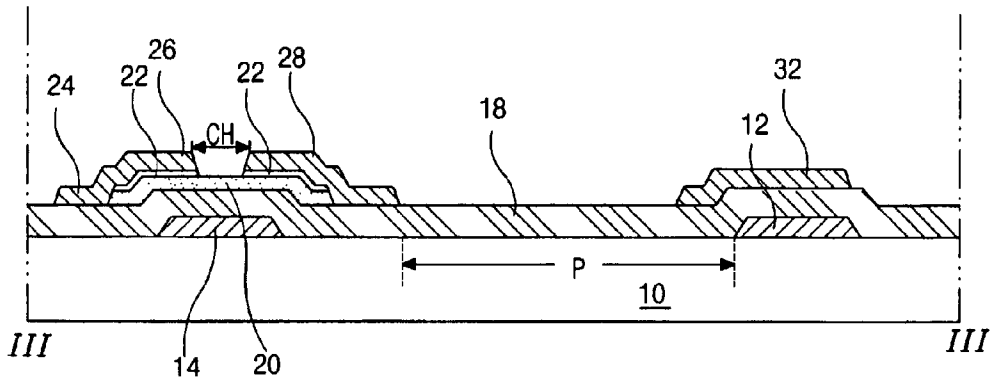
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FIG. 2



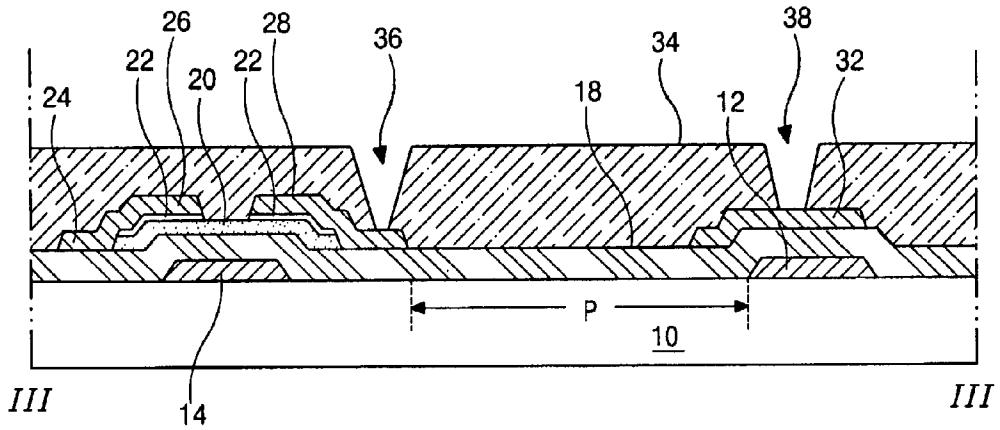
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FIG. 3A



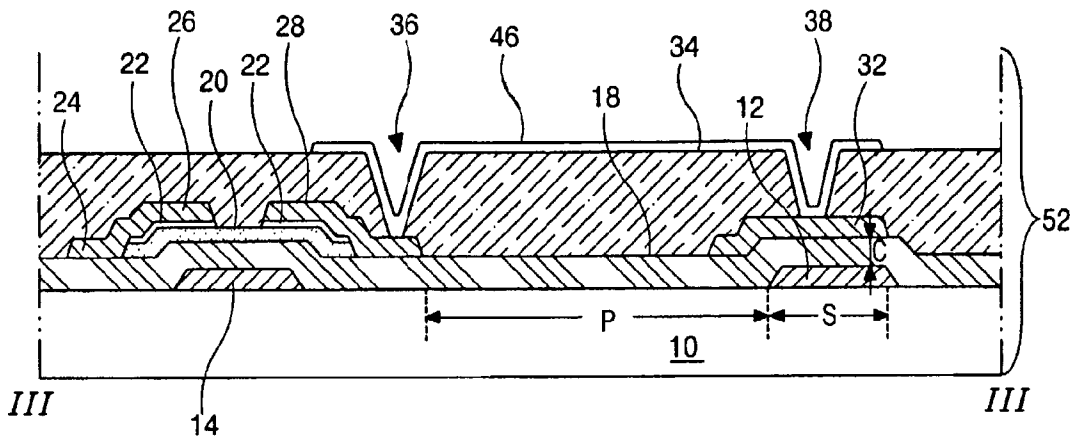
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FIG. 3B



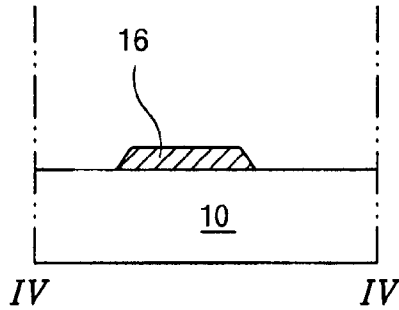
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FIG. 3C



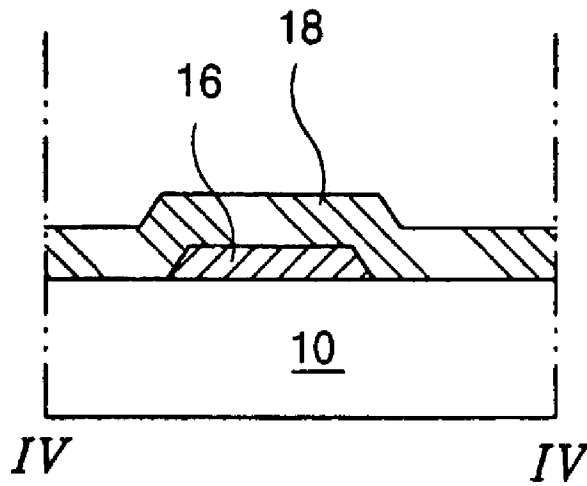
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FIG. 3D



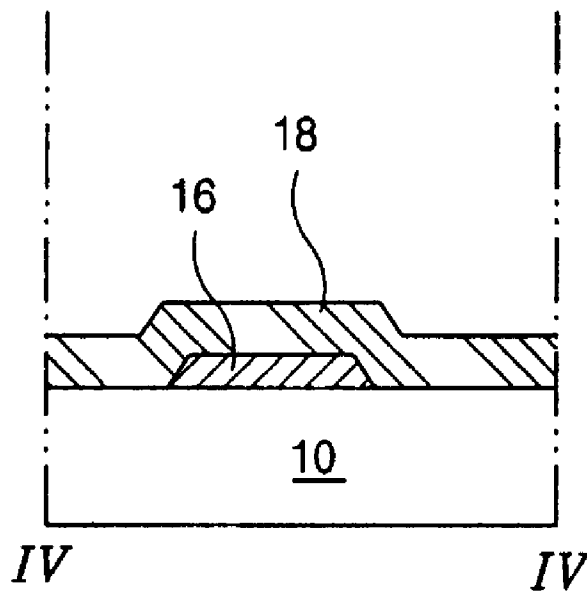
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FIG. 3E



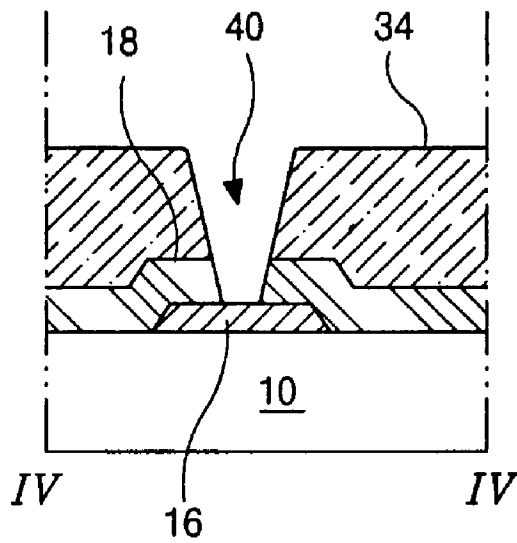
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FIG. 4A



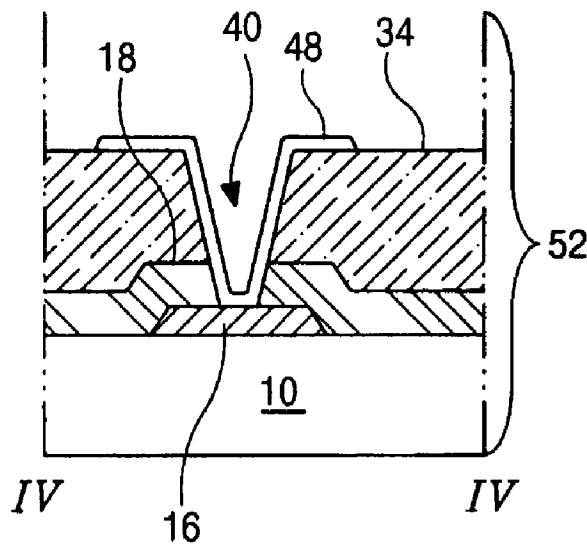
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FIG. 4B



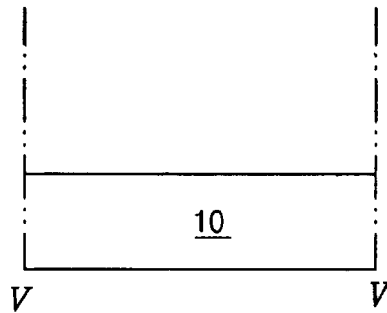
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FIG. 4C



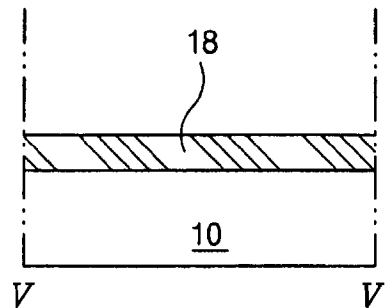
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FIG. 4D



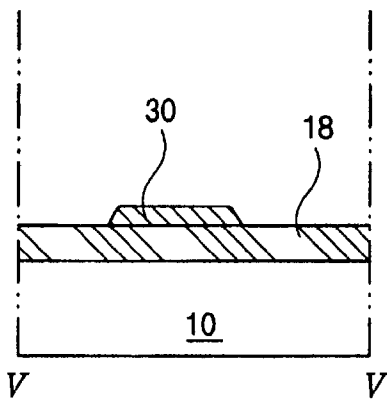
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FIG. 4E



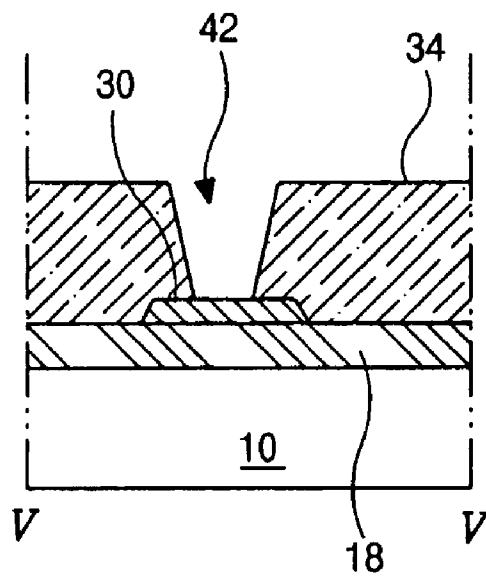
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FIG. 5A



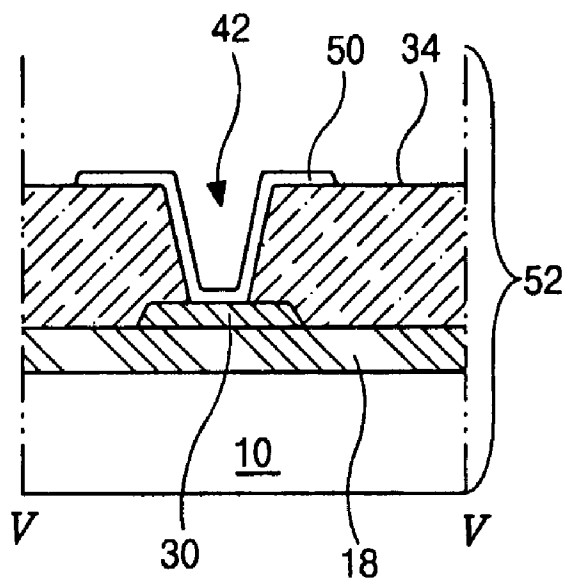
(RELATED ART)
FIG. 5B



(RELATED ART)
FIG. 5C



(RELATED ART)
FIG. 5D



(RELATED ART)
FIG. 5E

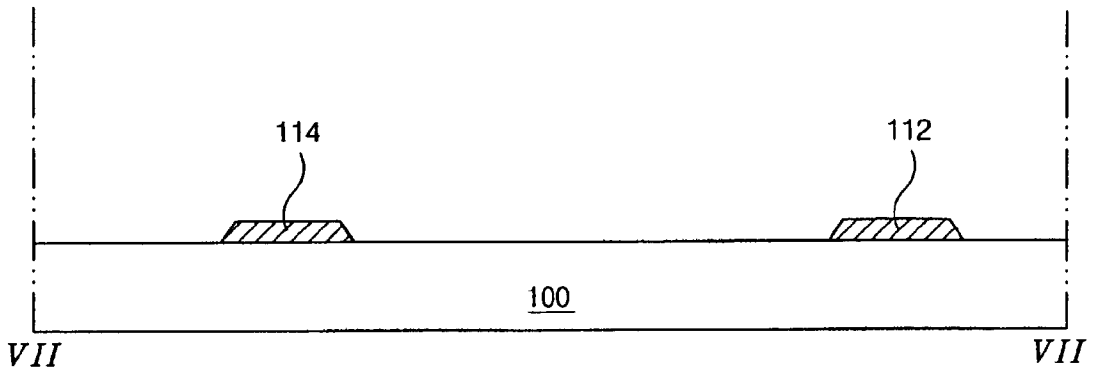


FIG. 7A

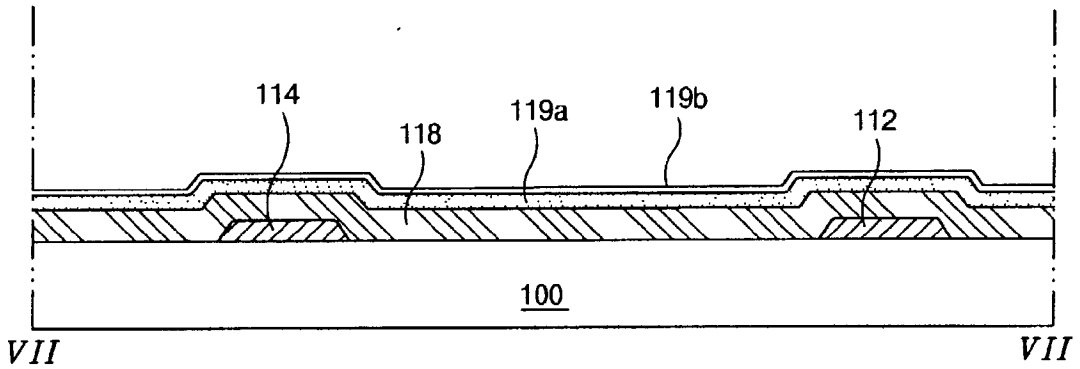


FIG. 7B

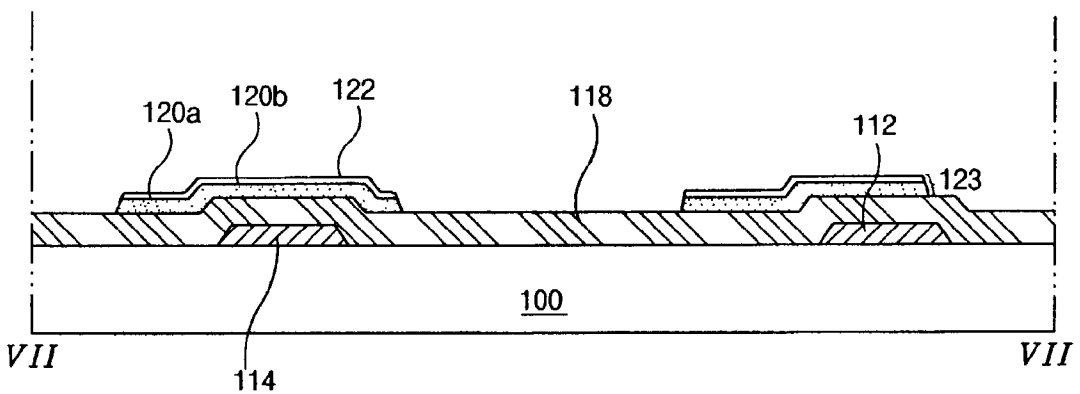


FIG. 7C

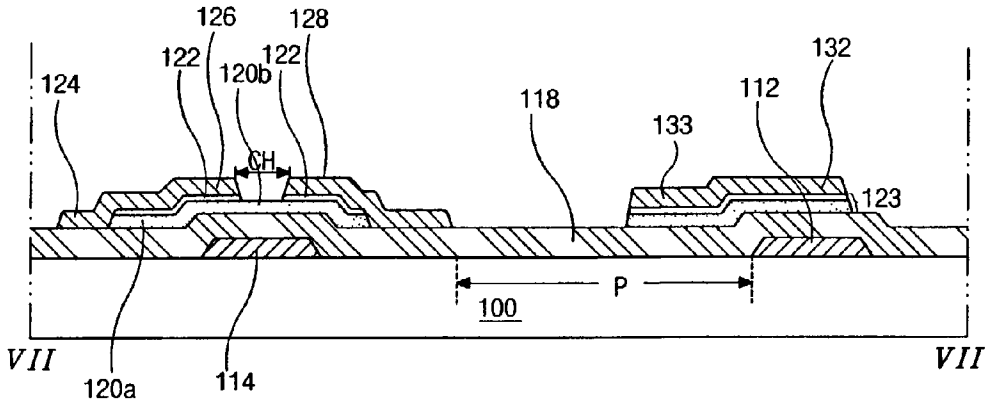


FIG. 7D

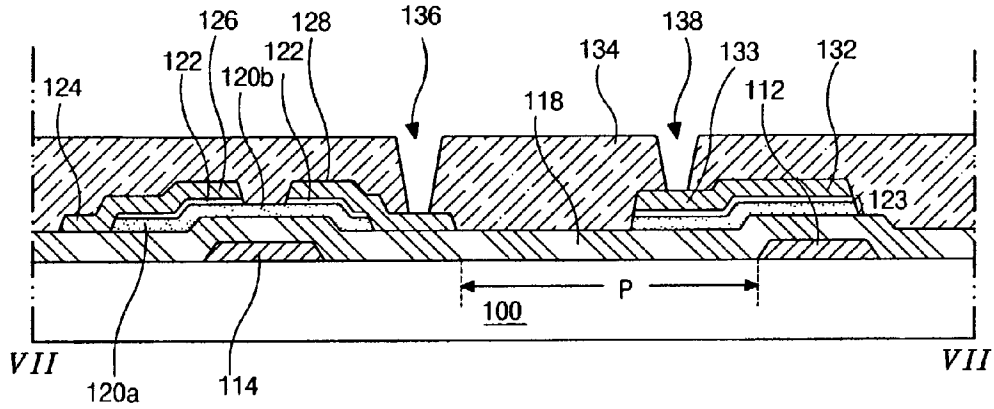


FIG. 7E

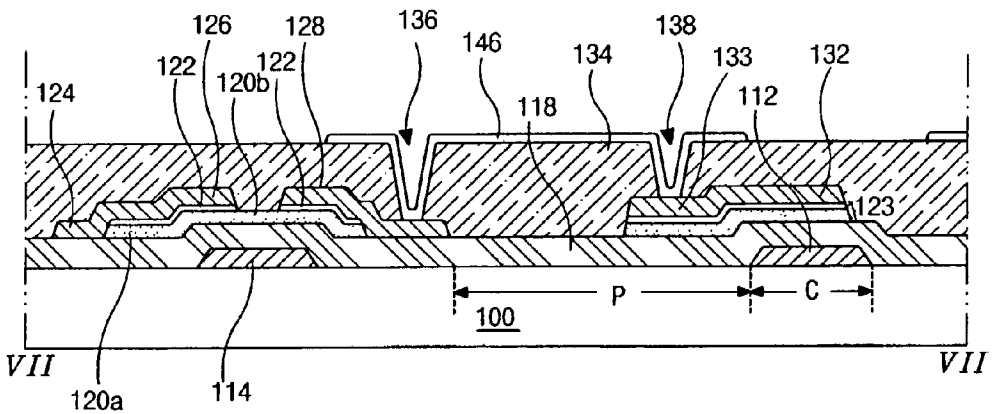


FIG. 7F

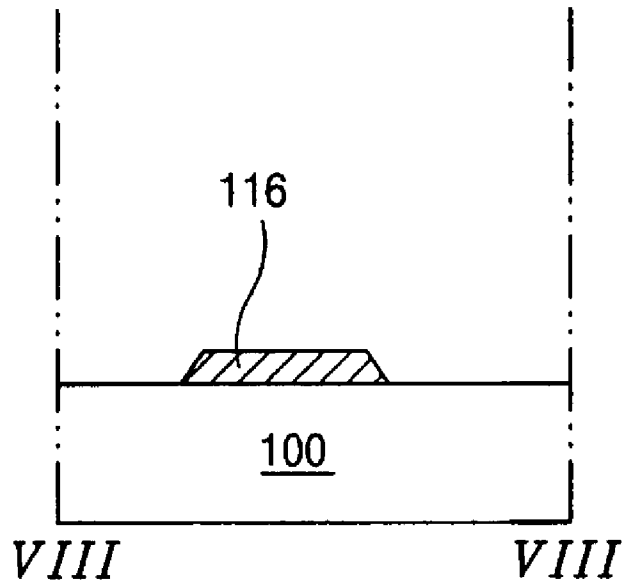


FIG. 8A

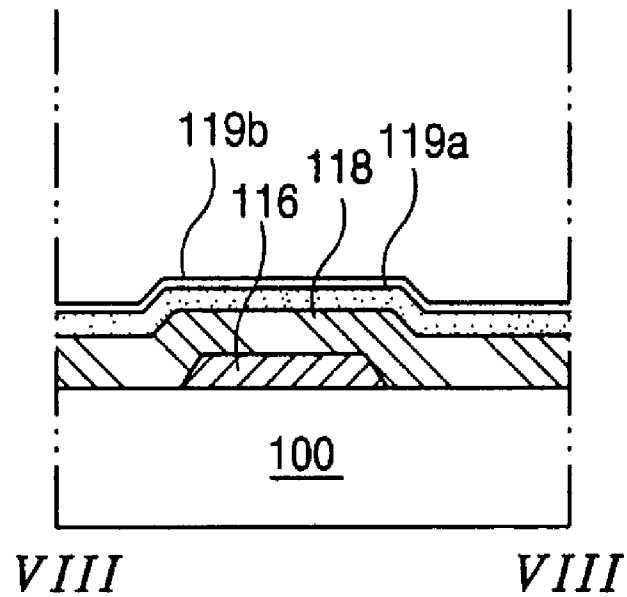


FIG. 8B

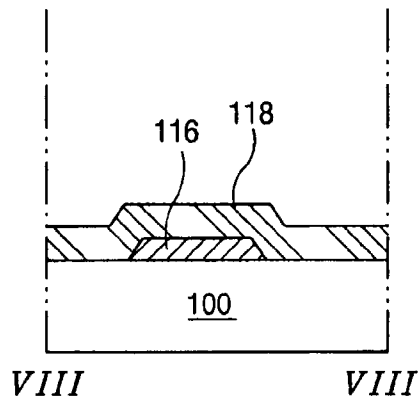


FIG. 8C

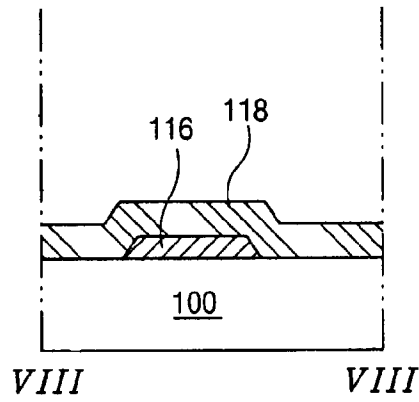


FIG. 8D

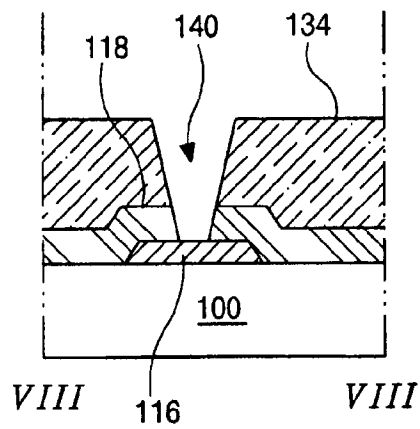


FIG. 8E

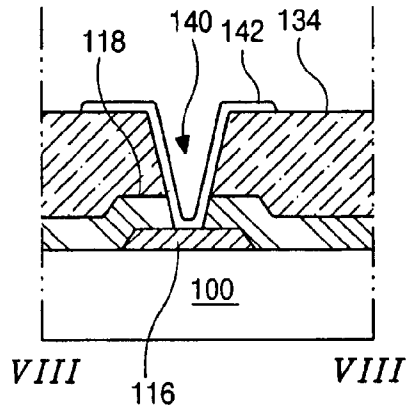


FIG. 8F

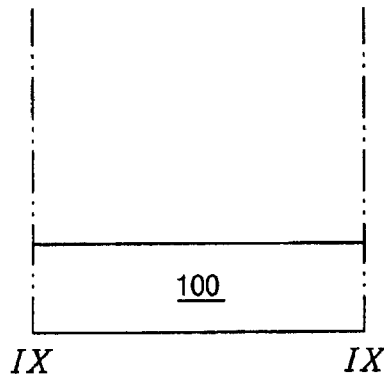


FIG. 9A

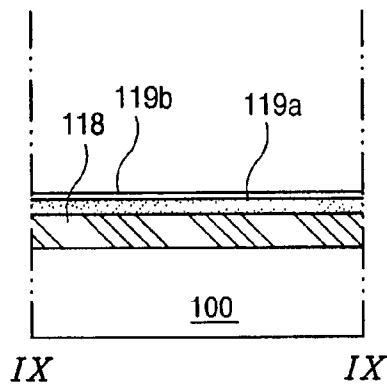


FIG. 9B

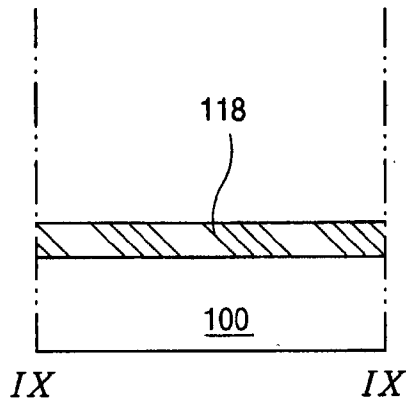


FIG. 9C

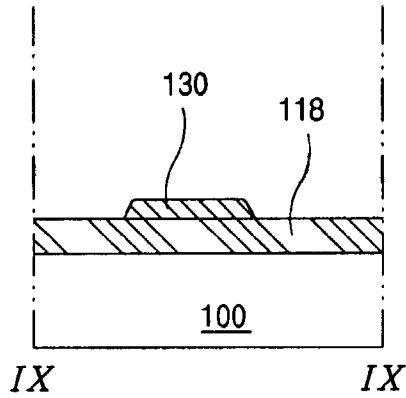


FIG. 9D

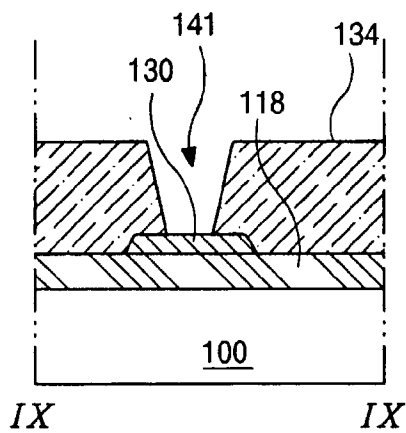


FIG. 9E

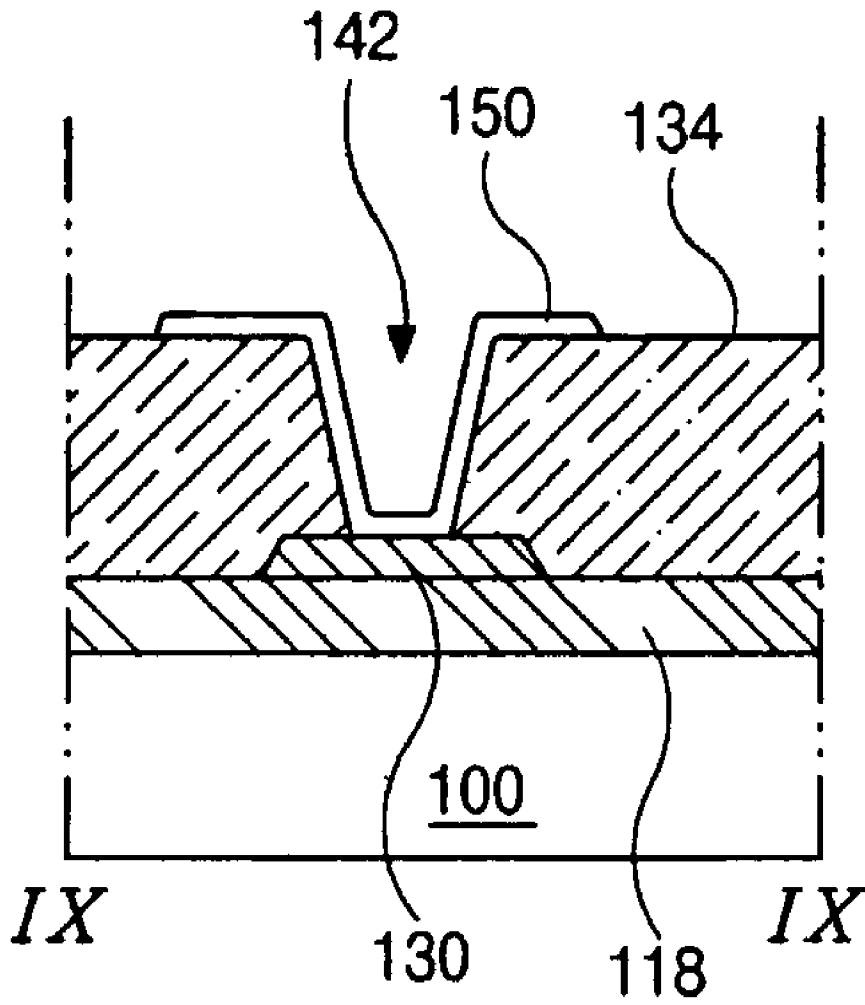


FIG. 9F

ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE

[0001] This application claims the benefit of Korean Patent Application No. 2001-51670, filed on Aug. 27, 2001 in Korea, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display device, and more particularly to an array substrate for use in the liquid crystal display (LCD) device.

[0004] 2. Discussion of the Related Art

[0005] Recently, light and thin liquid crystal display (LCD) devices with low power consumption are widely used in office automation equipment, video devices, and the like. Such LCDs typically use an optical anisotropy and spontaneous polarization of a liquid crystal (LC). The liquid crystal material has thin and long liquid crystal molecules, which cause a directional alignment of the liquid crystal molecules. Initially, an alignment direction of the liquid crystal molecules is controlled by applying an electric field to the liquid crystal molecules. With the alignment direction of the liquid crystal molecules properly adjusted, light is refracted along the alignment direction of the liquid crystal molecules to display image data. Of particular interest because of its high resolution and superiority in displaying moving pictures is an active matrix (AM) LCD, in which a plurality of thin film transistors and pixel electrodes are arranged in matrix array.

[0006] FIG. 1 shows an exploded perspective view illustrating a conventional LCD device. The LCD device 1 includes an upper substrate 5 and a lower substrate 10 that are spaced apart and face each other, and a liquid crystal layer 11 interposed therebetween. The upper substrate 5 and the lower substrate 10 are called a color filter substrate and an array substrate, respectively. On the rear surface of the upper substrate 5, a black matrix 6 and a color filter layer 7, including a plurality of red (R), green (G), and blue (B) color filters, are formed. The black matrix 6 surrounds each color filter forming an array matrix. The upper substrate 5 also includes a common electrode 9 covering the color filter layer 7 and the black matrix 6. The common electrode 9 is preferably made of a transparent conductive material.

[0007] On the front surface of the lower substrate 10, thin film transistors (TFTs) acting as switching elements are formed in the shape of an array matrix corresponding to the color filter layer 7. In addition, a plurality of gate and data lines 12 and 24 cross each other such that each TFT is positioned near each crossing of the gate and data lines 12 and 24. Each individual pair of gate and data lines 12 and 24 defines a pixel region P. In the pixel region P, a pixel electrode 46 is disposed. The pixel electrode 46 is formed of a transparent conductive material, such as indium tin oxide, which has an excellent transmissivity.

[0008] The LCD device having the above-mentioned structure displays color images by applying signals through the TFTs to the pixel electrodes 46. The gate line 12 applies a first signal to a gate electrode of the TFT, and the data line 24 applies a second signal to a source electrode of the TFT.

Therefore, the LCD device drives the liquid crystal molecules using their electro-optic characteristics.

[0009] The liquid crystal layer 11 is a dielectric anisotropic material having spontaneous polarization characteristics. Due to their dipole and spontaneous polarization when electric field signals are applied to the pixel electrode 46 and to the common electrode 9, the liquid crystal molecules of the liquid crystal layer 11 are re-arranged in accordance with the electric field. As the liquid crystal molecules are re-arranged, the optical property of the liquid crystal layer changes creating an electro-optic modulation effect.

[0010] FIG. 2 is an enlarged plan view illustrating a portion of an array substrate for the conventional LCD device of FIG. 1. The arrangement of the liquid crystal layer 11 is controlled by an array substrate 52 having the gate line 12 apply a scanning signal, the data line 24 apply an image signal. The thin film transistor (TFT) is connected to both the gate line 12 and the data line 24, and disposed near the crossing of the gate and data lines 12 and 24, with the pixel electrode 46 positioned in the pixel region P and connected to the TFT.

[0011] As mentioned above, the gate lines 12 are arranged in a transverse direction, and the data lines 24 are arranged perpendicular to the gate lines 12. A pair of gate lines 12 and a pair of data lines 24 define each the pixel region P. Each of thin film transistors (TFTs) is arranged at a position where the gate line 12 and the data line 24 cross one another. The pixel electrode 46 is disposed on the pixel region P defined by the pair of gate lines 12 and the pair data lines 24.

[0012] Each TFT includes a gate electrode 14 to receive the scanning signal from the gate line 12, a source electrode 26 to receive the image signal from the data line 24, and a drain electrode 28 to connect the image signal to the pixel electrode 46. Further, each TFT includes an active layer 20 between the source electrode 26 and the drain electrode 28, with the drain electrode 28 facing the source electrode across the active layer 20. The active layer 20 is made of for example, amorphous silicon (a-Si:H) or polycrystalline silicon. The gate electrode 14 extends from the gate line 12 and the source electrode 26 extends from the data line 24. The drain electrode 28 is connected to the pixel electrode 46 through a contact hole.

[0013] The pixel electrode 46 extends over the gate line 12 defining a storage capacitor C with a portion of the pixel electrode 46. Furthermore, gate pads 16 are formed at the end of the gate lines 12, respectively. A gate pad electrode 48 is disposed on each gate pad 16, to receive the scanning signal from a drive IC (not shown) and then applies the scanning signal to the gate lines 12 throughout the gate pad 16. Data pads 30 are disposed at the end of the data lines 24, respectively. A data pad electrode 50 is located on each data pad 30, to receive the image signal from a drive IC (not shown) and then to apply the image signal to the data line 24 through the data pad 30.

[0014] When the scanning signal is applied to the gate electrode 14 connected to the gate line 12, the TFT is activated (i.e., ON-STATE). The image signal is applied to the pixel electrode 46 throughout the TFT and the resulting electric field re-arranges the liquid crystal by polarizing action.

[0015] Alternatively, when the scanning signal is not applied to the gate electrode 14, the TFT is not activated (i.e., OFF-STATE) and the image signal is not applied to the pixel electrode 46. In the OFF-STATE, the electric field charges stored in the pixel region P are discharged to the TFT and to the liquid crystal. To prevent this discharge phenomenon, a storage capacitor C is connected in parallel to the pixel electrode 46. The storage capacitor C supplements the discharged electric charges with the stored electric charges. The storage capacitor C includes a capacitor electrode 32 that acts as a first electrode of the storage capacitor. A portion of the gate line 12 acts as a second electrode of the storage capacitor. The capacitor electrode 32 has an island shape and is positioned over the gate line 12, and the pixel electrode 46 contacts the island-shaped capacitor electrode 32 through a contact hole 38. With the capacitor electrode 32 interposed between the gate line 12 and the pixel electrode 46, the thickness of a dielectric layer of the storage capacitor C is minimized. Due to the thin dielectric layer, the capacitance of the storage capacitor can be raised.

[0016] With reference to FIGS. 3A to 3E, 4A to 4E and 5A to 5E, a fabrication process for the conventional array substrate is explained. FIGS. 3A to 3E are sequential cross-sectional views taken along line III-III of FIG. 2, and illustrate manufacturing the thin film transistor and the pixel region. FIGS. 4A to 4E are sequential cross-sectional views taken along line IV-IV of FIG. 2, and illustrate forming the gate pad. FIGS. 5A to 5E are sequential cross-sectional views taken along line V-V of FIG. 2, and illustrate forming the data pad.

[0017] The fabrication process begins as shown in FIGS. 3A, 4A and 5A, with a first metal deposited and patterned upon a transparent substrate 10 to form the gate line 12, the gate electrode 14, and the gate pad 16. Conventionally, the first metal employed is aluminum (Al), tungsten (W), molybdenum (Mo) or chromium (Cr). The gate line 12 extends from and connects with the gate pad 16, with the gate electrode 14 protruding from the gate line 12 (in FIG. 2). As discussed above, the gate pad 16 supplies the scanning signal to the gate line 12.

[0018] As shown in FIGS. 3B, 4B and 5B, a gate insulation layer 18 is formed on the transparent substrate 10 covering the metal layer previously formed. The gate insulation layer 18 may be an inorganic substance, such as silicon nitride (SiN_x) or silicon oxide (SiO_2), or an organic substance, such as benzocyclobutene (BCB) or acryl-based resin. Next, amorphous silicon (a-Si:H) and impurity-doped amorphous silicon (n^+/p^+ a-Si:H) are formed in series on the gate insulation layer 18. The amorphous silicon and impurity-doped amorphous silicon are simultaneously patterned to form an active layer 20 and an ohmic contact layer 22, respectively. The active layer 20 is formed on the gate insulation layer 18, particularly over the gate electrode 14, and the ohmic contact layer 22 is formed over the active layer 20.

[0019] Next, as shown in FIGS. 3C, 4C and 5C, the source electrode 26 and the drain electrode 28 are formed from a second metal over the ohmic contact layer 22. By depositing and patterning the second metal, both the source

electrode 26 and the drain electrode 28 are formed. Along with the data line 24 (in FIG. 2), the capacitor electrode 32 and the data pad 30 are formed on the gate insulation layer 18 such that the source electrode 26 extends from the data line 24. The source electrode 26 and the drain electrode 28 are spaced apart from each other and respectively overlap opposite ends of the gate electrode 14. The data pad 30 is positioned at the end of the data line 24 and supplies the image signal to the data line 24, as discussed above. The capacitor electrode 32 has an island shape and overlaps a portion of the gate line 12 to define the storage capacitor C of FIG. 2. Moreover, a portion of the ohmic contact layer 22 between the source electrode 26 and drain electrode 28 is eliminated to form a channel region CH.

[0020] Next, as shown in FIGS. 3D, 4D and 5D, a passivation layer 34 is formed on and over the above-mentioned intermediates with an organic substance such as benzocyclobutene (BCB) or an acryl-based resin. By patterning the passivation layer 34, a drain contact hole 36 is formed that exposes a portion of the drain electrode 28. Next, a capacitor contact hole 38 and a data pad contact hole 42 are also formed. The capacitor contact hole 38 exposes a portion of the capacitor electrode 32, and the data pad contact hole 42 exposes a portion of the data pad 30. Furthermore, by patterning both the passivation layer 34 and the gate insulation layer 18, a gate pad contact hole 40 is formed that exposes a portion of the gate pad 16.

[0021] Next, as shown in FIGS. 3E, 4E and 5E, a transparent conductive material, such as indium zinc oxide (IZO) or indium tin oxide (ITO), is deposited upon the passivation layer 34 having the contact holes and subsequently patterned to form the pixel electrode 46, the gate pad electrode 48 and the data pad electrode 50. As shown in FIG. 3E, the pixel electrode 46 electrically contacts the drain electrode 28 and the capacitor electrode 32 through the drain contact hole 36 and through the capacitor contact hole 38, respectively. As shown in FIG. 4E, the gate pad electrode 48 electrically contacts the gate pad 16 through the gate pad contact hole 40. As shown in FIG. 5E, the data pad electrode 50 electrically contacts the data pad 30 through the data pad contact hole 42.

[0022] In the array substrate fabricated by the process described above, the storage capacitor C includes the overlapping portion of the gate line 12 as a first electrode, the capacitor electrode 32 as a second electrode, and the gate insulation layer as a dielectric layer. The pixel electrode 46 is electrically connected with the capacitor electrode 32. Furthermore, since the gate insulation layer 18 is interposed between the gate line 12 and the capacitor electrode 32 in the above-mentioned storage capacitor C, the gate insulation layer 18 only acts as a dielectric layer, that increases the capacitance of the storage capacitor C. The capacitor C does not use both the gate insulation layer and the passivation layer as a dielectric layer.

[0023] However, during fabrication of the above array substrate, a short occurs between the pixel electrode and the gate line beneath. Generally, the capacitor contact hole, the gate pad contact hole and the data pad contact hole are formed by a dry etching method. Such a dry etch method is not as effective for selective management as compared to a wet etching method. Thus, the metal layers and the lower gate insulation layer are over-etched when forming the

contact holes. Even if the gate pad and the data pad beneath the pad contact holes are over-etched, the transparent pad electrodes can electrically contact the side of the gate and data pads. However, a short between the transparent pixel electrode and the gate line is caused if the capacitor electrode and the lower gate insulation layer are over-etched. If the first and second capacitor electrodes of the storage capacitor are short-circuited, it causes a misalignment of the liquid crystal layer.

SUMMARY OF THE INVENTION

[0024] Accordingly, the present invention is directed to a liquid crystal display (LCD) device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0025] An advantage of the present invention is to provide an array substrate for use in an LCD device which prevents a short circuit between a pixel electrode and a gate line even when an over-etch occurs in a capacitor electrode and a lower gate insulation layer, thereby increasing manufacturing yield.

[0026] Additional features and advantages of the invention will be set forth in the description that follows and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0027] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for use in a liquid crystal display device includes a substrate; at least a gate line and a gate electrode which are formed on the substrate, the gate line arranged in a transverse direction, the gate electrode extending from the gate line; a gate insulation layer formed on the substrate while covering the gate line and the gate electrode; an active line and an active layer on the gate insulation layer, the active line arranged in a longitudinal direction perpendicular to the gate line and the active layer extending from the active line over the gate electrode; an ohmic contact layer on the active line and on the active layer; at least a data line arranged in a longitudinal direction to overlap the active line, the data line defining a pixel region with the gate line; a source electrode on the ohmic contact layer, the source electrode extending from the data line; a drain electrode on the ohmic contact layer, the drain electrode spaced apart from the source electrode; a capacitor electrode over the gate line, the capacitor electrode having an island shape; an extension protruding from the capacitor electrode in the pixel region; a passivation layer on the gate insulation layer to cover the data line, the source electrode, the drain electrode, the capacitor electrode and the extension, wherein the passivation layer has a drain contact hole to the drain electrode and a storage contact hole to the extension of the capacitor electrode, and wherein the storage contact hole is disposed in the pixel region; and a pixel electrode formed in the pixel region, the pixel electrode contacting the drain electrode and the extension through the drain contact hole and through the storage contact hole, respectively.

[0028] In another aspect of the present invention, the array substrate further includes a silicon island pattern interposed

between the gate insulation layer and the capacitor electrode. Here, the silicon island pattern has the same shape as the capacitor electrode. The array substrate further includes a gate pad and a data pad, wherein the gate pad is formed at the end of the gate line and the data pad is formed at the end of the data line. The array substrate further includes a gate pad terminal that contacts the gate pad and a data pad terminal that contacts the data pad. The ohmic contact layer as discussed above, is interposed between the active line and the data line. Furthermore, the ohmic contact layer is interposed between the active layer and the source electrode and between the active layer and the drain electrode.

[0029] In another aspect, an array substrate for use in a liquid crystal display device includes a substrate; gate and data lines which cross each other to define a pixel region; a thin film transistor positioned near a crossing of the gate and data lines; a storage capacitor including a portion of the gate line as a first electrode and a capacitor electrode as a second electrode, wherein the capacitor electrode includes an extension protruding into the pixel region; and a pixel electrode positioned in the pixel region, the pixel electrode contacting the extension of the capacitor electrode through a contact hole. The thin film transistor includes a gate electrode, an active layer, an ohmic contact layer, a source electrode and a drain electrode. The active layer is formed of amorphous silicon and the ohmic contact layer is formed of impurity-doped amorphous silicon. The ohmic contact layer is interposed between the active layer and the source electrode and between the active layer and the drain electrode. The ohmic contact layer extends beneath the data line such that the data line overlaps the ohmic contact layer. The array substrate further includes a silicon island pattern interposed between the gate line and the capacitor electrode. Also, the silicon island pattern contacts and has the same shape as the capacitor electrode.

[0030] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0032] **FIG. 1** is an exploded perspective view illustrating a conventional LCD device;

[0033] **FIG. 2** is an enlarged plan view illustrating a portion of an array substrate for the conventional LCD device of **FIG. 1**;

[0034] **FIGS. 3A to 3E** are sequential cross-sectional views taken along line III-III of **FIG. 2** and illustrate manufacturing the thin film transistor and the pixel region;

[0035] **FIGS. 4A to 4E** are sequential cross-sectional views taken along line IV-IV of **FIG. 2** and illustrate forming the gate pad;

[0036] **FIGS. 5A to 5E** are sequential cross-sectional views taken along line V-V of **FIG. 2** and illustrate forming the data pad;

[0037] FIG. 6 is an enlarged plan view illustrating a portion of an array substrate for an LCD device according to the present invention;

[0038] FIGS. 7A to 7F are sequential cross-sectional views taken along line VII-VII of FIG. 6 and illustrate manufacturing a thin film transistor and a pixel region;

[0039] FIGS. 8A to 8F are sequential cross-sectional views taken along line VIII-VIII of FIG. 6 and illustrate forming a gate pad; and

[0040] FIGS. 9A to 9F are sequential cross-sectional views taken along line IX-IX of FIG. 6 and illustrate forming a data pad.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0041] Reference will now be made in detail to an illustrated embodiment of the present invention, which is illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0042] Referring to FIG. 6, an enlarged plan view illustrating a portion of an array substrate for an LCD device according to the present invention, gate lines 112 are arranged in a transverse direction, and data lines 124 are arranged in a longitudinal direction perpendicular to the gate lines 112. A pair of gate and data lines 112 and 124 define a pixel region P. Each of thin film transistors (TFTs) is arranged at a position where both the gate lines 112 and the data lines 124 cross one another. At the end of each gate line 112, a gate pad 116 is disposed, and a gate pad terminal 142 is disposed over the gate pad 116. The gate pad terminal 142 electrically contacts the gate pad 116 through a contact hole. A data pad 130 is disposed at the end of each data line 124, and a data pad terminal 150 is positioned over the data pad 130 contacting the data pad 130 through a contact hole.

[0043] The thin film transistor TFT includes a gate electrode 114 that extends from the gate line 112, a source electrode 126 that extends from the data line 124, and a drain electrode 128 that are spaced apart from the source electrode 126. The gate pad 116 supplies a scanning signal to the gate electrode 114 throughout the gate line 112, and the data pad 130 supplies an image signal to the source electrode 126 throughout the data line 124. An active layer 120b is disposed between the source 126 and drain 128 electrodes. The active layer 120b extends from an active line 120a that is formed just under the data line 124, and electrically contacts the source and drain electrodes 126 and 128. With the active line 120a beneath the data line 124 increases the adherence of the metallic data line 124 over the active line 120a.

[0044] Still referring to FIG. 6, pixel electrode 146 is disposed in the pixel region P and contacts the drain electrode 128 of the TFT through a contact hole. A portion of the pixel electrode 146 extends over the gate line 112 forming a storage capacitor C. A capacitor electrode 132 has an island shape and is disposed over the gate line 112. The island-shaped capacitor electrode 132 is also interposed between the gate line 112 and the pixel electrode 146. The capacitor electrode 132 has an extension 133 protruding into the pixel region P. Thus, in the present invention, the pixel electrode 146 contacts the extension 133 of the capacitor

electrode 132 through a storage contact hole 138. As shown in FIG. 6, the gate line 112 acts as a first electrode of the storage capacitor C, and the capacitor electrode 132 having the extension 133 acts as a second electrode of the storage capacitor C. Although not shown in FIG. 6, a gate insulation layer serves as a dielectric layer of the storage capacitor.

[0045] Still referring to FIG. 6, the storage capacitor C of the present invention, the storage contact hole 138 is positioned in the pixel region P since the capacitor electrode 132 has the extension 133 protruding into the pixel region P. Therefore, although the over-etching occurs when forming the storage contact hole 138, the pixel electrode 146 does not contact the gate line 112. Thus, unlike the conventional art, the short circuit between the pixel electrode 146 and the gate line 112 is prevented.

[0046] Next, shown in FIGS. 7A to 7F, 8A to 8F and 9A to 9F is a fabrication process for the inventive array substrate according to the present invention. FIGS. 7A to 7F show sequential cross-sectional views taken along line VII-VII of FIG. 6 and illustrate manufacturing the thin film transistor and the pixel region. FIGS. 8A to 8F are sequential cross-sectional views taken along line VIII-VIII of FIG. 6 and illustrate forming the gate pad. FIGS. 9A to 9F show sequential cross-sectional views taken along line IX-IX of FIG. 6 and illustrate a process forming the data pad.

[0047] The fabrication process begins as shown in FIGS. 7A, 8A and 9A, a first metal deposited and patterned upon a transparent substrate 100 to form the gate line 112, the gate electrode 114, and the gate pad 116. The present embodiment employs a first metal such as aluminum (Al), tungsten (W), molybdenum (Mo) or chromium (Cr). The gate line 112 extends from and connects with the gate pad 116, with the gate electrode 114 protruding from the gate line 112 (in FIG. 6). As discussed above, the gate pad 116 supplies the scanning signal to the gate line 112.

[0048] As shown in FIGS. 7B, 8B and 9B, a gate insulation layer 118 is formed on the transparent substrate 100 covering the metal layer previously formed. The gate insulation layer 118 may be an inorganic substance, such as silicon nitride (SiN_x) or silicon oxide (SiO_2), or an organic substance, such as benzocyclobutene (BCB) or acryl-based resin. Next, an amorphous silicon (a-Si:H) film 119a and an impurity-doped amorphous silicon (n^+/p^+ a-Si:H) film 119b are formed in series on the gate insulation layer 118.

[0049] Next, as shown in FIGS. 7C, 8C and 9C, the amorphous silicon film 119a and the impurity-doped amorphous silicon film 119b are simultaneously patterned to form the active line 120a, the active layer 120b and an ohmic contact layer 122. The active line 120a has the same shape as a data line that is formed in a later step. The active layer 120b extends from the active line 120a over the gate electrode 114. The ohmic contact layer 122 has the same shape as the active line 120a and layer 120b. The ohmic contact layer 122 is formed on the active layer 120b. Furthermore, a silicon island pattern 123 consisting of amorphous silicon and impurity-doped amorphous silicon is formed on the gate insulation layer 118, particularly over the gate line 112. The silicon island pattern 123 has the same shape as the capacitor electrode that is formed in a later step, so the silicon island pattern 123 helps to increase adherence of the metal layer (the capacitor electrode). Although the silicon island pattern 123 is formed using the silicon films in

the present invention, the silicon island pattern 123 can be omitted and eliminated in the present invention. Thus, the capacitor electrode (see reference 132 of FIG. 7D) can be directly formed just on the gate insulation layer 118. Meanwhile, as shown in FIGS. 8C and 9C, no silicon layers are formed in portions for the gate and data pads.

[0050] Next as shown in FIGS. 7D, 8D and 9D, the source electrode 126 and the drain electrode 128 are formed from a second metal over the ohmic contact layer 122. By depositing and patterning the second metal, both the source electrode 126 and the drain electrode 128 are formed. Along with the data line 124, the capacitor electrode 132 and the data pad 130 are formed. In the present embodiment, the data line 124 overlaps the active line 120a, and the source electrode 126 extends from the data line 124. The source electrode 126 and the drain electrode 128 are spaced apart from each other and respectively overlap opposite ends of the gate electrode 114. The data line 124 defines the pixel region P with the gate line 112. The data pad 130 is disposed at the end of the data line 124 such that the data pad 130 supplies the image signal to the data line 124.

[0051] Still referring to FIGS. 7D, 8D and 9D, the capacitor electrode 132 having an island shape is formed on the silicon island pattern 123. As discussed above, the capacitor electrode 132 overlaps a portion of the gate line 112 to define the storage capacitor C (in FIG. 6), and has the extension 133 protruding into the pixel region P. In this step of forming the capacitor electrode 132, the capacitor electrode 132 may be positioned just on the gate insulation layer 118 if the silicon island pattern 123 is not previously formed. Meanwhile, a portion of the ohmic contact layer 122 between the source electrode 126 and drain electrode 128 is eliminated to form a channel region CH.

[0052] Next as shown in FIGS. 7E, 8E and 9E, a passivation layer 134 is formed on and over the above-mentioned intermediates with an organic substance such as benzocyclobutene (BCB) or an acryl-based resin. By patterning the passivation layer 134, a drain contact hole 136 is formed that exposes a portion of the drain electrode 128. Next, the storage contact hole 138 and a data pad contact hole 142 are also formed. The storage contact hole 138 is formed in the pixel region P and exposes the extension 133 of the capacitor electrode 132. The data pad contact hole 142 exposes a portion of the data pad 130. Furthermore, by patterning both the passivation layer 134 and the gate insulation layer 118, a gate pad contact hole 140 is formed that exposes a portion of the gate pad 116. In the present embodiment as shown in FIG. 7E, although the over etch occurs when forming the contact holes, it is impossible for the storage contact hole 138 to expose the gate line 112.

[0053] Next, as shown in FIGS. 7F, 8F and 9F, a transparent conductive material, such as indium zinc oxide (IZO) or indium tin oxide (ITO), is deposited upon the passivation layer 134 having the aforementioned contact holes, and subsequently patterned to form the pixel electrode 146, the gate pad terminal 142 and the data pad terminal 150. For example, as shown in FIG. 7F, the pixel electrode 146 electrically contacts the drain electrode 128 and the capacitor electrode 132 through the drain contact hole 136 and through the storage contact hole 138, respectively. Further, as shown in FIG. 8F, the gate pad terminal 146 electrically contacts the gate pad 116 through the gate pad contact hole

140. Still further, as shown in FIG. 9F, the data pad terminal 150 electrically contacts the data pad 130 through the data pad contact hole 142.

[0054] In the array substrate according to the present invention, the storage capacitor C includes the overlapping portion of the gate line 112, the gate insulation layer 118, and the capacitor electrode 132 having the extension 133. The overlapping portion of the gate line 112 serves as a first electrode of the storage capacitor; the gate insulation layer 118 serves as a dielectric layer; and the capacitor electrode 132 having the extension 133 serves as a second electrode of the storage capacitor. During the fabrication process of the above array substrate, and although the over-etch occurs in the contact holes, including the storage contact hole 138, the pixel electrode 146 is not short-circuited with the gate line 112 since the storage contact hole 138 is formed in the pixel region P and is not formed over the gate line 112. Therefore, since the capacitor electrode 132 has the extension 133 over the pixel region P, and the storage contact hole 138 is formed to the extension 133, the pixel electrode 146 contacts the extension 133 through the storage contact hole 138. Accordingly, unlike the conventional art, the present invention does not create a short between the pixel electrode 146 and the gate line 112, thereby increasing the manufacturing yield.

[0055] It will be apparent to those skilled in the art that various modifications and variation can be made in the method of manufacturing a thin film transistor of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An array substrate for use in a liquid crystal display device, comprising:

- a substrate;
- at least a gate line and a gate electrode on the substrate, the gate line arranged in a transverse direction, the gate electrode extending from the gate line;
- a gate insulation layer on the substrate and covering the gate line and the gate electrode;
- an active line and an active layer on the gate insulation layer, the active line arranged in a longitudinal direction perpendicular to the gate line and the active layer extending from the active line over the gate electrode;
- an ohmic contact layer on the active line and on the active layer;
- at least a data line arranged in a longitudinal direction to overlap the active line, the data line defining a pixel region with the gate line;
- a source electrode on the ohmic contact layer, the source electrode extending from the data line;
- a drain electrode on the ohmic contact layer, the drain electrode spaced apart from the source electrode;
- a capacitor electrode over the gate line, the capacitor electrode having an island shape;
- an extension protruding from the capacitor electrode into the pixel region;

- a passivation layer on the gate insulation layer covering the data line, the source electrode, the drain electrode, the capacitor electrode and the extension, wherein the passivation layer has a drain contact hole to the drain electrode and a storage contact hole to the extension of the capacitor electrode, and wherein the storage contact hole is disposed in the pixel region; and
- a pixel electrode formed in the pixel region, the pixel electrode contacting the drain electrode and the extension through the drain contact hole and through the storage contact hole, respectively.
2. The array substrate of claim 1, further comprising a silicon island pattern interposed between the gate insulation layer and the capacitor electrode.
3. The array substrate of claim 2, wherein the silicon island pattern has the same shape as the capacitor electrode.
4. The array substrate of claim 1, further comprising a gate pad at the end of the gate line and a data pad at the end of the data line.
5. The array substrate of claim 4, further comprising a gate pad terminal that contacts the gate pad and a data pad terminal that contacts the data pad.
6. The array substrate of claim 1, wherein the ohmic contact layer is interposed between the active line and the data line.
7. The array substrate of claim 1, wherein the ohmic contact layer being interposed between the active layer and the source electrode and between the active layer and the drain electrode.
8. An array substrate for use in a liquid crystal display device, comprising:
- a substrate;
- gate and data lines which cross each other to define a pixel region;
- a thin film transistor positioned near a crossing of the gate and data lines;
- a storage capacitor including a portion of the gate line as a first electrode and a capacitor electrode as a second electrode, wherein the capacitor electrode includes an extension protruding into the pixel region; and
- a pixel electrode positioned in the pixel region, the pixel electrode contacting the extension of the capacitor electrode through a contact hole.
9. The array substrate of claim 8, wherein the thin film transistor includes a gate electrode, an active layer, an ohmic contact layer, a source electrode and a drain electrode.
10. The array substrate of claim 9, wherein the active layer being formed of amorphous silicon and the ohmic contact layer being formed of impurity-doped amorphous silicon.
11. The array substrate of claim 10, wherein the ohmic contact layer being interposed between the active layer and the source electrode and between the active layer and the drain electrode.
12. The array substrate of claim 11, wherein the ohmic contact layer extends beneath the data line such that the data line overlaps the ohmic contact layer.
13. The array substrate of claim 8, further comprising a silicon island pattern interposed between the gate line and the capacitor electrode.
14. The array substrate of claim 13, wherein the silicon island pattern contacts and has the same shape as the capacitor electrode.

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