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DEOKA

(54) **REPRODUCTION APPARATUS AND REPRODUCTION METHOD**

(75) Inventor: **Yoshihiko DEOKA**, Tokyo (JP)

Correspondence Address:
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314 (US)

(73) Assignee: **Sony Corporation**, Minato-ku (JP)

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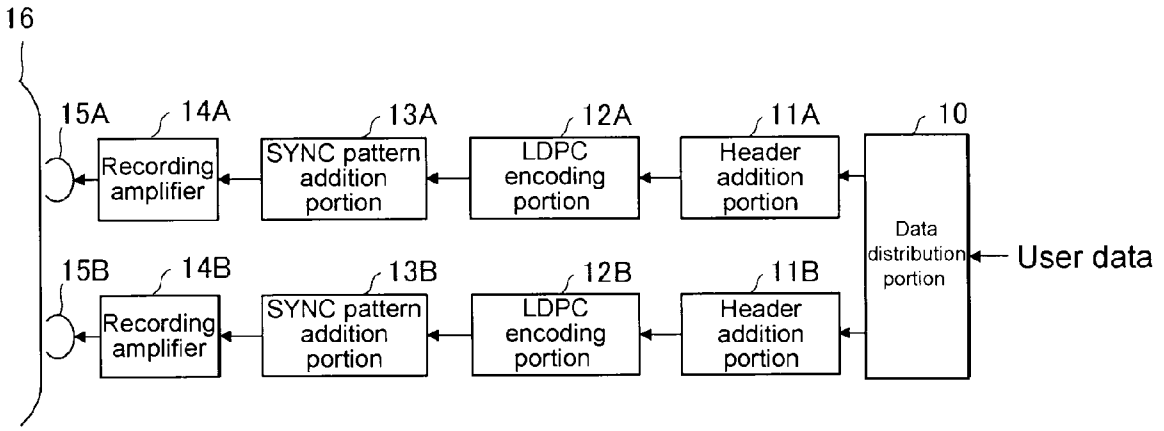
(57) **ABSTRACT**

Disclosed is a reproduction apparatus that reproduces signals of a plurality of channels including: a soft-decision portion that performs a soft decision on each bit of a block encoded with an LDPC code for each channel, as a bit string corresponding to a length of the LDPC code; a holding portion that holds a soft-decision result on the block basis for each channel; a decoding portion that inputs the soft-decision result on the block basis and obtains an estimated bit string by an iterative decoding; and a control portion that determines a priority order among channels for each of which a next block is subjected to the iterative decoding, based on an iteration count at an end of the iterative decoding for each channel, and controls the input of the soft-decision result so that the iterative decoding is performed for each channel in accordance with the priority order.



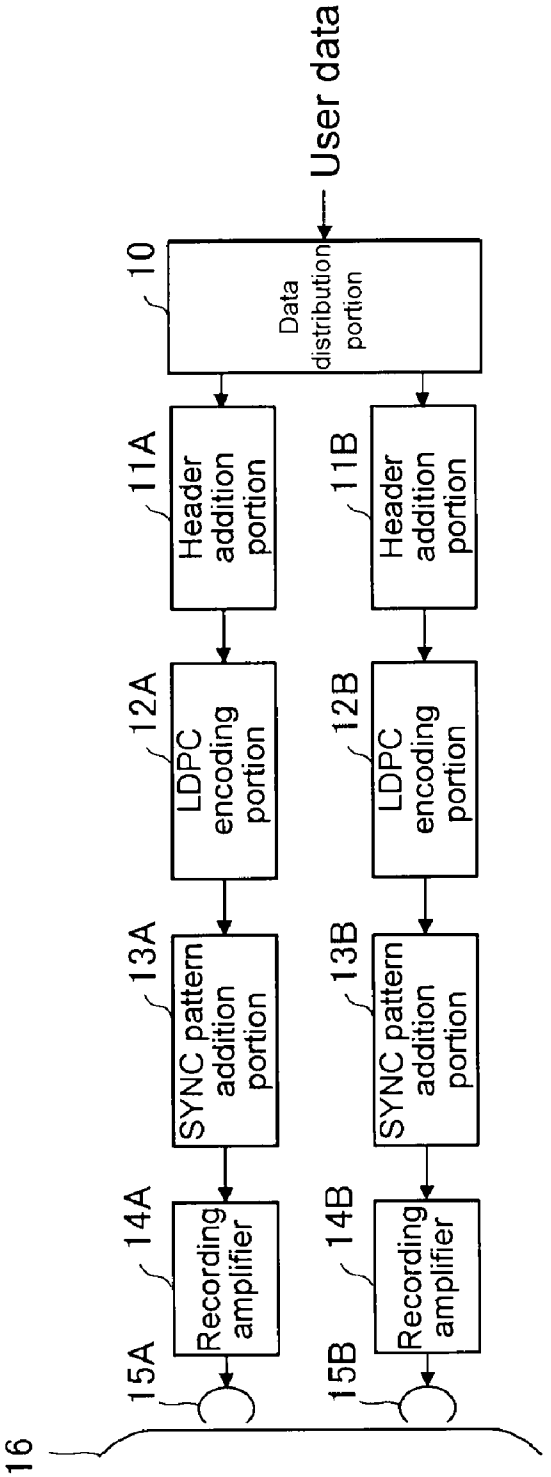

User data
10
Data distribution portion
11A
Header addition portion
11B
Header addition portion
12A
LDPC encoding portion
12B
LDPC encoding portion
13A
SYNC pattern addition portion
13B
SYNC pattern addition portion
14A
Recording amplifier
14B
Recording amplifier
15A
15B
16

FIG.1

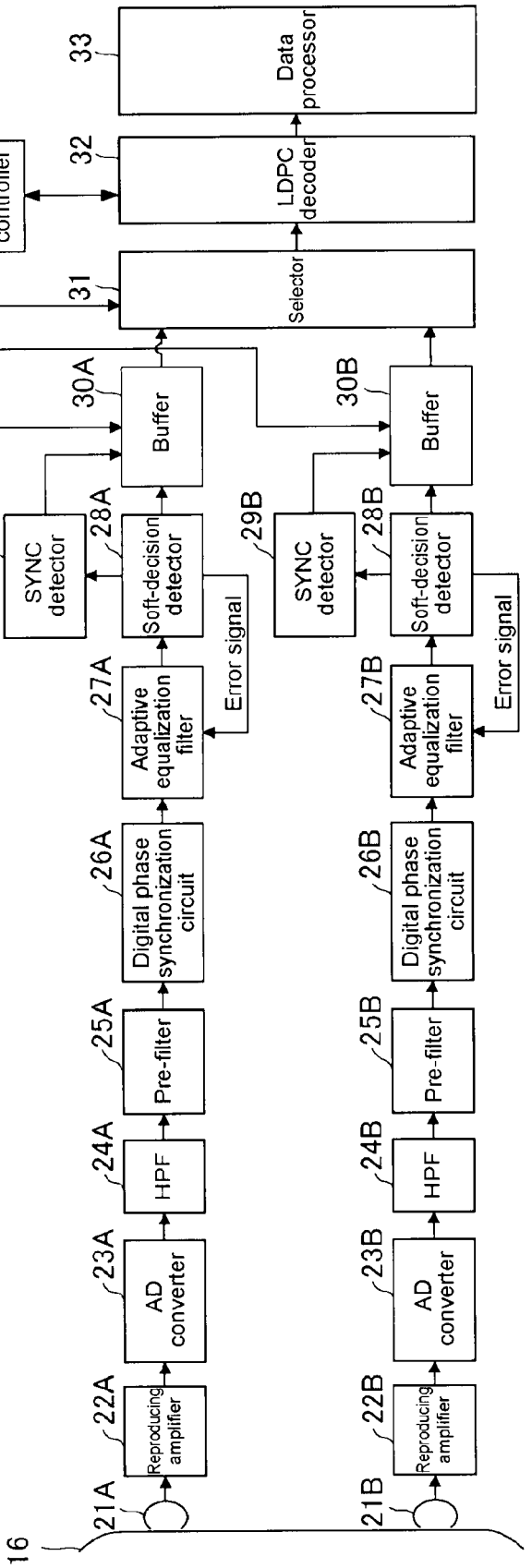

16
21A
21B
Reproducing amplifier
22A
22B
AD converter
23A
23B
HPF
24A
24B
Pre-filter
25A
25B
Digital phase synchronization circuit
26A
26B
Adaptive equalization filter
27A
27B
Error signal
Soft-decision detector
28A
28B
SYNC detector
29A
29B
Buffer
30A
30B
Selector
31
LDPC decoder
32
Data processor
33
Buffer/ selector controller
34

FIG.2

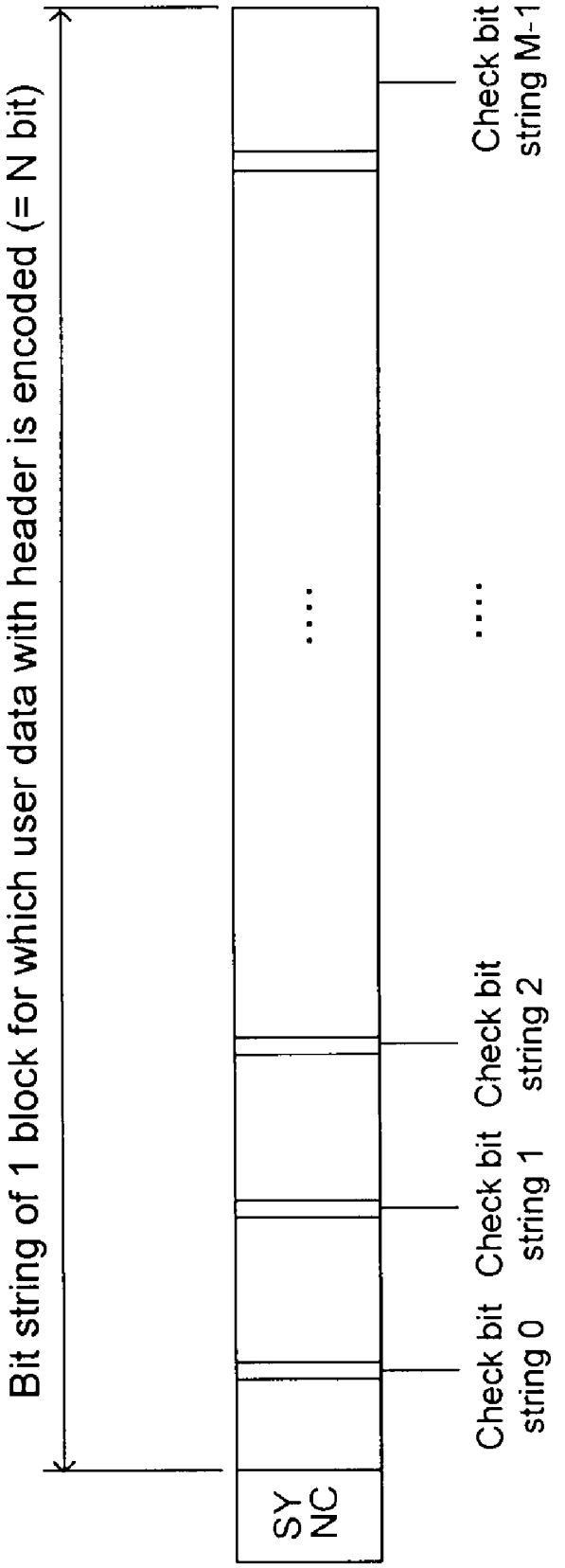

Bit string of 1 block for which user data with header is encoded (= N bit)
SY NC
Check bit string 0
Check bit string 1
Check bit string 2
Check bit string M-1

FIG.3

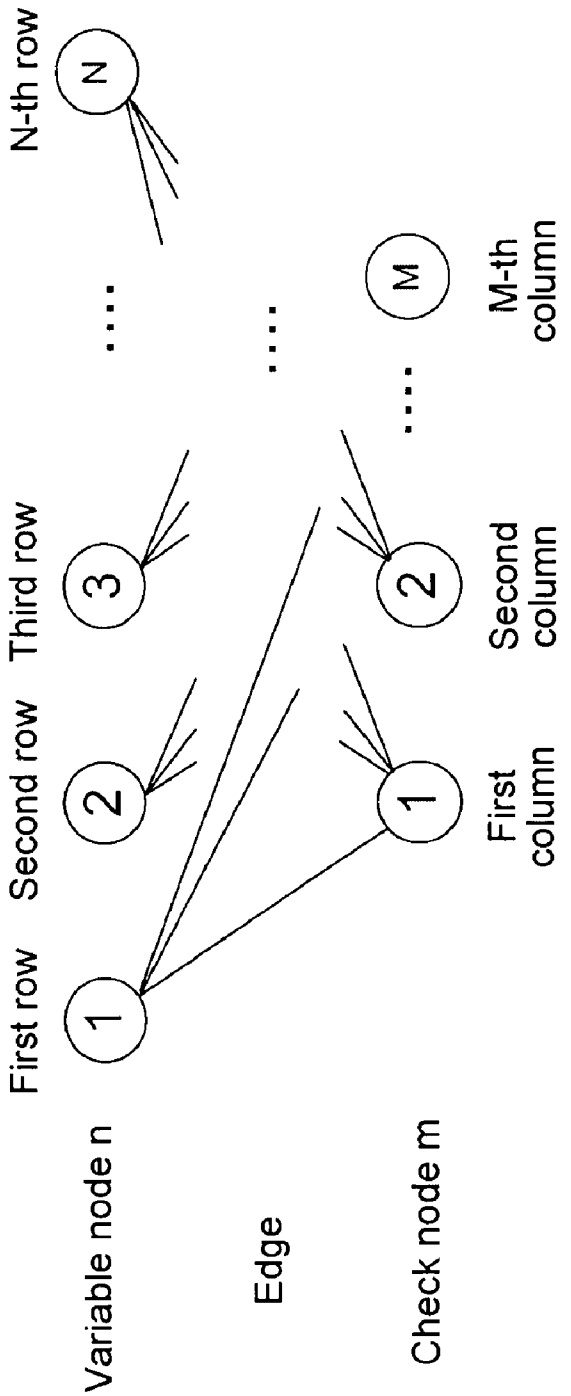

First row
Second row
Third row
N-th row
1
2
3
N
Variable node n
Edge
Check node m
First column
Second column
M-th column
1
2
M

FIG.4

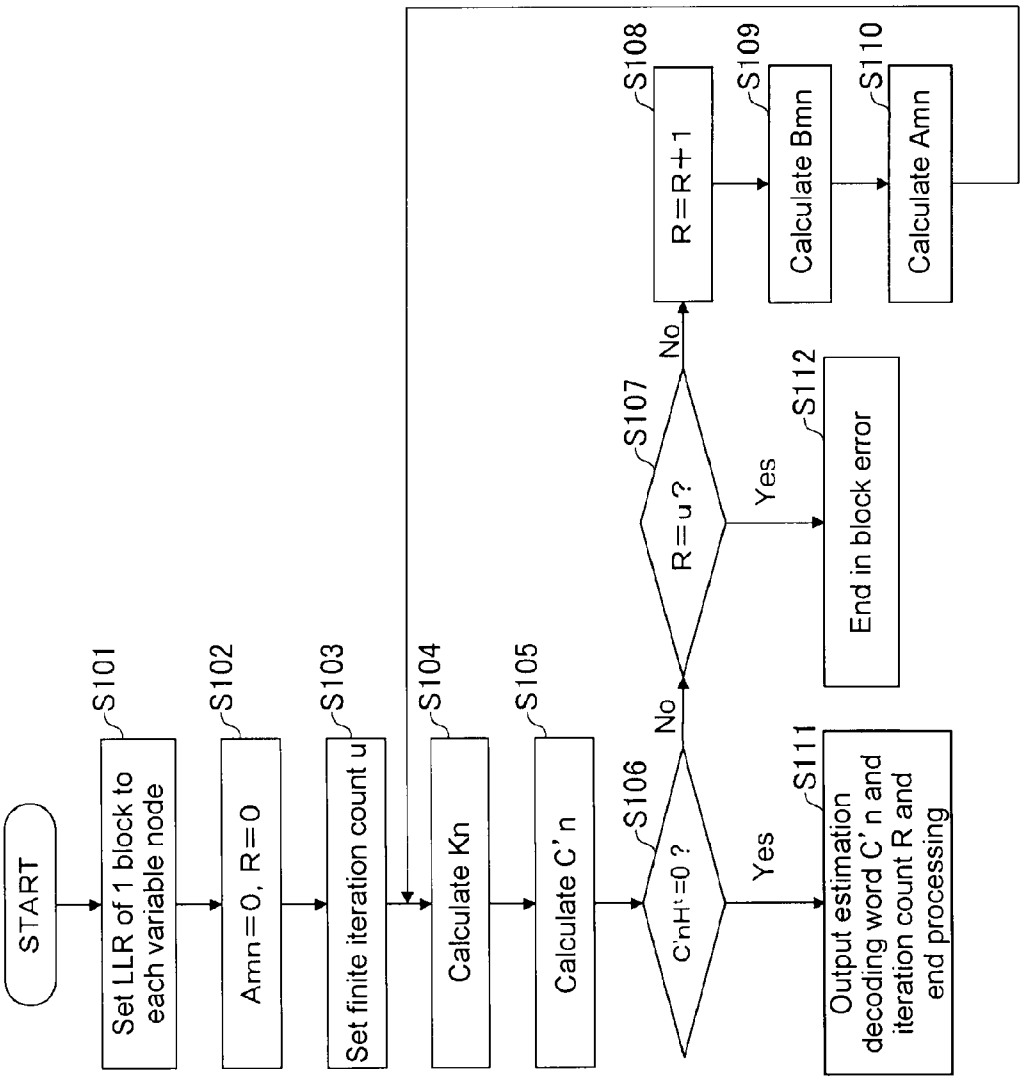

START
S101
Set LLR of 1 block to each variable node
S102
Amn=0, R=0
S103
Set finite iteration count u
S104
Calculate Kn
S105
Calculate C'n
S106
C'nH^t=0 ?
No
Yes
S107
R=u ?
No
Yes
S108
R=R+1
S109
Calculate Bmn
S110
Calculate Amn
S111
Output estimation decoding word C'n and iteration count R and end processing
S112
End in block error

FIG.5

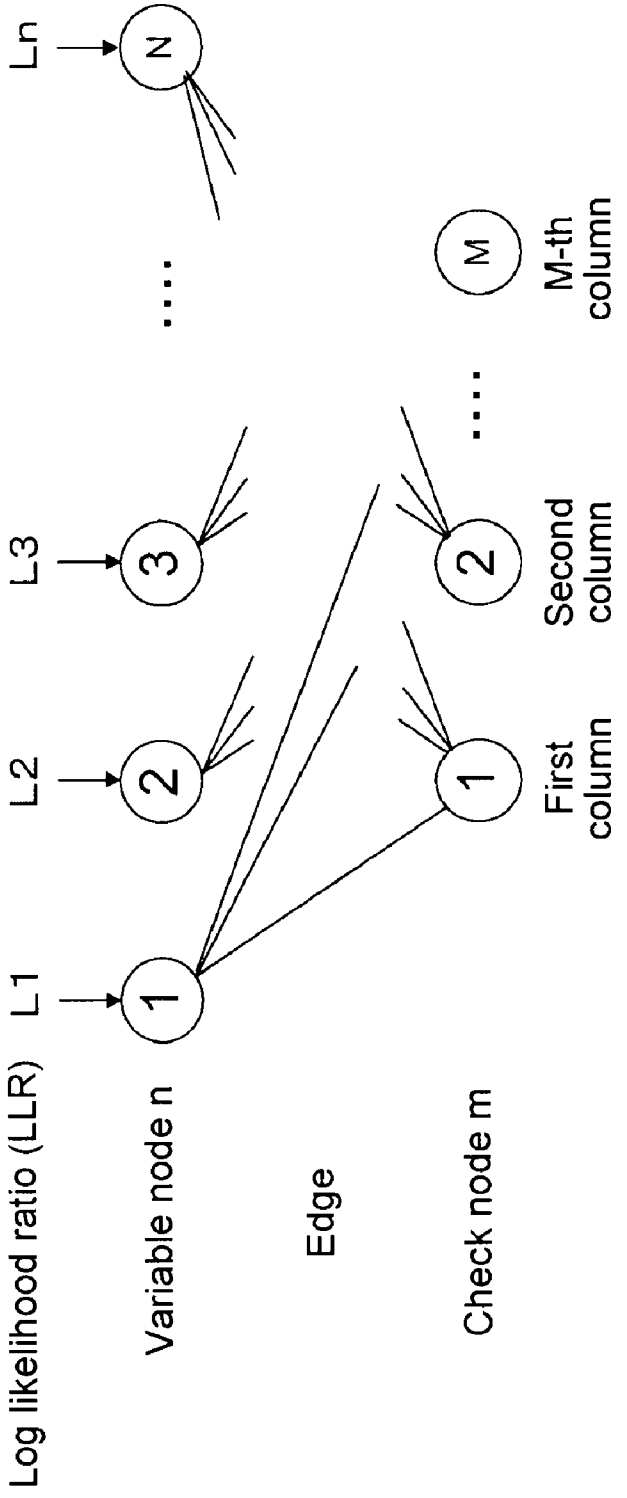

Log likelihood ratio (LLR)
L1
L2
L3
Ln
1
2
3
N
Variable node n
Edge
Check node m
1
2
M
First column
Second column
M-th column

FIG.6

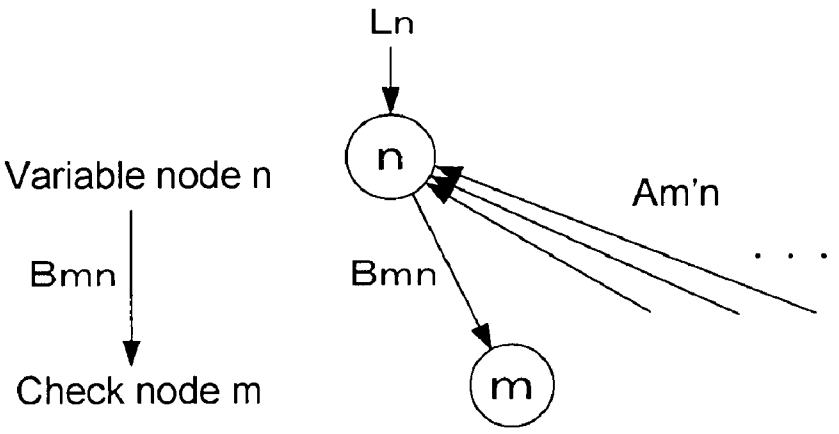


FIG.7

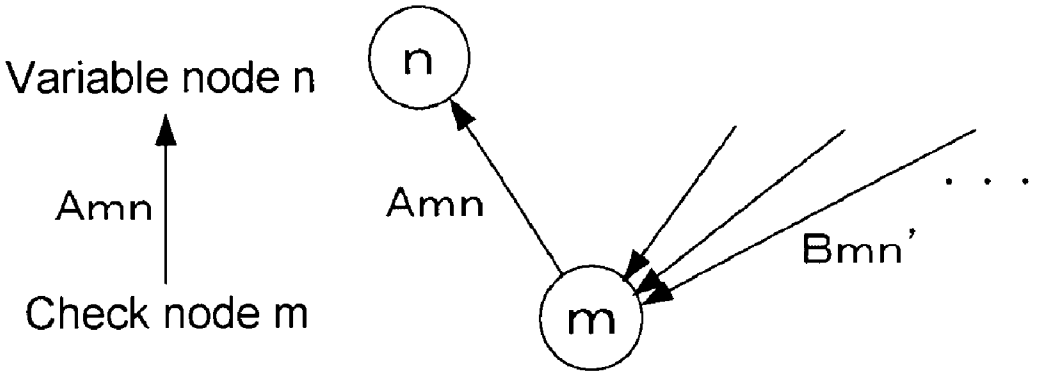


FIG.8

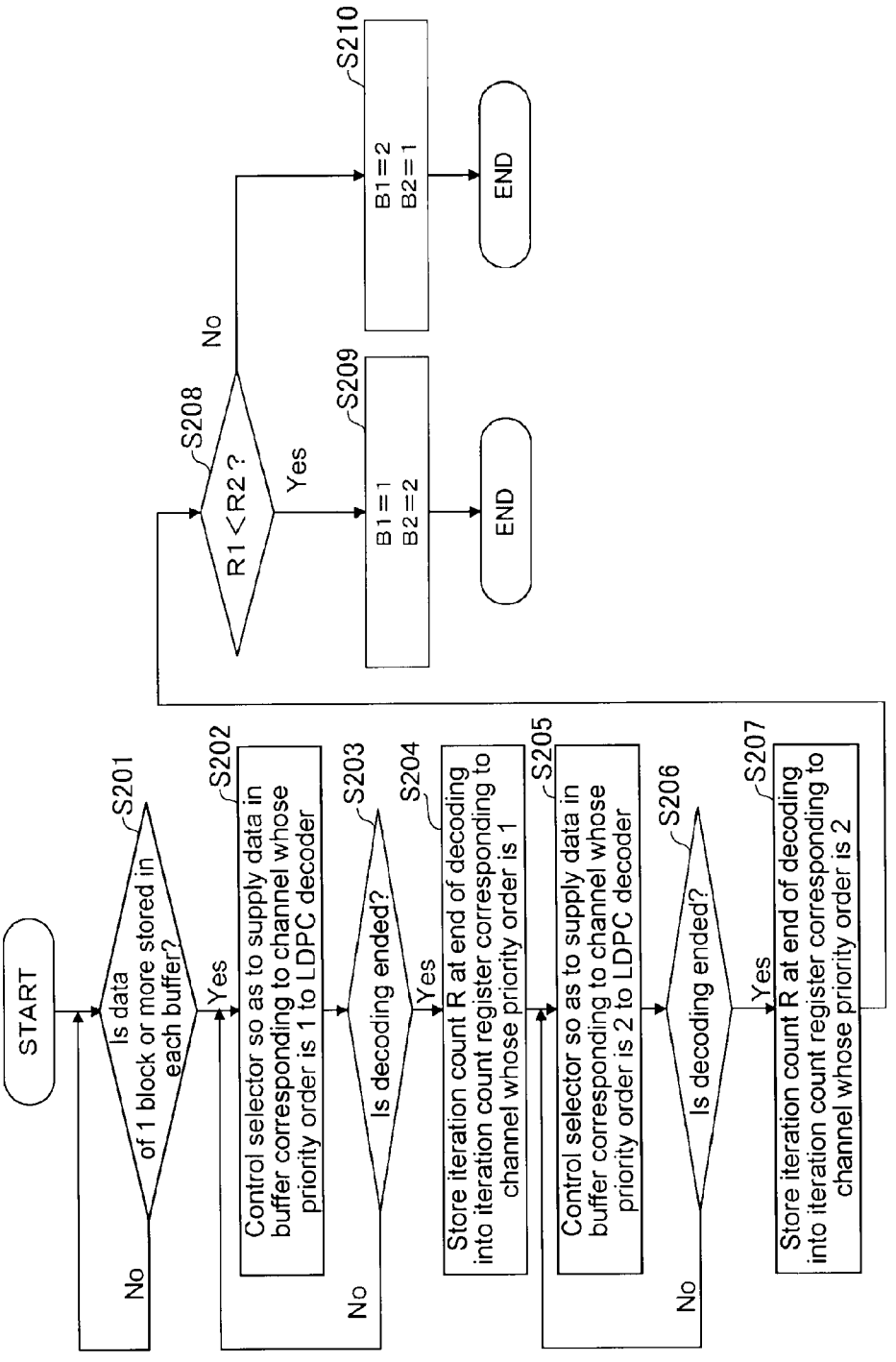

START
S201
Is data of 1 block or more stored in each buffer?
No
Yes
S202
Control selector so as to supply data in buffer corresponding to channel whose priority order is 1 to LDPC decoder
S203
Is decoding ended?
No
Yes
S204
Store iteration count R at end of decoding into iteration count register corresponding to channel whose priority order is 1
S205
Control selector so as to supply data in buffer corresponding to channel whose priority order is 2 to LDPC decoder
S206
Is decoding ended?
No
Yes
S207
Store iteration count R at end of decoding into iteration count register corresponding to channel whose priority order is 2
S208
R1<R2 ?
Yes
No
S209
B1=1
B2=2
END
S210
B1=2
B2=1
END

FIG.9

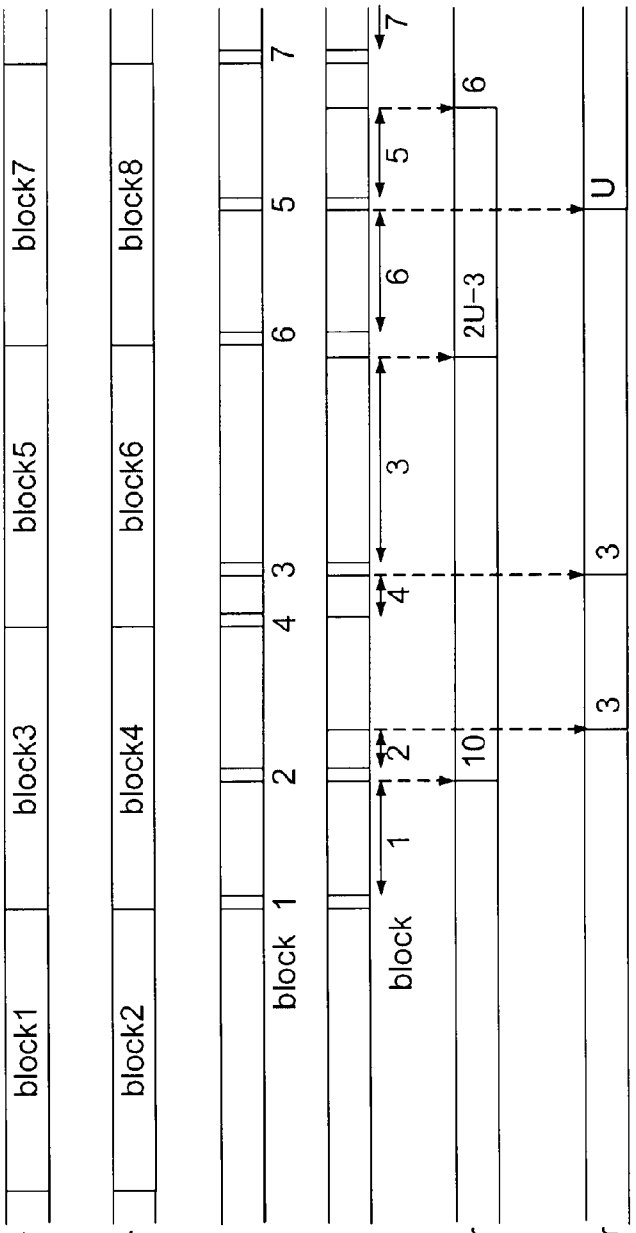

Block in ch1 buffer
block1
block3
block5
block7
Block in ch2 buffer
block2
block4
block6
block8
Selector output
block 1
2
4
3
6
5
7
LDPC decoding
block
1
2
4
3
6
5
7
Ch1 iteration count register
10
2U−3
6
Ch2 iteration count register
3
3
U
block Iteration count
1 10
2 3
3 2U-3
4 3
5 6
6 U

FIG.10

REPRODUCTION APPARATUS AND REPRODUCTION METHOD

CROSS REFERENCES TO RELATED APPLICATIONS

[0001] The present invention contains subject matter related to Japanese Patent Application JP 2007-259680 filed in the Japanese Patent Office on Oct. 3, 2007, the entire contents of which being incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a reproduction apparatus and a reproduction method for reproducing signals of a plurality of channels from a recording medium. In particular, the present invention relates to a reproduction apparatus and a reproduction method for performing reproduction by decoding an LDPC code.

[0004] 2. Description of the Related Art

[0005] A low-density parity-check code (hereinafter, referred to as an LDPC code) is attracting lots of attention. It is becoming clear that similar to a turbo code or the like, the LDPC code can exhibit performance close to a Shannon limit as a code length thereof is increased. Further, the LDPC code has such a feature that a minimum distance is proportional to the code length, and thus a block error probability characteristic is favorable. In addition, there hardly occurs a so-called error floor phenomenon, which is observed as a decoding characteristic of the turbo code or the like. These are advantages of the LDPC code.

[0006] The greatest characteristic of the LDPC code is that a parity check matrix that defines the LDPC code is a sparse matrix. Herein, the sparse matrix refers to a matrix having a significantly small number of components of "1". The encoding with the LDPC code is executed by generating a generator matrix G based on a check matrix H, and multiplying a binary information message by the generator matrix G, to thereby generate an encoding word. Specifically, an encoding apparatus that performs encoding with the LDPC code first calculates the generator matrix G that establishes an expression $GH^T=0$ in a relationship with a transposed matrix H^T of the check matrix H.

[0007] Meanwhile, as a method of decoding the LDPC code, a sum-product algorism is proposed. In the sum-product algorism, a calculation regarding a posterior probability is separated into a "variable node processing" and a "check node processing", and they are repeatedly performed to thereby determine a bit string having high estimation accuracy. The posterior probability refers to a conditional probability regarding encoding words based on a premise that a reception signal is known. The sum-product algorism is obtained by approximating a bitwise maximum posterior probability decoding method, which is a method of calculating the posterior probability without omission. The sum-product algorism significantly increases efficiency of an approximate calculation by using the sparse matrix.

[0008] In the sum-product algorism, as an iteration count of an iterative decoding is increased, the estimation accuracy is improved and a code error can be corrected. In general, an upper limit is put on the iteration count. This is because, in the sum-product algorism, such a convergence that the increase in iteration count provides a bit string that meets a parity search condition is not ensured.

[0009] When the method of decoding the LDPC code with the sum-product algorism is used for a system required to conduct a real-time operation, for example, to reproduce data on an apparatus that performs record/reproduction with respect to a tape-like magnetic recording medium in real time, the upper limit of the iteration count should be set under further severe restriction. If a bit string that meets the parity search condition is not obtained even when the upper limit of the iteration count is exceeded, the iterative decoding is forcibly terminated as an error in the error correction.

[0010] In addition, Japanese Patent Application Laid-open No. 2007-6382 discloses a technique of determining, in an iterative decoding of an LDPC code, a maximum iteration count of each code block in order to determine an optimal iteration count in terms of processing efficiency and power consumption, based on an allowed time assignable to an iterative decoding for one frame, the number of code blocks in one frame, and each code block size.

SUMMARY OF THE INVENTION

[0011] When the method of decoding the LDPC code with the sum-product algorism is used for data reproduction of a magnetic recording/reproducing apparatus for performing record/reproduction on multichannel with respect to a tape-like magnetic recording medium, an LDPC decoder for decoding the LDPC code is provided to each channel and the LDPC decoding on respective channels is performed in parallel, or the LDPC code is decoded on a channel one by one, that is, one LDPC decoder is used in a time-shared manner to perform a time-shared iterative decoding on each channel.

[0012] In consideration of a cost in preference to other issues, a structure in which the time-shared LDPC decoding is performed on the plurality of channels using one LDPC decoder in a time-shared manner is adopted. In this case, however, the following problem arises.

[0013] In the case where the time-shared LDPC decoding is performed on the plurality of (in this case, two) channels using one LDPC decoder in the time-shared manner, a large number of iterative processings is required to obtain a bit string that meets a parity search condition in the LDPC decoding on a former channel. Therefore, when the iterative processing is repeated the maximum number of times determined in a system or repeated the number of times close thereto, there is a fear that the LDPC decoding cannot be performed on the next channel or, even if possible, it cannot be performed sufficiently, with the result that the LDPC decoding may be forcibly terminated, which may lead to occurrence of an error in the error correction.

[0014] In view of the above, there is considered a method in which the number of times obtained by evenly dividing, by the number of channels, a maximum iteration count determined in the system is distributed and assigned to the LDPC decoding on each channel. In this method, however, the maximum iteration count assigned to the iterative processing for the LDPC decoding on each channel is limited to 1/(the number of channels), with the result that use efficiency of the maximum iteration count determined in the system is decreased and an error rate is increased.

[0015] In view of the above-mentioned circumstances, the present invention has been made to provide a reproduction apparatus and a reproduction method capable of optimizing assignment of a finite iteration count to each of the plurality of channels when the time-shared iterative decoding of the

LDPC code on the channels is performed using one LDPC decoder, and lowering the error rate.

[0016] To address the above-mentioned problems, in an embodiment of the present invention, it is desirable to provide a reproduction apparatus configured to reproduce signals of a plurality of channels. The reproduction apparatus includes a soft-decision means, a holding means, a decoding means, and a control means. The soft-decision means performs a soft decision on each bit of a block for each of the plurality of channels, the block being encoded with an LDPC (low-density parity-check) code as a bit string corresponding to a length of the LDPC code. The holding means holds a soft-decision result on a block basis for each of the plurality of channels, the soft-decision result being obtained by the soft-decision means. The decoding means inputs the soft-decision result on the block basis and obtains an estimated bit string by an iterative decoding. The control means determines a priority order among channels on each of which a next block is subjected to the iterative decoding, based on an iteration count at an end of the iterative decoding on each of the plurality of channels, and controls the input of the soft-decision result from the holding means to the decoding means on the block basis for each of the plurality of channels so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order.

[0017] In the embodiment of the present invention, the control means determines the priority order among channels on each of which the next block is subjected to the iterative decoding, based on the iteration count at the end of the iterative decoding on each of the plurality of channels, and controls the input of the soft-decision result on the block basis for each of the plurality of channels so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order. As a result, assignment of a finite iteration count to the channels in a case where a time-shared iterative decoding is performed on the LDPC code on the plurality channels using one LDPC decoder can be optimized, and thus an error rate can be reduced.

[0018] In the reproduction apparatus in the embodiment of the present invention, the soft-decision means may obtain a log-likelihood ratio of a posterior probability on a bit basis as the soft-decision result.

[0019] In the reproduction apparatus in the embodiment of the present invention, the control means may determine the priority order among the plurality of channels so that a next block on a channel on which the iterative decoding is performed a smaller number of times than any other channels at the end of the iterative decoding is subjected to the iterative decoding in priority to the others. With this structure, a possibility that the iterative decoding on the first channel is ended by a smaller iteration count becomes high, and thus larger iteration count can be assigned to the iterative decoding on a next channel, which can reduce a block error occurrence probability. That is, the iteration count for the iterative decoding of the LDPC code increases as an SN ratio becomes smaller due to a poor-quality reproduction signal. The quality of the reproduction signal heavily depends on, for example, a characteristic of a recording head or a reproducing head, so the iteration count at the time of the iterative decoding on a specific channel is likely to be larger than that on another channel. Therefore, by performing the iterative decoding first on a channel whose preceding iteration count is smaller, a probability by which the larger finite iteration count can be assigned to iterative decoding on the next channel is increased.

[0020] In the reproduction apparatus according to the embodiment of the present invention, the decoding means sets an upper limit of the iteration count when the iterative decoding is performed on the plurality of channels. When real-time data reproduction is required, the upper limit of the iteration count is determined in consideration of a time pressure. In the present invention, by optimizing the assignment of the finite iteration count to the channels in the case where the upper limit of the iteration count is set as described above, the error rate can be reduced.

[0021] In the reproduction apparatus according to the embodiment of the present invention, the decoding means performs a calculation on the posterior probability in a variable node processing and a check node processing, and performs an iterative processing therebetween. This method is referred as a sum-product algorism with which a bit string having high estimation accuracy can be determined by repetitively performing an iterative processing. The posterior probability refers to a conditional probability regarding encoding words based on a premise that a reception signal is known. The sum-product algorism is obtained by approximating a bitwise maximum posterior probability decoding method, which is a method of calculating the posterior probability without omission. The sum-product algorism significantly increases efficiency of an approximate calculation by using the sparse matrix.

[0022] According to another embodiment of the present invention, there is provided a method of reproducing signals of a plurality of channels. The method comprises: performing a soft decision on each bit of a block for each of the plurality of channels, the block being encoded with an LDPC (low-density parity-check) code as a bit string corresponding to a length of the LDPC code; inputting the soft-decision result on the block basis and obtaining an estimated bit string by an iterative decoding; and determining a priority order among channels for each of which a next block is subjected to the iterative decoding, based on an iteration count at an end of the iterative decoding for each of the plurality of channels and performing control so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order.

[0023] According to the embodiment of the present invention, by determining the priority order among channels on each of which the next block is subjected to the iterative decoding based on the iteration count at the end of the iterative decoding on each of the plurality of channels, and performing control so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order, assignment of the finite iteration count to the channels in a case where the time-shared iterative decoding is performed on the LDPC code on the plurality channels using one LDPC decoder can be optimized, and thus an error rate can be reduced.

[0024] Another reproduction apparatus configured to reproduce signals of a plurality of channels includes a soft-decision portion, a holding portion, a decoding portion, and a control portion. The soft-decision portion performs a soft decision on each bit of a block for each of the plurality of channels, the block being encoded with an LDPC (low-density parity-check) code as a bit string corresponding to a length of the LDPC code. The holding portion holds a soft-

decision result on a block basis for each of the plurality of channels, the soft-decision result being obtained by the soft-decision portion. The decoding portion inputs the soft-decision result on the block basis and obtains an estimated bit string by an iterative decoding. A control portion determines a priority order among the plurality of channels on each of which a next block is subjected to the iterative decoding, based on an iteration count at an end of the iterative decoding on each of the plurality of channels, and controls the input of the soft-decision result from the holding portion to the decoding portion on the block basis for each of the plurality of channels so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order.

[0025] According to the embodiments of the present invention, the assignment of the finite iteration count to the channels in the case where the time-shared iterative decoding is performed on the LDPC code on the plurality of channels using one LDPC decoder can be optimized, and thus the error rate can be reduced.

[0026] These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of best mode embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0027] FIG. **1** is a block diagram showing a structure of a recording apparatus in a magnetic recording/reproducing apparatus according to an embodiment of the present invention;

[0028] FIG. **2** is a block diagram showing a structure of a reproducing apparatus in the magnetic recording/reproducing apparatus according to the embodiment of the present invention;

[0029] FIG. **3** is a diagram showing a structure of a recorded bit string of 1 block recorded on a recording medium by the recording apparatus shown in FIG. **1**;

[0030] FIG. **4** is a diagram showing a node representation of a parity check matrix H of an LDPC code;

[0031] FIG. **5** is a flowchart of an iterative decoding of the LDPC code with an LDPC decoder;

[0032] FIG. **6** is a diagram showing a state where log-likelihood ratios (LLR) for each bit of 1 block are set to variable nodes;

[0033] FIG. **7** is a diagram showing a calculation of a message Bmn given from a variable node n to a check node m;

[0034] FIG. **8** is a diagram showing a calculation of a message Amn given from the check node m to the variable node n;

[0035] FIG. **9** is a flowchart regarding control on a buffer/selector controller in a case where a time-shared iterative decoding on two channels is performed using one LDPC decoder in a time-shared manner; and

[0036] FIG. **10** is a timing chart regarding control on an order of the iterative decoding between two channels.

DESCRIPTION OF PREFERRED EMBODIMENT

[0037] Hereinafter, an embodiment of the present invention will be described with reference to the drawings.

[0038] FIGS. **1** and **2** each show a structure of an embodiment in a case where a reproduction apparatus according to the embodiment of the present invention is applied to a magnetic recording/reproducing apparatus for performing record/reproduction with respect to a tape-like magnetic recording medium. FIG. **1** is a diagram showing a structure of a recording apparatus in the magnetic recording/reproducing apparatus. FIG. **2** is a diagram showing a structure of a reproducing apparatus in the magnetic recording/reproducing apparatus.

[0039] The magnetic recording/reproducing apparatus of this embodiment records signals of a plurality of channels on the tape-like magnetic recording medium with a plurality of recording heads, and reproduces the signals of the plurality of channels from the tape-like magnetic recording medium with a plurality of reproducing heads. In this embodiment, a description will be given on a case where the number of channels is two, but the number only have to be at least two in the present invention.

[0040] First, the structure of the recording apparatus will be described with reference to FIG. **1**. As shown in FIG. **1**, the recording apparatus includes a data distribution portion **10**, header addition portions **11**A and **11**B, LDPC encoding portions **12**A and **12**B, SYNC pattern addition portions **13**A and **13**B, recording amplifiers **14**A and **14**B, and recording heads **15**A and **15**B. Herein, the header addition portions **11**A and **11**B, the LDPC encoding portions **12**A and **12**B, the SYNC pattern addition portions **13**A and **13**B, the recording amplifiers **14**A and **14**B, and the recording heads **15**A and **15**B are respectively provided to each channel.

[0041] The data distribution portion **10** divides user data into the number of channels and distributes the divided data to the header addition portions **11**A and **11***b* on each channel.

[0042] The header addition portions **11**A and **11**B each add various additional information items as a header requisite for reproduction control to the user data divided for each channel.

[0043] The LDPC encoding portions **12**A and **12**B each perform LDPC encoding on the data to which the header is added and generate an LDPC encoding word.

[0044] The SYNC pattern addition portions **13**A and **13**B each add a SYNC pattern for detecting a block to a head of the encoding word generated by each of the LDPC encoding portions **12**A and **12**B.

[0045] The recording amplifiers **14**A and **14**B drive the recording heads **15**A and **15**B, respectively, based on a recording code string output from each of the SYNC pattern addition portions **13**A and **13**B. The recording heads **15**A and **15**B each record a signal on a tape-like magnetic recording medium **16**.

[0046] Next, an operation of the recording apparatus of the magnetic recording/reproducing apparatus in this embodiment will be explained. First, user data is input in the data distribution portion **10**, and divided into the number of channels to be distributed to the header addition portions **11**A and **11**B. A continuing operation for each channel is conducted as follows.

[0047] The header addition portions **11**A and **11**B each add, to the user data supplied from the data distribution portion **10**, various additional information items as a header requisite for reproduction control of the user data. Subsequently, the LDPC encoding portions **12**A and **12**B each encode the data to which the header has been added so that the data is represented by a bit count corresponding to an LDPC code length N. The LDPC encoding is performed by calculating a generator matrix G that establishes $GH^T=0$ from a check matrix H that defines a parity code, and multiplying the data to which the header has been added by the generator matrix G, for example. Herein, the check matrix H that defines the parity code is characterized by being constituted of elements of "0"

and "1" in M rows and N columns and being a sparse matrix. The sparse matrix refers to a matrix having a significantly small number of elements of "1". The bit count obtained by encoding is the LDPC code length N. The bit string corresponding to the LDPC code length N is regarded as 1 block.

[0048] Next, the SYNC pattern is added to the head of the block by each of the SYNC pattern addition portions **13**A and **13**B, to thereby obtain a recording bit string of 1 block.

[0049] FIG. **3** shows a structure of the recording bit string of 1 block. As shown in FIG. **3**, the SYNC pattern for block detection is added to the head of the recording bit string of 1 block. The SYNC pattern is followed by the encoding word as the bit string of 1 block obtained by encoding the user data to which the header has been added.

[0050] The encoding word is constituted of a message bit string of the user data to which the header has been added and the check bit string.

[0051] After that, the recording amplifiers **14**A and **14**B drive the recording heads **15**A and **15**B, respectively, based on the recording bit string, to thereby record signals on the tape-like magnetic recording medium **16**.

[0052] Next, with reference to FIG. **2**, the structure of the reproducing apparatus will be described. As shown in FIG. **2**, the reproducing apparatus includes reproducing heads **21**A and **21**B, reproducing amplifiers **22**A and **22**B, AD converters **23**A and **23**B, HPFs (high pass filters) **24**A and **24**B, pre-filters **25**A and **25**B, digital phase synchronization circuits **26**A and **26**B, adaptive equalization filters **27**A and **27**B, soft-decision detectors **28**A and **28**B, SYNC detectors **29**A and **29**B, buffers **30**A and **30**B, a selector **31**, an LDPC decoder **32**, a data processor **33**, and a buffer/selector controller **34**. The reproducing heads **21**A and **21**B, the reproducing amplifiers **22**A and **22**B, the AD converters **23**A and **23**B, the HPFs (high pass filters) **24**A and **24**B, the pre-filters **25**A and **25**B, the digital phase synchronization circuits **26**A and **26**B, the adaptive equalization filters **27**A and **27**B, the soft-decision detectors **28**A and **28**B, the SYNC detectors **29**A and **29**B, and the buffers **30**A and **30**B are respectively provided to each channel. The selector **31**, the LDPC decoder **32**, the data processor **33**, and the buffer/selector controller **34** are provided singly.

[0053] The reproducing heads **21**A and **21**B each read a signal recorded on the magnetic recording medium **16**. The reproducing amplifiers **22**A and **22**B each amplify the output from each of the reproducing heads **21**A and **21**B to a level processable in subsequent circuits. The AD converters **23**A and **23**B each convert an analog reproduction signal output from each of the reproducing amplifiers **22**A and **22**B to a digital value. The HPFs **24**A and **24**B each remove low frequency components unnecessary in the subsequent processing from the output from the AD converters **23**A and **23**B. The pre-filters **25**A and **25**B each perform equalization processing on reproduction signals that have passed through the HPFs **24**A and **24**B for phase synchronization. The digital phase synchronization circuits **26**A and **26**B each generate phase-synchronized data series from the reproduction signals that have been asynchronously sampled by the AD converters **23**A and **23**B. The adaptive equalization filters **27**A and **27**B each update a tap coefficient thereof to an optimal value based on an error signal output from each of the soft-decision detectors **28**A and **28**B in the subsequent stage, and equalize the input signals to a predetermined target equalization characteristic.

[0054] As the soft-decision detectors **28**A and **28**B, a posterior probability detector is used, for example. The posterior probability detector calculates a posterior probability P**0**=P (x=0|Y=y), P**1**=P (x=1|Y=y) for each bit based on an input value y, and outputs a log-likelihood ratio (LLR) $\lambda=\log(P1/P0)$. Herein, x represents a recording bit, and takes either "0" or "1", for example.

[0055] It is to be noted that the posterior probability detector may obtain the LLR from a plurality of input values including previous and next ones using a trellis diagram. The trellis diagram represents a code string generated in the course of change in state of the encoder according to an input bit string.

[0056] The SYNC detectors **29**A and **29**B each detect the SYNC pattern at the head of the block from the LLR determined by the soft-decision detectors **28**A and **28**B, and performs control so that the latest LLR of 1 block is held in the buffers **30**A and **30**B.

[0057] The buffers **30**A and **30**B each hold the LLR of 1 block for each channel. Write of the LLR on a block basis to the buffers **30**A and **30**B is controlled by the SYNC detectors **29**A and **29**B, and read thereof is controlled by the buffer/selector controller **34**.

[0058] The selector **31** selects one of the buffers **30**A and **30**B for supplying the LLR on the block basis to the LDPC decoder **32** under the control of the buffer/selector controller **34**.

[0059] The LDPC decoder **32** is a circuit for performing iterative decoding of the LDPC code with the LLR on the block basis input through the selector **31** as an input. The LDPC decoder **32** outputs, to the buffer/selector controller **34**, the iteration count at the end of the iterative decoding for each channel.

[0060] The buffer/selector controller **34** includes a register for storing the iteration count at the end of the iterative decoding for each channel, which has been input by the LDPC decoder **32**. Based on the iteration counts at the end of the iterative decoding for the channels, which are stored in the register, the buffer/selector controller **34** determines a priority order of the channels for which the iterative decodings are performed in the subsequent block. Then, the buffer/selector controller **34** reads data from the buffers **30**A and **30**B and controls the selector **31** so that the iterative decodings for the channels are successively performed in the order of priority.

[0061] The data processor **33** is a circuit for restoring data items for each channel based on an estimation encoding word obtained by the LDPC decoder **32** and connecting the data items to thereby restore the recording data.

[0062] Next, a detailed description will be given on iterative decoding of the LDPC code by the LDPC decoder **32**. In this embodiment, the iterative decoding of the LDPC code is performed using a sum-product algorism. In the sum-product algorism, the calculation on the posterior probability is performed in two processings of a "variable node processing" and a "check node processing". The processings are iteratively performed, to thereby determine a bit string having high estimation accuracy.

[0063] FIG. **4** is a diagram showing a node representation of the parity check matrix H of the LDPC code. The parity check matrix H (N rows and M columns) of the LDPC code is represented by N variable nodes, M check nodes, and edges. The edges connect a variable node n and a check node m when an element hmn in m-th row and n-th column of the parity check matrix H is "1".

[0064] FIG. **5** is a flowchart of the iterative decoding of the LDPC code by the LDPC decoder **32**. The LDPC decoder **32**

detects the head of the block based on a SYNC detection signal from the SYNC detectors **29**A and **29**B, and log-likelihood ratios (LLRs) L**1**, L**2**, . . . , Ln for each bit of 1 block are sequentially set to the N variable nodes (Step S**101**) as shown in FIG. **6**.

[0065] Next, the LDPC decoder **32** initializes a message Amn from a check node to a variable node and an iteration count R (Step S**102**), and sets the finite iteration count u of the iterative decoding (Step S**103**).

[0066] After that, Steps S**104**, S**105**, S**106**, and S**107** are skipped and then the iteration count R is incremented (Step S**108**). Thereafter, the first iterative processing is performed as follows.

[0067] As the variable node processing, the LDPC decoder **32** calculates, from the following expression, a message Bmn given from the variable node n to the check node m (Step S**109**). FIG. **7** is a diagram showing a method of calculating the message Bmn.

[0068] [Expression 1]

$$B_{mn} = \sum_{n' \in B(n) \cdot m} A_{mn} + L_n \tag{1}$$

[0069] Herein, B(n)−m ("−" means "excluding") is obtained by excluding a check node m from a check node set B(n) linking to a variable node n, which is represented as m' in FIG. **7**. Am'n shown in FIG. **7** is a message to the variable node n calculated with a check node m'. Because an initial value of the message Am'n is 0, the first message Bmn from the variable node n to the check node m is Ln.

[0070] Next, the LDPC decoder **32** calculates a message Amn from the check node m to the variable node n using the following expression (Step S**110**). FIG. **8** is a diagram showing a calculation method of the message Amn.

[0071] [Expression 2]

$$A_{mn} = \prod_{n' \in A(m) \cdot n} \operatorname{sign}(B_{mn}) f\left(\sum_{n' \in A(m) \cdot n} f(|B_{mn}|) \right) \tag{2}$$

[0072] Herein, a function f(x) is a Gallager function, and is determined from f(x)=ln((exp(x)+1)/(exp(x)−1)). A(m)−n ("−" means "excluding") is obtained by excluding the variable node n from a variable node set A(m) linking to the check node m, which is represented as n'. Bmn' shown in FIG. **8** is a message to the check node m calculated with the variable node n'.

[0073] Next, returning to Step S**103**, the LDPC decoder **32** calculates an approximate value Kn of a log posterior probability ratio using the following expression.

[0074] [Expression 3]

$$K_n = \sum_{m' \in B(n)} A_{mn} + L_n \tag{3}$$

[0075] It is to be noted that for implementation on an LSI, an approximate expression is used for calculating the message Amn, the message Bmn, and the function f(x).

[0076] When calculations of the above-mentioned message Amn, message Bmn, approximate value Kn of the log posterior probability ratio are ended, the LDPC decoder **32** determines an estimation decoding word C'n based on the approximate value Kn of the log posterior probability ratio (Step S**105**). Herein, C' is a substitute representation of C with circumflex. The determination of the estimation decoding word C'n is performed as follows. When the approximate value Kn of the log posterior probability ratio is equal to or more than 0, the LDPC decoder **32** determines the estimation decoding word C'n to be "0". When the approximate value Kn of the log posterior probability ratio is less than 0, the LDPC decoder **32** determines the estimation decoding word C'n to be "1".

[0077] Next, the LDPC decoder **32** judges whether the estimation decoding word C'n currently obtained meets a parity check condition of $C'nH^T=0$ (Step S**106**). Herein, H^T is a transposed matrix of the LDPC parity check matrix H. When the estimation decoding word C'n meets the parity check condition, the LDPC decoder **32** outputs the estimation decoding word C'n currently obtained to the data processor **33**, outputs the iteration count R at the end of the iterative decoding to the buffer/selector controller **34**, and ends the decoding (Step S**111**).

[0078] Herein, a processing starting from the calculations of the message Bmn, the message Amn, the approximate value Kn of the log posterior probability ratio, and the estimation decoding word C'n, to the judgment of whether the estimation decoding word C'n meets the parity check condition is referred to as "one iterative processing". The number of times the iterative processing is performed is referred to as the iteration count R.

[0079] When the result of the judgment in Step S**106** shows that the estimation decoding word C'n meets the parity check condition, the LDPC decoder **32** outputs the estimation decoding word C'n currently obtained to the data processor **33** as a decoding result, and ends the iterative decoding. When the estimation decoding word C'n does not meet the parity check condition, a judgment on whether a current iteration count R has reached the finite iteration count u is made (Step S**107**). When the current iteration count R has not reached the finite iteration count u, the LDPC decoder **32** increments the iteration count R (Step S**108**), and then carries out the subsequent iterative processing.

[0080] In the subsequent processings, the LDPC decoder **32** repeats the iterative processings until it is judged that the estimation decoding word C'n generated meets the parity check condition, or until just before the current iteration count R reaches the finite iteration count u. When it is judged that the current iteration count R has reached the finite iteration count u in Step S**107**, that is, when the estimation decoding word C'n does not meet the parity check condition even when iterative processings are repeated u times, the LDPC decoder **32** forcibly terminates the decoding processing with a block in processing as an error block (Step S**112**).

[0081] In the magnetic recording/reproducing apparatus according to this embodiment, one LDPC decoder **32** is used in a time-shared manner to perform a time-shared iterative decoding on a plurality of channels.

[0082] Next, a description will be given on control to perform the time-shared iterative decoding on the plurality of channels using one LDPC decoder **32** in the time-shared manner. Herein, the number of channels is assumed to be two.

In this case, the LDPC decoder **32** is required to be a circuit capable of performing decoding at a rate that is twice or more the channel frequency.

[0083] FIG. **9** is a flowchart of control by the buffer/selector controller **34** in the case where the time-shared iterative decoding is performed on two channels using one LDPC decoder **32** in the time-shared manner.

[0084] Herein, out of the two channels, one channel is referred to as a "first channel", while the other channel is referred to as a "second channel". The buffer/selector controller **34** includes a first priority order register, a second priority register, a first iteration count register, and a second iteration count register. The first priority order register stores a priority order of the iterative decoding on the first channel. The second priority order register stores a priority order of the iterative decoding on the second channel. The first iteration count register stores an iteration count at the end of the latest iterative decoding on the first channel. The second iteration count register stores an iteration count at the end of the latest iterative decoding on the second channel.

[0085] First, the buffer/selector controller **34** sets initial values to the priority order registers on the respective channels. For example, a numerical value 1 representing a first-order priority (hereinafter, referred to as "priority order 1") is set to the first priority order register as the initial value, while a numerical value 2 representing a second-order priority (hereinafter, referred to as "priority order 2") is set to the second priority order register as the initial value. As a result, at the start of the decoding, the iterative decoding on the first channel is started first, and then the iterative decoding on the second channel is started immediately after the iterative decoding on the first channel is ended.

[0086] After that, when detecting that the buffers **30**A and **30**B on the respective channels are each storing data (LLR) of 1 block or more (Yes in Step S**201**), the buffer/selector controller **34** outputs a selection signal to the selector **31** so that the data (LLR) in the buffer **30**A on the channel set as the priority order 1, that is, the first channel in this case is selected (Step S**202**). Based on the selection signal from the buffer/selector controller **34**, the selector **31** selects the data (LLR) in the buffer **30**A on the first channel to supply the data to the LDPC decoder **32**. Thus, at the LDPC decoder **32**, the iterative decoding with respect to the data (LLR) of 1 block read out from the buffer **30**A is carried out by the procedure described above.

[0087] For the iterative decoding on the channel selected first out of the plurality of channels, a count U is set to the LDPC decoder **32** as the finite iteration count u. The count U is obtained by dividing, by the total number of channels, the maximum count of iterations that can be performed within a time period required for entirely outputting the data (LLR) of 1 block to each of the buffers **30**A and **30**B. It is to be noted that the count U is stored in the system in advance. The finite iteration count u may be set upon receiving a notification of the finite iteration count u from the buffer/selector controller **34** by the LDPC decoder **32**. Alternatively, when the LDPC decoder **32** receives, from the buffer/selector controller **34**, a notification indicating that the decoding is performed on the firstly-selected channel out of the plurality of channels, the count U may be set as the finite iteration count u.

[0088] When the LDPC decoder **32** ends the iterative decoding of 1 block (Yes in Step S**203**), the buffer/selector controller **34** is notified of the iteration count R at the end of the iterative decoding of the block. The buffer/selector controller **34** stores the iteration count R notified from the LDPC decoder **32** in the iteration count register corresponding to the channel to which the priority order 1 has been given, that is, the first iteration count register corresponding to the first channel in this case (Step S**204**). Herein, the iteration count R stored in the first iteration count register is represented as an "iteration count R1".

[0089] Subsequently, the buffer/selector controller **34** outputs a selection signal to the selector **31** so that the data (LLR) of the buffer **30**B on the channel to which the priority order 2 has been given, that is, the second channel in this case is selected (Step S**205**). Based on the selection signal from the buffer/selector controller **34**, the selector **31** selects the data (LLR) of the buffer **30**B and supplies the data to the LDPC decoder **32**. Thus, at the LDPC decoder **32**, the iterative decoding with respect to the data (LLR) of 1 block read out from the buffer **30**B is carried out by the procedure described above.

[0090] For the iterative decoding on the secondly-selected channel out of the plurality of channels, a count (2U−R) is set to the LDPC decoder **32** as the finite iteration count u. The count (2U−R) is obtained by subtracting the iteration count R at the end of the iterative decoding on the firstly-selected channel from the maximum count (2U in the case where the number of channels is two) of iterations that can be performed within a time period required for entirely outputting the data (LLR) of 1 block to each of the buffers **30**A and **30**B. The finite iteration count u may be set upon receiving a notification of the finite iteration count u from the buffer/selector controller **34** by the LDPC decoder **32**. Alternatively, when the LDPC decoder **32** receives, from the buffer/selector controller **34**, a notification indicating that the decoding is performed on the secondly-selected channel, the count 2U−R may be set as the finite iteration count u.

[0091] When the LDPC decoder **32** ends the iterative decoding of 1 block (Yes in Step S**206**), the buffer/selector controller **34** is notified of the iteration count R at the end of the iterative decoding of the block. The buffer/selector controller **34** stores the iteration count R notified from the LDPC decoder **32** in the iteration count register corresponding to the channel to which the priority order 2 has been given, that is, the second iteration count register corresponding to the second channel in this case (Step S**207**). Herein, the iteration count R stored in the second iteration count register is represented as an "iteration count R2".

[0092] Next, the buffer/selector controller **34** compares the iteration count R**1** stored in the first iteration count register with the iteration count R**2** stored in the second iteration count register, and judges whether R**1**<R**2** is satisfied (Step S**208**). In a case where R**1**<R**2** is satisfied, a numerical value 1 is set to the first priority order register as a priority order B**1** for the iterative decoding on the first channel, and a numerical value 2 is set to the second priority order register as a priority order B**2** for the iterative decoding on the second channel (Step S**209**). In other words, the priority order registers on the channels still store the initial values. In a case where R**1**<R**2** is not satisfied, conversely, a numerical value 2 is set to the first priority order register as the priority order B**1** for the iterative decoding on the first channel, and a numerical value 1 is set to the second priority order register as the priority order B**2** for the iterative decoding on the second channel (Step S**210**).

[0093] The control by the buffer/selector controller **34** for an iterative decoding with respect to blocks on two channels

at the next time is performed according to the priority orders B1 and B2 set anew to the priority order registers on the channels, respectively. In other words, the next time-shared iterative decoding with respect to the blocks on the plurality of channels is carried out from a channel whose iteration count is smaller at the end of the preceding iterative decoding.

[0094] FIG. **10** is a diagram showing an example of a timing chart regarding control on an order of the iterative decoding between the two channels. In this example, the iterative decoding of a block (block **1**) stored in the buffer **30**A on the first channel (ch **1**) is started first. Immediately after the end of the iterative decoding of the block **1**, the iterative decoding of a block (block **2**) stored in the buffer **30**B on the second channel (ch **2**) is started. In this case, the iterative processings are performed ten times on the block (block **1**) on the first channel (ch **1**) and three times on the block (block **2**) on the second channel (ch **2**), that is, R**1**=10 and R**2**=3, which does not satisfy R**1**<R**2**. Therefore, the next iterative decoding is started from a block (block **4**) stored in the buffer **30**B on the second channel (ch **2**). Immediately after the end of the iterative decoding of the block (block **4**), the iterative decoding of a block (block **3**) stored in the buffer **30**A on the first channel (ch **1**) is performed.

[0095] As a result, for the iterative decoding on the two channels in this case, the iterative processing is performed on the block (block **4**) three times and on the block (block **3**) 2U−3 times. In this way, when a smaller iteration count is required by the end of the iterative decoding on the first channel, a larger iteration count can be assigned to the iterative decoding on the next channel, with the result that a block error occurrence probability can be reduced.

[0096] In general, the iteration count at the time of iterative decoding of the LDPC code increases as an SN ratio becomes smaller due to a poor-quality reproduction signal. The quality of the reproduction signal heavily depends on, for example, a characteristic of a recording head or a reproducing head, so the iteration count at the time of the iterative decoding on a specific channel is likely to be larger than that on another channel. Therefore, by performing the iterative decoding first on a channel whose preceding iteration count is smaller, a probability by which a larger finite iteration count u can be assigned to iterative decoding on the next channel is increased.

[0097] Heretofore, the case where the number of channels is two is described. Also in a case where the number of channels is three, the iterative decoding is only required to be performed from a channel whose preceding iteration count is smaller among the channels, and thus the present invention can be applied to this case. Of course, in this case, the LDPC decoder **32** must be a circuit capable of performing decoding at a rate of threefold or more the channel frequency.

[0098] As described above, according to this embodiment, in the case where the iterative decoding on the plurality of channels is performed using one LDPC decoder **32** in the time-shared manner, by performing such control that the iterative decoding is performed from a channel whose preceding iteration count R is smaller, the larger finite iteration count u can be assigned to the iterative decoding on a channel which tends to require a larger iteration count, with the result that the block error occurrence probability can be reduced.

[0099] The present invention is not limited to the above embodiment, and can of course be variously changed without departing from the gist of the present invention.

What is claimed is:

1. A reproduction apparatus configured to reproduce signals of a plurality of channels, comprising:
- a soft-decision means for performing a soft decision on each bit of a block for each of the plurality of channels, the block being encoded with an LDPC (low-density parity-check) code as a bit string corresponding to a length of the LDPC code;
- a holding means for holding a soft-decision result on a block basis for each of the plurality of channels, the soft-decision result being obtained by the soft-decision means;
- a decoding means for inputting the soft-decision result on the block basis and obtaining an estimated bit string by an iterative decoding; and
- a control means for determining a priority order among the plurality of channels on each of which a next block is subjected to the iterative decoding, based on an iteration count at an end of the iterative decoding on each of the plurality of channels, and controlling the input of the soft-decision result from the holding means to the decoding means on the block basis for each of the plurality of channels so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order.

2. The reproduction apparatus according to claim **1**,
wherein the soft-decision means obtains a log-likelihood ratio of a posterior probability on a bit basis as the soft-decision result.

3. The reproduction apparatus according to claim **1**,
wherein the control means determines the priority order among the plurality of channels so that a next block on a channel on which the iterative decoding is performed a smaller number of times than any other channels at the end of the iterative decoding is subjected to the iterative decoding in priority to the others.

4. The reproduction apparatus according to claim **1**,
wherein the decoding means sets an upper limit of the iteration count when the iterative decoding is performed on the plurality of channels.

5. The reproduction apparatus according to claim **1**,
wherein the decoding means performs a calculation on a posterior probability in a variable node processing and a check node processing, and performs an iterative processing therebetween.

6. A method of reproducing signals of a plurality of channels, comprising:
- performing a soft decision on each bit of a block for each of the plurality of channels, the block being encoded with an LDPC (low-density parity-check) code as a bit string corresponding to a length of the LDPC code;
- inputting the soft-decision result on the block basis and obtaining an estimated bit string by an iterative decoding; and
- determining a priority order among channels for each of which a next block is subjected to the iterative decoding, based on an iteration count at an end of the iterative decoding for each of the plurality of channels, and performing control so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order.

7. A reproduction apparatus configured to reproduce signals of a plurality of channels, comprising:
- a soft-decision portion for performing a soft decision on each bit of a block for each of the plurality of channels, the block being encoded with an LDPC (low-density parity-check) code as a bit string corresponding to a length of the LDPC code;

a holding portion for holding a soft-decision result on a block basis for each of the plurality of channels, the soft-decision result being obtained by the soft-decision portion;

a decoding portion for inputting the soft-decision result on the block basis and obtaining an estimated bit string by an iterative decoding; and

a control portion for determining a priority order among the plurality of channels on each of which a next block is subjected to the iterative decoding, based on an iteration count at an end of the iterative decoding on each of the plurality of channels, and controlling the input of the soft-decision result from the holding portion to the decoding portion on the block basis for each of the plurality of channels so that the iterative decoding is performed for each of the plurality of channels in accordance with the priority order.

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