(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 July 2005 (07.07.2005)

PCT

(10) International Publication Number
WO 2005/062563 A1

(51) International Patent Classification[7]: H04L 25/03, 27/12, 27/20, H03C 3/09, H03L 7/197

(21) International Application Number: PCT/US2004/010959

(22) International Filing Date: 22 April 2004 (22.04.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/734,117 15 December 2003 (15.12.2003) US

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Mailstop SC4-202, Santa Clara, CA 95052-8119 (US).

(72) Inventors: **YELLIN, Daniel**; 71 Hertzel Street, 43353 Ra'anana (IL). **PICK, Kobby**; 43/2 Emek Haela Street, 71700 Modiin (IL).

(74) Agent: **COHEN, Mark, S.**; Eitan, Pearl, Latzer & Cohen Zedek, L.L.P., 10 Rockefeller Plaza, Suite 1001, New York, NY 10020 (US).

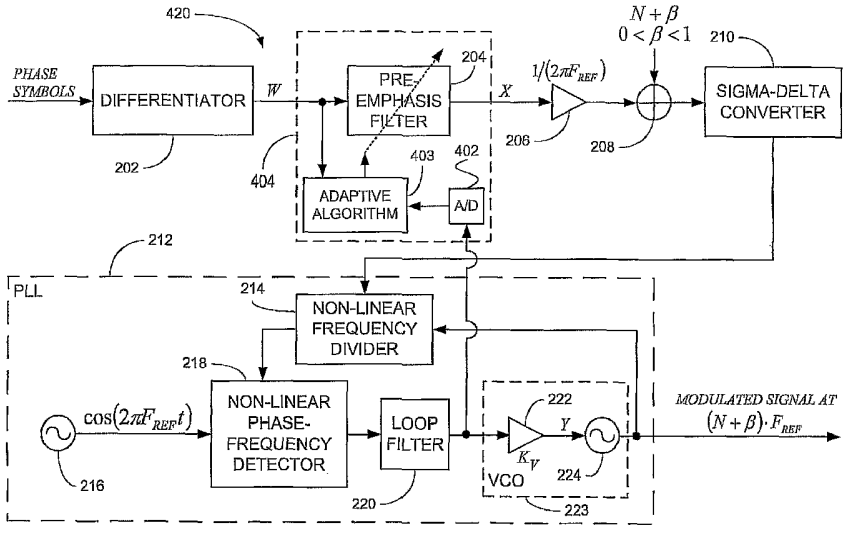
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: FRACTIONAL-N SIGMA-DELTA MODULATOR COMPRISING AN ADAPTIVE COMPENSATION FILTER THAT COMPENSATES FOR THE UNDESIRED EFFECTS OF THE PHASE LOCKED LOOP AND METHODS THEREOF



(57) Abstract: In some exemplary embodiments of the invention, a transfer function of a filter for a fractional-N sigma-delta modulator may be calculated to be optimized according to predefined optimization criteria. For example, the optimization criteria may include spectral cleanliness at the output of the modulator, or the mean squared error of the input to the filter and the input to a voltage controlled oscillator of the fractional-N phase locked loop (PLL). In some exemplary embodiments, the filter may be adjusted to compensate for variations and/or impairments in the analog fractional-N PLL. A non-exhaustive list of examples for the transfer function includes a finite impulse response and an infinite impulse response.

WO 2005/062563 A1

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

FRACTIONAL-N SIGMA-DELTA MODULATOR COMPRISING AN ADAPTIVE COMPENSATION FILTER THAT COMPENSATES FOR THE UNDESIRED EFFECTS OF THE PHASE LOCKED LOOP AND METHOD THEREOF

BACKGROUND OF THE INVENTION

[001] In polar modulation, a signal is separated into its instantaneous amplitude and phase/frequency components (rather than into the classical in-phase (I) and quadrature (Q) components), and the amplitude component and phase/frequency component are modulated independently. The amplitude component may be modulated with any suitable amplitude modulation (AM) technique, while the phase/frequency component may be modulated using an analog phase locked loop (PLL).

[002] To allow reasonable operation, the bandwidth of the PLL may be quite small, much smaller than the actual bandwidth of the transmission signal's instantaneous phase/frequency. For example, in the case where the PLL is fed by a sigma-delta converter that has a high pass noise nature, the loop filter may be narrow enough to attenuate the sigma-delta quantization noise and the phase noise of the PLL. A pre-emphasis filter may emphasize, prior to modulation, those frequency components that would be attenuated by the PLL. The pre-emphasis filter may employ inverse filtering to the linearized response of the PLL. This inverse filtering may yield a high-order infinite impulse response (IIR), which may suffer from stability problems.

[003] Conventional practice involves calibration mechanisms in order to accurately calibrate the PLL to the predefined pre-emphasis filter. Without calibration, there is a risk that the pre-emphasis filter will not match the inverse to the PLL closed loop transfer function, which may result in enhancement of the phase noise.

BRIEF DESCRIPTION OF THE DRAWINGS

[004] Embodiments of the invention are illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like reference numerals indicate corresponding, analogous or similar elements, and in which:

[005] FIG. 1 is a block-diagram illustration of an exemplary communication system including a transmitter according to some embodiments of the invention;

[006] FIG. 2 is a block-diagram illustration of an exemplary fractional-N sigma-delta modulator according to some embodiments of the invention;

[007] FIG. 3 is a flowchart illustration of an exemplary method to determine a transfer function of a filter, according to some embodiments of the invention;

[008] FIG. 4 is a block-diagram illustration of an exemplary fractional-N sigma-delta modulator including an adaptive filter, according to some embodiments of the invention;

[009] FIG. 5 is a block-diagram illustration of an exemplary linearized approximation to the exemplary fractional-N sigma-delta modulator of FIG. 2, according to some embodiments of the invention;

[0010] FIG. 6 is a block diagram of an exemplary system including an equalizer.

[0011] It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity.

DETAILED DESCRIPTION OF THE INVENTION

[0012] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of embodiments of the invention. However it will be understood by those of ordinary skill in the art that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the description of embodiments of the invention.

[0013] FIG. 1 is a block-diagram illustration of an exemplary communication system including a transmitter according to an embodiment of the invention. A communication device 100 is able to communicate with a communication device 102 over a communication channel 104. Although the scope of the invention is not limited in this respect, the communication system shown in FIG. 1 may be part of a cellular communication system (with one of communication devices 100, 102 being a base station and the other a mobile station, or with both communication devices 100, 102 being mobile stations), a pager communication system, a personal digital assistant and a server, etc. A non-exhaustive list of examples for the communication system shown in FIG. 1 includes a Global System for Mobile Communications (GSM) system, a General Packet Radio Service (GPRS) system, an Enhanced Data for GSM Evolution (EDGE) system, code division multiple access (CDMA), CDMA2000, Wideband-CDMA (WCDMA), AMPS and any other wireless standard.

[0014] Communication device 100 may include at least a transmitter 106 and an antenna 108. Communication device 102 may include at least a receiver 110 and an antenna 112. Antennas 108 and 112 may be of any desired kind such as, but not limited to, dipole, Yagi and multi-pole and the like. Moreover, communication device 100 may include a receiver (not shown). Similarly, communication device 102 may include a transmitter (not shown).

[0015] Transmitter 106 may include at least a baseband symbol generator 114 to generate a signal of baseband symbols, a splitter 116 to split the signal into its instantaneous amplitude and phase/frequency components, an amplitude path 118 to modulate and amplify the amplitude components, a fractional-N sigma-delta modulator 120 to modulate and up-convert the phase/frequency components, and a power amplifier 122 to amplify the output of fractional-N sigma-delta modulator 120

with a gain controlled by the output of amplitude path 1 18. Antenna 108 is coupled to power amplifier 122 to transmit the output of power amplifier 122.

[0016] Baseband symbol generator 114 may be implemented in accordance with a wireless standard. Splitter 116 may be implemented in hardware, software or firmware or any combination thereof.

[0017]FIG. 2 is a block-diagram illustration of an exemplary fractional-N sigma-delta modulator according to an embodiment of the invention, such as, for example, fractional-N sigma-delta modulator 120 of FIG. 1. Fractional-N sigma-delta modulator 120 has a digital portion and an analog portion. The digital portion may include at least a differentiator 202, a filter 204 (such as, for example, a pre-emphasis filter), an amplifier 206, a summer 208, and a sigma-delta converter 210. The analog portion, which implements an analog phase locked loop (PLL) 212, may include at least a non-linear frequency divider 214, a reference oscillator 216 to produce a signal having a frequency F_{REF}, a non-linear phase-frequency detector 218, a loop filter 220, an amplifier 222 having a gain K_V, and a voltage-controlled oscillator (VCO) 224. The input of VCO 224 is denoted Y. PLL 212 is also known as a "fractional-N phase locked loop" unit. Amplifier 222 and VCO 224 may be implemented as a single unit (VCO 223); the separation into two elements is for the sake of analysis.

[0018]Reference oscillator 216 may produce a signal having a reference frequency F_{REF}. An example of reference frequency F_{REF} is approximately 26 MHz, although other reference frequencies may be used instead.

[0019]Differentiator 202 may differentiate the phase symbols received from splitter 116 of FIG. 1 to obtain the instantaneous frequency W of the baseband signal. Differentiator 202 may be implemented in hardware, software or firmware or any combination thereof.

[0020]Filter 204 may be determined so that the instantaneous frequency W is transferred to the input Y of VCO 224 with little or no distortion, as will be described in more detail hereinbelow. Any implementation of a digital filter is suitable for filter 204.

[0021]Amplifier 206 may normalize the output of filter 204, denoted X, to PLL reference frequency units.

[0022] Summer 208 may add the output of amplifier 206 with a number $N+\beta$. Both the integer number N and the non-integer number β having a value between 0 and 1 may be set according to an instruction from a base station regarding the average output frequency of a transmitter of a mobile station. For example, if reference frequency F_{REF} is approximately 26 MHz, then N may have a value in the range of 29 – 32 so that $N \cdot F_{REF}$ has a value of approximately 800 MHz.

[0023] Sigma-delta converter 210 may convert the output of summer 208 into an integer number that represents the instantaneous frequency division ratio of the PLL.

[0024] Non-linear frequency divider 214 may divide the output of VCO 224 by the integer number provided by sigma-delta converter 210 to produce a divided-frequency signal.

[0025] Non-linear phase-frequency detector 218 may compare the divided-frequency signal to the reference frequency signal produced by reference oscillator 216. Non-linear phase-frequency detector 218 may produce a control signal that corresponds to the phase difference and/or frequency difference between the two signals. Any implementation of a phase-frequency detector is suitable for phase-frequency detector 218.

[0026] The control signal, after smoothing by loop filter 220 and amplification by amplifier 222, may be applied to VCO 224 so that VCO 224 synthesizes a modulated output carrier signal.

[0027] As mentioned above, filter 204 may be determined so that the instantaneous frequency W is transferred to the input Y of VCO 224 with little or no distortion (e.g. the overall response from W to Y is close to flat in the frequencies of interest).

[0028] FIG. 3 is a flowchart illustration of an exemplary method to determine a transfer function C of filter 204, according to an embodiment of the invention. The method may include the following:

a) building a linear model for PLL 212 and calculating the transfer function $H(w)$ from the output X of filter 204 to the input Y to VCO 224 (block 302);

b) optionally adding various impairments of the different PLL components (e.g. phase noises, variations of the PLL parameters from their nominal values, and the like) to the model (block 304) – the variations of PLL parameters from their nominal values,

such as, for example, capacitors, resistors, open loop gain, etc., may be due to production inaccuracies;

c) deciding on a topology for the transfer function C of filter 204 (block 306), and

d) calculating a transfer function C to minimize a predefined cost function related to the instantaneous frequency W and the input Y to VCO 224 (block 308).

[0029] In some embodiments, the transfer function C is a stable transfer function.

[0030] Mathematically, the transfer function C may be expressed as follows:

$C = ArgMin_C\{Cost(W,Y)\}$.

[0031] In one embodiment, the cost function may be the mean square error (MSE) between the instantaneous frequency W and the input Y to VCO 224, as follows: $Cost(W,Y) = E\{|W(t)-Y(t)|^2\}$, where t is a time variable and E is an expectation operator. In yet another embodiment, the expectation operator is replaced by time averaging and the cost function becomes:

$$Cost(W,Y) = \frac{1}{T}\int_{-T/2}^{T/2}|W(t)-Y(t)|^2 dt$$

where T is a design parameter determining the integration time window.

[0032] In another embodiment, the cost function may be a weighted MSE in the frequency domain, as follows:

$$Cost(W,Y) = E\left\{\int_{-\infty}^{+\infty}P(w)|W(w)-Y(w)|^2 dw\right\},$$

where $P(w)$ is a user-defined, positive, weight function. For example, weight function $P(w)$ may give more weight to those frequencies where spectral cleanliness is more important.

[0033] In other embodiments, other cost functions may be used, such as, for example, a cost function that measures the spectral cleanliness of the overall transmission signal.

[0034] In the event that an MSE or weighted MSE cost function is used, then block 304 of the method may be redundant if all impairments may be represented as additive noise terms, since different choices of transfer function C will not affect that total contribution of these additive impairments to the MSE or weighted MSE cost.

[0035] Certain cost functions may be minimized using equalization theory, as will be described hereinbelow for a particular example.

[0036] Any suitable topology for transfer function C may be used in block 306. For example, transfer function C may be a finite impulse response (FIR) of order p (in which case stability is guaranteed), or an infinite impulse response (IIR) having a rational transfer function of orders (p,q), etc.

[0037] FIG. 4 is a block diagram of an exemplary fractional-N sigma-delta modulator 420 including an adaptive filter, according to some embodiments of the invention. Fractional-N sigma-delta modulator 420 is similar to fractional-N sigma-delta modulator 120 of FIG. 2, and therefore similar components are referenced with the same reference numerals and will not be described in further detail. Fractional-N sigma-delta modulator 420 may include at least an adaptive filter 404 (such as, for example, an adaptive pre-emphasis filter). Adaptive filter 404 may include at least filter 204, an analog-to-digital (A/D) converter 402 and an adaptive algorithm 403.

[0038] Adaptive algorithm 403 compares the input to filter 204 (the instantaneous frequency W) to the input to VCO 223 (after digitization). Adaptive algorithm 403 adapts filter 204 according to the comparison. For example, if the error between instantaneous frequency W and input Y is defined by a particular cost function, then adaptive algorithm 403 may reduce the error iteratively. A non-exhaustive list of examples of adaptive mechanisms include Least Mean Squares (LMS), Recursive Least Squares (RLS), and the like. Thus, any impairments, offsets, drifts, etc. of the analog portion of the PLL may drive the filter values to those values that minimize a pre-specified adaptive mechanism cost function such as, for example, a mean squared error cost function. Variations in the PLL, such as for example, variations in temperature, voltage, aging, etc., may be compensated for by the adaptive algorithm.

[0039] Since adaptive algorithm 403 enables the digital values of filter 204 to be adapted to variations in the analog PLL, it may not be necessary to calibrate PLL 212 to predefined values for filter 204.

[0040] Block 302 of the method of FIG. 3 includes building a linear model of a PLL. FIG. 5 is a block diagram of an exemplary linearized approximation to the exemplary fractional-N sigma-delta modulator of FIG. 2. In this approximation, which is made in the phase domain, PLL 212 has been approximated by a linearized PLL 512, and

sigma-delta converter 210 has been approximated by a linearized sigma-delta converter 510 including an all pass filter and an additive noise $n(\Sigma-\Delta)$.

[0041]Non-linear frequency divider 214 has been approximated by a linearized frequency divider 514 including an amplifier 511 having a gain of $2\pi F_{REF}$, a differentiator block 530 having a transfer function of s, where s is a Laplace domain variable, a subtraction block 532, an amplifier 534 having a gain of $1/(N+\beta)$, and an integrator block 536 having a transfer function of *1/s*.

[0042]VCO 224 has been approximated by a block 524 having a transfer function of *1/s*. Non-linear phase-frequency detector 218 has been approximated by a subtraction block 518, and loop filter 220 has been approximated by a block 520 having a transfer function *T(s)*.

[0043]The transfer function from the output *X* of filter 204 to input *Y* to block 524 is then given by the following expression:

$$\frac{Y(s)}{X(s)}=\frac{(K_V/(N+\beta))\cdot T(s)/s}{1+(K_V/(N+\beta))\cdot T(s)/s} \qquad \text{(Equation 1)}$$

[0044]The design of the transfer function *C* of filter 204 may then be performed as follows. In order that the instantaneous frequency *W* be transferred to the input *Y* of VCO 224 with little or no frequency and phase distortion, the overall transfer function from *W* to *Y* may be of substantially 0 dB gain up to a cut-off frequency f_0 and may have substantially linear phase up to the cut-off frequency f_0.

[0045]The cut-off frequency f_0 may be defined experimentally by observing the spectrum of the instantaneous frequency *W* signal. Alternatively, the cut-off frequency f_0 may be defined as narrow as possible while still meeting the requirements of a communication standard. Other definitions of the cut-off frequency f_0 are also within the scope of the invention.

[0046]One straightforward solution is to define the transfer function *C* from *W* to *X* up to the cut-off frequency f_0 as the inverse IIR to the transfer function *Y(s)/X(s)*, as given by the following expression:

$$\frac{X(s)}{W(s)}=\frac{1+(K_V/(N+\beta))\cdot T(s)/s}{(K_V/(N+\beta))\cdot T(s)/s},\ s=j\cdot 2\pi f, f<f_0 \qquad \text{(Equation 2)}$$

where j is the square root of -1.

[0047]However, if the transfer function C were implemented as the inverse IIR to the transfer function $Y(s)/X(s)$, then the following problems might arise:

a) zeros and poles may need to be added to the inverse IIR to stabilize the filter;

b) additional poles or filters may need to be added to the inverse IIR to attenuate the frequencies above the cut-off frequency f_0 so that the sigma-delta converter will not be forced into saturation and so as not to increase the quantization noise; and

c) the order of the transfer function C would no longer be a design parameter; rather, it would have a one-to-one relation to the order of the closed loop transfer function.

Therefore, according to some embodiments of the present invention, the transfer function C is not the inverse IIR to the transfer function $Y(s)/X(s)$. Rather, the transfer function C of the filter is calculated to optimize predefined optimization criteria, as described hereinabove with respect to FIG. 3.

[0048]Block 302 of the method of FIG. 3 includes calculating the transfer function C to minimize a predefined cost function related to the instantaneous frequency W and the input Y to the VCO of the PLL. The transfer function C may be calculated in a manner similar to the calculation of a minimum mean squared error (MMSE) equalizer, as will be explained in greater detail. FIG. 6 is a block diagram of an exemplary system including an equalizer.

[0049]A known digital input signal $u(i)$ may be subjected to an impulse response h, where the impulse response h is defined as the bi-linear transform of the transfer function $Y(s)/X(s)$.

[0050]An additive white Gaussian noise $n\_AWGN(i)$ may be shaped by a shaping filter g. Noise shaping filter g may be a high pass filter with a cut-off above frequency f_0, so that the equalizer response at high frequencies will be attenuated.

[0051]The combination of shaped noise $n(i)$ and the output of impulse response h is denoted $v(i)$. The digital signal $v(i)$ may be subjected to a FIR filter C to yield a digital signal $\hat{u}(i)$.

[0052]FIR filter C may be calculated analytically to minimize the mean square error that is defined as

$$e \equiv u(i) - \hat{u}(i). \qquad \text{(Equation 3)}$$

[0053] The following expressions may be useful in the calculation of FIR filter C:

$$\hat{u}(i) = \overline{C}^H \cdot \overline{V}, \qquad \text{(Equation 4a)}$$

$$\overline{V} = H \cdot \overline{U} + \overline{N}, \qquad \text{(Equation 4b)}$$

$$H \equiv \begin{bmatrix} h(M+L) & \cdots & h(L) & \cdots & h(-M+L) \\ \vdots & & \vdots & & \vdots \\ h(M) & & h(0) & & h(-M) \\ \vdots & & \vdots & & \vdots \\ h(M-L) & \cdots & h(-L) & \cdots & h(-M-L) \end{bmatrix}_{[(2L+1)\times(2M+1)]}, \qquad \text{(Equation 4c)}$$

$$\overline{U} \equiv \begin{bmatrix} u(i-M) \\ \vdots \\ u(i) \\ \\ u(i+M) \end{bmatrix}_{[(2M+1)\times 1]}, \qquad \text{(Equation 4d)}$$

$$\overline{N} \equiv \begin{bmatrix} n(i+L) \\ \vdots \\ n(i) \\ \\ n(i-L) \end{bmatrix}_{[(2L+1)\times 1]}, \qquad \text{(Equation 4e)}$$

where the bar denotes vector notation, the superscript H denotes the conjugate transpose, 2M+1 is assumed to be the length (i.e. number of coefficients) of impulse response h, and 2L+1 is assumed to be the length (i.e. number of coefficients) of the equalizer.

[0054] The following assumptions may be made:

1. There is no correlation between the error and the observations. Thus, $E\{e(i)\cdot \overline{V}^H\} = \overline{0}^H$, where, again, E is an expectation operator.

2. There is no correlation between the input signal and the shaped noise. Thus $E\{u(i)\cdot n(i+k)^*\} = 0, \forall k$, where the asterisk denotes the complex conjugate.

3. The input signal is independently distributed (ID). Thus $E\{u(i)\cdot u(i+k)^*\} = \begin{cases} \sigma_U^2(i), k=0 \\ 0, k\neq 0 \end{cases}$, where $\sigma_U^2(i) = E\{|u(i)|^2\}$.

4. n_AWGN is additive white Gaussian noise. Thus $E\{n\_AWGN(i)\cdot n\_AWGN(i+k)^*\}=\begin{cases}\sigma^2_{N\_AWGN}, k=0\\ 0, k\neq 0\end{cases}$, where $\sigma^2_{N\_AWGN}=E\{|n\_AWGN(i)|^2\}$ is a fixed value for all i.

[0055] From assumption 1 it follows that

$$E\{u(i)\cdot\overline{V}^H\}=E\{\hat{u}(i)\cdot\overline{V}^H\}. \quad \text{(Equation 5)}$$

[0056] By substituting Equations 4a, 4b, 4d and 4e into Equation 5, it follows that:

$$\begin{aligned}E\{\hat{u}(i)\cdot\overline{V}^H\}&=\overline{C}^H\cdot E\{\overline{V}\cdot\overline{V}^H\}\\&=\overline{C}^H\cdot E\{(H\cdot\overline{U}+\overline{N})\cdot(\overline{U}^H\cdot H^H+\overline{N}^H)\}\\&=\overline{C}^H\cdot[E\{H\cdot\overline{U}\cdot\overline{U}^H\cdot H^H\}+E\{\overline{N}\cdot\overline{N}^H\}],\\&=\overline{C}^H\cdot[H\cdot H^H\cdot\sigma_U^2+G\cdot G^H\cdot\sigma^2_{N\_AWGN}]\end{aligned} \quad \text{(Equation 6)}$$

where for simplicity, $\sigma_U^2(i)$ is denoted by σ_U^2, and where matrix G is defined in terms of shaping filter g in a similar manner to the definition of matrix H in terms of impulse response h.

[0057] Similarly, using Equation 4b and assumptions 2 and 3, it follows that:

$$\begin{aligned}E\{u(i)\cdot\overline{V}^H\}&=E\{u(i)\cdot(H\cdot\overline{U}+\overline{N})\}\\&=\sigma_U^2\cdot[h(L)\quad \text{?}\quad h(0)\quad \text{?}\quad h(-L)]\end{aligned} \quad \text{(Equation 7)}$$

[0058] From Equations 5, 6 and 7, and applying the complex conjugate operator, the MMSE analytical calculation of the FIR filter C is as follows:

$$\overline{C}=[H\cdot H^H\cdot\sigma_U^2+G\cdot G^H\cdot\sigma^2_{N\_AWGN}]^{-1}\cdot\begin{bmatrix}h(L)\\ \blacksquare\\ h(0)\\ \blacksquare\\ h(-L)\end{bmatrix}\cdot\sigma_U^2. \quad \text{(Equation 8)}$$

[0059] FIR filter C may be calculated empirically. For example, a simulation environment may be built in which *u(i)* is the instantaneous frequency at the baseband, *h(i)* is the total response from the input to the sigma-delta converter until the input to the VCO, shaping filter *g(i)* is chosen so that shaped noise *n(i)* will be a high pass noise a cutoff frequency of which is beyond the band of interest of the total response. A simulation may then be run to determine empirical values for *v(i)*. The following quantities may then be calculated:

$$R_{VV} = \frac{1}{L} \cdot \sum_{k=0}^{L-1} \overline{V}(i-k) \cdot \overline{V}^{H}(i-k), \text{ and} \qquad \text{(Equation 9a)}$$

$$R_{VU} = \frac{1}{L} \cdot \sum_{k=0}^{L-1} \overline{V}(i-k) \cdot u^{*}(i-k). \qquad \text{(Equation 9b)}$$

[0060] The empirically calculated FIR MMSE filter is then given by:

$$\overline{C} = R_{VV}^{-1} \cdot \overline{R}_{VU}. \qquad \text{(Equation 9c)}$$

[0061] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those of ordinary skill in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the spirit of the invention.

What is claimed is:

1. A method comprising:

building a linear model of an analog fractional-N phase locked loop unit having a voltage controlled oscillator; and

determining a transfer function of a filter that is optimized according to predefined optimization criteria,

wherein said optimization criteria are related to an input to said filter and are related to an input to said voltage controlled oscillator.

2. The method of claim 1, further comprising:

including in said model impairments of one or more components of said phase locked loop unit.

3. The method of claim 1, further comprising:

including phase noise in said model.

4. The method of claim 1, further comprising:

including in said model variations of parameters of said phrase locked loop unit from nominal values.

5. The method of claim 1, wherein determining said transfer function includes determining said transfer function to be optimized according to said predefined optimization criteria that includes a mean squared error of an input to said filter and an input to said voltage controlled oscillator.

6. The method of claim 1, wherein determining said transfer function includes determining said transfer function to be optimized according to said predefined optimization criteria that includes spectral cleanliness of an output of said voltage controlled oscillator.

7. The method of claim 1, further comprising:

selecting a topology for said transfer function.

8. The method of claim 1, wherein determining said transfer function includes determining a finite impulse response transfer function.

9. The method of claim 1, wherein determining said transfer function includes determining an infinite impulse response transfer function.

10. A method comprising:

adjusting digital values of a filter to compensate for variations in an analog fractional-N phase locked loop unit.

11. The method of claim 10, wherein adjusting said digital values includes adjusting said digital values to compensate at least for variations in voltage, temperature, aging, or any combination thereof.

12. The method of claim 10, wherein adjusting said digital values includes adjusting said digital values to compensate at least for variations of parameters of said phase locked loop unit from nominal values.

13. The method of claim 10, further comprising:

determining adjusted digital values so that a transfer function of said filter is optimized according to predefined optimization criteria.

14. A fractional-N sigma-delta modulator comprising:

a filter having a finite impulse response transfer function, said filter coupled to an input of a sigma-delta converter; and

a fractional-N phase locked loop unit coupled to an output of said sigma-delta converter.

15. The fractional-N sigma-delta modulator of claim 14, wherein said transfer function is substantially equivalent to a transfer function of a minimum mean squared error equalizer.

16. The fractional-N sigma-delta modulator of claim 14, wherein digital values of said filter are to be adjusted so that said transfer function is optimized according to predefined optimization criteria.

17. The fractional-N sigma-delta modulator of claim 16, wherein said optimization criteria includes a mean squared error of an input to said filter and an input to a voltage controlled oscillator of said fractional-N phase locked loop unit.

18. The fractional-N sigma-delta modulator of claim 16, wherein said optimization criteria includes spectral cleanliness of an output of a voltage controlled oscillator of said fractional-N phase locked loop unit.

19. A fractional-N sigma-delta modulator comprising:

a sigma-delta converter;

a fractional-N phase locked loop unit coupled to an output of said sigma-delta converter and including a voltage controlled oscillator; and

a filter having an infinite impulse response transfer function, said filter coupled to an input of said sigma-delta converter, wherein said infinite impulse response transfer function is not an inverse of a transfer function from an output of said filter to an input of said voltage controlled oscillator.

20. The fractional-N sigma-delta modulator of claim 19, wherein digital values of said filter are to be adjusted so that said infinite impulse response transfer function is optimized according to predefined optimization criteria.

21. The fractional-N sigma-delta modulator of claim 20, wherein said optimization criteria are related to an input to said filter and are related to an input to said voltage controlled oscillator

22. The fractional-N sigma-delta modulator of claim 20, wherein said optimization criteria includes spectral cleanliness of an output of said voltage controlled oscillator.

23. A fractional-N sigma-delta modulator comprising:

an adaptive filter coupled to an input of a sigma-delta converter; and

a fractional-N phase locked loop unit coupled to an output of said sigma-delta converter.

24. The modulator of claim 23, wherein a transfer function of said adaptive filter is a finite impulse response.

25. The modulator of claim 23, wherein said fractional-N phase locked loop unit includes a voltage controlled oscillator, and wherein a transfer function of said

adaptive filter is not an inverse of a transfer function from an output of said filter to an input of said voltage controlled oscillator.

26. A communication device comprising:

a dipole antenna;

a power amplifier coupled to said dipole antenna; and

a fractional-N sigma-delta modulator coupled to said power amplifier, said fractional-N sigma-delta modulator including at least:

a filter coupled to an input of a sigma-delta converter; and

a fractional-N phase locked loop unit coupled to an output of said sigma-delta converter,

wherein a transfer function of said filter is to be optimized according to predefined optimization criteria.

27. The communication device of claim 26, wherein said transfer function is a finite impulse response.

28. The communication device of claim 26, wherein said transfer function is an infinite impulse response.

29. A communication system comprising:

a first communication device; and

a second communication device including at least:

a fractional-N sigma-delta modulator including at least:

a filter coupled to an input of a sigma-delta converter; and

a fractional-N phase locked loop unit coupled to an output of said sigma-delta converter,

wherein a transfer function of said filter is to be optimized according to predefined optimization criteria.

30. The communication system of claim 29, wherein said transfer function is a finite impulse response.

31. The communication system of claim 29, wherein said transfer function is an infinite impulse response.

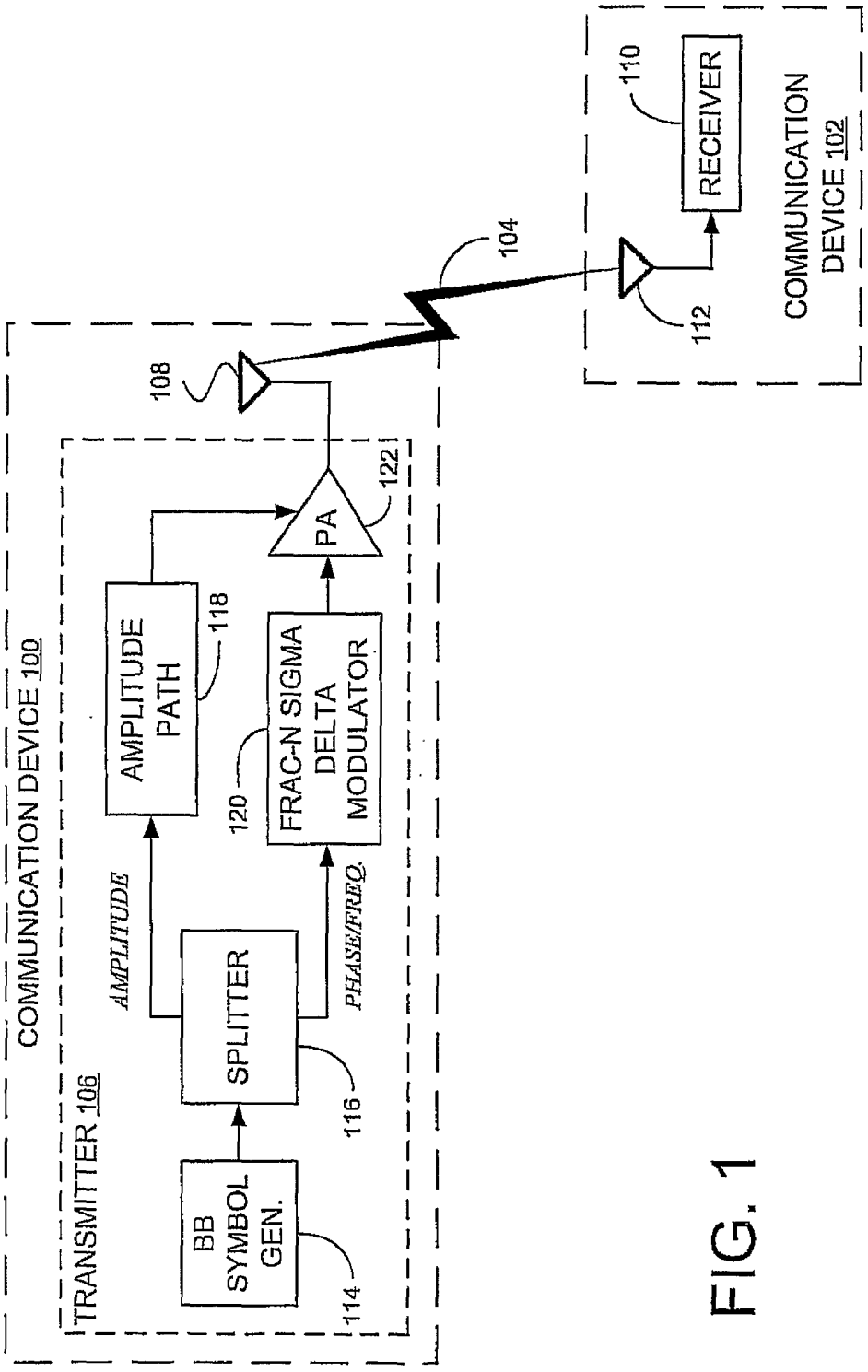
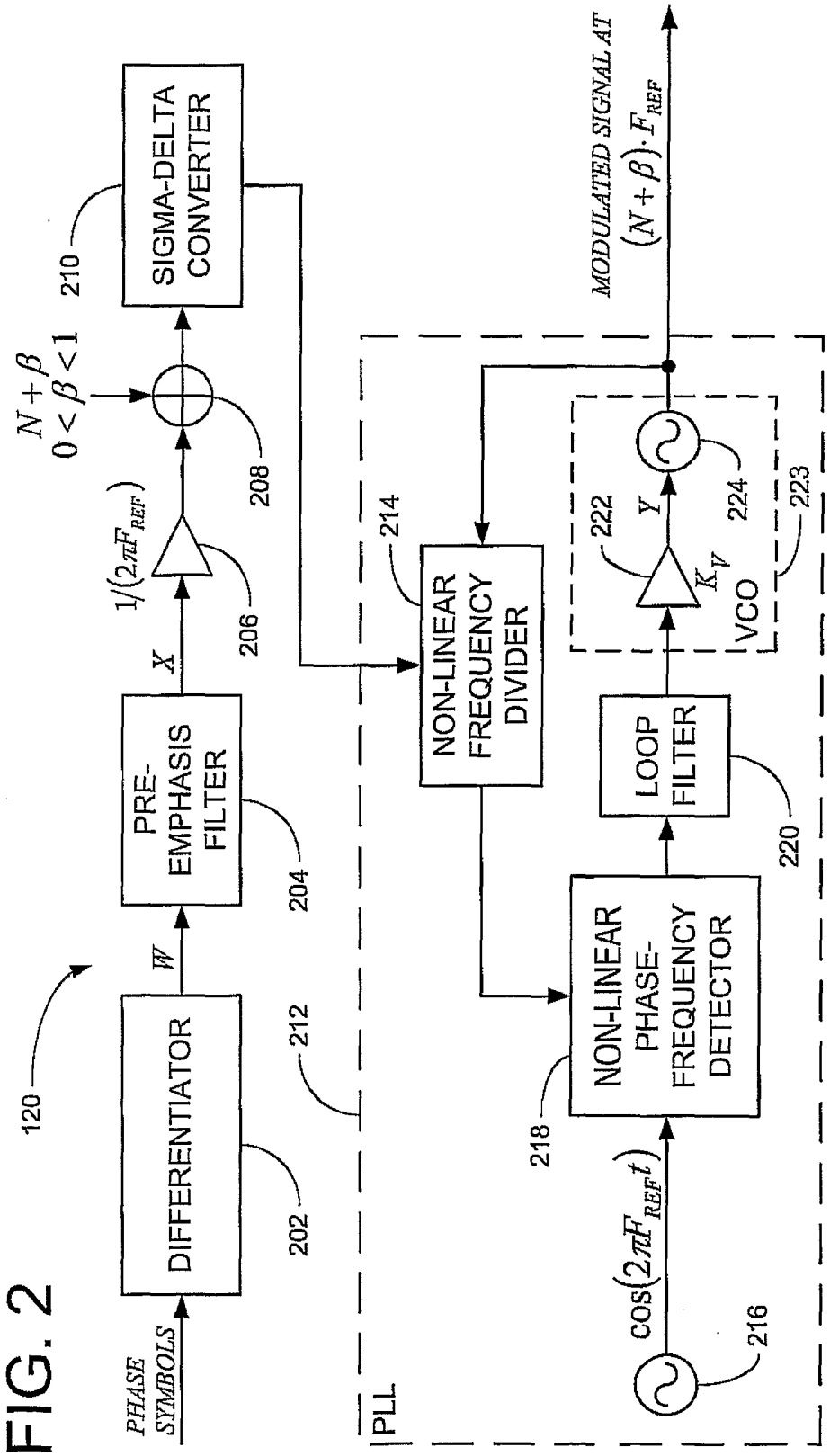

COMMUNICATION DEVICE 100
TRANSMITTER 106
BB SYMBOL GEN.
114
SPLITTER
116
AMPLITUDE
PHASE/FREQ.
AMPLITUDE PATH
118
FRAC-N SIGMA DELTA MODULATOR
120
PA
122
108
104
112
RECEIVER
110
COMMUNICATION DEVICE 102

FIG. 1

FIG. 2


PHASE SYMBOLS
120
DIFFERENTIATOR
202
W
PRE-EMPHASIS FILTER
204
X
1/(2πF_REF)
206
N + β
0 < β < 1
208
SIGMA-DELTA CONVERTER
210
212
PLL
NON-LINEAR FREQUENCY DIVIDER
214
NON-LINEAR PHASE-FREQUENCY DETECTOR
218
LOOP FILTER
220
VCO
223
222
Y
K_V
224
MODULATED SIGNAL AT (N + β)·F_REF
cos(2πF_REF t)
216

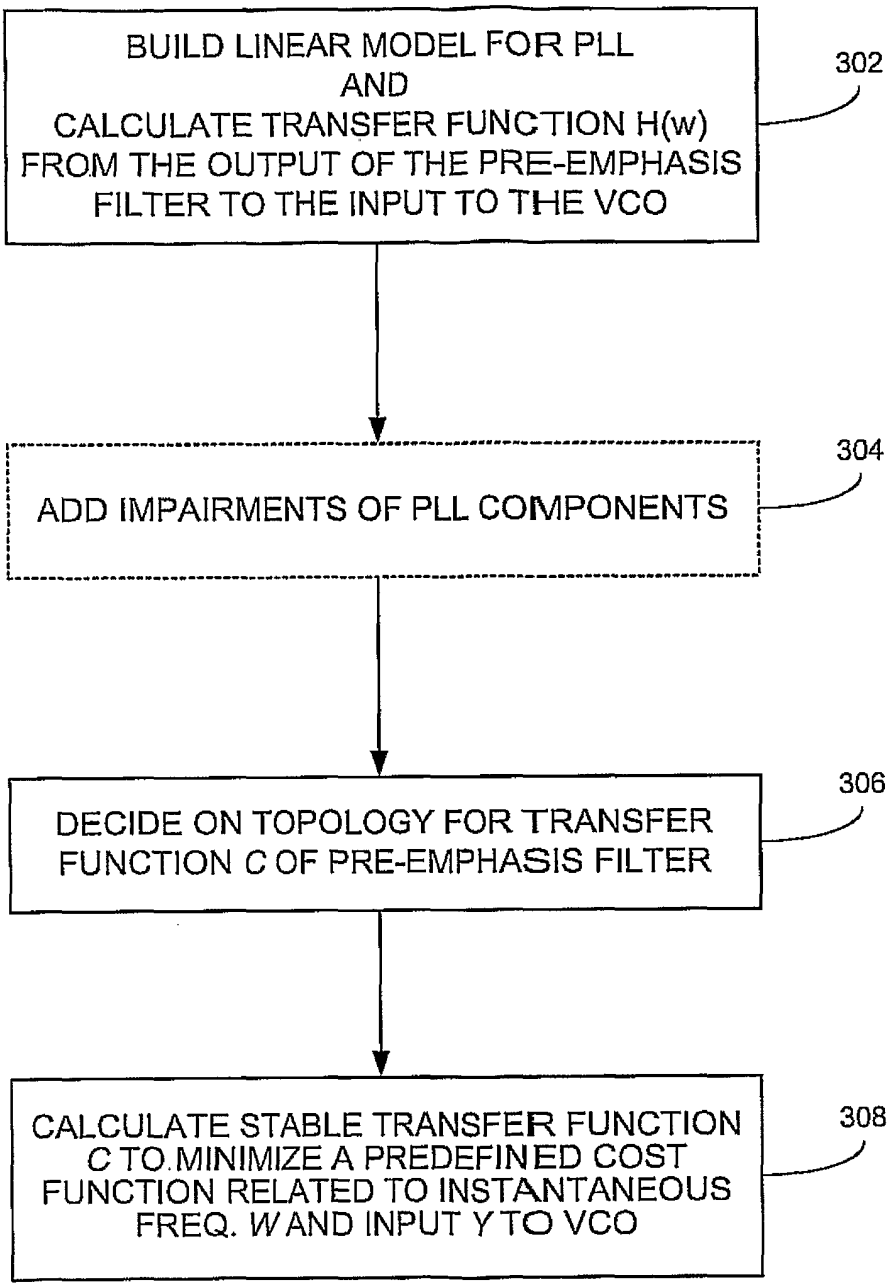

BUILD LINEAR MODEL FOR PLL
AND
CALCULATE TRANSFER FUNCTION H(w)
FROM THE OUTPUT OF THE PRE-EMPHASIS
FILTER TO THE INPUT TO THE VCO
302
ADD IMPAIRMENTS OF PLL COMPONENTS
304
DECIDE ON TOPOLOGY FOR TRANSFER
FUNCTION C OF PRE-EMPHASIS FILTER
306
CALCULATE STABLE TRANSFER FUNCTION
C TO MINIMIZE A PREDEFINED COST
FUNCTION RELATED TO INSTANTANEOUS
FREQ. W AND INPUT Y TO VCO
308

FIG. 3

FIG. 4

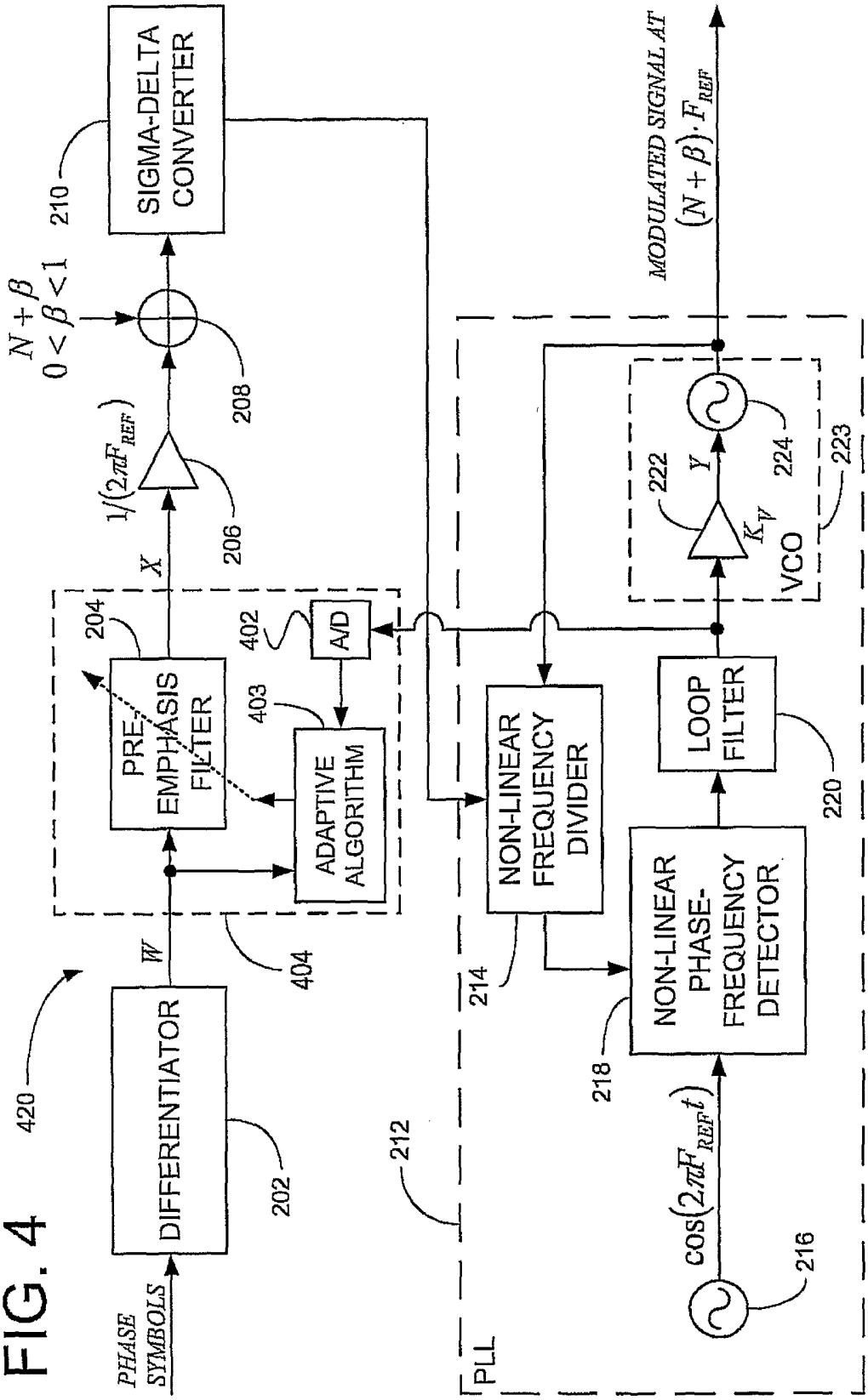
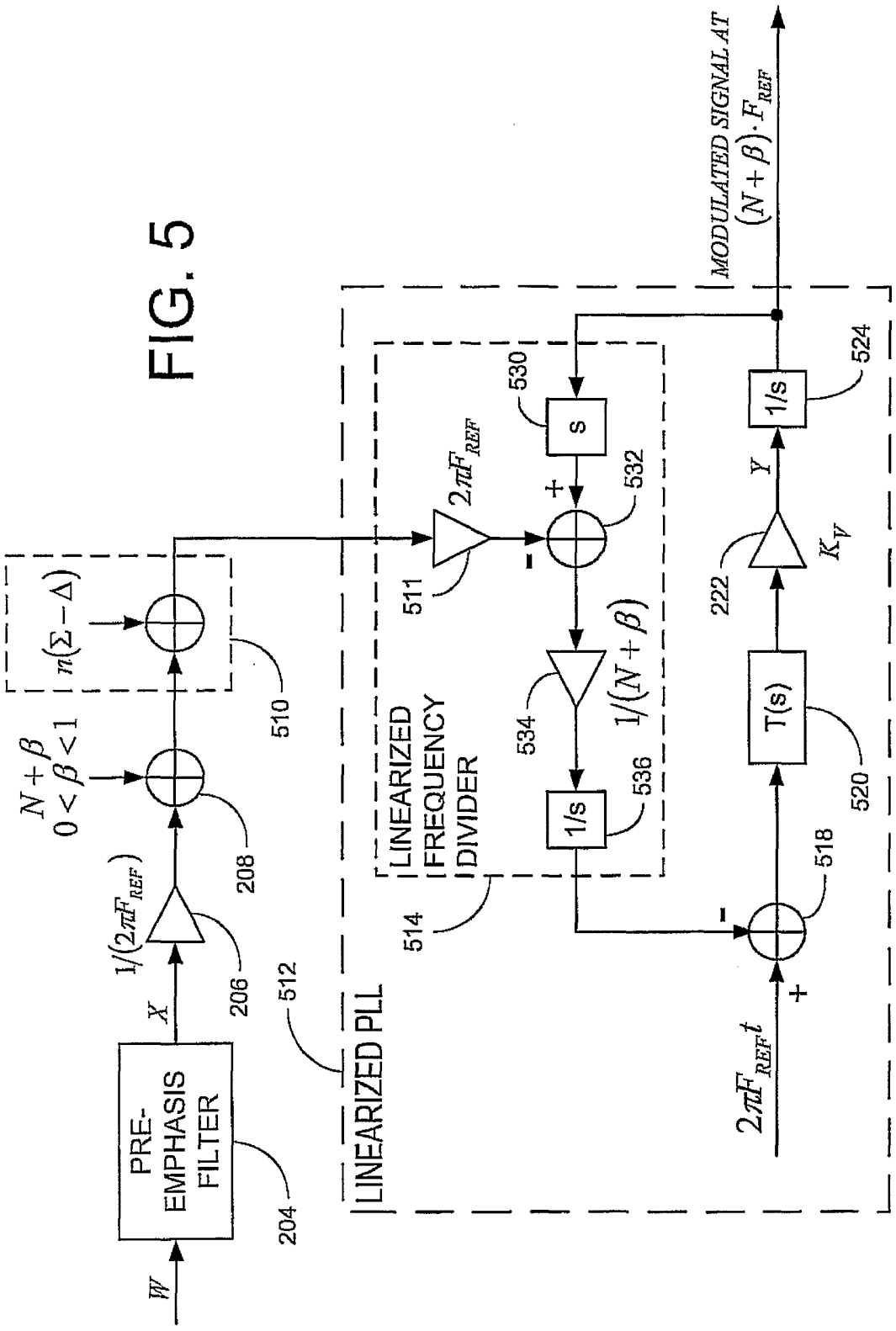

PHASE SYMBOLS
DIFFERENTIATOR
202
W
404
PRE-EMPHASIS FILTER
204
X
ADAPTIVE ALGORITHM
403
A/D
402
1/(2πF_REF)
206
N + β
0 < β < 1
208
SIGMA-DELTA CONVERTER
210
420
PLL
212
NON-LINEAR FREQUENCY DIVIDER
214
NON-LINEAR PHASE-FREQUENCY DETECTOR
218
LOOP FILTER
220
VCO
223
Y
222
K_V
224
MODULATED SIGNAL AT (N + β)·F_REF
cos(2πF_REF t)
216

FIG. 5


W
PRE-EMPHASIS FILTER
204
X
1/(2πF_REF)
206
N + β
0 < β < 1
208
n(Σ − Δ)
510
LINEARIZED PLL
512
LINEARIZED FREQUENCY DIVIDER
514
2πF_REF
511
530
s
532
534
1/(N + β)
536
1/s
MODULATED SIGNAL AT (N + β)·F_REF
524
1/s
Y
222
K_V
T(s)
520
518
2πF_REF t

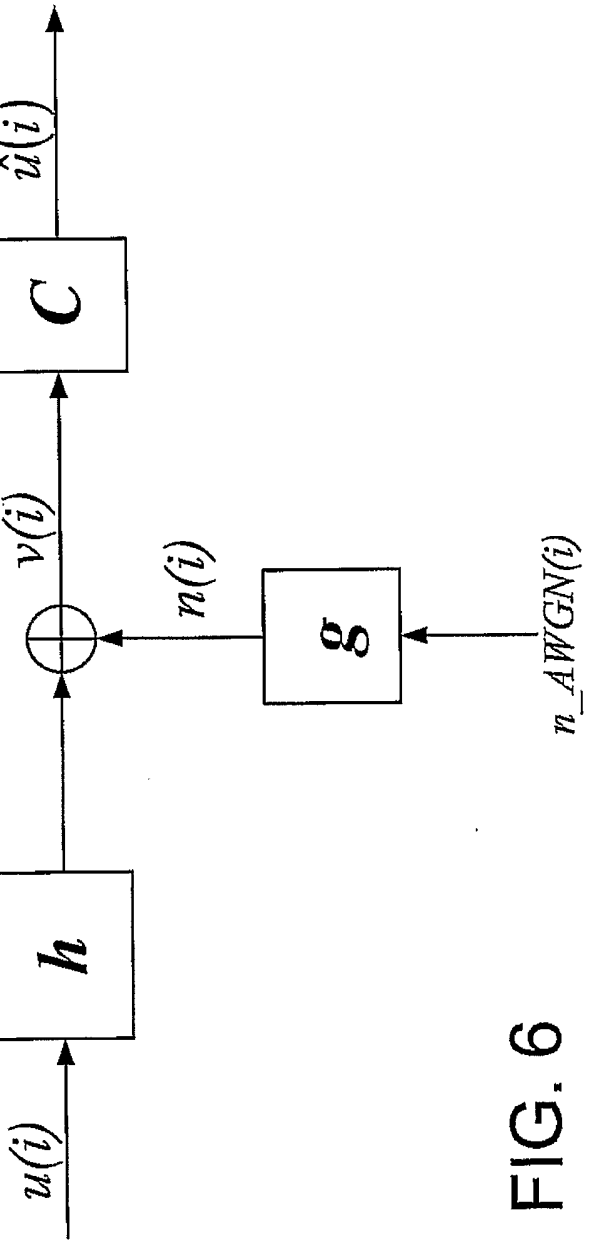


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/010959

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L25/03 H04L27/12 H04L27/20 H03C3/09 H03L7/197

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H03C H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, IBM-TDB, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PERROTT M H ET AL: "A 27-MW CMOS FRACTIONAL-N SYNTHESIZER USING DIGITAL COMPENSATION FOR 2.5-MB/S GFSK MODULATION" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 32, no. 12, 1 December 1997 (1997-12-01), pages 2048-2060, XP000767454 ISSN: 0018-9200 page 2049, right-hand column, last paragraph - page 2050, left-hand column, paragraph 2 page 2050, last paragraph page 2051, right-hand column, last paragraph - page 2052, left-hand column, paragraph 3 ----- -/--	1-31

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 May 2005	03. 06. 2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Agudo Cortada, E

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/010959

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	M.H. PERROTT: ""Techniques for High Data Rate Modulation and Low Power Operation of Fractional-N Frequency Synthesizers"" PH.D. DISSERTATION, MIT, 1997, September 1997 (1997-09), XP002297180 Retrieved from the Internet: URL:http://www-mtl.mit.edu/~perrott/pages/thesis.pdf> [retrieved on 2004-09-20] page 33, paragraph 1; figure 1.13 page 65, paragraph 2 - paragraph 4	1-31
A	US 6 008 703 A (PERROTT MICHAEL H ET AL) 28 December 1999 (1999-12-28) column 2, line 39 - line 54 page 3, line 62 - page 4, line 4 column 8, line 38 - line 54 column 10, line 6 - line 17	1-31
A	US 2003/206056 A1 (HIETALA ALEXANDER WAYNE) 6 November 2003 (2003-11-06) paragraph [0027] - paragraph [0028]	1-31

INTERNATIONAL SEARCH REPORT

Information on patent family members

In tional Application No
PCT/US2004/010959

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6008703 A	28-12-1999	WO 9834339 A1	06-08-1998
US 2003206056 A1	06-11-2003	NONE	