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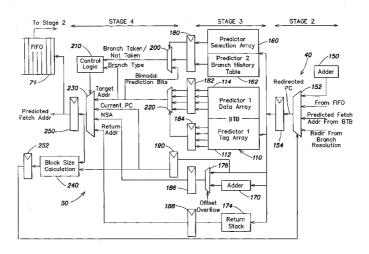
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(54) Title: METHOD AND APPARATUS FOR BRANCH PREDICTION BASED ON BRANCH TARGETS



(57) Abstract: Methods and apparatus are provided for branch prediction in a digital processor. A method includes providing a branch target buffer having a tag array and a data array, wherein each entry in the tag array provides an index to a corresponding entry in the data array, storing in a selected entry in the tag array information representative of a branch target of a current branch instruction, storing in a corresponding entry in the data array information representative of a branch target of a next branch instruction, and providing the information representative of the branch target of the next branch instruction in response to a match to an entry in the tag array. The information representative of the branch target of the next branch instruction may include a taken branch target address of the next branch instruction and an offset value. The offset value may represent an address of a next sequential instruction following the next branch instruction.

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER IPC 7 G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

 $\begin{array}{ccc} \text{Minimum documentation searched (classification system followed by classification symbols)} \\ IPC & 7 & G06F \end{array}$

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	REINMAN G ET AL: "A SCALABLE FRONT-END ARCHITECTURE FOR FAST INSTRUCTION DELIVERY" PROCEEDINGS OF THE 26TH INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE. ATLANTA, GA, MAY 2 - 4, 1999, INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE. (ISCA), LOS ALAMITOS, CA: IEEE COMP. SOC, US, vol. CONF. 26, 2 May 1999 (1999-05-02), pages 234-245, XP000887621	1-5, 8-22, 26-29
	ISBN: 0-7695-0171-0 section 4.2: "Fetch Target Buffer" figures 1,2/	30-33

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X Further documents are listed in the continuation of box C.	Patent family members are listed in annex.		
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Date of the actual completion of the international search 6 October 2005	Date of mailing of the international search report $18/10/2005$		
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo ni, Fax: (+31-70) 340-3016	Authorized officer Daskalakis, T		

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