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(54) Title: SPACED-ONE-HOT RECEIVER

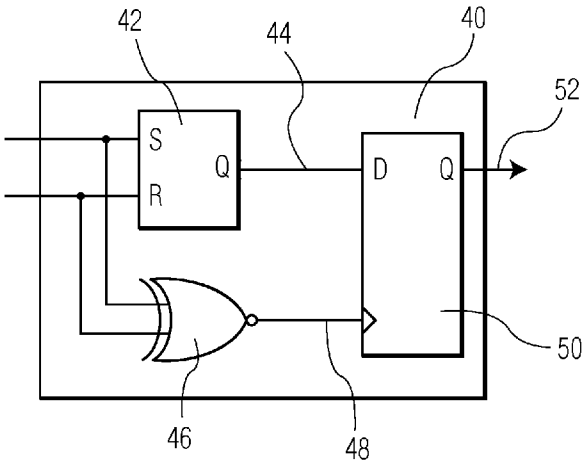

FIG. 4

(57) Abstract: A mobile device that incorporates the MIPI D-PHY specification has data lanes for carrying data between electronic modules within the device. The data lanes may incorporate a spaced-one-hot approach for asynchronously receiving a data signal over a two-wire interface. A two-wire receive interface is provided that uses an exclusive-NOR to capture a timing signal along with a set-reset flip-flop which holds the state of the data line so that a D flip-flop that is clocked on the falling edge of the timing signal received from the exclusive-NOR gate can sample the data and provide an accurate asynchronous data output.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	MARCO STORTO AND ROBERTO SALETTI.: "Time-multiplexed dual-rail protocol for lowpower delay-insensitive asynchronous communication." POWER AND TIMING MODELING, OPTIMIZATION AND SIMULATION (PATMOS), October 1998 (1998-10), page 136, XP002475259 the whole document	1-16
A	IEEE: "IEEE Std 1394-1995" IEEE STANDARD 1394-1995, 1995, page 32, XP002475297 USA the whole document	1-16

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[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Name and mailing address of the ISA/	Authorized officer
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ANTHONY J. MCAULEY: "Four State Asynchronous Architectures" IEEE TRANSACTIONS ON COMPUTERS,, vol. 41, no. 2, 2 February 1992 (1992-02-02), pages 129-142, XP002475258 the whole document	1-16
A	MARK B. JOSEPHS, STEVEN M. NOWICK, AND C. H. (KEES) VAN BERKEL: "Modeling and Design of Asynchronous Circuits" PROCEEDINGS OF THE IEEE,, vol. 87, no. 2, February 1999 (1999-02), pages 234-242, XP002475260 the whole document	1-16
A	PEDRO A. MOLINA P. Y. K. CHEUNG DAVID S. BORMANN: "QUASI DELAY-INSENSITIVE BUS FOR FULLY ASYNCHRONOUS SYSTEMS" CIRCUITS AND SYSTEMS, 1996. ISCAS '96., 'CONNECTING THE WORLD'., 1996 IEEE INTERNATIONAL SYMPOSIUM ON, vol. 4, 15 May 1996 (1996-05-15), XP002475275 the whole document	1-16