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Hudait et al.

(54) **DOPANT CONFINEMENT IN THE DELTA DOPED LAYER USING A DOPANT SEGREGRATION BARRIER IN QUANTUM WELL STRUCTURES**

(76) Inventors: **Mantu K. Hudait**, Portland, OR (US); **Aaron A. Budrevich**, Portland, OR (US); **Dmitri Loubychev**, Bethlehem, PA (US); **Jack T. Kavalieros**, Portland, OR (US); **Suman Datta**, Beaverton, OR (US); **Joel M. Fastenau**, Bethlehem, PA (US); **Amy W. Liu**, Mountain View, CA (US)

Correspondence Address:
INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040 (US)

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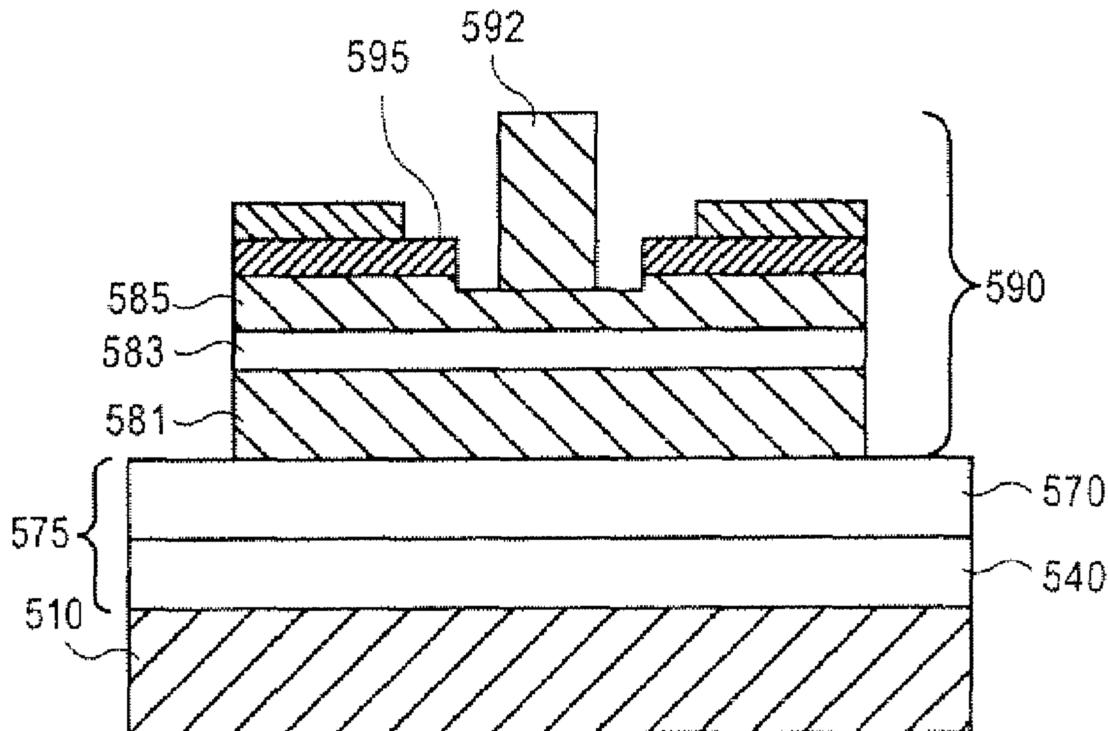
(52) **U.S. Cl.** **438/478**; 257/E29.069; 257/E21.09; 257/E21.407; 257/E21.119; 977/755

(57) **ABSTRACT**

A device grade III-V quantum well structure and method of manufacture is described. Embodiments of the present invention enable III-V InSb quantum well device layers with defect densities below 1×10^{8} cm^{-2} to be formed. In an embodiment of the present invention, a delta doped layer is disposed on a dopant segregation barrier in order to confine delta dopant within the delta doped layer and suppress delta dopant surface segregation.



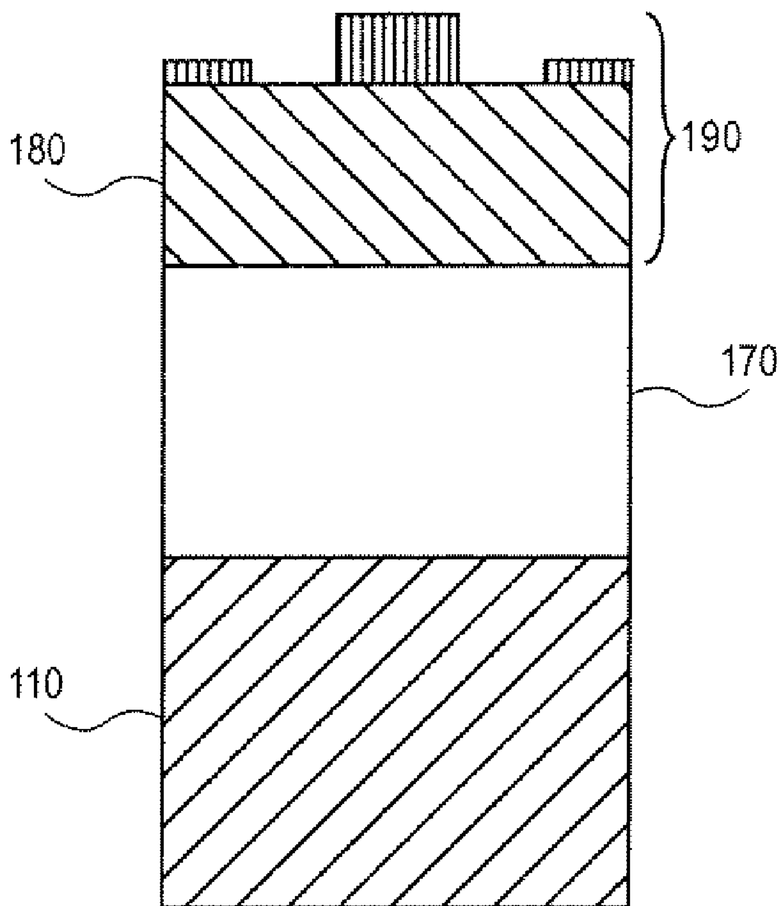


FIG. 1A
(PRIOR ART)

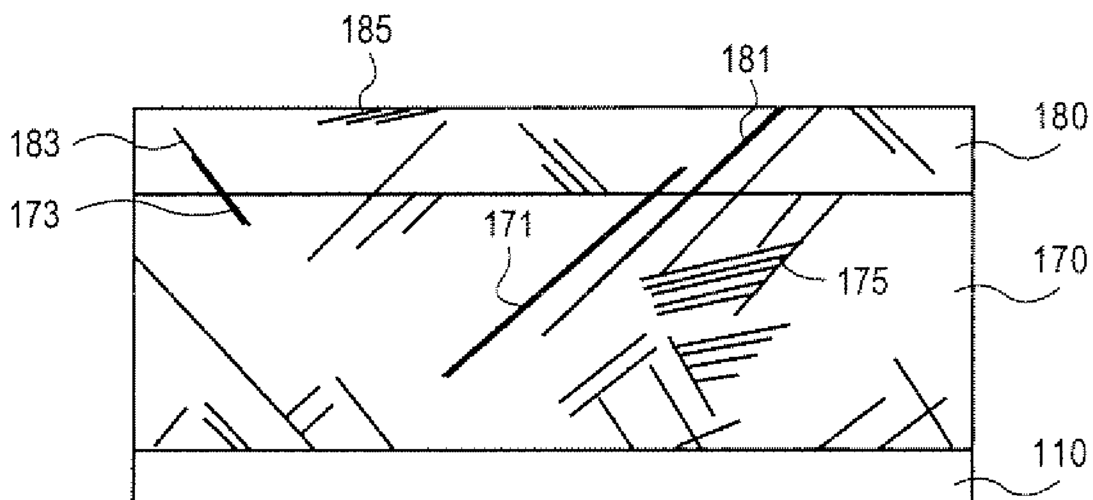


FIG. 1B
(PRIOR ART)

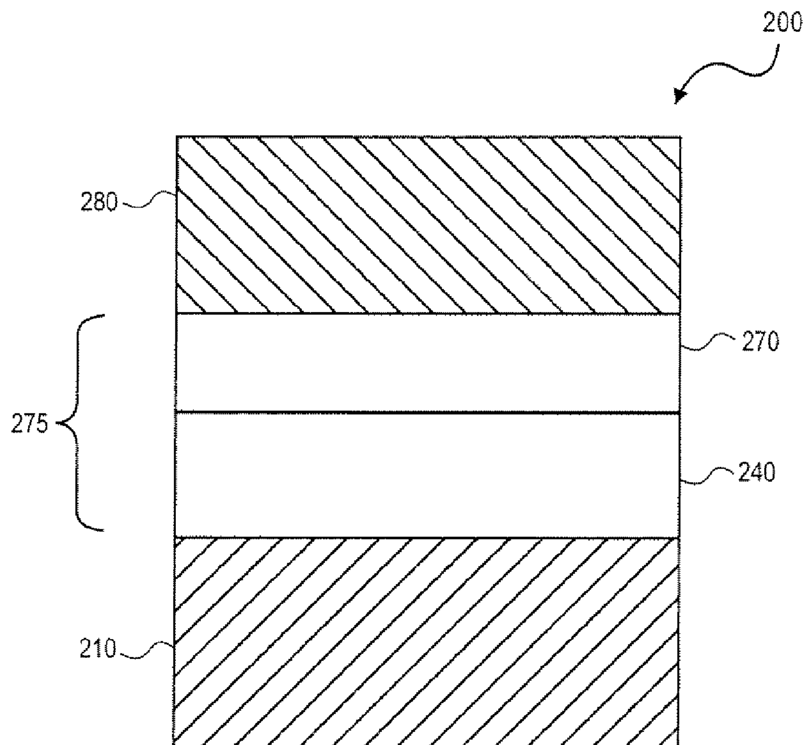


FIG. 2A

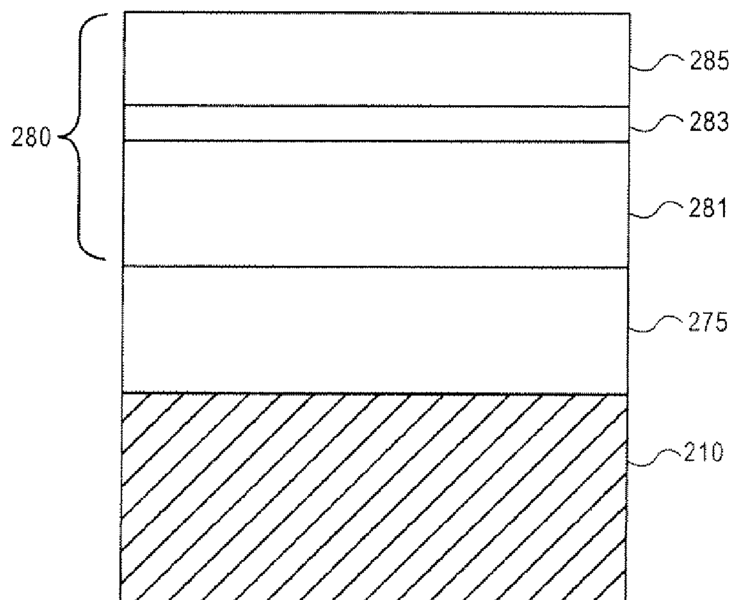


FIG. 2B

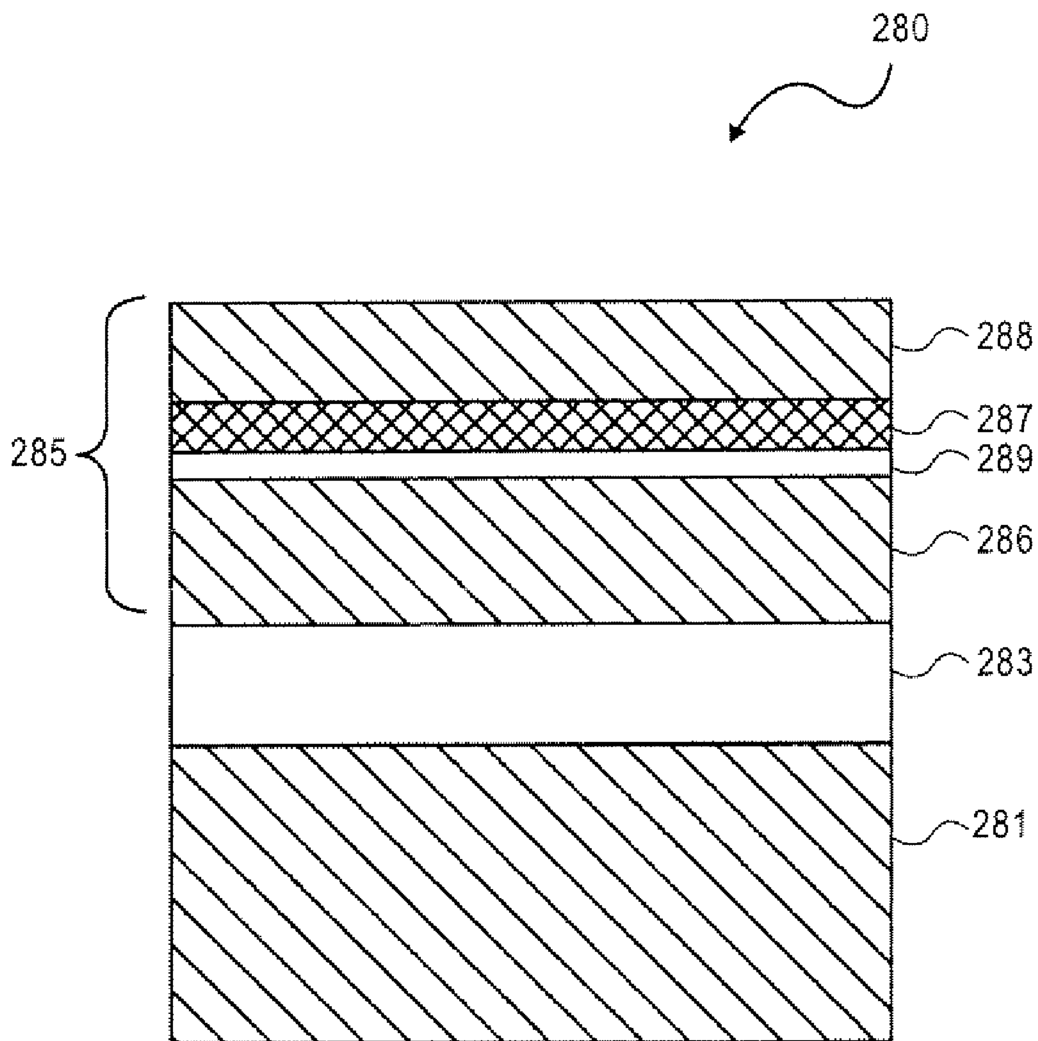


FIG. 2C

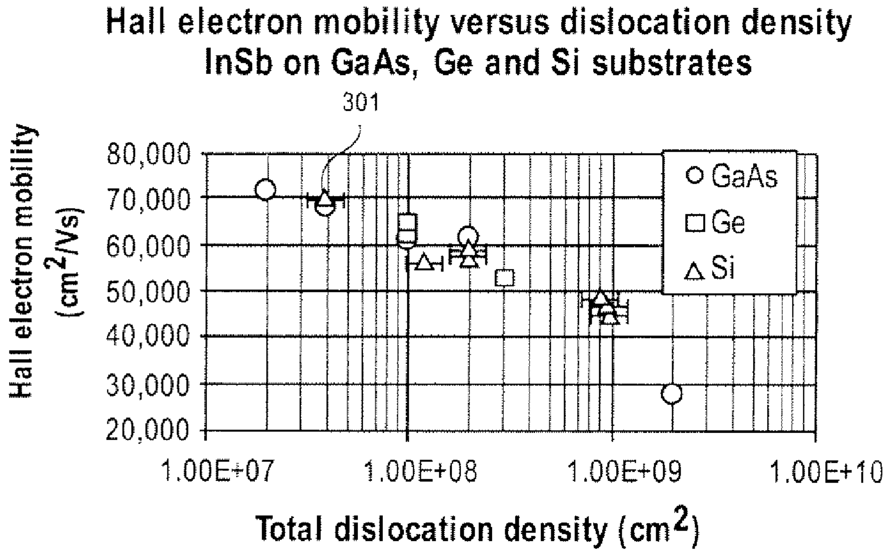


FIG. 3A

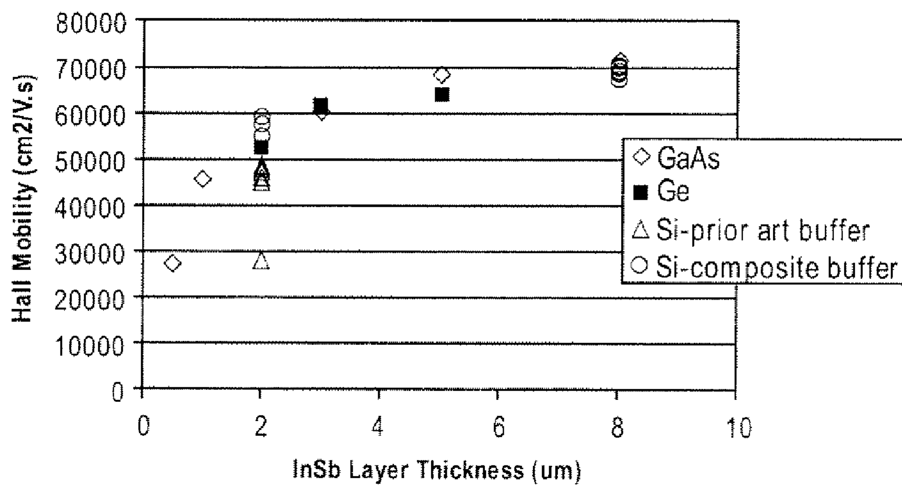


FIG. 3B

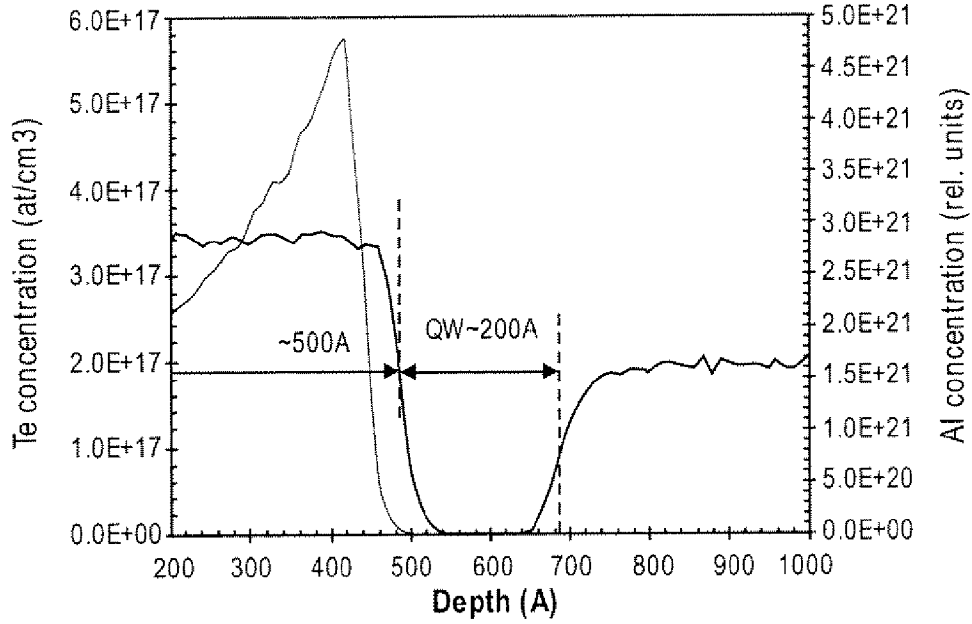


FIG. 3C

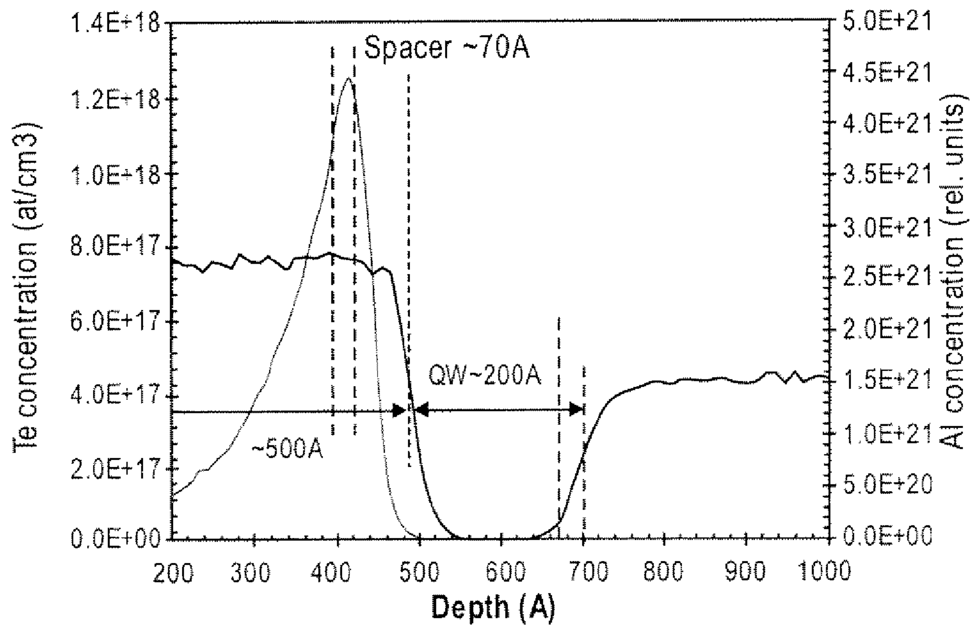


FIG. 3D

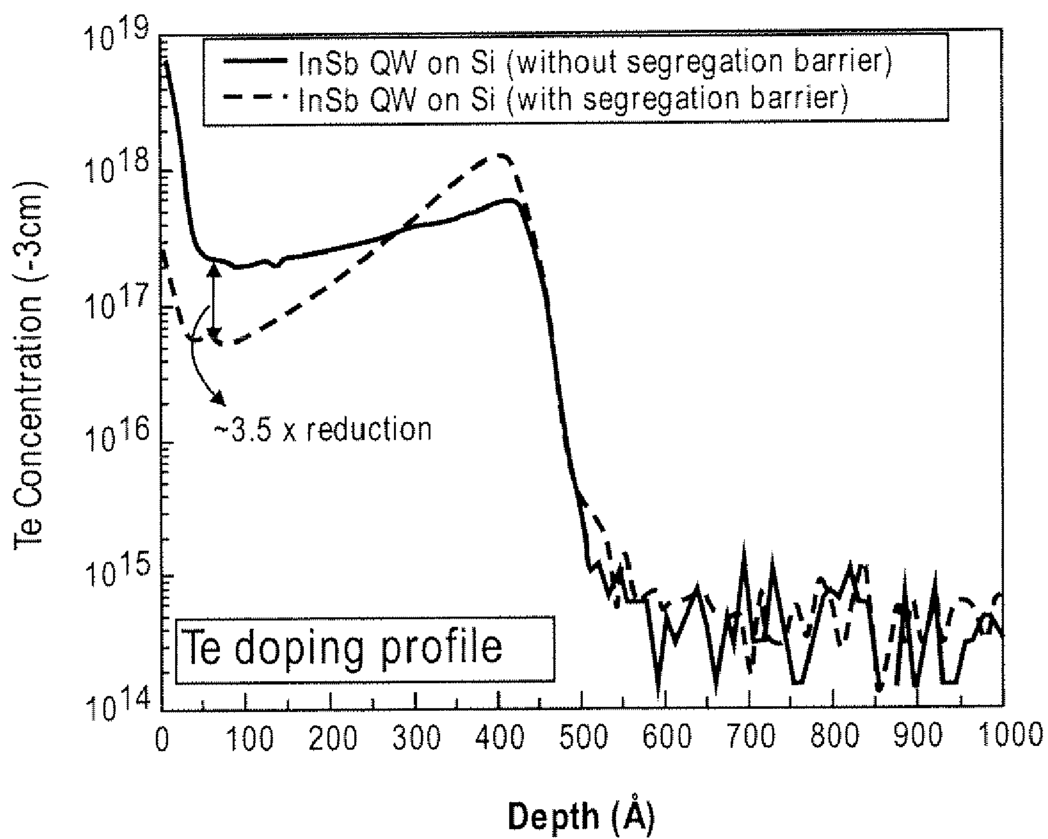


FIG. 3E

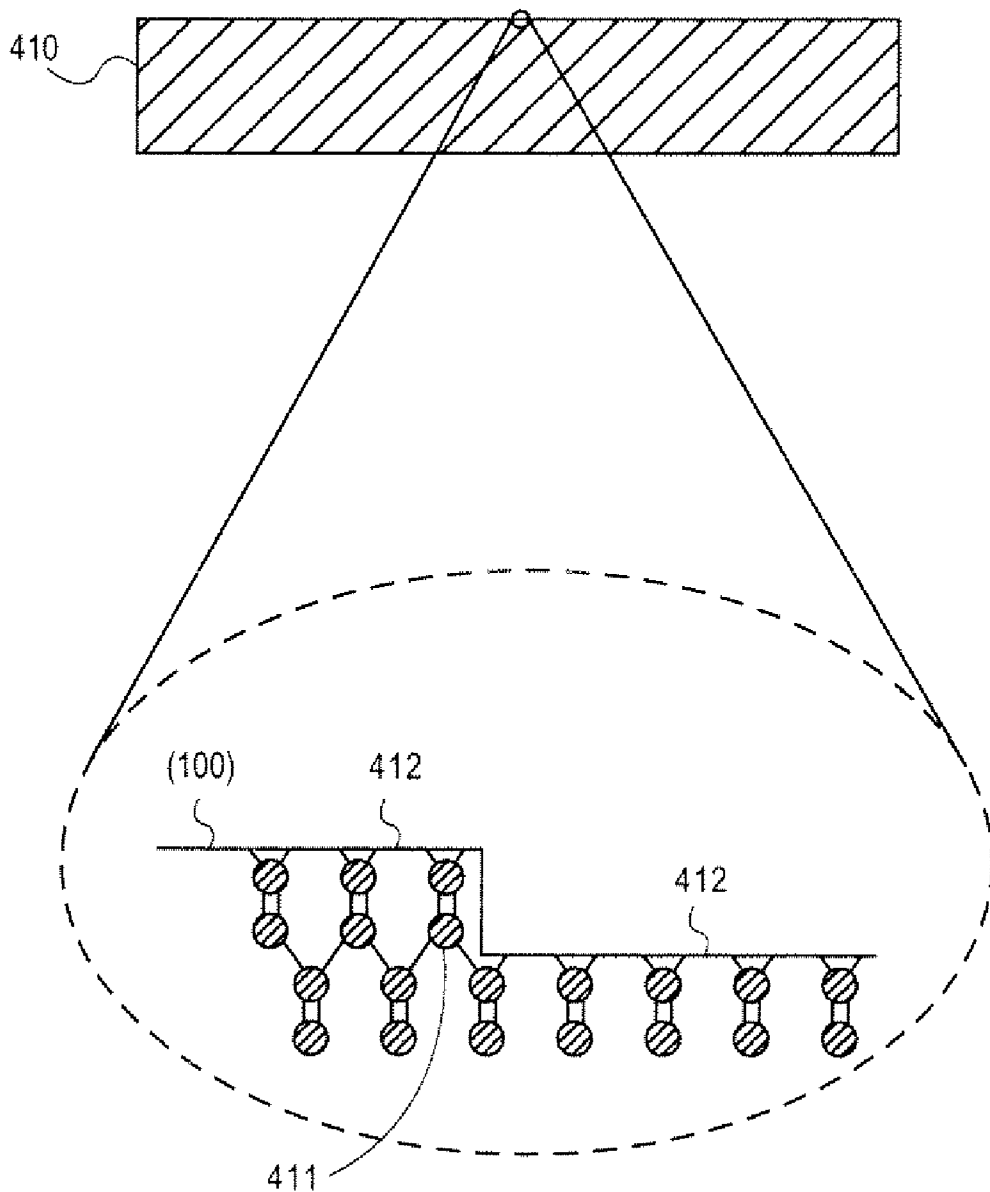


FIG. 4A

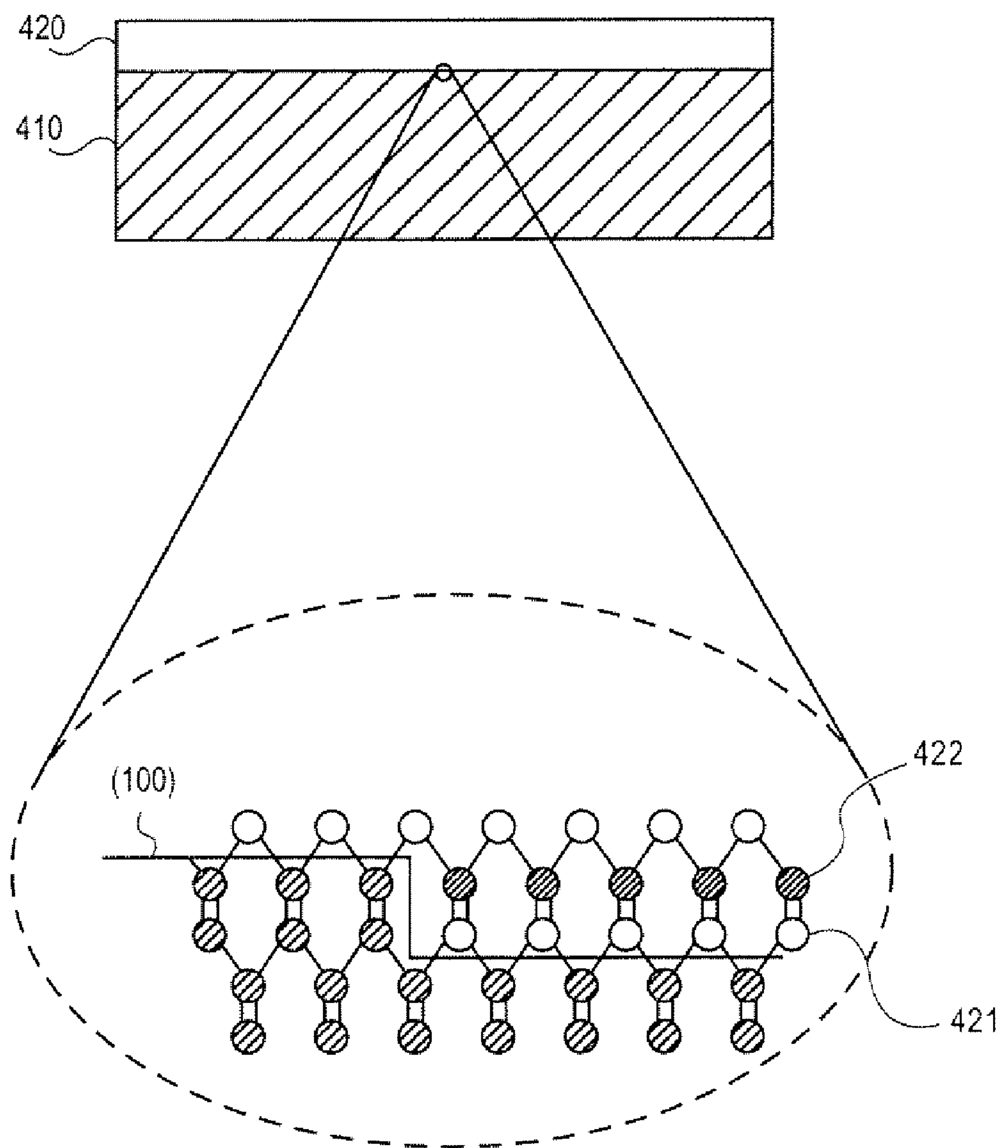


FIG. 4B

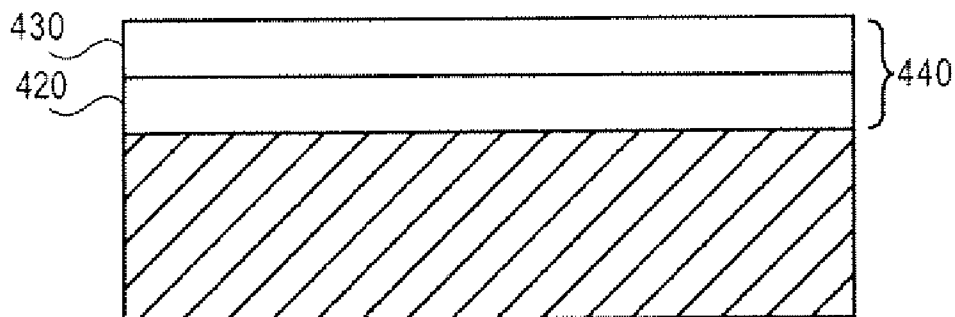


FIG. 4C

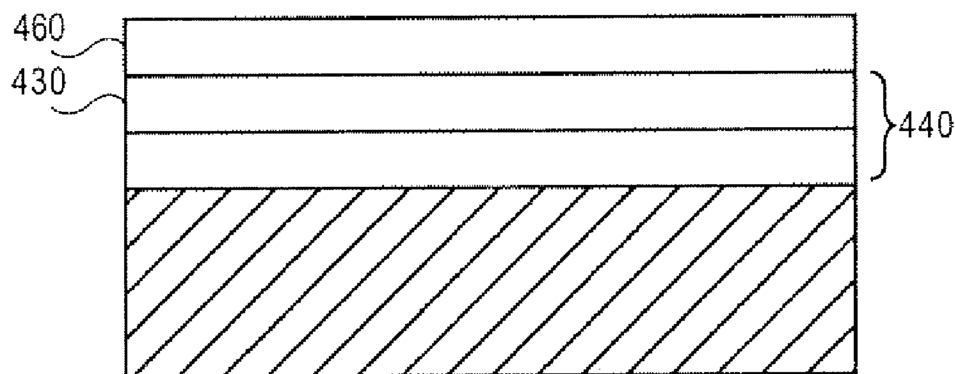


FIG. 4D

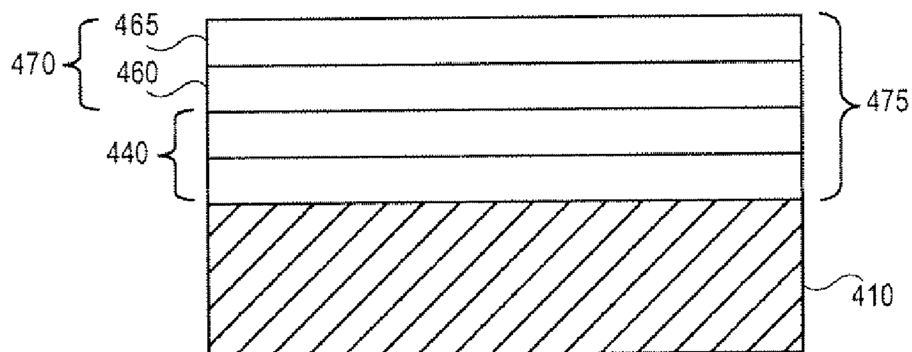


FIG. 4E

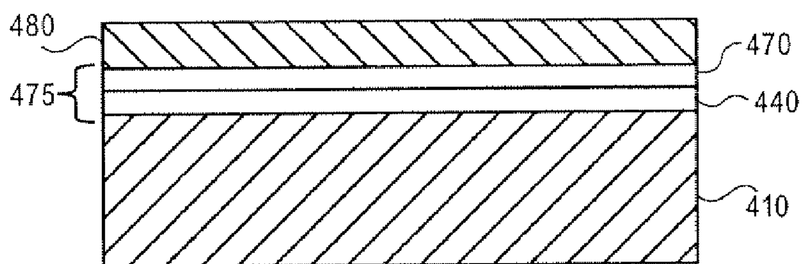


FIG. 4F

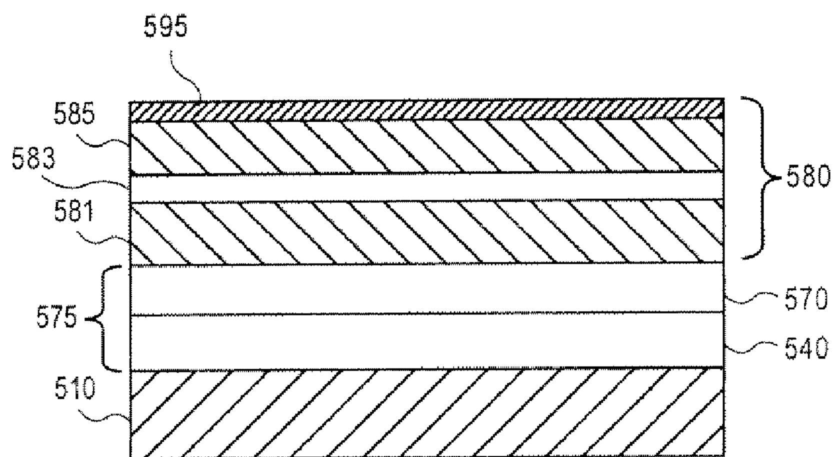


FIG. 5A

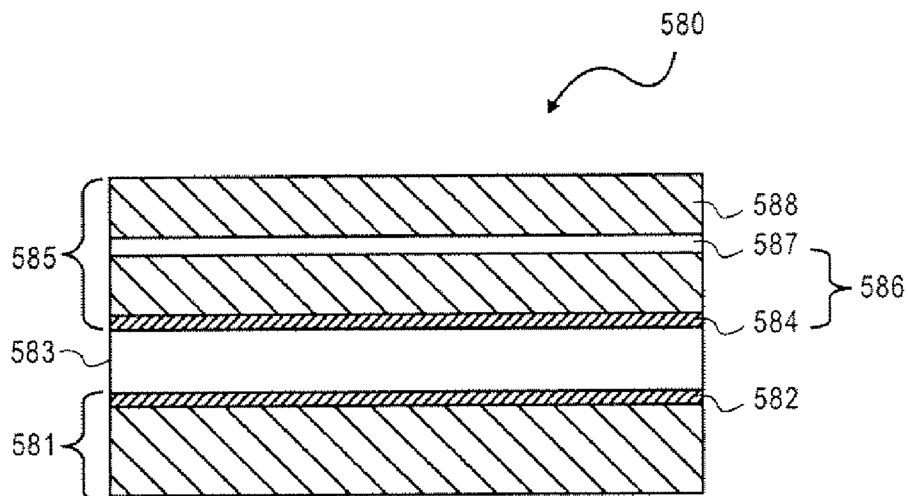


FIG. 5B

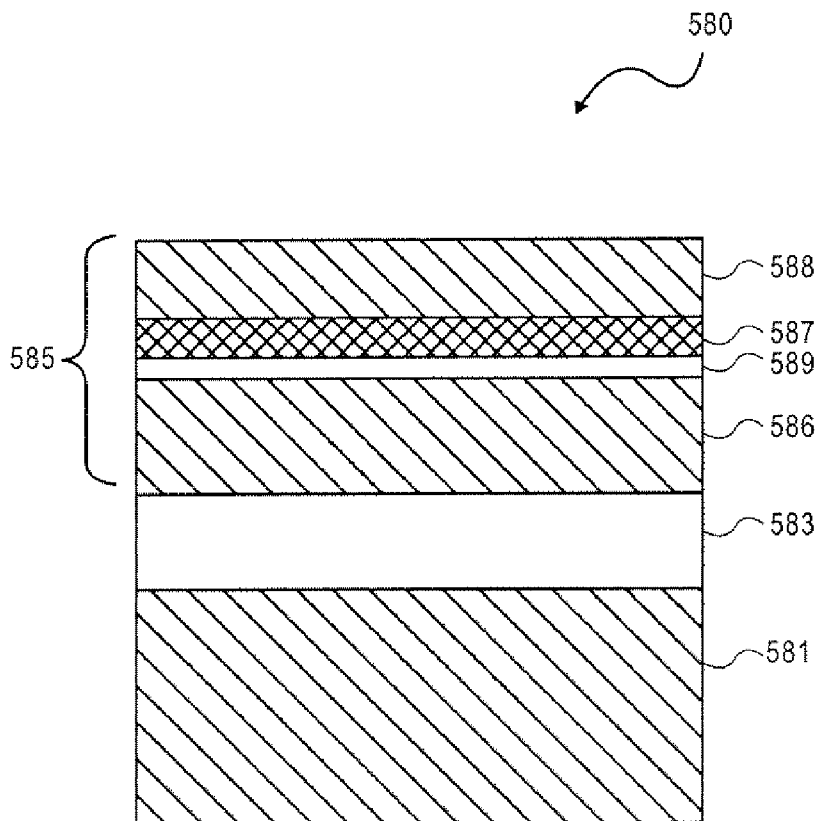


FIG. 5C

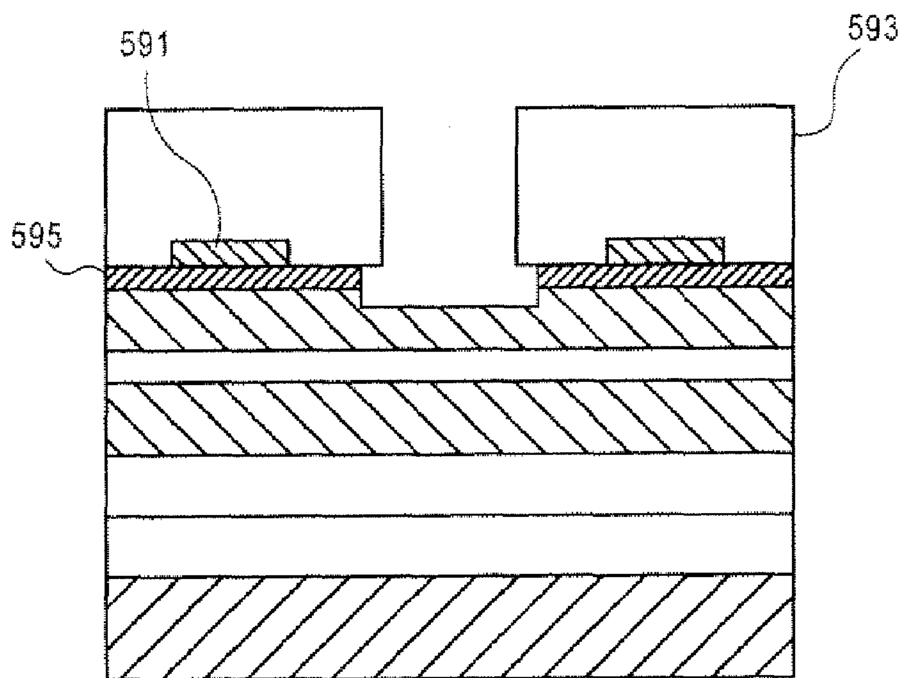


FIG. 5D

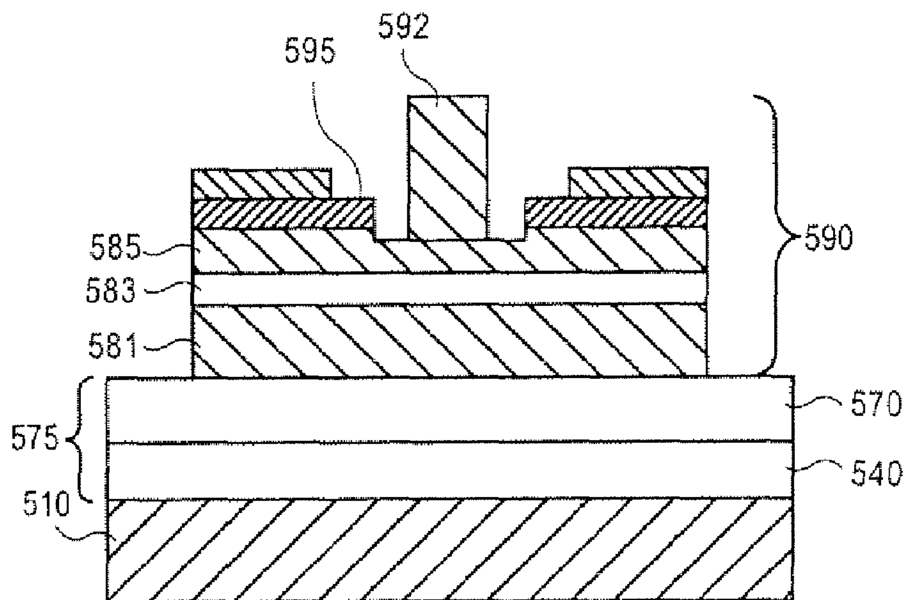


FIG. 5E

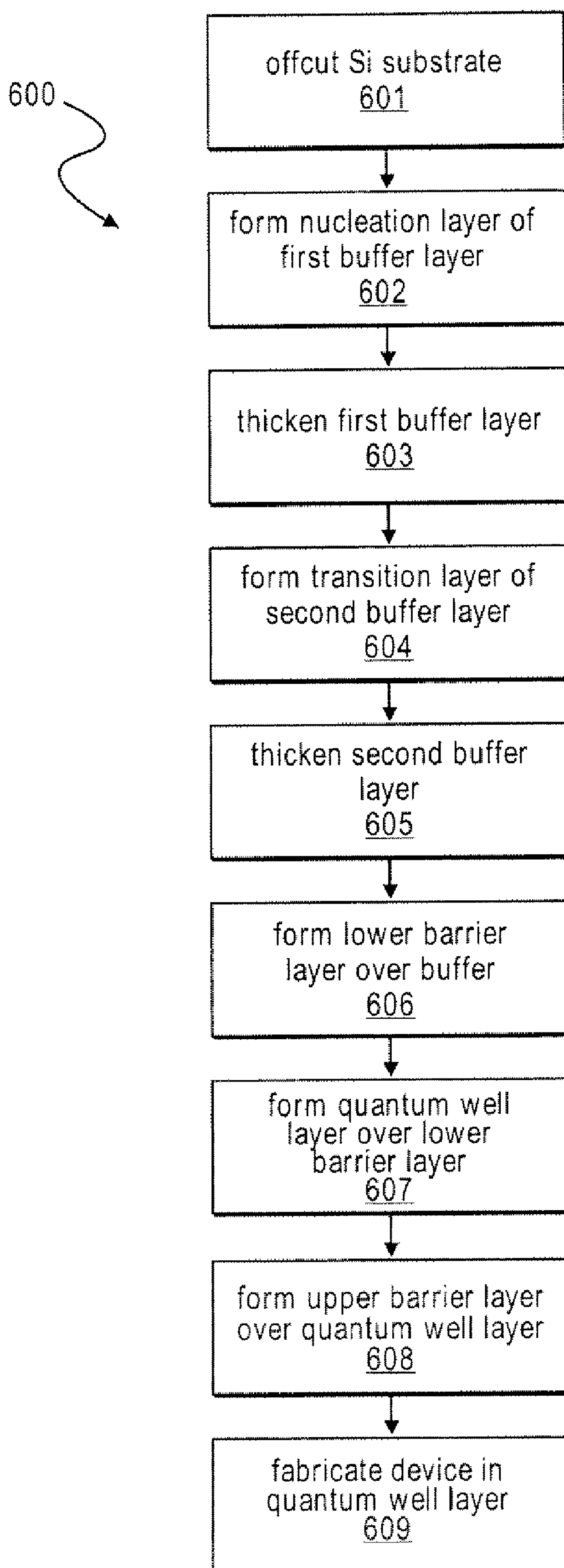


FIG. 6

DOPANT CONFINEMENT IN THE DELTA DOPED LAYER USING A DOPANT SEGREGRATION BARRIER IN QUANTUM WELL STRUCTURES

[0001] This is a Divisional Application of Ser. No. 11/647,989 filed Dec. 29, 2006 which is presently pending.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to the formation of device grade quantum well structures. More particularly this invention relates to dopant segregation barrier layers in quantum well structures.

[0004] 2. Discussion of Related Art

[0005] Recently there has been much interest generated in the study of III-V materials for future high-speed and lower power computation applications. III-V materials in general have 50-100 times higher electron mobility than Si, and III-V quantum well field effect transistors (QWFETs) pose attractive merits over scaled Si MOSFETs. Researchers have already begun investigating the performance advantages of QWFETs fabricated from extreme high mobility materials such as, but not limited to indium antimonide (InSb), gallium arsenide (GaAs), indium gallium arsenide ($In_xGa_{1-x}As$: x>0.53) and indium arsenide (InAs). InSb in particular shows great promise as an ultra-fast, very low power digital logic technology as it has the highest electron mobility and saturation velocity of any known semiconductor.

[0006] Conventional quantum well devices are characterized by employing a narrower band gap quantum well layer sandwiched between two wider band gap barrier layers. The wider band gap barrier layers serve to confine carriers in the quantum well layer, and to reduce junction leakage and transistor off-state leakage current I_{OFF} reduction. Electrons and holes are free to move in the direction perpendicular to the crystal growth direction, but not in the direction of crystal growth, hence, are 2-dimensionally “confined” and display characteristics distinctly different than in the “open” 3-dimensional crystal.

[0007] While III-V materials generally have higher carrier mobility than Si, one disadvantage is that III-V materials generally have a lower charge carrier density than Si. Accordingly, conventional quantum well devices often include modulation doping or delta doping in a region near the quantum well channel layer such that the modulation or delta doping contributes carriers to the quantum well channel layer. However, segregation and desorption of dopants during formation of the barrier layers leads to broadening of the doping profile, thereby deteriorating the characteristics of the device. Thus, what is needed is a structure and a method for reducing segregation and desorption of dopants.

[0008] Another disadvantage with the growth of III-V materials on silicon are the crystal defects generated by lattice mismatch, polar-on-nonpolar mismatch and thermal mismatch between a III-V epitaxial layer and the substrate. When the lattice mismatch between the epitaxial layer and substrate exceeds a few percent, the strain induced by the mismatch becomes too large and defects are generated in the epitaxial layer when the epitaxial film relaxes the strain. Once the film thickness is greater than the critical thickness (film is strained below this thickness and relaxed above this thickness), the strain is relaxed by creating misfit dislocations at the film and substrate interface as well as in the epitaxial film. The epitaxial crystal defects are typically in the form of threading dislocations, stacking faults and twins (periodicity breaks where one portion of the lattice is a mirror image of another). Many defects, particularly threading dislocations and twins, tend to propagate into the quantum well structure where the semiconductor device is fabricated.

[0009] Generally, the severity of defect generation correlates to the amount of lattice mismatch between the III-V semiconductor and the substrate. For these reasons, the large lattice mismatch (approximately 19.2% between the exemplary indium antimonide (InSb) and silicon (Si) combination) typically results in an epitaxial InSb device layer having a high defect density, on the order of 1×10^9 cm^{-2} to 1×10^{10} cm^{-2}. The high defect density reduces the carrier mobility theoretically possible in bulk InSb, eliminating many of the technical advantages of “InSb-on-silicon” integration for high-speed and low-power logic applications. For example the electron mobility in bulk InSb films is estimated to be approximately 76,000 cm^2/Vs. However, to date, the best reported electron mobility of an InSb film formed over a silicon substrate is significantly lower, approximately 40,000-50,000 cm^2/Vs.

[0010] Various buffer layers have been used in attempts to relieve the strain induced by the lattice mismatch between a substrate and the III-V device layer and thereby reduce the detrimental defect density of the device layer. For example as shown in apparatus **100** of FIG. **1**A, a material forms a buffer layer **170** between a silicon substrate **110** and a III-V device layer **180**. A semiconductor device **190** is then fabricated in or upon device layer **180**. Various materials have been utilized as the buffer layer **170**. For example, both aluminum antimonide (AlSb) and strontium titanate ($SrTiO_3$) have been suggested as a buffer layer **170** between a silicon substrate **110** and a III-V device layer **180**. In practice however, as depicted in FIG. **1**B, these buffer layers are unable to prevent twins **171**, threading dislocations **173** and stacking faults **175** from propagating into the III-V device layer **180** as Sins **181**, threading dislocations **183**, and stacking faults **185**. Thus, there also remains a need for a buffer layer architecture that enables lower defect density III-V semiconductor device layers formed upon silicon substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1**A is an illustration of a cross-sectional view of a conventional group III-V semiconductor device formed upon a silicon substrate.

[0012] FIG. **1**B is an illustration of a cross-sectional view of a conventional group III-V semiconductor device layer formed upon a silicon substrate.

[0013] FIGS. **2**A-**2**B are illustrations of a cross-sectional view of a group III-V semiconductor device layer formed upon a silicon substrate in accordance with the present invention.

[0014] FIG. **2**C is an illustration of a quantum well structure including a dopant segregation barrier layer.

[0015] FIG. **3**A is a graph of the dependency of defect density on carrier mobility of a III-V semiconductor device layer achieved with embodiments in accordance with the present invention.

[0016] FIG. **3**B is a graph of the carrier mobility of a III-V semiconductor device layer achieved with embodiments in accordance with the present invention.

[0017] FIG. **3**C illustrates a Te-doping concentration for a quantum well structure without a dopant segregation barrier layer.

[0018] FIG. **3**D illustrates a Te-doping concentration for a quantum well structure with a dopant segregation barrier layer.

[0019] FIG. **3**E illustrates Te-dopant surface segregation reduction with a dopant segregation barrier layer.

[0020] FIGS. **4**A-**4**F are illustrations of cross-sectional views of a method of fabricating a group III-V semiconductor device layer upon a silicon substrate in accordance with the present invention.

[0021] FIGS. **5**A-**5**E are illustrations of cross-sectional views of a method of fabricating a quantum well (QW) transistor in accordance with the present invention.

[0022] FIG. **6** is a flow diagram of a method of fabricating a group III-V semiconductor device layer upon a silicon substrate in accordance with the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0023] In various embodiments, a device grade III-V quantum well structure formed on a buffer architecture is described with reference to figures. However, certain embodiments may be practiced without one or more of these specific details, or in combination with other known methods and materials. In the following description, numerous specific details are set forth, such as specific materials, dimensions and processes, etc., in order to provide a thorough understanding of the present invention. In other instances, well-known semiconductor processes and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention. Reference throughout this specification to "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

[0024] In a first aspect, embodiments of the present invention reduce the dislocations within a III-V device layer formed over a silicon substrate to near bulk-like quality by utilizing a buffer architecture and specific fabrication techniques tailored to the particular III-V device layer desired. As shown in FIG. **2**A, embodiments of the present invention utilize a composite buffer **275** formed between silicon substrate **210** and III-V device layer **280** to form a semiconductor stack **200**. Specific embodiments utilize a composite buffer **275** of a first III-V semiconductor material, layer **240**, and a second III-V semiconductor material, layer **270**. In embodiments of the present invention, the composite buffer **275** architecture is engineered for a particular III-V device layer material **280** with the materials for the first III-V buffer layer **240** and second III-v buffer layer **270** selected with consideration of lattice constant, band gap and melting point for the purpose of controlling nucleation and propagation of defects generated by lattice mismatch strain.

[0025] In a second aspect embodiments of the present invention provide a structure and method for reducing segregation and desorption of dopants in a quantum well structure. The quantum well structure may be formed on any known available substrate. In one embodiment, a III-V quantum well structure is disposed above a GaAs substrate. In still other embodiments a III-V quantum well structure is disposed above a Si substrate utilizing a composite buffer architecture.

[0026] As shown in FIG. **2**B, in specific embodiments, device layer **280** is quantum well structure **280** comprised of a lower barrier layer **281**, a quantum well layer **283**, and upper barrier layer **285**. As shown in FIG. **2**C, in specific embodiments, upper barrier layer **285** may further comprise spacer layer **286**, dopant segregation barrier layer **289**, delta doped layer **287**, and top barrier layer **288**. Inclusion of the dopant segregation barrier layer **289** provides several advantages. One advantage the dopant segregation barrier layer **289** serves is to improve confinement of the delta dopant in the subsequently deposited delta doped layer **287**. Thus, less delta dopant segregates to the surface of the upper barrier layer **285**, and as a result the delta doped layer **287** may better contribute carriers to the quantum well layer **283**. These advantages lead to several applications. For example, improved dopant confinement may allow for a reduced top barrier layer **288** thickness, which is useful in enhancement mode devices where it is desirable to position the gate close the quantum well layer. Reduced top barrier layer **288** thickness can also lead to reduced power consumption for the device.

[0027] In particular embodiments, the first III-V buffer layer **240** is formed on a vicinal surface of silicon substrate **210** having regular arrays of double-stepped (100) terraces across the substrate surface. A vicinal surface is a higher order crystal plane of the silicon substrate, such as, but not limited to the (211), (511), (013), (711) planes. A vicinal substrate surface having double-stepped terraces is capable of suppressing anti-phase domains (APD) in the first III-V buffer layer **240**. An APP is created when a first polar crystal domain of layer **240**, having group III atoms attached to the nonpolar silicon substrate surface, meets a second polar crystal domain of layer **240**, having group V atoms attaches to the silicon substrate. A crystal discontinuity forms in layer **240** at the border between these first and second domains providing recombination-generation centers detrimental to the operation of a semiconductor device. The term "polar" refers to the partially ionic bonding character between the constituents of a III-V compound semiconductor.

[0028] Embodiments providing the double atomic step in the silicon substrate **210** provide for a terrace level of sufficient depth to prevent the growth species of buffer layer **24** from bonding to a higher level terrace even after all binding sites in the lowest terrace are occupied. Thus, the double step terrace prevents ad-hoc surface bonding so that the growth of the first III-V buffer layer **240** proceeds in a stepwise fashion with each polar group III-V atomic bi-layer sequentially filling the lowest terrace of the nonpolar group IV, silicon substrate. In alternative embodiments, anti-phase domains are eliminated by growing layer **240** to a thickness greater than approximately 1.5 um. At such thicknesses, anti-phase domains are substantially annihilated and a single domain film can be formed even on first order planes, such as, but not limited to, the (100) silicon substrates commonly used for microelectronic fabrication.

[0029] In embodiments of the present invention, the total lattice mismatch between the silicon substrate and the III-V device layer is partitioned by the two III-V buffer layers, **240** and **270** comprising the composite buffer **275**. Partitioning of the total lattice mismatch into three material interfaces pro-

vides an additional degree of freedom to incrementally control and direct the generation and propagation of the defects unavoidably formed by heteroepitaxy of materials having significantly different lattice constants. To partition the total lattice mismatch, each material layer within the composite buffer **275** possesses a lattice constant intermediate between the silicon substrate **210** and the desired III-V semiconductor device layer **280**. Proper partitioning of the total lattice mismatch avoids too large of a lattice mismatch between adjacent materials. In a particular embodiment, the lattice constant of each material layer within the composite buffer **275** is intermediate between the layer upon which that layer is grown and the layer subsequently grown upon that layer. Thus, in a particular embodiment, the first III-V buffer layer **240** has a lattice spacing larger than the silicon substrate **210**, the second III-V buffer layer **270** has a lattice spacing larger than the first III-V buffer layer **240** and the III-V device layer **280** has a lattice spacing larger than the second III-V buffer layer **270**. In one such an embodiment, composite buffer **275** is comprised of a gallium antimonide (GaSb) layer **240** and an aluminum antimonide (AlSb) layer **270** formed between the silicon substrate **210** and an indium antimonide (InSb) device layer **280**. The 6.09 Å lattice constant of GaSb layer **240** is approximately 12.2% larger than the 5.43% lattice constant of the Silicon substrate **210** upon which layer **240** is formed. The 6.13 Å lattice constant of AlSb layer **270** is then approximately 0.65% larger than the GaSb layer **240**. Finally, the 6.48 Å lattice constant of the InSb layer **280** is approximately 5.6% larger than the AlSb layer **270**. Thus, in this particular embodiment, the lattice constant of the materials comprising the composite buffer **275** is gradually incremented from the lattice spacing of the silicon substrate **210** to the lattice spacing of the III-V device layer **280**, thereby partitioning the total lattice mismatch between three separate material interfaces. In this manner, the InSb device layer **280** need only accommodate the strain of a 5.6% lattice mismatch with AlSb layer **270** rather than the entire 19.2% mismatch with the silicon substrate **210**.

[0030] It should be appreciated that various III-V device layers, such as, but not limited to, indium arsenide (InAs) device layers may be similarly integrated with silicon substrates using other composite buffer embodiments. For example in another embodiment of the present invention, buffer **275** is comprised of a gallium arsenide (GaAs) slayer **240** and aluminum arsenide (AlAs) layer **270** is formed between the silicon substrate **210** and indium arsenide (InAs) device layer **280** to graduate the lattice constant between the layers **240** and **270** of the composite buffer **275** in a manner analogous to that just described for the InSb embodiment.

[0031] In embodiments of the present invention, the composite buffer **275** comprises materials which glide dislocations and terminate a significant percentage of the dislocations within the buffer layer **275**. In particular embodiments, the first III-V buffer layer **240** is comprised of a relatively narrow band gap III-V semiconductor material. Generally, the extent of dislocation glide is dependent on the hardness of the material, with glide occurring more readily in softer materials. Semiconductor materials of narrower band gap are typically softer and it has been found more dislocation glide occurs in narrower band gap materials. Furthermore, more of the dislocations are terminated or contained as the thickness of a material capable of dislocation glides is increased. In one particular embodiment, the first III-V buffer layer **240** is GaSb having a thickness between approximately 0.3 um and 5.0 um. GaSb readily glides defects because the band gap of GaSb is relatively narrow, approximately 0.7 eV. Dislocation glide occurring within the GaSb changes the direction a defect propagates. This is particularly true for threading dislocations which typically propagate at an approximate sixty degree angle from the substrate surface. Gliding can change the direction of a threading dislocation to an angle more parallel to the surface of the film to terminate or contain the dislocations within the film as the buffer layer is thickened. For this reason, many of the defects induced by the strain of the 12.2% lattice mismatch between the silicon substrate **210** and a first III-V buffer layer **240** of GaSb are glided and contained within the GaSb layer **240**. Because many such glided dislocations will not propagate into subsequently grown films, it is therefore possible to avoid simply accumulating defects within the subsequent epitaxial layers. Thus, embodiments utilizing a III-V buffer layer comprising at least one relatively narrow band gap III-V buffer material are capable of incrementing the lattice spacing without propagating the defects generated by the lattice spacing increment. In this manner, the lattice mismatch between the silicon substrate **210** and the first III-V buffer layer **240** can be partitioned by the buffer layers without accumulating the associated defects.

[0032] In a further embodiment, the III-V buffer layer with the greatest ability to glide dislocations accommodates the largest portion of the total lattice mismatch between the silicon substrate **210** and the III-V device layer **280**. In one such embodiment, the composite buffer **275** comprises a first III-V buffer layer of GaSb and a second III-V buffer layer of AlSb. As previously discussed, the 6.09 Å lattice constant of GaSb layer **240** is approximately 12.2% larger than the 5.43 Å lattice constant of the silicon substrate **210** upon which layer **240** is formed. The 6.13 Å lattice constant of AlSb layer **270** is then approximately 0.65% larger than the GaSb layer **240**. Because the band gaps of GaSb and AlSb are approximately 0.7 eV and 1.7 eV, respectively, the GaSb layer **240** is relatively softer and able to glide more dislocations than AlSb. Although the larger band gap AlSb has relatively less glide capability than GaSb, relatively fewer defects are introduced into the AlSb by the smaller strain from the 0.65% lattice mismatch between the GaSb layer **240** and AlSb layer **270**. This is therefore another advantage the composite buffer **275** offers over a buffer comprised of a single layer of a material such as AlSb.

[0033] The interaction between the amount of lattice mismatch between two adjacent materials and the ability for a material to glide the ensuing dislocations is an important consideration of the design of composite buffer layer **275**. For example, in an embodiment of the present invention utilizing GaAs for the first III-V buffer layer **240** and AlAs for the second III-V buffer layer **270**, the relatively lower band gap of GaAs provides better gliding and lower defects than the wider band gap AlAs. For this reason, even though GaAs and AlAs have nearly the same lattice mismatch with the silicon substrate **210**, a composite buffer of GaAs and AlAs will propagate fewer defects into a subsequently grown device layer than a buffer comprised of AlAs alone due to the lattice mismatch partitioning and the relatively better gliding ability of GaAs. In the same vein, it should be apparent that an embodiment utilizing GaSb provides better dislocation glide characteristics than an embodiment utilizing GaAs for the first III-V buffer layer **240** because the band gap of GaSb is lower than GaAs.

[0034] In embodiments of the present invention, the first III-V buffer layer **240** has a lower melting point than the second III-V buffer layer **270**. The lower melting point temperature of the first III-V buffer layer **240** improves the thermal activation of dislocation glide within layer **240** during the subsequent growth of the second III-V buffer layer **270**. A composite buffer architecture wherein the first III-V buffer layer **240** has a melting point that is lower than the melting point of the second III-V buffer layer **270** reduces the propagation of threading dislocations, stacking faults and twins into the second buffer layer **270**. In a particular embodiment, for example, a first III-V buffer layer **240** of GaSb has a melting point of approximately 712 C and a second III-V buffer layer **270** of AlSb has a melting point of approximately 1060 C. In another particular embodiment, the melting point of a GaAs layer **240** is approximately 1237 C while the melting point of an AlAs layer **270** is approximately 1740 C. Generally, the lower the melting point of the material, the better the dislocation glide. As shown by these two exemplary embodiments, the relatively high melting points of aluminum containing compound semiconductor materials making them useful for the second III-V buffer layer **270** because the high temperature epitaxial growth process increases the thermally activated dislocation gliding in buffer layer **240**, which is discussed in greater detail below.

[0035] In embodiments of the present invention, the composite buffer **275** provides a highly resistive buffer layer over which the III-V device layer **280** can be fabricated. Generally, semiconductor resistivity depends directly on the band gap of a material, with wider band gap materials having higher resistivity. If the band gap is greater than approximately 1.4 eV, the semiconductor is commonly referred to as "semi-insulating" or "isolative" because the resistivity of the material is very high, on the order of approximately 1×10^7 ohm-cm. GaAs and indium phosphide (InP) are two examples. Thus, while dislocation glide improves with smaller band gap, electrical resistivity improves with larger band gap. However in embodiments of the present invention, both dislocation glide and isolation can be achieved with the composite buffer **275**.

[0036] In particular embodiments, the composite buffer **275** includes a wide band gap buffer layer having a thickness ranging from approximately 0.2 um to many microns. Specifically, in one embodiment a second III-V buffer layer **270** comprising AlSb having a thickness between approximately 0.2 um and 5.0 um provides high resistivity for excellent device isolation and low capacitance. Similarly, for a GaAs/AlAs composite buffer embodiment, the second III-V buffer layer **270** comprising AlAs is semi-insulating or highly resistive. In an alternate embodiment the second III-V buffer layer **270** can be formed of an aluminum gallium antimonide alloy ($Al_xGa_{1-x}Sb$), wherein the Al content ranges from 0.1 to 1.0. In one such embodiment, the second III-V buffer layer **270** contains sufficient aluminum for the band gap to be at least approximately 1.4 eV and therefore semi-insulating. In a specific embodiment, the aluminum (Al) faction, x, is between 0.3 and 0.6. This $Al_xGa_{1-x}Sb$ alloy may be a compositionally graded from GaSb to AlSb using either linear or step-graded compositions of Al. For example, the second III-V buffer layer can be graded from 0% Al at the interface of the first III-V buffer layer **240** to 60% Al at the interface of the III-V device layer **280**. Optionally, the grading can be continued to 100%, Al (AlSb) in the second III-V buffer layer. In still other embodiments, composite buffer layer **275** provides device isolation by doping at least one of the buffer layers **240** or **270** to a conductivity type that is complementary to the conductivity type of the devices formed in the III-V device layer **280**. Such complementary duping provides junction isolation, as commonly known in the art. In one such embodiment, buffer layer **270** is p-type and device layer **280** comprises an n-type quantum well (QW) transistor.

[0037] In particular embodiments, the composite buffer **275** architecture achieves a device layer having an acceptably low final defect density. Shown in FIG. **3**A is the dependency of Hall electron mobility of InSb formed on various substrates as a function of the InSb defect density. FIG. **3**A indicates the InSb device layer defect density must be below 1×10^8 cm^{-2} to approach the bulk InSb mobility of approximately 76,000 cm^2/Vs. Data point **301** represents an experimental measurement of a particular embodiment of the present invention wherein the composite buffer **275** of FIG. **2**A is comprised of a GaSb layer **240** and an AlSb layer **270** between a silicon substrate **210** and InSb layer **280**. For such embodiments, the composite buffer **275** accommodates the approximate 19% lattice mismatch between InSb device layer **280** and silicon substrate **210** to obtain a device layer having a defect density of approximately 4×10^7 cm^{-2}.

[0038] In embodiments of the present invention, the III-V device layer **280** of FIG. **2**A is of the desired material and of a sufficient thickness to achieve low defect density. Because the lattice spacing of the III-V device layer **280** is considered in the design of the composite buffer **275**, the III-V device layer **280** has significantly less lattice mismatch relative to the composite buffer **275** than to the silicon substrate **210**. A substantial portion of the defects in device layer **280** generated by lattice mismatch strain or propagated from the composite buffer **275** are glided within III-V device layer **280** as the thickness of **280** is increased. Thus, as shown in FIG. **3**B, thicker device layers display superior Hall electron mobility. In a particular embodiment of the present invention incorporating a GaSb/AlSb composite buffer **275**, an InSb device layer **280** less than 2.5 um thick displays a Hall-measured electron mobility of approximately 55,000-60,000 cm^2/Vs. In another particular embodiment of the present invention incorporating a GaSb/AlSb composite buffer **275**, an InSb device layer **280** at least 7.5 um thick displays a Hall-measured electron mobility of approximately 70,000 cm^2/Vs. Thus, the present embodiments provide for device-grade InSb on silicon substrates enabling electronic structures such as quantum well transistors to be formed on silicon substrates.

[0039] As shown in FIG. **2**B, in an embodiment of the present invention, the III-V device layer **280** is a quantum well structure **280** comprised of a lower barrier layer **281**, a quantum well layer **283**, and upper barrier layer **285**. In particular embodiments, the lower barrier layer **281** and upper barrier layer **285** are comprised of a material having a wider band gap than the quantum well layer **283**, thereby confining a majority of charge carriers within the quantum well layer **283** for reduced device leakage. Specifically, in one embodiment, the barrier layers **281** and **285** are comprised of aluminum indium antimonide, $Al_xIn_{1-x}Sb$, where x is between approximately 0.1 and 1.0, and the quantum well layer **283** is comprised of InSb. In certain embodiments, the quantum well layer **283** is strained. In one embodiment, the barriers layers **281** and **285** have the same composition. In another embodiment upper barrier layer **285** has a wider band gap than lower barrier layer **281**. In yet another embodiment, the barrier layers **281** and **285** may be graded.

[0040] As shown in FIG. **2**C, in an embodiment of the present invention, the III-V device layer **280** is a quantum well structure **280** comprised of a lower barrier **281**, a quantum well layer **283**, and upper barrier **285**. Upper barrier **285** may be a composite structure further comprising spacer layer **286**, dopant segregation barrier layer **289**, delta doped layer **287**, and top barrier layer **288**. In an embodiment, spacer layer **286** and top barrier layer **288** are comprised of a material having a wider band gap than the quantum well layer **283**, thereby confining a majority of charge carriers within the quantum well layer **283** for reduced device leakage. Specifically, in one embodiment, spacer layer **286** and top barrier layer **288** are comprised of aluminum indium antimonide $Al_xIn_{1-x}Sb$, where x is between approximately 0.1 and 1.0, In one embodiment, spacer layer **286** and top barrier layer **288** have the same composition. In another embodiment, spacer layer **286** and top barrier layer **288** may be graded.

[0041] Inclusion of the dopant segregation barrier layer **289** provides several advantages. One advantage the dopant segregation barrier layer **289** provides is to improve confinement of the delta dopant in the delta doped layer **287**. Thus, less delta dopant segregates to the surface of the upper barrier layer **285**, and as a result the delta doped layer **287** may better contribute carriers to the quantum well layer **283**. These advantages lead to several applications. For example, improved dopant confinement may allow for reduced top barrier layer **288** thickness, which is useful in enhancement mode devices where it is desirable to position the gate close to the quantum well layer. Reduced top barrier layer **288** thickness can also lead to reduced power consumption for the device.

[0042] In one embodiment, quantum well structure **280** is n-type. In such an embodiment, dopant segregation barrier layer **289** may be comprised of, but is not limited to, a group III element. For example, dopant segregation barrier layer **289** may be an indium (In) layer. In an embodiment dopant segregation barrier layer **289** is less than 10 Å thick. In an embodiment, delta doped layer **287** may be comprised of a group VI element. For example, delta doped layer **287** may be tellurium (Te). For example, delta doped layer **287** may also be a tellurium antimonide (TeSb) layer. In an embodiment delta doped layer **287** is less than 30 Å thick.

[0043] In one embodiment, quantum well structure **280** is p-type. In such an embodiment, dopant segregation barrier layer **289** may be comprised of, but is not limited to, a group V element. For example, dopant segregation barrier layer **289** may be an antimonide (Sb) layer. In an embodiment dopant segregation barrier layer **289** is less than 10 Å thick. In an embodiment, delta doped layer **287** may be, but is not limited to, a beryllium (Be) or zinc (Zn) layer. In an embodiment delta doped layer **287** is less than 30 Å thick.

[0044] Top barrier layer **288** may be formed to a thickness depending on whether a depletion mode or enhancement mode device is desired. In one embodiment, where an enhancement mode is desired, top barrier layer **288** is formed to 50 Å thickness or less. In an alternative embodiment, top barrier layer **288** may be formed to a thickness of 500 Å where a depletion mode device is desired.

[0045] It is to be appreciated that some embodiments of the invention provide a dopant segregation barrier latter **289** to reduce out diffusion and segregation of the delta dopant to the surface of top barrier layer **288**. For enhancement mode devices in particular, it may be preferred to retain a peak dopant concentration in the delta doped layer of at least approximately 1.0×10^{18} (atoms/cm3). FIG. **3**C provides secondary ion mass spectroscopy (SIMS) data of a Te-doped InSb quantum well structure without a segregation barrier layer in accordance with embodiments of this invention. As shown, quantum well layer **283** is approximately 200 Å thick and the composite upper barrier **285** is approximately 500 Å thick, including a spacer layer **286** approximately 70 Å thick and delta doped layer **587** less than approximately 30 Å thick. As shown in FIG. **3**C, the maximum delta dopant concentration is below 6.0×10^{17} (atoms/cm3), well below the preferred peak concentration of at least approximately 1.0×10^{18} (atoms/cm3).

[0046] FIG. **3**D provides a SIMS profile similar to the structure of FIG. **3**C, except the quantum well structure of FIG. **3**D includes a dopant segregation barrier layer **289** in accordance with embodiments of this invention. As shown, quantum well layer **283** is approximately 200 Å thick and the composite upper barrier **285** is approximately 500 Å thick, including a spacer layer **286** approximately 70 Å thick, a dopant segregation barrier layer **289** less than approximately 10 Å thick, and a delta doped layer **587** less than approximately 30 Å thick. As shown in FIG. **3**D the maximum delta dopant concentration is above 1.0×10^{18} (atoms/cm3). As a result of the dopant segregation barrier layer, the maximum delta dopant concentration is improved, and less dopant out diffuses to the surface of top barrier **288**.

[0047] FIG. **3**E provides a SIMS profile for Te concentration inside a top barrier layer in accordance with embodiments of this invention. As shown, when a dopant segregation barrier layer is used, there is a 3.5 times reduction of Te surface segregation compared with a quantum well without using a dopant segregation barrier layer. As shown in FIG. **3**E, reduction in surface segregation is correlated to an improvement in peak dopant concentration.

[0048] Reduced dopant surface segregation results in several benefits. For example, the top barrier layer **288** may be grown to a reduced thickness or etched back to a reduced thickness for application in an enhancement mode device. In a specific embodiment, the top barrier layer **288** is etched back to a thickness of approximately 50 Å or less. As shown in FIG. **3**D, the resulting structure would result in a dopant concentration less than approximately 6.0×10^{17} (atoms/cm3) at the surface of top barrier layer **288** while retaining a peak dopant concentration greater than 1.0×10^{18} (atoms/cm3). Alternatively, a similar device may be grown by simply growing top barrier **288** to approximately 50 Å thick or less rather than growth and etch-back.

[0049] It is to be appreciated that although embodiments of the invention describe a quantum well structure grown above a silicon substrate, quantum well structures grown above other substrates such as, but not limited to, GaAs are also within the scope of the invention. For example, in another embodiment of the present invention, quantum well layer **283** may be formed above a GaAs substrate **210**, and buffer **275**, comprised of aluminum indium antimonide ($Al_xIn_{1-x}Sb$), is used to graduate the lattice constant between the GaAs substrate **210** and quantum well structure **280**.

[0050] FIG. **6** is a flow diagram of a method to fabricate a III-V device layer in accordance with an embodiment of the present invention. Method **600** of FIG. **6** begins with an offcut silicon substrate at step **601**. At step **602**, a nucleation layer is formed as the initial step of a two step process to form a first buffer layer. At step **603**, the first buffer layer is thickened with a growth process distinct from that used at step **602**. In

step **604**, a transition layer is formed as the initial step of a two step process to form a second buffer layer upon the first buffer layer. Ten, at step **605**, the second buffer layer is thickened with a growth process distinct from that used at step **604**. In step **606**, a lower barrier layer is formed over the composite buffer. Then, at step **607** a quantum well layer is formed over the barrier layer. At step **608**, an upper barrier layer is formed over the quantum well layer. The upper barrier layer may optionally be doped. For example, the upper barrier layer may be a composite upper barrier layer including a spacer layer, dopant segregation barrier layer, delta doped layer, and top barrier layer. Then, at step **609** a device is fabricated in the quantum well layer. Each of these steps is discussed in greater detail below in reference to FIGS. **4**A-**5**E.

[0051] In one embodiment, fabrication begins with silicon substrate **410**. In a particular embodiment, substrate **410** has a vicinal surface, as shown in FIG. **4**A. A vicinal surface is prepared by off-cutting the substrate from an ingot. In one such embodiment, the ingot is grown to provide wafer slices having (100) surfaces. The (100) substrate surface is then offcut at an angle between 2 and 12 degrees towards the [110] direction to produce a surface having terraces **412**. Terraces **412** include a surface having a (100) crystal plane. The (100) plane surface area of each terrace **412** depends on the specific offcut angle, with a greater angle producing a greater number of terraces, each terrace having lesser (100) surface area. In such embodiments, the offcut produces a vicinal surface having an array of (100) terraces, many of which are separated by a double atomic step. As shown in the expanded view of FIG. **4**A, a double step terrace has a height of two silicon atoms **411**. In another embodiment, the silicon substrate offcut orientations are (211), (511), (013), (711) and other high index plans. Optionally, silicon substrate **410** is without an offcut (zero degree offcut), such as, but not limited to, common (100) substrates. Such a substrate (not pictured) typically does not have a substantial number of double atomic step terraces.

[0052] Next, the first III-V buffer layer is formed upon the silicon substrate **410**. Commonly known growth techniques may be used to form the III-V buffer layers, such as, but not limited to, metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). As previously discussed, in particular embodiments, the buffer is formed in a manner that either avoids the formation of anti-phase domains (APD) or annihilates them as the film thickness is increased.

[0053] In a particular embodiment, as shown in FIG. **4**B and FIG. **4**C, the first III-V buffer layer is formed using a two step process, wherein the growth conditions of each step are distinct. In the first step, as shown in FIG. **4**B, a nucleation layer **420** is formed. The growth of nucleation layer **420** as shown in the expanded view, successively fills the lowest silicon substrate terraces with atomic bi-layers of the III-V semiconductor buffer material. In this embodiment, the mobility of both the group III and group V species of the nucleation layer **420** are sufficiently high that the atomic species introduced to the silicon surface travel about the surface of silicon substrate **410** and either fall into a terrace or completely off the silicon substrate surface. A species which falls down a terrace wall lacks the energy to scale back up the terrace wall, therefore the otherwise substantially random species motion can be effectively funneled in a direction dictated by the substrate terracing. Once the species reaches the lowest terrace, the silicon substrate bonding sites are located by the mobile species until every site is filled. Because of the double atomic step in the silicon substrate **410**, a terrace completely filled with species **421** presents a single atomic step which the mobile species is unable to scale, and so excess species travel off the substrate surface without a significant number bonding to sites in the upper terrace levels. Subsequent introduction of the second species of the polar atomic pair is similarly funneled to the lowest terrace to bond with the first atomic species **421** to completely fill the lowest terrace with species **422**. The growth process then proceeds in this iterative fashion until all terraces are filled and no non-polar silicon substrate surface remains, at which point there is no longer risk of forming an APD in the polar buffer materials. Thus, depending on the offcut angle of the substrate, the number of terraces which must be successively filled varies. As the offcut angle increases, the number of terrace levels increases and the thickness of the nucleation layer must be increased to fill every terrace. In particular embodiments, therefore the nucleation layer **420** is between approximately 30 Å and approximately 500 Å.

[0054] The high mobility required to ensure the terraces are successively filled is provided for by the growth parameters of the nucleation layer **420** and these parameters therefore depend on the particular mobility characteristics of species comprising the material of layer **420**. For example, in one embodiment, a nucleation layer **420** is formed using migration enhanced epitaxy (MEL) at a temperature of between 300 C and 600 C. MEE proceeds in a fashion similar to that of atomic layer deposition (ALD). MEE has a relatively slower growth rate, approximately 0.1 um/hr, because once the group V element is introduced to the substrate there is a hold time during which both the group V source and group III source shutters are closed (shuttered). This hold time accommodates the relatively lower mobility of the group V species. No hold time is required for group III species because surface migration of this species relatively higher mobility. In a particular MEE embodiment, the substrate surface is exposed to an antimony (Sb) source for approximately 10 seconds to form a monolayer of Sb on the lowest terrace level. The Sb source and is then shuttered for a hold time of approximately 60 seconds. This relatively long hold time allows for the Sb species to migrate on the surface of the silicon substrate to ensure the bonding sites of the lowest terrace level are filled. Then, the substrate surface is exposed to a gallium (Ga) source for approximately 10 seconds. No hold time is required because of the high surface mobility of Ca. Next the Sb is reopened for approximately 10 second and then again closed or a hold time. This process is repeated to form a GaSb nucleation layer **420** sufficiently thick to fill all the terraces of the silicon substrate **410**, approximately 150 Å in a particular embodiment. In an embodiment, GaSb nucleation temperatures are in between 300 C and 600 C. In particular GaSb embodiment, the MEE growth temperature is between approximately 400 C and approximately 510 C. Higher temperature embodiments enable a higher quality film. In other embodiments, MEE can be utilized to form a nucleation layer of an alternate buffer material, such as, but not limited to GaAs.

[0055] In yet another embodiment a nucleation layer **420** is formed on the vicinal silicon substrate **410** utilizing traditional MBE (without migration enhancement). The relatively higher flux of this particular embodiment using traditional MBE provides higher film growth rates and therefore higher throughput than MEE embodiments. In a particular MBE

nucleation embodiment, GaSb is formed on the silicon substrate **410** at a temperature between approximately 400 C and approximately 510 C. The high-flux embodiments are well suited to GaSb because of the relatively low vapor pressure and high sticking coefficient of antimony (Sb) as compared to arsenic (As) of GaAs films.

[0056] Next, as shown in FIG. **4**C, a second growth step completes the formation of the first III-V buffer layer **440**. This second growth step, performed at a higher temperature than that used for the nucleation layer **420**, forms layer **430** to thicken the first III-V buffer layer **440** and glide dislocations. The film quality of layer **430** is superior to that of the nucleation layer **420** because it is formed at a higher growth temperature. Also, during the formation of layer **430**, the flux rate can be relatively high because the polar nucleation layer **420** eliminates any danger of APD formation. In an embodiment, a GaSb film **430** is grown upon a GaSb nucleation layer **420** at a growth temperature in the range of 500 C and 700 C. In a particular embodiment, a GaSb film **430** is grown upon a GaSb nucleation layer **420** at a growth temperature between approximately 510 C and approximately 570 C. In embodiments of the present invention, the GaSb film **430** is grown to a thickness between approximately 0.3 um and 5.0 um. In an alternate embodiment, a GaAs film **430** is grown in a similar fashion upon a GaAs nucleation layer **420**.

[0057] In still another embodiment, the first III-V buffer layer **440** is formed on a traditional silicon substrate **410** having a lower order plane surface, such as, but not limited to (100). The first III-V buffer layer is grown without a nucleation step and permitted to formed anti-phase domains. In an embodiment the single-step growth is performed at a temperature between 500 C and 700 C. Once the film thickness is greater than approximately 1.5 um, the anti-phase domains are substantially annihilated and the film becomes single-domain. In a particular embodiment, a first III-V buffer layer **440** comprising between approximately 1.5 and 2.0 um GaSb is formed on a traditional (**100**) silicon substrate **410** that has a 0 degree offcut.

[0058] Following the completion of the first III-V buffer layer **440**, a second III-V buffer layer **470** is formed. In particular embodiments, a two step growth process is utilized for form the second III-V buffer layer **470** wherein the growth conditions of each step are distinct. As shown in FIG. **4**D, the first growth step forms a transition layer **460** upon the first III-V buffer layer **440**. Transition layer **460** should be of sufficient thickness to prevent out migration of species from the first III-V buffer layer **440** during the growth of the isolative buffer material. In particular embodiments the thickness of the transition layer **460** is between approximately 0.05 um and 0.25 um. Out migration from the first III-V buffer layer **440** is a concern, especially for the high vapor pressure group V species, because, in certain embodiments, the isolative buffer material is grown at a higher temperature than the growth temperature of the first III-V buffer layer **440**. To prevent out migration of the first III-V buffer layer **440** during formation of the transition layer **460**, the growth temperature of transition layer **460** is no higher than the highest growth temperature of the III-V buffer layer **440**. In an embodiment AlSb transition layer **460** is be grown at the same growth temperature of GaSb layer **430**. For example, in a specific embodiment wherein a GaSb layer **430** is grown at approximately 510 C, an AlSb transition layer **460** is also grown at approximately 510 C to a thickness between 0.05 um and 0.2 um.

[0059] In particular embodiments, as shown in FIG. **4**E, the second III-V buffer layer **470** is formed at temperature significantly higher than the highest growth temperature of the first III-V buffer layer **440**. The higher growth temperature step forming layer **465** is limited by the melting point of the first III-V buffer layer **440**. A high growth temperature serves two purposes. First wide band gap semiconductors typically require relatively high temperatures to form high quality isolative films. For example, aluminum has relatively poor mobility and so aluminum containing films require a relatively higher deposition temperature to form films with a smooth surface. Second, the relatively higher growth temperature of layer **463** thermally activates dislocation guide within the first III-V buffer layer **440** to minimize the propagation of threading dislocations into the subsequently grown films. Thus, the high temperature growth step of the second III-V buffer layer **470** anneals the first III-V buffer layer **440**. In a further embodiment, an AlSb layer **465** is grown at a temperature between approximately 510 C and approximately 570 C upon an AlSb transition layer **460** over a GaSb buffer layer **440**. The thickness of the layer **465** depends on the resistivity desired. In particular embodiments, the thickness of layer **465** is between approximately 0.2 um and 5.0 um. In a specific embodiment, an AlSb layer **465** is grown to approximately 1 um thick. In an alternative embodiment a thin AlSb layer **465** is grown to approximately 0.3 um thick in order to prevent origination of new defects such as twins and stacking faults. In another embodiment, a percentage of gallium (Ga) is included to form an $Al_xGa_{1-x}Sb$ buffer layer **465**. In this embodiment, commonly known methods are used to incorporate between approximately 30% to approximately 60% aluminum (Al) so that the band gap of layer **465** is above approximately 1.4 eV. In certain embodiments, the second III-V buffer layer **470** comprising transition layer **460** and layer **465** may be step graded from the composition of the GaSb first III-V buffer layer until the desired band gap is reached or to the full band gap of AlSb. In such an embodiment, the composition of transition layer **460** can be integrated with the grading of layer **465** to form the graded second III-V buffer layer **470**. In vet another embodiment, the second III-V buffer layer **470** can be in-situ doped to provide for junction isolation between the second III-V buffer layer **470** and a subsequently formed device layer. In such embodiments, either or both layers **460** and **465** of the second III-V buffer layer **470** may be doped. In a particular embodiment, the entire second III-V buffer layer **470** is doped p-type.

[0060] The interaction between the growth of the first III-V buffer layer **440** and the growth of second III-V buffer layer **470** is a further consideration in the architecture of the composite buffer. For example, in one embodiment, both the first III-V buffer layer **440** and second III-V buffer layer **470** are formed successively without breaking vacuum (in-situ). In a particular embodiment, an AlSb buffer layer **470** is grown in-situ upon a GaSb layer **440**. While there is no detrimental interaction between a GaSb buffer layer **440** and an in-situ grown AlSb buffer layer **470**, because the vapor pressure of antimony (Sb) is less than that of arsenic (As), an in-situ growth of an AlSb buffer layer **470** over a GaAs buffer layer **440** can result in a detrimental incorporation of As from the chamber walls of the epitaxial reactor into an in-situ grown AlSb buffer layer **470**. Thus, the architecture of the composite buffer must consider the impact that growth of first III-V buffer layer **440** will have on the film quality of the second III-V buffer layer **470**.

[0061] Finally, with the completion of the composite buffer **475**, device layer **480** is formed, as shown in FIG. **4**F. Device layer **480** is grown at a temperature appropriate for the particular III-V material desired. In a particular embodiment, wherein composite buffer **4175** comprises a GaSb buffer layer **440** and AlSb buffer layer **470**, an InSb device layer **480** is formed at a growth temperature between approximately 350 C and approximately 475 C. Depending on the amount of lattice mismatch between the composite buffer **475** and the III-V device layer **480**, as well as the ability for the device layer to glide dislocations, the device layer **480** is grown to a thickness sufficient to give an acceptable defect density. In a particular embodiment, an InSb device layer **480** is grown to a thickness greater than approximately 2 um. In a further embodiment, an InSb device layer **480** is grown to a thickness of approximately 8 um to achieve a defect density of approximately 4×10^{7} cm^{-2}, referring back to FIG. **3**A and FIG. **3**B.

[0062] FIGS. **5**A-**5**E depict embodiments of methods to fabricate a quantum well transistor in a III-V device layer on a substrate incorporating embodiments of the III-V buffer architecture discussed. FIG. **5**A shows device layer **580** comprising a quantum well **583** between an upper barrier layer **585** and a lower barrier layer **581** formed upon the composite buffer **575** over silicon substrate **510**.

[0063] Generally, the lower barrier layer **581** is formed of a higher band gap material than the overlying quantum well **583**. The lower barrier layer **581** is of sufficient thickness to provide a potential barrier to charge carriers in the transistor channel. In one embodiment, the lower barrier layer thickness is between about 100 Å and about 250 Å. In other embodiments, the lower barrier is InAlSb between 2 um and 5 um thick. In still other embodiments, lower barrier layer **581** is microns thick to further reduce defect density in the quantum well **583**. The lower barrier **581** may also be fully relaxed. In certain embodiments wherein the buffer **575** is comprised of a GaSb buffer layer **540** and AlSb buffer layer **570**, the lower barrier layer **581** is comprised of aluminum indium antimonide ($Al_xIn_{1-x}Sb$). In some embodiments the lower barrier layer **581** comprises between about 10% and 100% aluminum, ($Al_xIn_{1-x}Sb$, with x=0.1-1.0). In a particular embodiment, the lower barrier layer **581** is $Al_xIn_{1-x}Sb$ with 15% aluminum ($Al_{0.15}In_{0.85}Sb$).

[0064] In some embodiments, the $Al_xIn_{1-x}Sb$ lower barrier layer **581** is grown between approximately 415 C and 445 C. In general, the higher aluminum concentration, the higher the growth temperature. In a specific embodiment, a lower barrier layer **581** with 15% aluminum ($Al_{0.15}In_{0.85}Sb$) is grown at 415 C.

[0065] Additionally, the lower barrier **581** may be graded. In one embodiment, the lower barrier **581** is linearly graded from x=1.0 (AlSb) at the interface with the buffer layer **570** to x=0 (InSb) at the interface with the quantum well layer **583**. In such an embodiment, the graded lower barrier layer **581** and subsequently grown InSb quantum well layer **583** are lattice matched at their interface, and the graded lower barrier layer **581** does not induce strain into the InSb quantum well layer **583**.

[0066] In another embodiment, the lower barrier **581** is linearly graded from x=1.0 (AlSb) at the interface with the buffer layer **570** to x=0.1 ($Al_{0.1}In_{0.9}Sb$) at the interface with the quantum well layer **583**. In such an embodiment, the lower barrier **581** induces strain in the subsequently grown quantum well layer **583**. In some embodiments the lower barrier layer **581** is graded at a rate of less than 25% Al/um. In one embodiment, the lower barrier layer **581** is graded at a rate of 5% Al/um. Alternatively, the lower barrier **581** may be step graded using a series of layers with decreasing aluminum concentration. In one embodiment, the lower barrier **581** is step graded in a series of decreasing 5% (x=0.05) aluminum increments. In certain other embodiments, wherein the composite buffer **575** comprises GaAs buffer layer **540** and AlAs buffer layer **570**, the lower barrier layer **581** is comprised of indium aluminum arsenide (InAlAs).

[0067] Over the lower barrier layer **581**, a quantum well **583** is formed of a material with a smaller band gap than that of the lower barrier. In an embodiment wherein the composite buffer **575** comprises GaSb buffer layer **540** and AlSb buffer layer **570**, the quantum well **583** is doped or undoped and formed of InSb. In some embodiments, where the quantum well layer **583** is formed of InSb, the growth temperature is between approximately 385 C and 430 C. In a specific embodiment, the InSb quantum well layer **583** is grown at 400 C. In another embodiment wherein the composite buffer **575** comprises GaAs buffer layer **540** and AlAs buffer layer **570**, the quantum well **583** is doped or undoped and formed of indium gallium arsenide ($In_xGa_{1-x}As$) or InAs, as two examples.

[0068] Quantum well **583** is of a sufficient thickness to provide adequate channel conductance. In a particular embodiment, the thickness of the quantum well **583** is between about 10 nm and about 50 nm. In certain embodiments quantum well layer **583** is below its critical thickness so that additional defects are not introduced due to lattice mismatch. The quantum well layer **583** may be strained by the lower barrier layer **581**, the upper barrier layer **585**, or both.

[0069] Over the quantum well **583** is the upper barrier layer **585**. Upper barrier layer **585** has a larger band gap than the quantum well **583**, thereby confining a majority of charge carriers within the quantum well **583** for reduced device leakage. The upper barrier layer **585** may be formed of the same or different materials as the lower barrier layer **581**. In certain embodiments wherein the composite buffer **575** comprises a GaSb layer **540** and AlSb layer **570**, the upper barrier layer **585** comprises aluminum indium antimonide ($Al_xIn_{1-x}Sb$). In some embodiments the upper barrier layer **585** comprises between about 10% and 40% aluminum, ($Al_xIn_{1-x}Sb$, with x=0.1-0.4). At above approximately 40% aluminum, the upper device layer may oxidize upon removal from the deposition chamber. In a particular embodiment, the upper barrier layer **585** is $Al_xIn_{1-x}Sb$ with 15% aluminum ($Al_{0.15}In_{0.85}Sb$). In an alternative embodiment, the upper barrier layer **585** may contain greater than 40% aluminum. In such an embodiment, a capping layer (not shown) may be deposited on the upper barrier layer **585** in order to suppress oxidation.

[0070] In another embodiment, as shown in FIG. **5**B, the region **584** of the upper barrier layer **585** at the interface with the quantum well layer **583** has a lower lattice constant and larger band gap than the region **582** of the lower barrier layer **581** at the interface with the quantum well layer **583**. Such a structure may be beneficial for more effectively confining charge carriers within the quantum well **583** for reduced device leakage. This may be accomplished, for example, by having a higher aluminum concentration in the upper $Al_xIn_{1-x}Sb$ barrier layer **585** than in the lower $Al_xIn_{1-x}Sb$ barrier layer **581**. Increasing aluminum concentration, then leads to a larger band gap in $Al_xIn_{1-x}Sb$. In a particular embodiment, the upper barrier layer **585** contains 20% aluminum in the region **584** at the interface with quantum well layer **583**, and lower

barrier layer **581** contains 15% aluminum in the region **582** at the interface with quantum well layer **583**.

[0071] Additionally, the amount of strain induced in the quantum well layer **583** may be tailored by controlling the thickness and lattice mismatch with the lower barrier layer **581** and upper barrier layer **585**. In a specific embodiment, wherein the quantum well **583** is InSb and the lower barrier layer **581** and upper barrier layer **585** are composed of $Al_xIn_{1-x}Sb$ with 15% aluminum, the quantum well layer **583** is compressively strained.

[0072] The upper barrier **585** may also be graded. In one embodiment the upper barrier is graded from x=0 (InSb) in region **584** at the interface with the quantum well layer **583** to x=0.15 ($Al_{0.15}In_{0.85}Sb$). In such an embodiment, the InSb quantum well layer **583** and graded upper barrier layer **585** and are lattice matched at their interface, and the graded upper barrier layer **585** does not induce strain into the InSb quantum well layer **583**. In another embodiment, the upper barrier **585** is linearly graded from x=0.1 ($Al_{0.1}In_{0.9}Sb$) in region **584** at the interface with the quantum well layer **583** to x=0.4 ($Al_{0.4}In_{0.6}Sb$) at the opposite surface. In such an embodiment, the upper barrier **585** may induce a strain in the quantum well layer **583**. The upper barrier layer **585** may have various thicknesses and in certain embodiments the upper barrier layer **585** is between about 20 nm and 500 nm thick.

[0073] In certain other embodiments, wherein the composite buffer **575** comprises GaAs buffer layer **540** and AlAs buffer layer **570**, the upper barrier layer **585** comprises indium aluminum arsenide (InAlAs).

[0074] In some embodiments, the lower barrier **581**, the upper barrier layer **585**, or both may be doped to supply carriers to the quantum well **583**. In a specific embodiment, the upper barrier layer **585** includes a doped layer **587**, as shown in FIG. **5**B and supplies carriers where the quantum well is undoped. In one embodiment, doped layer **587** is delta doped. In another embodiment doped layer **587** is modulation doped. For an n-type device utilizing an $Al_xIn_{1-x}Sb$ upper barrier **5851** the doping may be done using silicon (Si) or tellurium (Te) impurities, as two examples. In one embodiment the doped layer **587** is delta doped and has a thickness of approximately 3 Å to 5 Å. In other embodiments the doped layer **587** is modulation doped and has a thickness between approximately 5 Å and 50 Å.

[0075] In some embodiments upper barrier **585** is a composite structure comprising spacer layer **586**, doped layer **587**, and top barrier layer **588**. In such embodiments, region **584** of the upper barrier layer **585** is located in the spacer layer **586** at the interface with the quantum well layer **583**. In embodiments where upper barrier **585** is comprised of $Al_xIn_{1-x}Sb$, doped layer **587** may be delta doped by closing the sources for In and Al. The source for Sb is optionally left open, and the source for an n-type dopant such as Te, for example, is opened. In such exemplary embodiments, delta doped layer **587** may comprise Te and Sb, or Te only. In a particular embodiment, spacer layer **586** is between approximately 3 Å and 100 Å thick, delta doped layer **587** is less than 25 Å thick, and top barrier layer **588** is between approximately 50 Å and 500 Å thick in order to confine two-dimensional electron gas (2DEG) carriers in the quantum well **583**. Alternatively, in embodiments where upper barrier **585** is comprised of $Al_xIn_{1-x}Sb$, doped layer **587** may be modulation doped by opening the source for an n-type dopant such as Te, for example, while sources or Al, In, and Sb are also open. In a particular embodiment, spacer layer **586** is approximately 30 Å and 100 Å thick, modulation doped layer **587** has a thickness between approximately 5 Å and 50 Å, and top barrier layer **588** is between approximately 50 Å and 500 Å thick in order to confine two-dimensional electron gas (2DEG) carriers in the quantum well **583**.

[0076] Specific embodiments have been described where upper barrier **585** includes a doped layer **587**. However, additional embodiments are within the scope of the invention where lower barrier layer **581** may alternatively or also be doped to supply carriers to the quantum well **583**. For an n-type device utilizing an $Al_xIn_{1-x}Sb$ lower barrier **581**, the doping may, for example, be done in situ using silicon (Si) or tellurium (Te) impurities, as two examples. In some embodiments, the lower barrier layer **581** may comprise a doped layer (not shown) similar to that described for upper barrier **585**. The doped layer may be, for example, modulation or delta doped.

[0077] An alternative embodiment for forming a quantum well structure is illustrated in FIG. **5**C. As shown in FIG. **5**C, the quantum well structure **280** comprises lower barrier layer **581**, quantum well layer **583**, and upper barrier layer **585**. Upper barrier layer **585** may be a composite structure further comprising spacer layer **586**, dopant segregation barrier layer **589**, delta doped layer **587**, and top barrier layer **588**.

[0078] Lower barrier layer **581** is disposed similarly as in previous embodiments. For example lower barrier **581** may be comprised of $Al_xIn_{1-x}Sb$, grown between approximately 415 C and 445 C, and range from 100 Å to 5 um thick. Additionally, lower barrier layer **581** may also be graded. Quantum well layer **583** is formed of a material with a smaller band gap than that of the lower barrier **581**. For example the quantum well layer **583** may be formed of InSb, grown between approximately 385 C and 430 C, and range from 10 nm to 50 nm thick.

[0079] Upper barrier layer **585** is disposed above quantum well layer **583**. In one embodiment, upper barrier layer **585** may be a composite structure further comprising spacer layer **586**, dopant segregation barrier layer **589**, delta doped layer **587**, and top barrier layer **588**. Dopant segregation barrier layer **589** serves to improve confinement of the delta dopant in the subsequently deposited delta doped layer **587** and the improved dopant confinement may allow for reduce top barrier layer **588** thickness, which is useful in enhancement mode devices where it is desirable to position the gate close the quantum well layer.

[0080] In addition to inclusion of the dopant segregation barrier layer **589**, deposition and growth temperature for upper barrier layer **585** may also be reduced in order to reduce delta dopant segregation. In one embodiment, a composite upper barrier layer **585**, including a spacer layer **586** and top barrier layer **588** comprising $Al_xIn_{1-x}Sb$, is deposited at a lower temperature range of approximately 400 C to 410 C. The lower temperature range of 400 C to 414 C, as opposed to 415 C to 445 C, may help reduce out diffusion and surface migration of the delta dopant, which, in some embodiments, may be characterized as possessing a comparatively higher vapor pressure than components of the top barrier layer **588**.

[0081] Spacer layer **586** may for example, comprise $Al_xIn_{1-x}Sb$, grown between approximately 400 C and 410 C, and range from 30 to 100 nm thick. In an embodiment, spacer layer **586** may include increased Al concentration, and/or be graded.

[0082] Dopant segregation barrier layer **589** is then disposed above spacer layer **586**. In an embodiment dopant

segregation barrier is deposited between approximately 400 C and 410 C. In one embodiment, where spacer layer **586** comprises III-V materials, dopant segregation barrier layer is composed of a group III element. In such an embodiment, where spacer layer **586** comprises $Al_xIn_{1-x}Sb$, dopant segregation barrier layer **589** is a few monolayers of In. For example, this may be accomplished by turning off the source gases for Al and Sb while leaving open the In source. In one embodiment a 2 monolayer thick, approximately 6 Å thick, layer is grown by leaving the In source open for 2 seconds. The result is a two monolayer thin group III element layer disposed over a III-V spacer layer **586**, thereby creating an artificial vacancy for a group V element. In another embodiment, dopant segregation barrier layer **589** is one to three monolayers thick.

[0083] In an alternative embodiment, where spacer layer **86** comprises III-V materials, dopant segregation barrier layer **589** is comprised of a group V element. In such an embodiment, where spacer layer **586** comprises $Al_xIn_{1-x}Sb$, dopant segregation barrier layer **589** is one to three monolayers of Sb. For example, this may be accomplished where source gases for Al and In are turned off while the Sb source is left open for 2 seconds, thereby depositing a thin Sb segregation barrier layer **589**. In this case, an artificial vacancy for a group III element is created.

[0084] Deposition of the delta doped layer **587** directly on the dopant segregation barrier layer **589** fills the deficit of the artificial vacancy. In an embodiment delta doped layer **587** is deposited between approximately 400 C and 410 C. Where the device is an n-type device, the delta dopant may be for example, tellurium (Te) and fill the artificial vacancy for a group V element. Where the device is a p-type device, the delta dopant may be for example beryllium (Be) or zinc (Zn) and fill the artificial vacancy for a group III element. In an embodiment, delta doped layer **587** is less than 30 Å thick. This may be accomplished by leaving the dopant source gas open for approximately 40 seconds. In one embodiment, the source gas for Sb is optionally left open with a Te dopant source gas, to form a Te delta doped layer **587**. In an alternative embodiment, the source gas for In is optionally left open with a Be or Zn dopant source gas to form a Be or Zn delta doped layer **587**.

[0085] Top barrier layer **588** is then deposited over delta doped layer **587**. In an embodiment, top barrier layer **588** is deposited between approximately 400 C and 410 C to a thickness of less than or equal to approximately 50 Å. In an alternative embodiment top barrier layer **588** is grown to a thickness of up to 500 Å. Out migration of the delta doped layer **587** to the surface of top barrier layer **588** is a concern, especially for delta dopants characterized by a vapor pressure comparatively higher than that for the top barrier layer **588** components. The dopant segregation barrier layer **589** and the artificial vacancies created assist in reducing out diffusion of the delta dopants by holding the dopants in the artificial vacancies. Reduction in growth temperature for the top barrier layer **588** can also assist in reducing out diffusion by reducing the effects of vapor pressure. Accordingly the growth temperature for the entire upper barrier layer **585** comprising spacer layer **586**, dopant segregation barrier layer **589**, delta doped layer **587**, and top barrier layer **588** is reduced to between approximately 400 C and 410 C.

[0086] Finally, to complete device layer **580** as shown in FIG. **5**A, a highly-doped source drain layer **595** is formed above the upper barrier layer **85**. In a particular embodiment, the source drain layer **595** is n+ doped InSb between about 30 Å to about 300 Å thick.

[0087] As shown in FIG. **5**D, source and drain contact metallizations **591** are then formed by commonly known deposition processes, such as electron beam evaporation or reactive sputtering. In various embodiments, as shown in FIG. **5**D, a mask material **593** is used to selectively remove a portion of the semiconductor device stack in preparation for the placement of the gate electrode. Depending on whether a depletion mode or enhancement mode device is desired, selective etches may be used to form a recess having a particular depth. In certain embodiments implementing an enhancement mode device it is desirable to place the gate electrode close to the delta doped layer. In such an embodiment the top barrier layer **588** portion of upper barrier **585** may be etched to a thickness of less than approximately 50 Å. In alternative embodiments implementing a depletion mode device it may be desirable to have a thicker top barrier layer **588**.

[0088] In particular embodiments, source drain layer **595** is removed during the gate recess etch to expose a suitable Schottky surface on the upper barrier layer **585**. Commonly known dry or wet etch techniques may be utilized to form the gate recess. The etchant may be selective to the composition of the semiconductor, for example, in an embodiment, an n+ doped indium antimonide (InSb) source drain layer **595** is selectively removed using a wet etch process comprised of citric acid and peroxide. Through application of similar commonly known selective etch techniques, the recess etch depth may be tightly controlled by terminating on a stop layer grown upon the upper barrier layer **585** (not shown).

[0089] As shown in FIG. **5**E, the gate electrode **592** is formed over the upper barrier layer **585**. In some embodiments of the present invention, commonly known techniques are used to form the gate electrode **592** directly on the upper barrier layer **585**, thereby creating Schottky junction through which the gate controls the quantum well **583**. In other embodiments, commonly known techniques are used to form the gate electrode **592** on a dielectric layer over the upper barrier layer **585**, thereby creating a MOS junction. In particular embodiments, the gate electrode **592** is formed using commonly known lift-off methods relying on lithography and highly directional deposition techniques, such as electron beam deposition, to separate the gate electrode **592** from the source drain layer **595**.

[0090] Then, as shown in FIG. **5**E, the quantum well transistor **590** is isolated using commonly known techniques. In particular embodiments, the epitaxial device layer of the quantum well transistor **590** is etched through to form an active device mesa upon the composite buffer **57**D over silicon substrate **510**. The isolation etch removes the source drain layer **589**, upper barrier **585**, quantum well **583** and lower barrier **581** along a perimeter of the active device to form the mesa. As previously described the isolative character of the composite buffer **575** provides sufficient device isolation between the transistor **590** and neighboring devices. Thus, in particular embodiments, the isolation etch is stopped when the composite buffer **575** is exposed. This enables device isolation to be achieved with minimal topography. With the quantum well transistor **590** substantially complete, backend processing is performed using commonly known techniques to connect quantum well transistor **590** to the external environment.

[0091] Although the present invention has been described in language specific to structural features and/or methodological acts, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or acts described. The specific features and acts disclosed are instead to be understood as particularly graceful implementations of the claimed invention useful for illustrating the present invention.

What is claimed is:

1. A method for forming a quantum well structure comprising:

disposing a lower barrier layer;

disposing a quantum well layer above the lower barrier layer;

disposing a spacer layer above the quantum well layer;

disposing a dopant segregation barrier layer above the spacer layer;

disposing a delta doped layer disposed on the dopant segregation barrier layer; and

disposing a top barrier layer above the delta doped layer.

2. The method of claim **1**, wherein disposing the dopant segregation barrier layer comprises shutting off a Sb source gas and an Al source gas.

3. The method of claim **1**, wherein disposing the dopant segregation barrier layer comprises In.

4. The method of claim **1**, wherein disposing the dopant segregation barrier layer comprises shutting off an In source gas and an Al source gas.

5. The method of claim **1**, wherein disposing the dopant segregation barrier layer comprises disposing a Sb layer.

6. The method of claim **1**, wherein the top barrier layer is deposited at a lower temperature than the lower barrier layer.

7. The method of claim **1**, further comprising disposing the lower barrier layer over a composite buffer layer comprising a GaSb layer and an $Al_xGa_{1-x}Sb$ layer disposed on the GaSb layer, wherein x is between approximately 0 and 1.0.

8. The method of claim **1**, further comprising disposing the lower barrier over a GaAs substrate.

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