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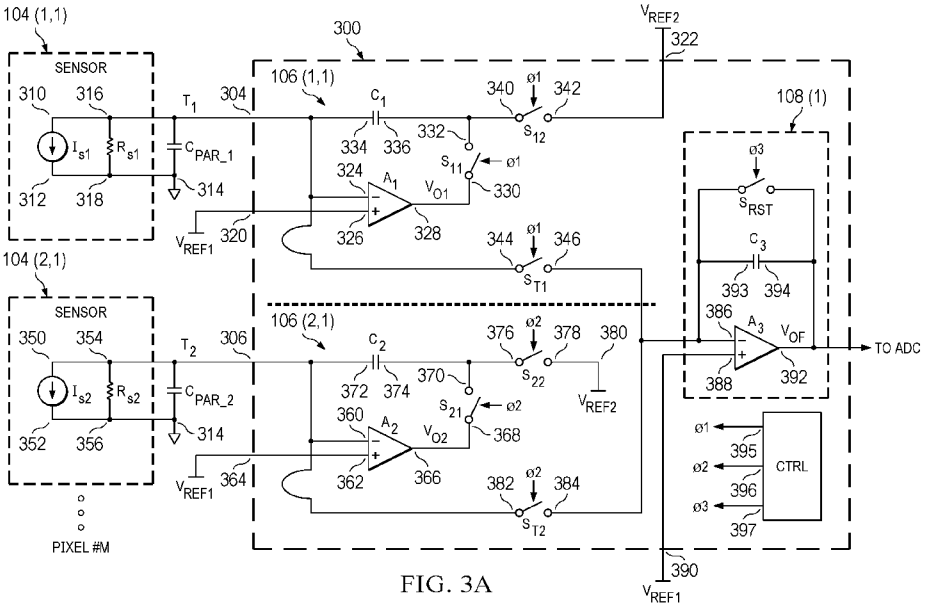

FIG. 3A

(57) **Abstract:** A circuit (300) includes a plurality of first stage integrators (106 (1,1) - 106(2,1)). Each of the plurality of first stage integrators (106 (1, 1) - 106(2, 1)) includes a first input (324), a. second input (326), a third input (322) and an output (328). The first input (324) of each of the plurality of first stage integrators is coupled to a. different one of circuit inputs (304), the second input (326) is coupled to a first reference input, the third input (322) is coupled to a second reference input and the output (328) of each of the plurality of first stage integrators is coupled to the first input (324) of such first stage integrator. The circuit (300) includes a second stage integrator (108(1)) which includes a first input (386) coupled to each of the first inputs of the plurality' of first stage integrators, a second input. (388) coupled to the first reference input, and an output (392) coupled to the first input (386) of the second stage integrator (108(1)).

[Continued on next page]

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CIRCUIT FOR INTEGRATING CURRENTS FROM HIGH-DENSITY SENSORS

[0001] This description relates generally to circuits for integrating currents from sensors.

BACKGROUND

[0002] Image sensors are used for the conversion of optical image information to electrical signals. Image sensors generate electrical currents according to an amount of light incident on the sensors. Image sensors are used in, for example, electronic imaging devices, medical imaging devices and thermal imaging devices.

[0003] Optical nanopore sensors are used in the detection and characterization of clinical biomarkers and for DNA/RNA sequencing. Optical nanopore sensors generally operate by detecting changes in the ionic current through a nanopore.

[0004] A sensor system may include hundreds or even thousands of individual sensors (e.g., sensor elements). The individual sensors may be arranged, for example, in a two-dimensional array. Each sensor may be coupled to an electronic processing circuit via a conductor (e.g., signal trace, channel, wire). The electronic processing circuit converts the electrical current produced by the sensor into a voltage. The electronic processing circuit may include an amplifier which integrates the current and provides an output voltage representing the current. A drawback of many amplifiers is that noise signals (e.g., flicker noise signals or thermal noise signals) that may be present at an input of an amplifier may be amplified and produced at an output of the amplifier. Also, parasitic capacitances of the sensor and the signal trace increase the noise signals.

[0005] As noise signals increase, a signal-to-noise ratio (SNR) of an amplifier degrades. To reduce noise signals and increase the SNR, a precision amplifier may be used to convert an electrical current into a voltage. A precision amplifier may have a large bandwidth, a high gain and a low noise and may be implemented with multiple gain stages each having several transistors. Thus, a precision amplifier requires a relatively large area to implement in an integrated circuit or a semiconductor die and draws higher current. Because a sensor system may include several thousand sensors which are densely fabricated in an integrated circuit or a semiconductor die and the individual sensors may be coupled to respective precision amplifiers, a high-density sensor system can take a relatively large area in an integrated circuit or in a semiconductor die and can

draw higher current which increases power consumption.

SUMMARY

[0006] In one aspect, a circuit includes a plurality of circuit inputs. At least one of the plurality of circuit inputs is adapted to receive an input current. The circuit includes a first reference input adapted to receive a first reference voltage and includes a second reference input adapted to receive a second reference voltage. The circuit includes a plurality of first stage integrators. Each of the plurality of first stage integrators includes a first input, a second input, a third input and an output. The first input of each of the plurality of first stage integrators is coupled to a different one of the circuit inputs, the second input is coupled to the first reference input, the third input is coupled to the second reference input and the output of each of the plurality of first stage integrators is coupled to the first input of such first stage integrator by a first feedback path for such first stage integrator. The circuit includes a second stage integrator which includes a first input, a second input and an output. The first input of the second stage integrator is coupled to each of the first inputs of the plurality of first stage integrators, the second input of the second stage integrator is coupled to the first reference input, and the output of the second stage integrator is coupled to the first input of the second stage integrator by a second feedback path.

[0007] In an additional aspect, the circuit includes a plurality of transfer switches. Each of the plurality of transfer switches includes a first terminal and a second terminal. The first terminal of each of the plurality of transfer switches is coupled to a different one of the first inputs of the plurality of first stage integrators and the second terminal of each of the plurality of transfer switches is coupled to the first input of the second stage integrator.

[0008] In an additional aspect, the first feedback path of each of the plurality of first stage integrators includes a first switch which includes a first terminal coupled to the output of such first stage integrator and includes a second terminal. The first feedback path of each of the plurality of first stage integrators includes a first feedback capacitor which includes a first terminal coupled to the first input of such first stage integrator and a second terminal coupled to the second terminal of the first switch.

[0009] In an additional aspect, each of the plurality of first stage integrators further includes a second switch which includes a first terminal coupled to the second terminal of the first feedback capacitor of such first stage integrator and a second terminal adapted to receive the second reference voltage.

[0010] In an additional aspect, a circuit includes a circuit input adapted to receive an input current, a first reference input adapted to receive a first reference voltage and a second reference input adapted to receive a second reference voltage. The circuit includes a first stage integrator which includes a first input coupled to the circuit input, a second input coupled to the first reference input, a third input coupled to the second reference input and an output coupled to the first input of the first stage integrator by a first feedback path. The circuit includes a transfer switch which includes a first terminal coupled to the first input of the first stage integrator and includes a second terminal. The circuit includes a second stage integrator which includes a first input coupled to the second terminal of the transfer switch, a second input coupled to the first reference input, and an output coupled to the first input of the second stage integrator by a third feedback path.

[0011] In an additional aspect, a circuit includes a circuit input adapted to receive an input current, a first reference input adapted to receive a first reference voltage and a second reference input adapted to receive a second reference voltage. The circuit includes a first amplifier which includes a first input coupled to the circuit input, a second input coupled to the first reference input and includes an output. The circuit includes a first switch which includes a first terminal coupled to the output of the first amplifier and includes a second terminal. The circuit includes a first feedback capacitor which includes a first terminal coupled to the first input of the first amplifier and a second terminal coupled to the second terminal of the first switch. The circuit includes a second switch which includes a first terminal coupled to the second terminal of the first feedback capacitor and a second terminal coupled to the second reference input. The circuit includes a transfer switch which includes a first terminal coupled to the first input of the first amplifier and includes a second terminal. The circuit includes a second amplifier which includes a first input coupled to the second terminal of the transfer switch, a second input coupled to the first reference input and includes an output. The circuit includes a second feedback capacitor which includes a first terminal coupled to the first input of the second amplifier and a second terminal coupled to the output of the second amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a block diagram illustrating an example sensor system.

[0013] FIG. 2 is a block diagram illustrating a plurality of sensors coupled to respective first stage integrators which are coupled to a second stage integrator.

[0014] FIGS. 3A, 3B and 3C are schematic diagrams illustrating an example circuit.

[0015] FIG. 4 is a timing diagram illustrating timing signals and voltages in the circuit of FIGS. 3A-3C.

[0016] The same reference numerals or other reference designators are used in the drawings to designate the same or similar (functionally and/or structurally) features.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0017] FIG. 1 is a block diagram illustrating system 100 of an example. System 100 includes a plurality of sensors 104 (1,1) – 104 (M,N) that are arranged in a two-dimensional array consisting of M rows and N columns. Sensor 104 (1,1) refers to a sensor in row number 1 and column number 1, and sensor 104 (M,N) refers to a sensor in row number M and column number N. The sensors may, for example, be photodiodes, nanopores or other type of sensors. The sensors may be used in electronic imaging devices, medical imaging devices, thermal imaging devices, and/or in systems for detection and/or characterization of clinical biomarkers and DNA/RNA sequencing.

[0018] When energy (e.g., light) is incident on sensors 104 (1,1) – 104 (M,N), they generate electrical charge according to the amount of incident energy. In some examples, sensors 104 (1,1) – 104 (M,N) are coupled to respective first stage integrators 106 (1,1) – 106 (M,N), which may be incorporated with the corresponding sensor (as shown in FIG. 1). Thus, each sensor may be coupled to a corresponding first stage integrator. The charges generated by each sensor is integrated by the corresponding first stage integrator.

[0019] System 100 includes second stage integrators 108 (1) – 108 (N). Each second stage integrator may be coupled to a corresponding group (such as a column, as illustrated in FIG. 1, or a row) of first stage integrators. For example, second stage integrator 108 (1) may be coupled to the first stage integrators of column number 1, and second stage integrator 108 (N) may be coupled to the first stage integrators of column number N. The charges integrated by the first stage integrators of column number 1 are transferred to second stage integrator 108 (1), and similarly the charges integrated by the first stage integrators of column number N are transferred to second stage integrator 108 (N). Responsive to the charges transferred by the first stage integrators of column number 1, second stage integrator 108 (1) provides output voltages representing the transferred charges to, for example, one input of multiplexer 110. Similarly, responsive to the charges transferred by the first stage integrators of column N, second stage integrator 108 (N) provides output voltages representing the transferred charges to, for example, another input of multiplexer 110.

[0020] In some examples, the output voltages provided by second stage integrators 108 (1) – 108 (N) are multiplexed by multiplexer (MUX) 110, and the multiplexed output voltages are provided to analog-to-digital converter (ADC) 112. ADC 112 digitizes the output voltages and provides digital information (e.g., digital codes) representing the output voltages to circuitry (such as a processor, state machine, logic circuitry, memory and or a combination thereof) which may include software. Switching of MUX 110 may be controlled by a processor, logic circuitry and/or control circuitry that may be on the same integrated circuit as MUX 110 or may be external to the integrated circuit.

[0021] FIG. 2 is a block diagram illustrating sensors 104 (1,1) – 104 (M,1) of column number 1 coupled to respective first stage integrators 106 (1,1) – 106 (M,1), which are coupled to second stage integrator 108 (1). In response to receiving incident energy (such as light), sensor 104 (1,1) generates input current I_{S1}. First stage integrator 106 (1,1) integrates charges (e.g., charges produced by sensor 104 (1,1) in response to the received incident energy) output by sensor 104 (1,1) in the form of input current I_{S1} and outputs the resulting integrated charges CH_1. Similarly, in response to incident energy, sensor 104 (M,1) generates charges which is output as input current I_{SM}. First stage integrator 106 (M,1) integrates the charges output by sensor 104 (M,1) as input current I_{SM} and outputs the resulting integrated charges CH_M. Second stage integrator 108 (1) generates output voltages based on the currents/integrated charges provided by first stage integrators 106 (1,1) through 106 (M,1).

[0022] In some examples, first stage integrators 106 (1,1) – 106 (M,1) integrate charges over respective integration periods and output the resulting integrated charges to second stage integrator 108 (1) over respective transfer periods. The integration periods may be different, or they may overlap in time. The transfer periods may be different, or they may overlap in time. A transfer period may be time delayed from a corresponding integration period to allow adequate time for the integration of charges by a first stage integrator. As described below in more details, the number of transfer periods (may also be referred to as a "transfer phase") may be any integer value (e.g., 2), and the number of integration periods (may also be referred to as an "integration phase") may be any integer value (e.g., 2).

[0023] FIG. 3A is a schematic diagram of a circuit 300 of an example. Circuit 300 includes examples of sensors 104 (1,1) and 104 (2,1), first stage integrators 106 (1,1) and 106 (2,1) and second stage integrator 108 (1). Circuit 300 is configured to receive input currents from a plurality

of sensors (e.g., sensors 104 (1,1) and 104 (2,1)) and provide output voltages based on the input currents.

[0024] Circuit 300 includes first stage integrator 106 (1,1) coupled to sensor 104 (1,1) and includes first stage integrator 106 (2,1) coupled to sensor 104 (2,1). Circuit 300 includes second stage integrator 108 (1) coupled to first stage integrators 106 (1,1) and 106 (2,1). Circuit 300 includes first circuit input 304 adapted to be coupled to sensor 104 (1,1) and includes second circuit input 306 adapted to be coupled to sensor 104 (2,1).

[0025] Sensor 104 (1,1) is modeled by a current source I_{S1} and a parallel resistor R_{S1}, where the current is generated by the charge collected by the energy incident to the sensor. The current source I_{S1} (e.g., between around a few nano-amperes to around a few pico-amperes) includes first terminal 310 coupled to first circuit input 304 and includes second terminal 312 coupled to common potential 314 (e.g., ground). Sensor resistor R_{S1} (e.g., between around 1M ohms to around 1G ohms) includes first terminal 316 coupled to first terminal 310 of I_{S1} and includes second terminal 318 coupled to common potential 314. Sensor 104 (1,1) is coupled to first circuit input 304 via signal trace T_1 (e.g., conductor, wire, channel and/or circuit board trace). Parasitic capacitance C_{PAR_1} may be present between signal trace T_1 and common potential 314. Parasitic capacitance C_{PAR_1} may represent the sum of a sensor parasitic capacitance, a signal trace parasitic capacitance, and any other parasitic capacitance.

[0026] Circuit 300 includes first reference input 320 which is adapted to receive first reference voltage V_{REF1} (e.g., around 0V to around 1V) and includes second reference input 322 which is adapted to receive second reference voltage V_{REF2} (e.g., around 0V to around 1.5V).

[0027] First stage integrator 106 (1,1) includes first operational amplifier A_1 which includes first input 324 (e.g., inverting input), second input 326 (e.g., non-inverting input) and output 328. First input 324 of A_1 is coupled to first circuit input 304 and second input 326 of A_1 is coupled to first reference input 320.

[0028] First stage integrator 106 (1,1) includes switch S_{11} (also referred to as first switch) which includes first terminal 330 coupled to output 328 of first operational amplifier A_1 and includes second terminal 332. Feedback capacitor C_1 is coupled via switch S_{11} between output 328 of A_1 and first input 324 of A_1. Feedback capacitor C_1 includes first terminal 334 coupled to first terminal 324 of A_1 and includes second terminal 336 coupled to second terminal 332 of switch S_{11}.

[0029] First stage integrator 106 (1,1) includes switch S_{12} (also referred to as second switch)

which includes first terminal 340 coupled to second terminal 336 of feedback capacitor C_1 and includes second terminal 342 coupled to second reference input 322 which is adapted to receive second reference voltage V_{REF2}. First stage integrator 106 (1,1) includes transfer switch S_{T1} which includes first terminal 344 coupled to first input 324 of first operational amplifier A_1 and includes second terminal 346.

[0030] The model of sensor 104 (2,1) includes current source I_{S2} which includes first terminal 350 and includes second terminal 352 coupled to common potential 314. In addition, the model of sensor 104 (2,1) includes sensor resistor R_{S2} (e.g., between around 1M ohms to around 1G ohms) which includes first terminal 354 coupled to first terminal 350 of I_{S2} and includes second terminal 356 coupled to common potential 314. Sensor 104 (2,1) is coupled to second circuit input 306 via signal trace T_2 (e.g., conductor, wire, channel and/or printed circuit board trace). Parasitic capacitance C_{PAR_2} may be present between signal trace T_2 and common potential 314. Parasitic capacitance C_{PAR_2} may represent the sum of a sensor parasitic capacitance, a signal trace parasitic capacitance and any other parasitic capacitance.

[0031] First stage integrator 106 (2,1) includes second operational amplifier A_2 which includes first input 360 (e.g., inverting input) coupled to second circuit input 306, second input 362 (e.g., non-inverting input) coupled to third reference input 364 and includes output 366. Third reference input 364 is adapted to receive first reference voltage V_{REF1}. First stage integrator 106 (2,1) includes switch S_{21} (also referred to as third switch) which includes first terminal 368 coupled to output 366 of second operational amplifier A_2 and includes second terminal 370. Feedback capacitor C_2 is coupled between output 366 of A_2 and first input 360 of A_2. Feedback capacitor C_2 includes first terminal 372 coupled to first terminal 360 of A_2 and includes second terminal 374 coupled to second terminal 370 of switch S_{21}.

[0032] First stage integrator 106 (2,1) includes switch S_{22} (also referred to as fourth switch) which includes first terminal 376 coupled to second terminal 374 of feedback capacitor C_2 and includes second terminal 378 coupled to second reference input 380 which is adapted to receive second reference voltage V_{REF2}. First stage integrator 106 (2,1) includes transfer switch S_{T2} which includes first terminal 382 coupled to first input 360 of second operational amplifier A_2 and includes second terminal 384.

[0033] Circuit 300 includes second stage integrator 108 (1) which includes third operational amplifier A_3 coupled to first and second operational amplifiers A_1 and A_2 via first and second

transfer switches S_{T1} and S_{T2}, respectively. Third operational amplifier A_3 includes first input 386 (e.g., inverting input) coupled to second terminals 346 and 384 of respective transfer switches S_{T1} and S_{T2}. Third operational amplifier A_3 includes second input 388 (e.g., non-inverting input) coupled to fifth reference input 390 which is adapted to receive first reference voltage V_{REF1}. Third operational amplifier A_3 includes output 392, which may be coupled to ADC 112 via multiplexer 110. Feedback capacitor C_3 is coupled between output 392 of A_3 and first input 386 of A_3. Feedback capacitor C_3 includes first terminal 393 coupled to first input 386 of A_3 and includes second terminal 394 coupled to output 392 of A_3. Second stage integrator 108 (1) includes reset switch S_{RST} coupled between first and second terminals 393 and 394 of C_3.

[0034] In some examples, circuit 300 includes timing control circuit CTRL (e.g., a processor, logic circuitry, memory, state machine and/or software) configured to provide timing signals to switches S_{11}, S_{12}, S_{T1}, S_{21}, S_{22} and S_{T2}. Timing control circuit CTRL may include a clock (not shown in FIG. 3) which provides a clock signal. In response, timing control circuit CTRL provides first, second and third timing signals ø1, ø2, ø3 at respective outputs 395, 396 and 397. Timing signal ø1 is applied to control (e.g., to cause the applicable switches to open (cause to be non-conducting) or close (cause to be conducting)) switches S_{11}, S_{12} and S_{T1}, timing signal ø2 is applied to control switches S_{21}, S_{22} and S_{T2}, and timing signal ø3 is applied to control switch S_{RST}.

[0035] In some examples, circuit 300 is operated in two phases: (1) an integration phase; and (2) a transfer phase. In an integration phase, input current from a sensor (e.g., sensor 104 (1,1)) is received by its corresponding first stage integrator (e.g., first stage integrator 106 (1,1)) and sensor charges that form the input current are integrated over an integration period. In a transfer phase, the first stage integrator (e.g., first stage integrator 106 (1,1)) transfers the resulting integrated charges to a second stage integrator (e.g., second stage integrator 108 (1)) over a transfer period. The second stage integrator (e.g., second stage integrator 108 (1)) provides an output voltage representing the transferred charges.

[0036] Similarly, in an integration phase, input current from sensor 104 (2,1) is received by first stage integrator 106 (2,1) which integrates charges that form the input current over an integration period. In a transfer phase, first stage integrator 106 (2,1) transfers the resulting integrated charges to second stage integrator 108 (1) over a transfer period. Second stage integrator 108 (1) provides an output voltage representing the transferred charges.

[0037] FIG. 3B illustrates circuit 300 during a first and a second integration phase. During the

first integration phase, charges are integrated by first stage integrator 106 (1,1) and during the second integration phase, charges are integrated by first stage integrator 106 (2,1).

[0038] During the first integration phase, first timing signal ø1 is asserted LOW (e.g., a logic "0", a low voltage, such as around ground). In response, switch S_{11} is closed (e.g., conducting) but switches S_{12} and S_{T1} are opened (e.g., non-conducting). Thus, output 328 of first operational amplifier A_1 is coupled to first input 324 of A_1 via feedback capacitor C_1, thereby forming a feedback path. Due to the feedback path, first input 324 of A_1 is held at a virtual ground with respect to second input 326 of A_1. Input current I_{S1} from sensor 104 (1,1) flows into feedback capacitor C_1, and charges of I_{S1} are integrated into feedback capacitor C_1 over a first integration period. Because switch S_{T1} remains open during the first integration phase, first stage integrator 106 (1,1) is disconnected from second stage integrator 108 (1).

[0039] Similarly, during a second integration phase, second timing ø2 is asserted LOW. In response, switch S_{21} is closed but switches S_{22} and S_{T2} are opened. Thus, output 366 of second operational amplifier A_2 is coupled to first input 360 of A_2 via feedback capacitor C_2, thus forming a feedback path. Due to the feedback path, first input 360 of A_2 is held at a virtual ground with respect to second input 362 of A_2. Input current I_{S2} from sensor 104 (2,1) flows into feedback capacitor C_2, and charges of I_{S2} are integrated into feedback capacitor C_2 over a second integration period. Because switch S_{T2} remains open during the second integration phase, first stage integrator 106 (2,1) is disconnected from second stage integrator 108 (1).

[0040] In some examples, first and second integration periods may be different in duration and/or starting time. In other examples, first and second integration periods may overlap (at least partially) in time.

[0041] FIG. 3C illustrates circuit 300 during a first and a second transfer phase. During the first transfer phase, first timing signal ø1 is asserted HIGH. In response, switch S_{11} is opened but switches S_{12} and S_{T1} are closed. Because S_{11} is opened, output 328 of first operational amplifier A_1 is disconnected from first input 324 of A_1, thus disconnecting the feedback path. Also, because S_{21} and S_{T1} are both closed, feedback capacitor C_1 is coupled to second reference voltage V_{REF2} and first input 324 of A_1 is coupled to first input 386 of third operational amplifier A_3. As a result, charges integrated into feedback capacitor C_1 are transferred to feedback capacitor C_3 over a first transfer period.

[0042] Similarly, during the second transfer phase, second timing signal ø2 is asserted HIGH.

In response, switch S_{21} is opened but switches S_{22} and S_{T2} are closed. Because S_{21} is opened, output 366 of second operational amplifier A_2 is disconnected from first input 360 of A_2, thus disconnecting the feedback path. Also, because S_{22} and S_{T2} are both closed, feedback capacitor C_2 is coupled to second reference voltage V_{REF2} and first input 360 of A_2 is coupled to first input 386 of third operational amplifier A_3. Thus, charges integrated into feedback capacitor C_2 are transferred to feedback capacitor C_3 over a second transfer period.

[0043] During the first transfer period, the feedback path formed by feedback capacitor C_1 is disconnected. Thus, during the first transfer period a virtual ground does not exist at first input 324 of first operational amplifier A_1 with respect to second input 326 of A_1, and output voltage V_{O1} is no longer capacitively coupled to first input 324 of A_1. Thus, any noise that may be present at second input 326 of A_1 is not present at first input 324 of A_1 due to the absence of a virtual ground, and any noise that may be present at output 328 of A_1 is not capacitively coupled to first input 324 of A_1. Thus , during the first transfer phase any noise from first input 324 of A_1 or any noise from output 328 of A_1 are not transferred to third operational amplifier A_3. Similarly, during the second transfer phase any noise from first input 360 of A_2 or any noise from output 366 of A_2 are not transferred to third operational amplifier A_3.

[0044] In some examples, first and second transfer periods may be different in duration and/or starting time. In other examples, first and second transfer periods may overlap (at least partially) in time.

[0045] During the integration phase, first stage integrator 106 (1,1) temporarily stores charges from input current I_{S1} and during the transfer phase, first stage integrator 106 (1,1) transfers the charges to second stage integrator 108 (1). Also, during the transfer phase, first stage integrator 106 (1,1) transfers charges from parasitic capacitor C_{PAR_1} to second stage integrator 108 (1). However, first stage integrator 106 (1,1) does not transfer output voltage V_{O1} to second stage integrator 108 (1). Thus, any noise that may be present at output 328 of A_1 (e.g., noise signals in output voltage V_{01}) is not transferred to second stage integrator 108 (1) and does not degrade the performance of second stage integrator 108 (1). Thus, first operational amplifier A_1 may be implemented as a low-gain, low-bandwidth amplifier which requires fewer gain stages and fewer transistors than required by a high-gain, large-bandwidth amplifier. Similarly, first stage integrator 106 (2,1) may be implemented as a low-gain, low-bandwidth amplifier. Thus, the described examples allow implementing A_1 and A_2 as low-gain, low-bandwidth amplifiers, yet not lessening

the precision of data acquisition. There are several benefits of using low-gain, low-bandwidth amplifiers instead of using high-gain, large-bandwidth amplifiers. A low-gain, low-bandwidth amplifier consumes considerably less power than a high-gain, large-bandwidth amplifier due to its relaxed noise specifications. Also, because a low-gain, low-bandwidth amplifier has fewer number of transistors, it is less expensive and requires less area to implement in an integrated circuit or a semiconductor die. If a system requires a very large number (e.g., 10K or 100K) of sensors or pixels, thus increasing the number of first stage integrators, these advantages may become considerable.

[0046] In some example, third operational amplifier A_3 may be implemented as a high-gain, large-bandwidth amplifier which has a low noise (also referred to as a precision amplifier). Because A_3 provides output voltage V_{OF} responsive to charges transferred from A_1 and A_2, any noise generated by A_3 may also be transferred to output voltage V_{OF}. Thus, it is beneficial to implement A_3 as a high-gain, large-bandwidth amplifier which has a low noise.

[0047] To ensure that output voltage V_{OF} of A_3 is a measure of charges transferred by first stage integrators (e.g., 106 (1,1) and 106 (2,1) of FIG. 3C), feedback capacitor C_3 is reset by switch S_{RST} prior to a transfer period. In some examples, timing signal ø3 is used to control the state of switch S_{RST}. Prior to a transfer period, ø3 is asserted HIGH, which causes S_{RST} to be closed. As such, feedback capacitor C_3 is shorted and is discharged or reset. After C_3 is reset, ø3 is asserted LOW, which causes S_{RST} to be opened. Thus, in the next transfer period, feedback capacitor C_3 is charged only by transferred charges from a first stage integrator, and as such output voltage V_{OF} of A_3 is representative of the transferred charges. In some examples, feedback capacitor C_3 may be reset to a known potential by coupling C_3 to a known reference voltage.

[0048] In some examples, after a predetermined duration that is necessary for charges to be transferred from first operational amplifier A_1 to third operational amplifier A_3 or from second operational amplifier A_2 to A_3 and for output voltage V_{OF} to settle, output voltage V_{OF} may be sampled and digitized by an analog-to-digital converter (not illustrated in FIGS. 3A-3C).

[0049] In some examples, charges from sensors 104 (1,1) – 104 (M,N) may be transferred sequentially in a frame. Thus, for example, charges may be transferred sequentially from the sensors of column number 1, beginning with sensor 104 (1,1). After charges from the last sensor of column number 1 (e.g., sensor 104 (M,1) is transferred, the next frame (e.g., column number 2) may be initiated and the process is repeated.

[0050] In some examples, sensors 104 (1,1) – 104 (M,N), first stage integrators 106 (1,1) – 106 (M,N) and second stage integrators 108 (1) – 108 (N) may be implemented in an integrated circuit or a semiconductor die. In some examples, first stage integrators 106 (1,1) – 106 (M,N) and second stage integrators 108 (1) – 108(N) may be implemented in an integrated circuit which may be coupled to sensors 104 (1,1) -104 (M,N) via an external connection, signal trace, wire, or a conductor. Other variations are possible within the scope of the description.

[0051] FIG. 4 illustrates timing signals and voltages in circuit 300 of an example. The x-axis represents time, and the y-axis represents voltage. Initially, at time T0, timing signals ø1 (indicated by reference numeral 404) and ø2 (indicated by reference numeral 408) are LOW and timing signal ø3 (indicated by reference numeral 412) is HIGH. Thus, feedback capacitor C_3 of third operational amplifier A_3 is reset. In some examples, C_3 is reset to a known voltage (e.g., V_R). Although at time T0, switches S_{11} and S_{21} are closed, output V_{O1} (indicated by reference numeral 416) of operational amplifier A_1 and output V_{O2} (indicated by reference numeral 420) of operational amplifier A_2 are both zero because feedback capacitors C_1 and C_2 are not yet fully charged. At time T0, output V_{OF} (indicated by reference numeral 424) of operational amplifier A_3 is at V_R because feedback capacitor C_3 is reset to V_R.

[0052] At time T1, ø1 is asserted HIGH. Thus, switch S_{11} is opened and switches S_{21} and S_{T1} are closed. As such, C_1 is coupled to second reference voltage V_{REF2}, and first input 324 of first operational amplifier A_1 is coupled to first input 386 of third operational amplifier A_3. Thus, at time T1, charges from C_1 are transferred to C_3 and output V_{OF} begins to drop. At time T2, V_{OF} settles and it is sampled (indicated by reference numeral 428) and digitized by an ADC.

[0053] At time T3, transfer of charges from C_1 to C_3 is completed, ø1 is asserted LOW and ø3 is asserted HIGH. Thus, C_3 is reset to V_R and switch S_{11} is closed. As such, output voltage V_{OF} rises back to V_R.

[0054] At time T4, ø2 is asserted HIGH. Thus, switches S_{22} and S_{T2} are closed but switch S_{21} is opened. Thus, at time T4 transfer of charges from C_2 to C_3 starts. At time T5, output V_{OF} settles and the ADC samples and digitizes V_{OF}. At time T6, transfer of charges from C_2 to C_3 is completed and ø2 is asserted LOW. Thus, V_{OF} rises back to VR.

[0055] The circuits described herein may include one or more semiconductor elements (such as transistors), one or more passive elements (such as resistors, capacitors and/or inductors), and/or one or more sources (such as voltage and/or current sources). The circuits may include only

semiconductor elements within a single physical device (e.g., a semiconductor die and/or integrated circuit (IC) package) and may be adapted to be coupled to at least some of the passive elements and/or the sources to form the described structure either at a time of manufacture or after a time of manufacture, such as by an end-user and/or a third party. While some examples may include certain elements implemented in an integrated circuit and other elements are external to the integrated circuit, in other examples, additional or fewer features may be incorporated into the integrated circuit. In addition, some or all the features illustrated as being external to the integrated circuit may be included in the integrated circuit and/or some features illustrated as being internal to the integrated circuit may be incorporated outside of the integrated. As used herein, the term "integrated circuit" means one or more circuits that are: (i) incorporated in/over a semiconductor substrate; (ii) incorporated in a single semiconductor package; (iii) incorporated into the same module; and/or (iv) incorporated in/on the same printed circuit board.

[0056] In this description, the term "couple" may cover connections, communications, or signal paths that enable a functional relationship consistent with this description. For example, if device A provides a signal to control device B to perform an action, then: (a) in a first example, device A is coupled to device B; or (b) in a second example, device A is coupled to device B through intervening component C if intervening component C does not substantially alter the functional relationship between device A and device B, such that device B is controlled by device A via the control signal provided by device A. Also, in this description, a device that is "configured to" perform a task or function may be configured (e.g., programmed and/or hardwired) at a time of manufacturing by a manufacturer to perform the function and/or may be configurable (or reconfigurable) by a user after manufacturing to perform the function and/or other additional or alternative functions. The configuring may be through firmware and/or software programming of the device, through a construction and/or layout of hardware components and interconnections of the device, or a combination thereof. Furthermore, in this description, a circuit or device that includes certain components may instead be adapted to be coupled to those components to form the described circuitry or device. For example, a structure described as including one or more semiconductor elements (such as transistors), one or more passive elements (such as resistors, capacitors and/or inductors), and/or one or more sources (such as voltage and/or current sources) may instead include only the semiconductor elements within a single physical device (e.g., a semiconductor die and/or integrated circuit (IC) package) and may be adapted to be coupled to at

least some of the passive elements and/or the sources to form the described structure either at a time of manufacture or after a time of manufacture, such as by an end-user and/or a third party.

[0057] As used herein, the terms "terminal", "node", "interconnection" and "pin" are used interchangeably. Unless specifically stated to the contrary, these terms are generally used to mean an interconnection between or a terminus of a device element, a circuit element, an integrated circuit, device or other electronics or semiconductor component.

[0058] While some examples suggest that certain elements are included in an integrated circuit while other elements are external to the integrated circuit, in other examples, additional or fewer features may be incorporated into the integrated circuit. In addition, some or all of the features illustrated as being external to the integrated circuit may be included in the integrated circuit and/or some features illustrated as being internal to the integrated circuit may be incorporated outside of the integrated. As used herein, the term "integrated circuit" means one or more circuits that are: (i) incorporated in/over a semiconductor substrate; (ii) incorporated in a single semiconductor package; (iii) incorporated into the same module; and/or (iv) incorporated in/on the same printed circuit board.

[0059] While the use of particular transistors are described herein, other transistors (or equivalent devices) may be used instead with little or no change to the remaining circuitry. For example, a metal-oxide-silicon FET ("MOSFET") (such as an n-channel MOSFET, nMOSFET, or a p-channel MOSFET, pMOSFET), a bipolar junction transistor (BJT – e.g., NPN or PNP), insulated gate bipolar transistors (IGBTs), and/or junction field effect transistor (JFET) may be used in place of or in conjunction with the devices described herein. The transistors may be depletion mode devices, drain-extended devices, enhancement mode devices, natural transistors or other type of device structure transistors. Furthermore, the devices may be implemented in/over a silicon substrate (Si), a silicon carbide substrate (SiC), a gallium nitride substrate (GaN) or a gallium arsenide substrate (GaAs).

[0060] While certain elements of the described examples are included in an integrated circuit and other elements are external to the integrated circuit, in other examples, additional or fewer features may be incorporated into the integrated circuit. In addition, some or all of the features illustrated as being external to the integrated circuit may be included in the integrated circuit and/or some features illustrated as being internal to the integrated circuit may be incorporated outside of the integrated. As used herein, the term "integrated circuit" means one or more circuits that are: (i) incorporated

in/over a semiconductor substrate; (ii) incorporated in a single semiconductor package; (iii) incorporated into the same module; and/or (iv) incorporated in/on the same printed circuit board.

[0061] While certain components may be described herein as being of a particular process technology, these components may be exchanged for components of other process technologies. Circuits described herein are reconfigurable to include the replaced components to provide functionality at least partially similar to functionality available before the component replacement. Components shown as resistors, unless otherwise stated, are generally representative of any one or more elements coupled in series and/or parallel to provide an amount of impedance represented by the shown resistor. For example, a resistor or capacitor shown and described herein as a single component may instead be multiple resistors or capacitors, respectively, coupled in series or in parallel between the same two nodes as the single resistor or capacitor. Also, uses of the phrase "ground terminal" in this description include a chassis ground, an Earth ground, a floating ground, a virtual ground, a digital ground, a common ground, and/or any other form of ground connection applicable to, or suitable for, the teachings of this description. Unless otherwise stated, "about", "approximately", or "substantially" preceding a value means +/- 10 percent of the stated value, or, if the value is zero, a reasonable range of values around zero.

[0062] Modifications are possible in the described examples, and other examples are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit having a plurality of circuit inputs, at least one of the plurality of circuit inputs adapted to receive an input current, the circuit having a first reference input adapted to receive a first reference voltage and having a second reference input adapted to receive a second reference voltage, the circuit comprising:

a plurality of first stage integrators, each of the plurality of first stage integrators including a first input, a second input, a third input and an output, the first input of each of the plurality of first stage integrators coupled to a different one of the circuit inputs, the second input coupled to the first reference input, the third input coupled to the second reference input and the output of each of the plurality of first stage integrators coupled to the first input of such first stage integrator by a first feedback path for such first stage integrator; and

a second stage integrator including a first input, a second input and an output, the first input of the second stage integrator coupled to each of the first inputs of the plurality of first stage integrators, the second input of the second stage integrator coupled to the first reference input, and the output of the second stage integrator coupled to the first input of the second stage integrator by a second feedback path.

2. The circuit of claim 1, further comprising a plurality of transfer switches, each of the plurality of transfer switches including a first terminal and a second terminal, the first terminal of each of the plurality of transfer switches coupled to a different one of the first inputs of the plurality of first stage integrators and the second terminal of each of the plurality of transfer switches coupled to the first input of the second stage integrator.

3. The circuit of claim 1, wherein the first feedback path comprises:

a first switch including a first terminal coupled to the output of the first stage integrator and including a second terminal; and

a first feedback capacitor including a first terminal coupled to the first input of the first stage integrator and a second terminal coupled to the second terminal of the first switch.

4. The circuit of claim 3, wherein each of the plurality of first stage integrators further comprises a second switch including a first terminal coupled to the second terminal of the first feedback capacitor of such first stage integrator and a second terminal adapted to receive the second reference voltage.

5. The circuit of claim 1, wherein each of the plurality of first stage integrators further comprises a transfer switch including a first terminal coupled to the first input of such first stage integrator and a second terminal coupled to the first input of the second stage integrator.

6. The circuit of claim 1, wherein the second feedback path includes a second feedback capacitor including a first terminal coupled to the first input of the second stage integrator and a second terminal coupled to the output of the second stage integrator.

7. The circuit of claim 1, wherein the second stage integrator comprises a reset switch including a first terminal coupled to the first input of the second stage integrator and a second terminal coupled to the output of the second stage integrator.

8. The circuit of claim 7, wherein the reset switch is configured to reset the second feedback capacitor.

9. A circuit having a circuit input adapted to receive an input current, the circuit having a first reference input adapted to receive a first reference voltage and having a second reference input adapted to receive a second reference voltage, the circuit comprising:

a first stage integrator including a first input coupled to the circuit input, a second input coupled to the first reference input, a third input coupled to the second reference input and an output coupled to the first input of the first stage integrator via a first feedback path;

a transfer switch including a first terminal coupled to the first input of the first stage integrator and including a second terminal; and

a second stage integrator including a first input coupled to the second terminal of the transfer switch, a second input coupled to the first reference input, and an output coupled to the first input of the second stage integrator by a third feedback path.

10. The circuit of claim 9, wherein the first feedback path comprises:

a first switch including a first terminal coupled to the output of the first stage integrator and including a second terminal; and

a first feedback capacitor including a first terminal coupled to the first input of the first stage integrator and a second terminal coupled to the second terminal of the first switch.

11. The circuit of claim 9, wherein the second feedback path includes a second feedback capacitor including a first terminal coupled to the first input of the second stage integrator and a second terminal coupled to the output of the second stage integrator.

12. The circuit of claim 9, wherein the second stage integrator comprises a reset switch including a first terminal coupled to the first input of the second stage integrator and a second terminal coupled to the output of the second stage integrator.

13. A circuit having a circuit input adapted to receive an input current, the circuit having a first reference input adapted to receive a first reference voltage and having a second reference input adapted to receive a second reference voltage, the circuit comprising:

a first amplifier including a first input coupled to the circuit input, a second input coupled to the first reference input and including an output;

a first switch including a first terminal coupled to the output of the first amplifier and including a second terminal;

a first feedback capacitor including a first terminal coupled to the first input of the first amplifier and a second terminal coupled to the second terminal of the first switch;

a second switch including a first terminal coupled to the second terminal of the first feedback capacitor and a second terminal coupled to the second reference input;

a transfer switch including a first terminal coupled to the first input of the first amplifier and including a second terminal;

a second amplifier including a first input coupled to the second terminal of the transfer switch, a second input coupled to the first reference input and including an output; and

a second feedback capacitor including a first terminal coupled to the first input of the second amplifier and a second terminal coupled to the output of the second amplifier.

14. The circuit of claim 13, further comprising a reset switch including a first terminal coupled to the first terminal of the second feedback capacitor and a second terminal coupled to the second terminal of the second feedback capacitor.

15. A circuit having a plurality of circuit inputs, at least one of the plurality of circuit inputs adapted to receive an input current, the circuit having a first reference input adapted to receive a first reference voltage and having a second reference input adapted to receive a second reference voltage, the circuit comprising:

a plurality of first stage integrators, wherein each first stage integrator of the plurality of first stage integrators includes a first input coupled to a different one of the circuit inputs, a second input coupled to the first reference input, a third input coupled to the second reference input and an output coupled to the first input of such first stage integrator by a first feedback path; and

a second stage integrator including a first input coupled to the first inputs of each of the plurality of first stage integrators, a second input coupled to the first reference input, and an output coupled to the first input of the second stage integrator by a second feedback path.

16. The circuit of claim 15, wherein each of the plurality of first stage integrators further comprises a transfer switch including a first terminal coupled to the first input of such first stage integrator and a second terminal coupled to the first input of the second stage integrator.

17. The circuit of claim 15, further comprising a reset switch including a first terminal coupled to the first terminal of the second stage integrator and a second terminal coupled to the output of the second stage integrator.

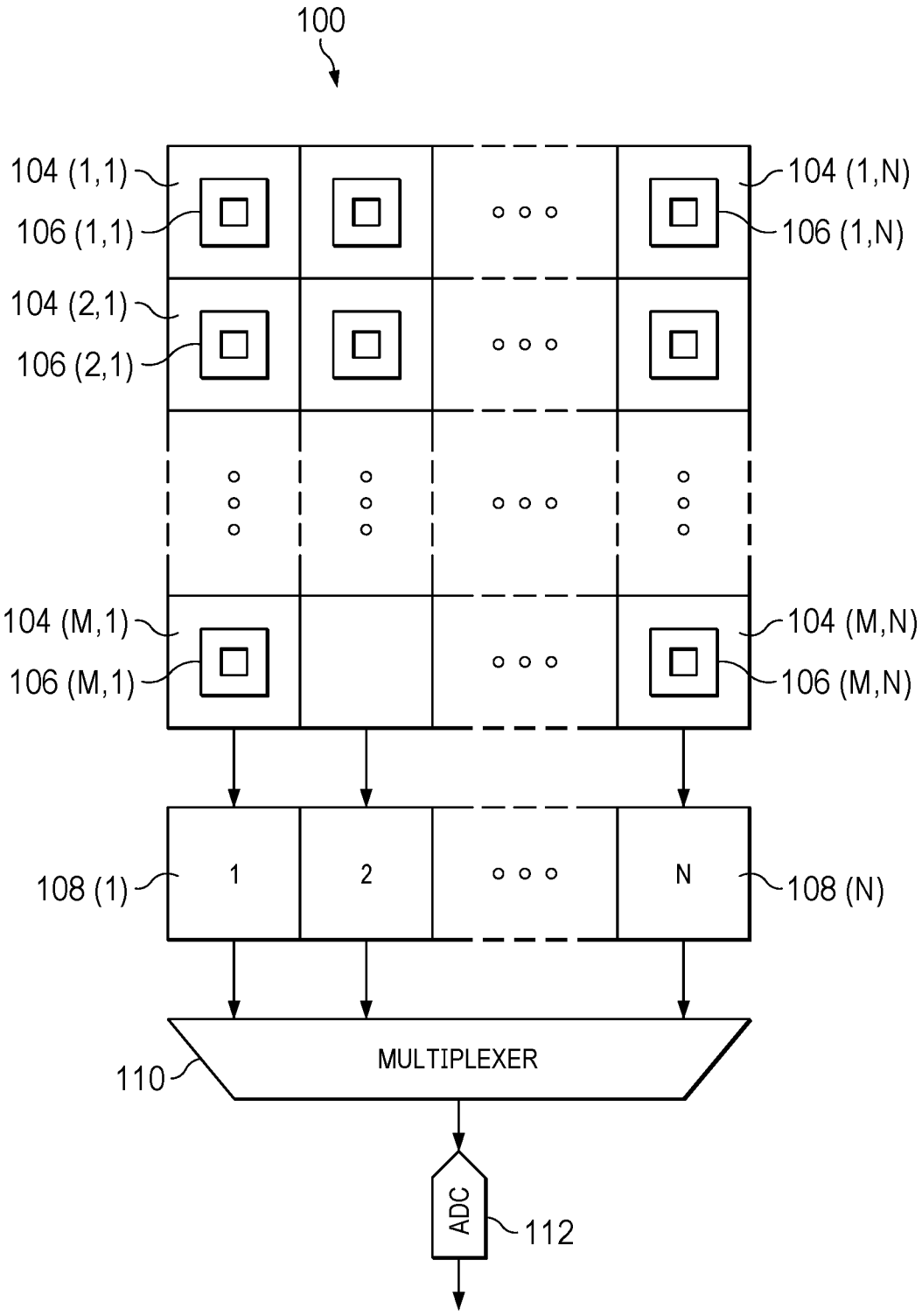

100
104 (1,1)
106 (1,1)
104 (1,N)
106 (1,N)
104 (2,1)
106 (2,1)
104 (M,1)
106 (M,1)
104 (M,N)
106 (M,N)
108 (1)
1
2
N
108 (N)
MULTIPLEXER
110
ADC
112

FIG. 1

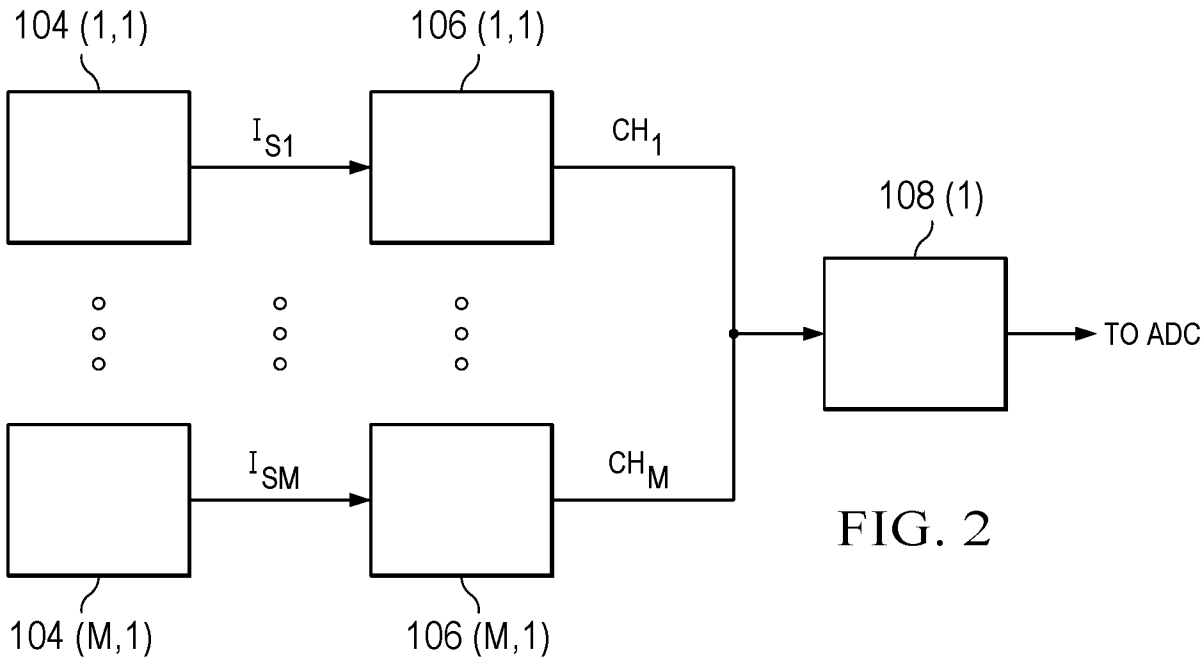
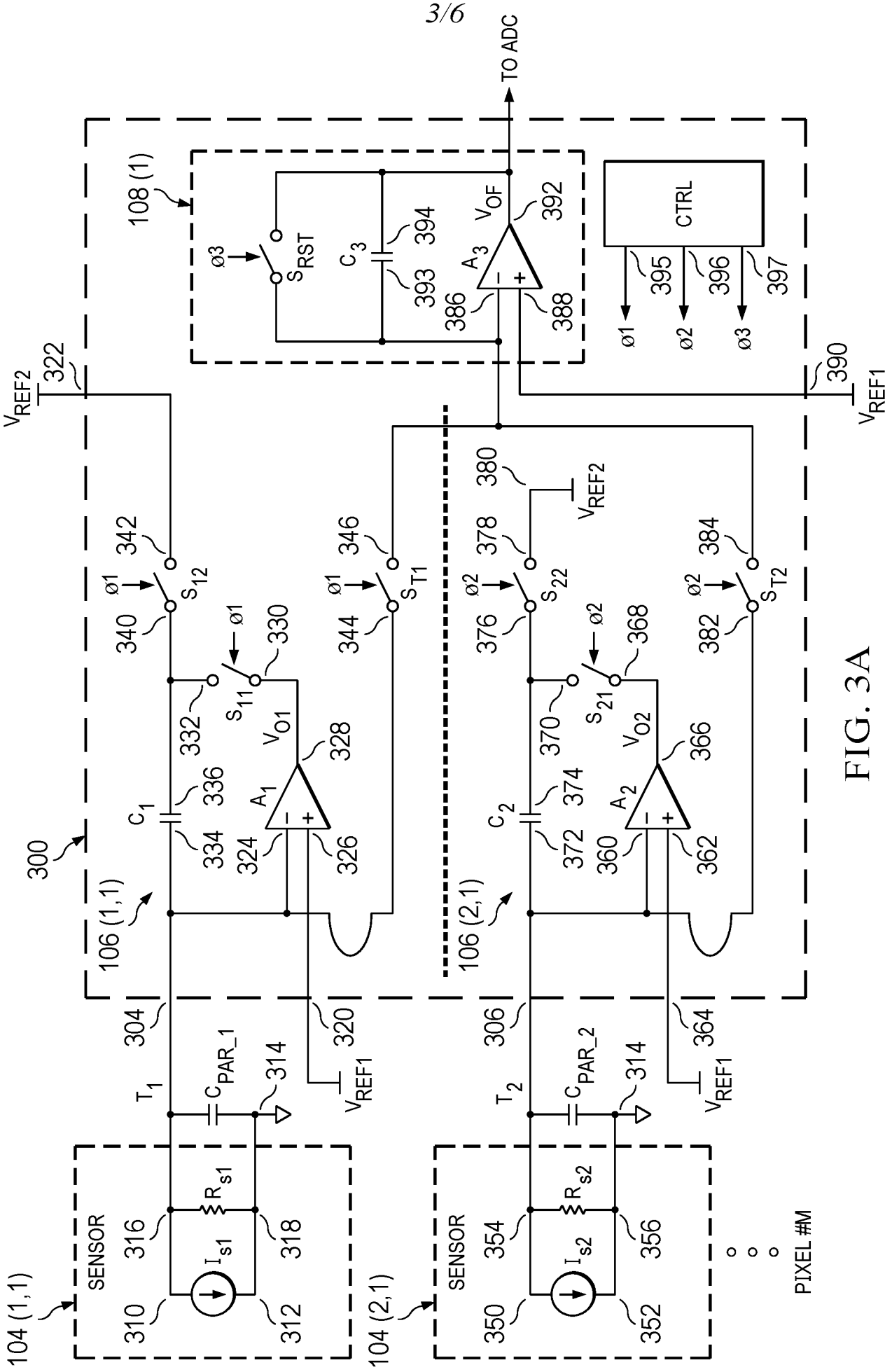


FIG. 2


TO ADC
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CTRL
ø1
ø2
ø3
395
396
397
S_{RST}
C_3
A_3
V_{OF}
392
394
393
386
388
V_{REF2}
322
V_{REF1}
390
300
106 (1,1)
106 (2,1)
S_{12}
S_{11}
S_{T1}
S_{22}
S_{21}
S_{T2}
C_1
C_2
A_1
A_2
V_{O1}
V_{O2}
V_{REF2}
V_{REF1}
T_1
T_2
C_{PAR_1}
C_{PAR_2}
104 (1,1)
104 (2,1)
SENSOR
R_{s1}
R_{s2}
I_{s1}
I_{s2}
PIXEL #M

FIG. 3A

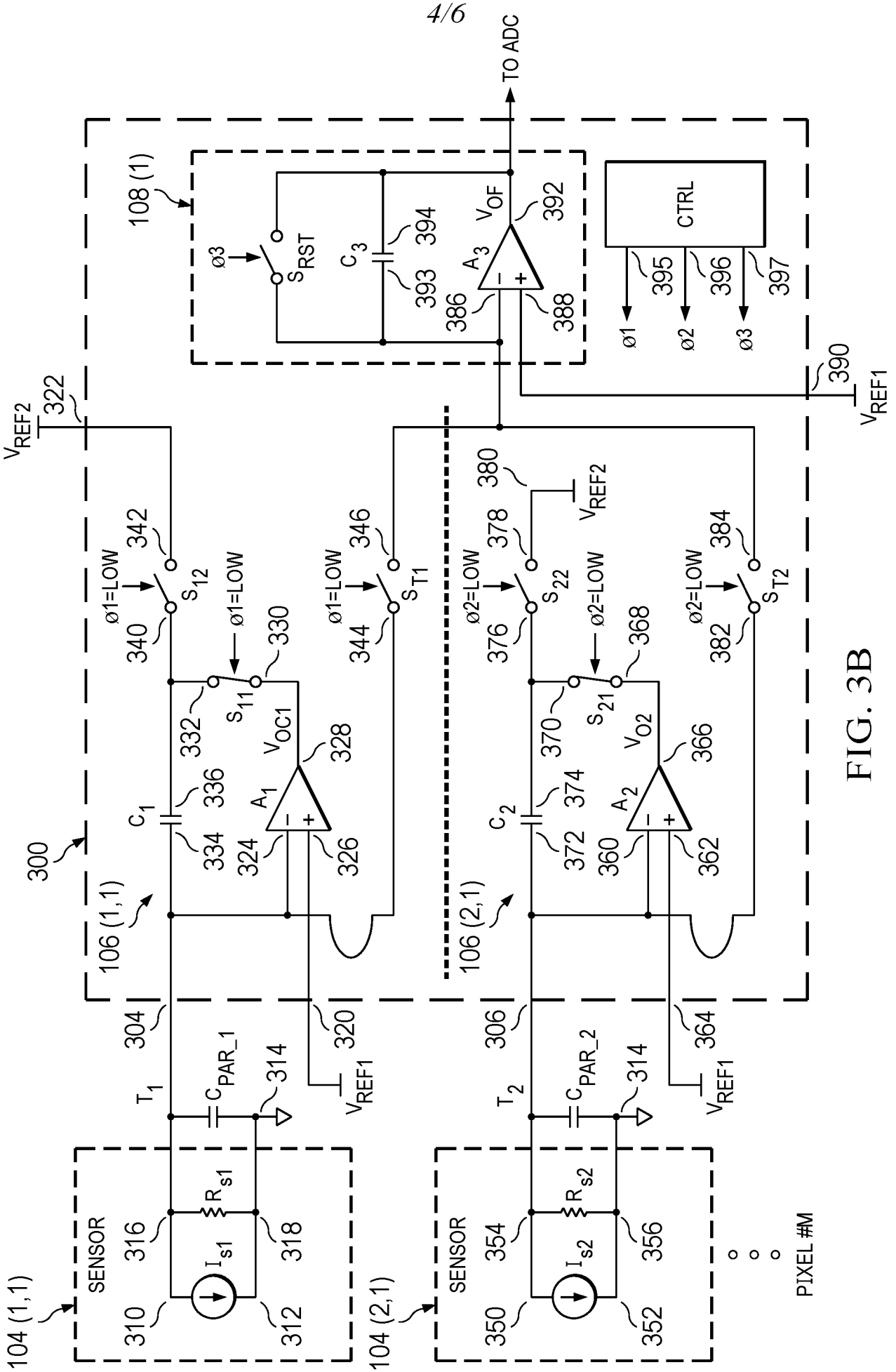
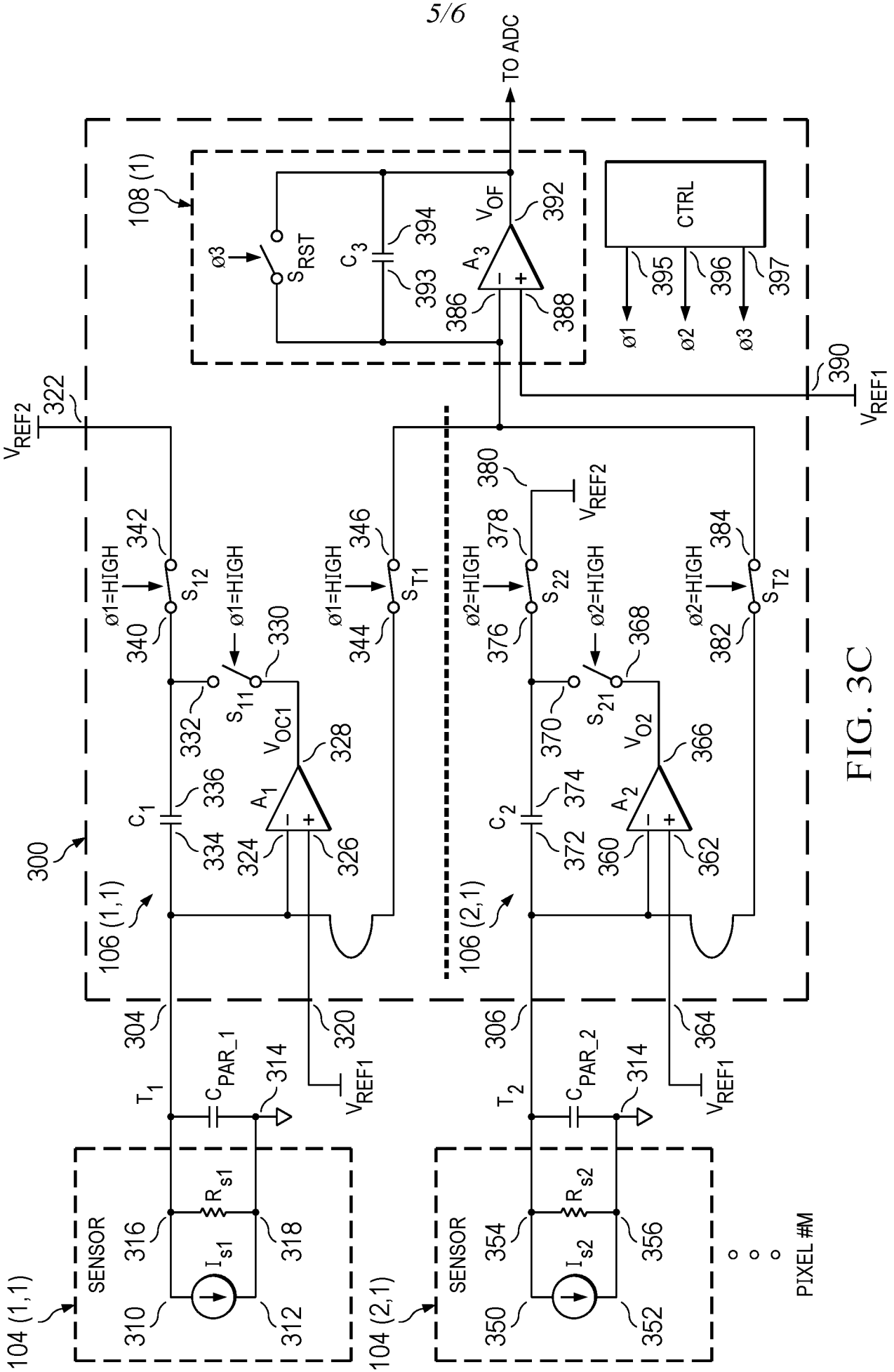

TO ADC
108 (1)
ø3
S_RST
C_3
394
393
A_3
V_OF
392
386
388
CTRL
395
396
397
ø1
ø2
ø3
390
V_REF1
V_REF2
322
300
106 (1,1)
106 (2,1)
ø1=LOW
342
S_12
340
330
S_11
332
V_OC1
328
C_1
336
334
A_1
324
326
346
S_T1
344
ø2=LOW
380
S_22
378
376
368
S_21
370
V_O2
366
C_2
374
372
A_2
360
362
384
S_T2
382
304
306
320
364
T_1
T_2
C_PAR_1
C_PAR_2
314
104 (1,1)
104 (2,1)
SENSOR
R_s1
R_s2
I_s1
I_s2
316
318
310
312
354
356
350
352
PIXEL #M

FIG. 3B


TO ADC
108 (1)
ø3
S_RST
C_3
394
393
A_3
V_OF
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386
388
CTRL
395
396
397
ø1
ø2
ø3
390
V_REF1
V_REF2
322
300
106 (1,1)
106 (2,1)
ø1=HIGH
342
S_12
340
330
S_11
332
C_1
336
334
V_OC1
328
A_1
324
326
346
S_T1
344
ø2=HIGH
380
S_22
378
376
368
S_21
370
C_2
374
372
V_O2
366
A_2
360
362
384
S_T2
382
304
306
320
364
T_1
T_2
C_PAR_1
C_PAR_2
314
V_REF1
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104 (2,1)
SENSOR
316
318
R_s1
I_s1
310
312
354
356
R_s2
I_s2
350
352
PIXEL #M

FIG. 3C

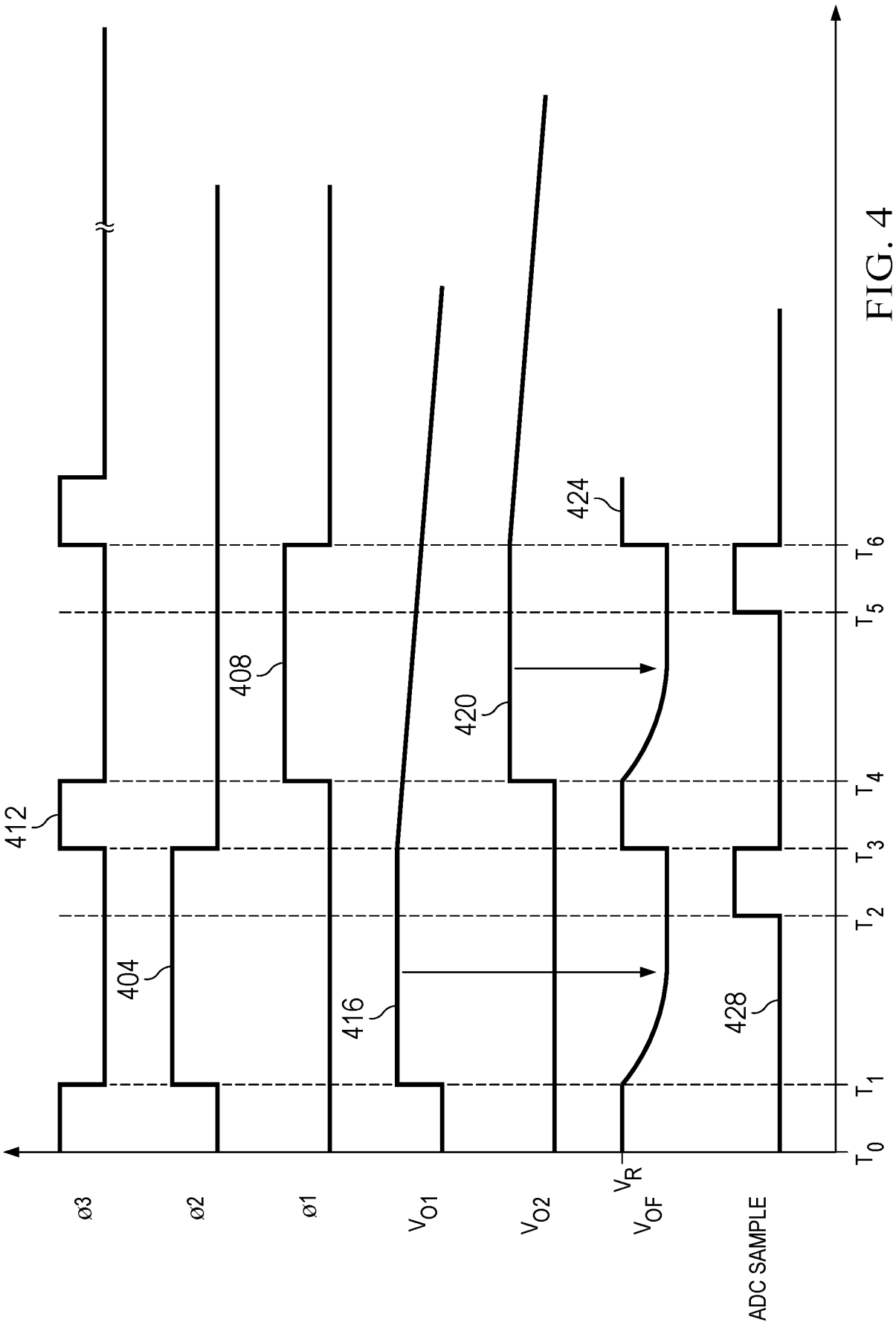
ø3
ø2
ø1
V_{O1}
V_{O2}
V_R
V_{OF}
ADC SAMPLE
T_0
T_1
T_2
T_3
T_4
T_5
T_6
404
408
412
416
420
424
428

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2023/033844

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/70
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 10 984 732 B2 (APPLE INC [US]) 20 April 2021 (2021-04-20) figure 10 column 1, line 1 - column 12, line 53	1-17
X A	JP 3 464228 B2 (APPLE) 5 November 2003 (2003-11-05) figure 3	1-8, 15-17 9-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 February 2024	20/02/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jespers, Michaël

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2023/033844

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 10984732 B2	20-04-2021	NONE	
JP 3464228 B2	05-11-2003	EP 0974119 A1	26-01-2000
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		WO 9845798 A1	15-10-1998