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(54) INTEGRATION CMOS COMPATIBLE OF MICRO/NANO OPTICAL GAIN MATERIALS

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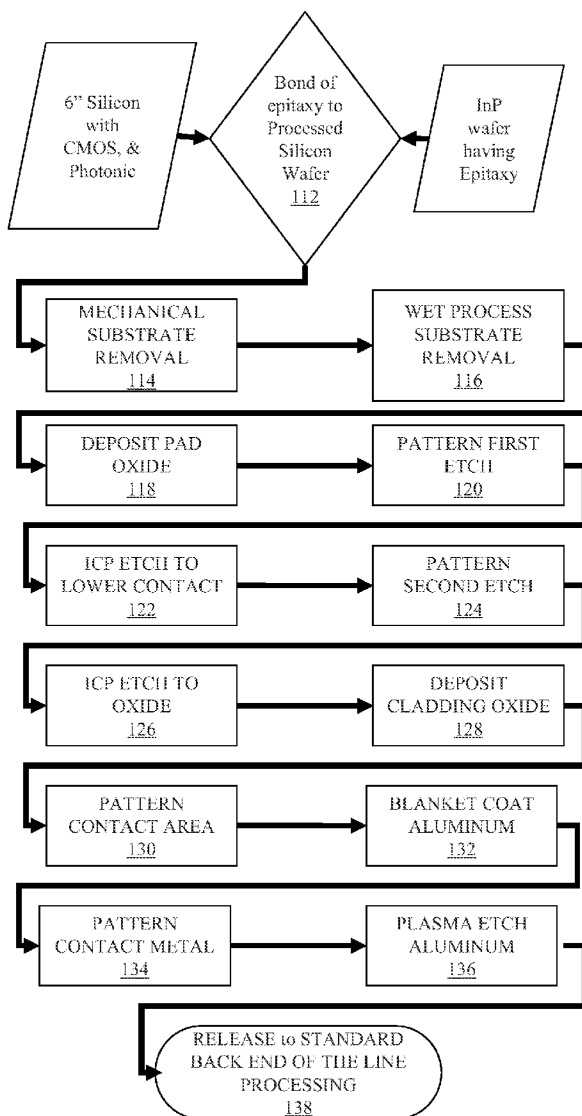
(57) **ABSTRACT**

A method is provided for the integration of an optical gain material into a Complementary metal oxide semiconductor device, the method comprising the steps of: configuring a workpiece from a silicon wafer upon which is disposed an InP wafer bearing an epitaxy layer; mechanically removing the InP substrate; etching the InP remaining on epitaxy layer with hydrochloric acid; depositing at least one Oxide pad on revealed the epitaxy layer; using the Oxide pad as a mask during a first pattern etch removing the epitaxy to an N level; etching with a patterned inductively coupled plasma (ICP) technique; isolating the device on the substrate with additional pattern etching patterning contacts, applying the contacts.



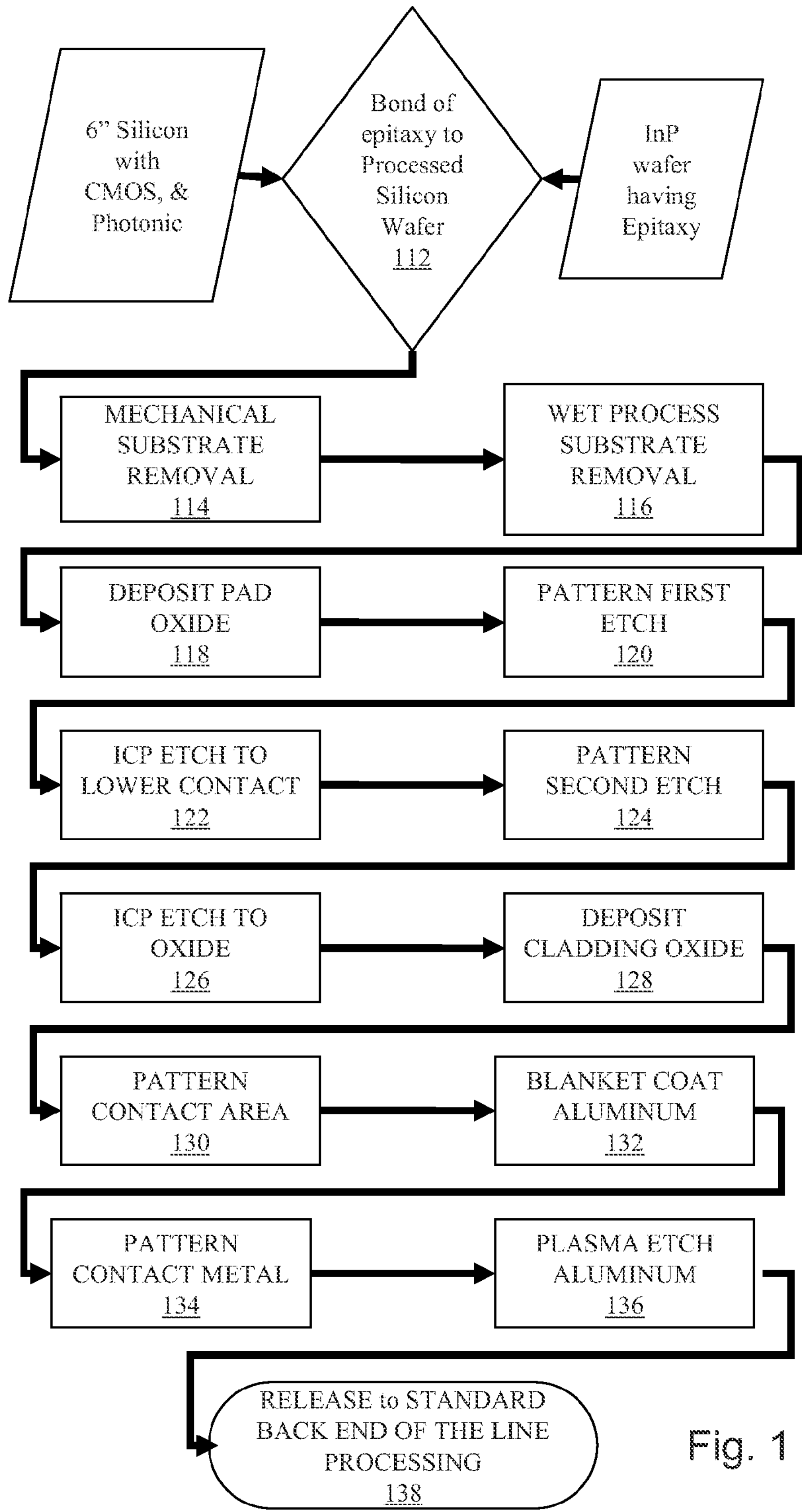
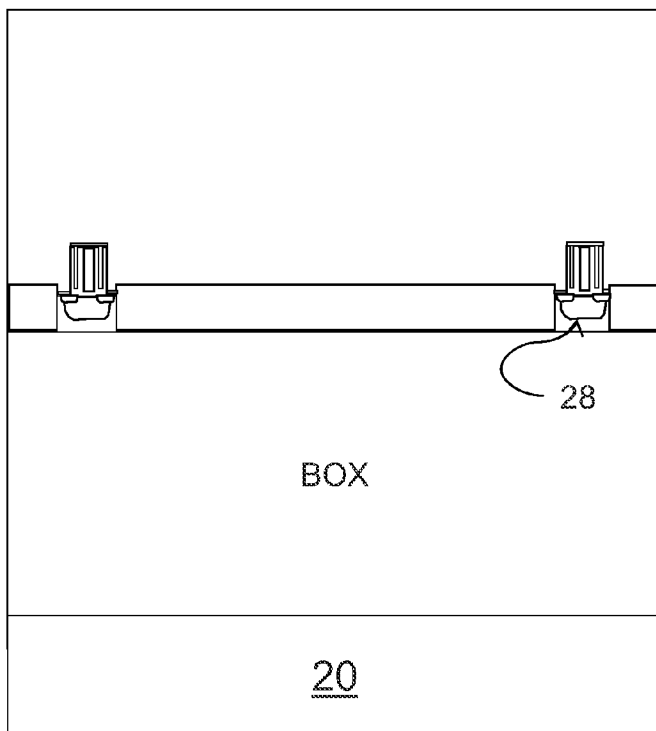
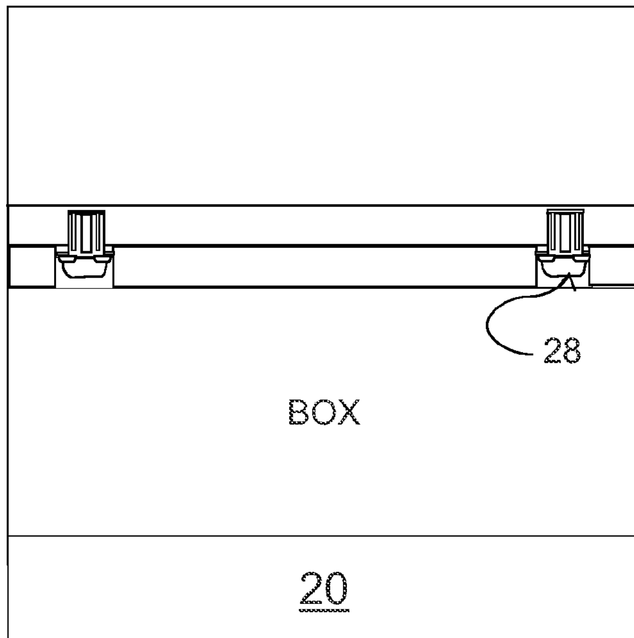


Fig. 1



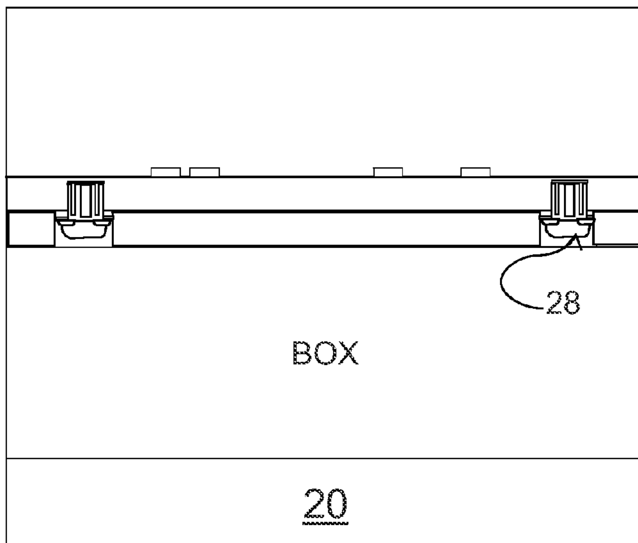
Starting from just after contact and gate salicidation step

Fig. 2A



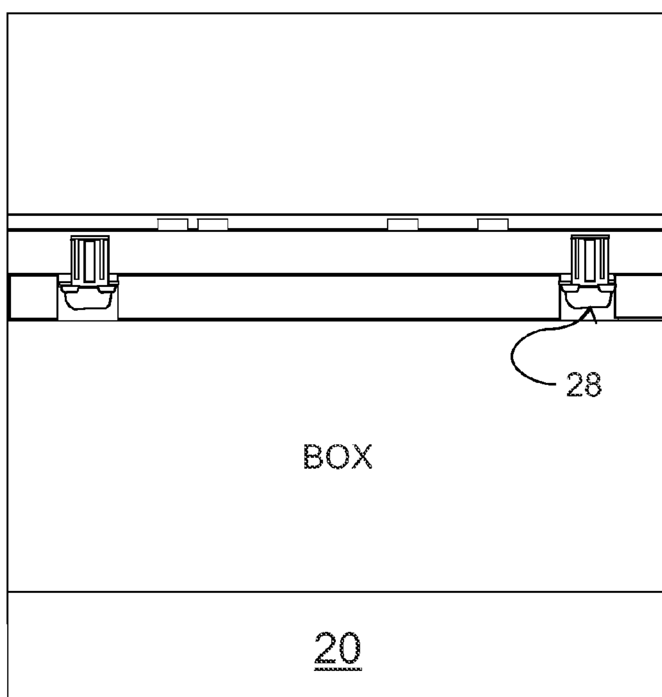
Dielectric Deposition and CMP to re-planerize surface

Fig. 2B



Deposit and Etch deposited silicon waveguide material.

Fig. 2C



Deposit SIO2 and CMP Back to near top of guide.

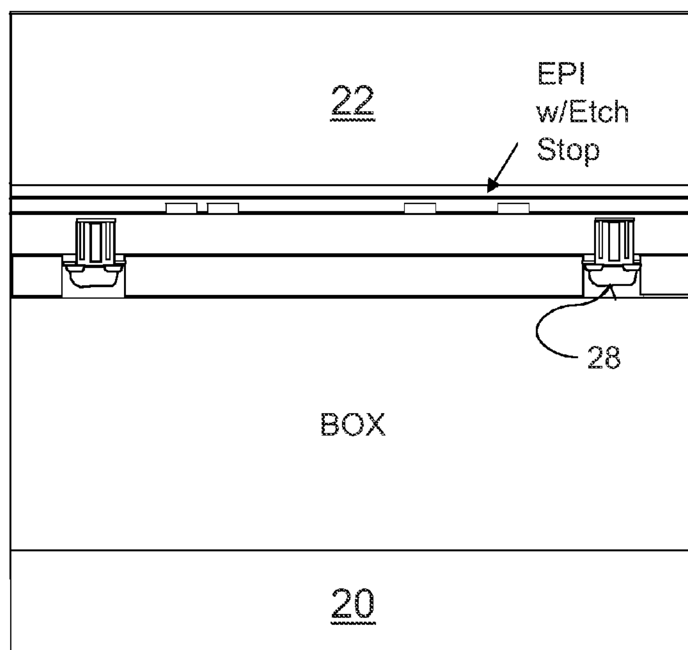
(Deposit coupling, bond layer of SIO2. or leave enough SiO2 surface to ensure bond.)

Fig. 2D

Ziptronix bond of InP Epi Materials,

Bond diced materials to allow improved alignment and work within bounds of exsisting InP substrate material, will also allow different materials to be bonded to the different die on the same wafer facilitating a wider range of testable structures.

Fig. 2E



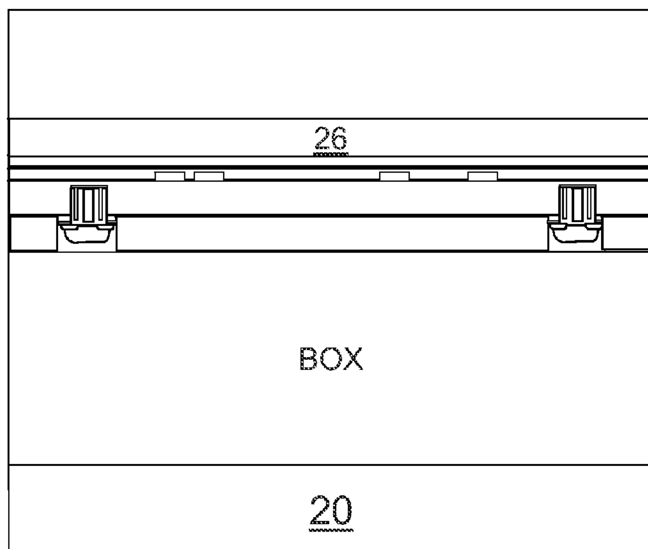
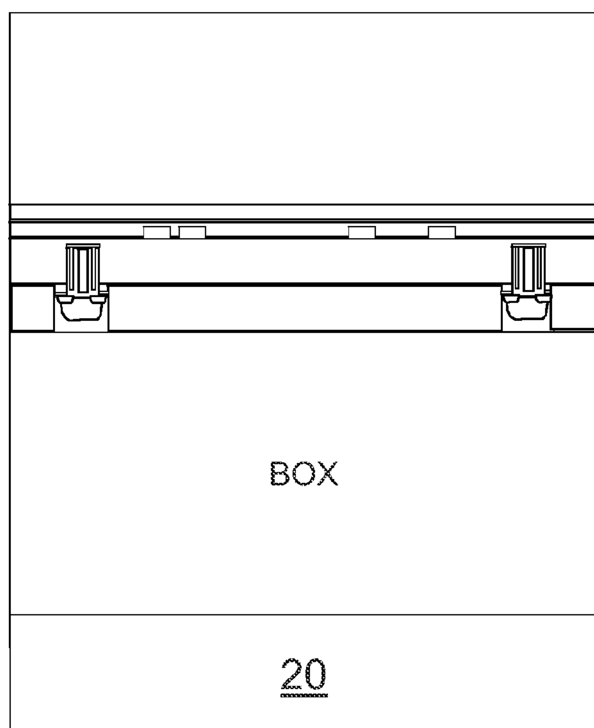


Fig. 2F



A HCL based etch is used to remove remaining InP substrate to InGaAs etch stop.

(HCL should not erode remaining SiO2 Surface.)

Fig. 2G

Epitaxy is patterned and etched (2 step, 1st to lower contact 2nd for Isolation

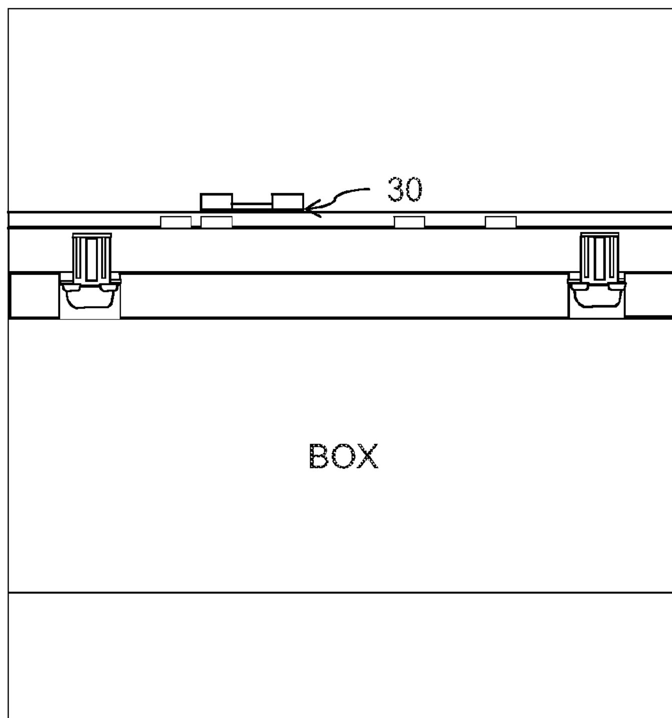


Fig. 2H

Top Contact, spacer (if needed) and lower contact Metals are applied

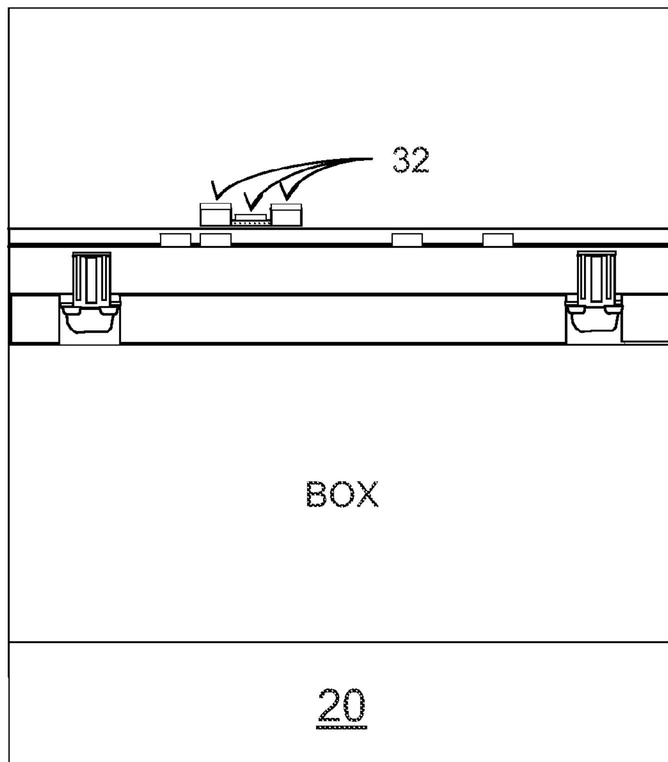


Fig. 2I

Cladding oxide is applied and planerised.

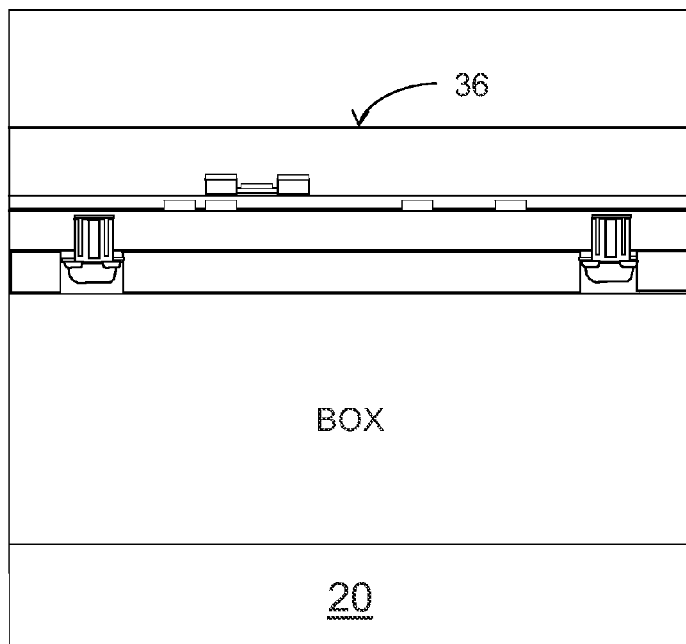
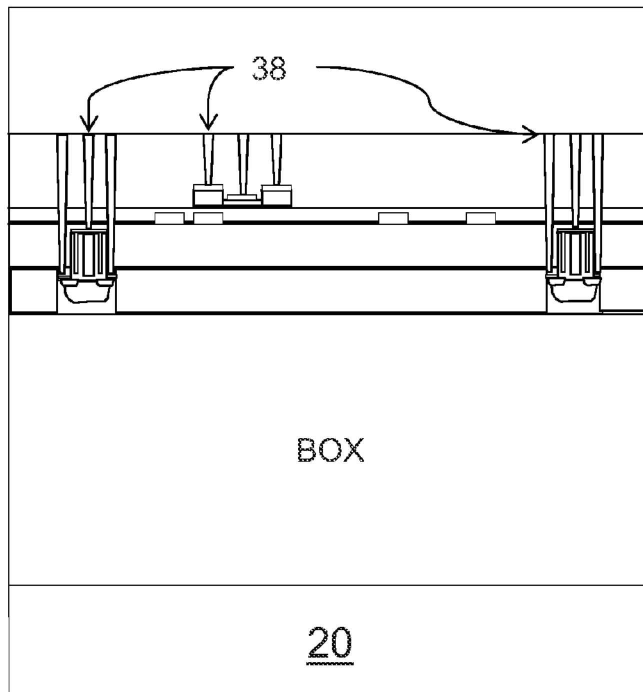


Fig. 2J



Vias are cut, Filled and Polished. (Employ 2 layers of via)

Fig. 2K

Deposit and cut
Metal 1

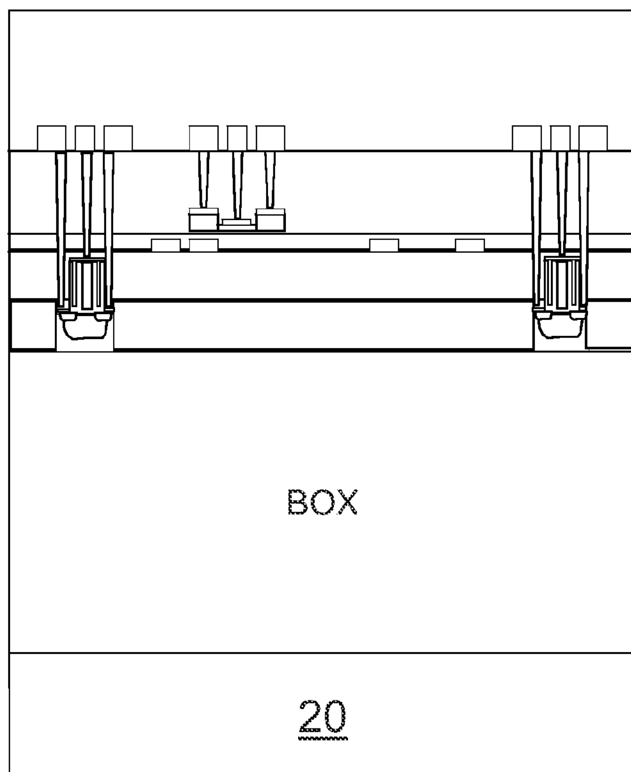


Fig. 2L

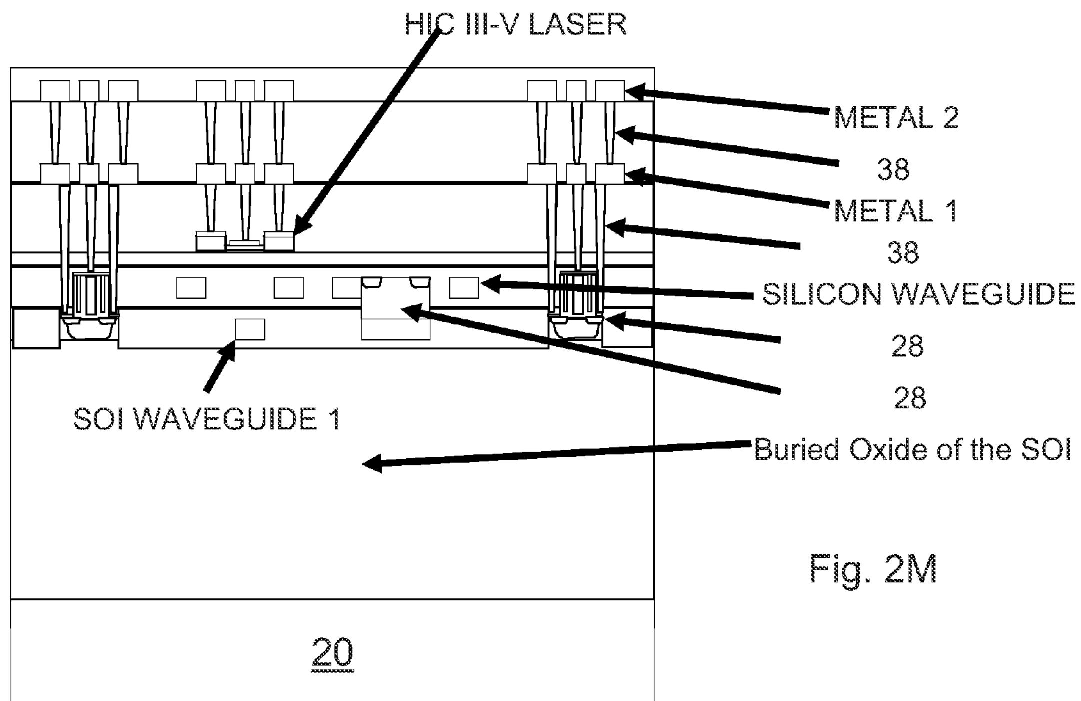


Fig. 2M

INTEGRATION CMOS COMPATIBLE OF MICRO/NANO OPTICAL GAIN MATERIALS

RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 12/201618, filed Aug. 29, 2008. This application is herein incorporated by reference in its entirety for all purposes.

FIELD OF THE INVENTION

[0002] The invention relates to micro/nano gain materials, and more particularly, to the integration thereof into complementary metal oxide semiconductor devices.

BACKGROUND OF THE INVENTION

[0003] Integrated optical systems, such as optical bus architectures and ultra-stable nano RF local oscillators are composed of fundamental device structures requiring improved integrated optical gain materials. In the past, InGaAlAs/InGaAs laser structure have been over looked as laser materials because as the TM and TE absorption is roughly equal and while it demonstrates exceptional gain for photons absorbed through the TE mode, the gain through TM absorption is zero. While in traditional configurations, this would be detrimental in the formation of lasers and amplifiers having a standard geometry, in a highly confined optical environment in which the TE can be selectively guided this becomes a significant advantage.

SUMMARY OF THE INVENTION

[0004] One embodiment of the present invention will provide an InGaAlAs/InGaAs laser structure to achieve a unique integrated gain structure.

[0005] One embodiment of the present invention provides a method for the integration of an optical gain material into a Complementary metal oxide semiconductor device, the method comprising the steps of: configuring a workpiece from a silicon wafer upon which is disposed an InP wafer bearing an epitaxy layer; mechanically removing the InP substrate; etching the InP remaining on epitaxy layer with hydrochloric acid; depositing at least one Oxide pad on revealed epitaxy layer; using the Oxide pad as a mask during a first pattern etch removing the epitaxy to an N level; etching with a patterned inductively coupled plasma (ICP) technique; isolating the device on the substrate with additional pattern etching patterning contacts, applying the contacts.

[0006] Another embodiment of the present invention provides such a method further comprising planarization of the epitaxy layer.

[0007] A further embodiment of the present invention provides such a method further comprising bonding the epitaxial surface to the silicon wafer.

[0008] The features and advantages described herein are not all-inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and not to limit the scope of the inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a flow chart illustrating a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0010] FIG. **2**A is an elevation view of CMOS substrate illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0011] FIG. **2**B is an elevation view of planarization of a surface of a CMOS substrate illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0012] FIG. **2**C is an elevation view of CMOS substrate and silicon waveguides illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0013] FIG. **2**D is an elevation view of CMOS substrate and planarized waveguides illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0014] FIG. **2**E is an elevation view of CMOS substrate and InP Epitaxy layer illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0015] FIG. **2**F is an elevation view of CMOS substrate and mechanically thinned InP Epitaxy layer illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0016] FIG. **2**G is an elevation view of CMOS substrate and InGaAs etch stop layer illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0017] FIG. **2**H is an elevation view of CMOS substrate and etched Epitaxy layer illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0018] FIG. **2**I is an elevation view of CMOS substrate and etched Epitaxy layer with top contacts illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0019] FIG. **2**J is an elevation view of CMOS substrate and cladding oxide illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0020] FIG. **2**K is an elevation view of CMOS substrate and with vias cut in a cladding oxide layer illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0021] FIG. **2**L is an elevation view of CMOS substrate and metal deposition illustrating a step in a method for the integration of a gain material configured in accordance with one embodiment of the present invention.

[0022] FIG. **2**M is an elevation view of a CMOS device with integrate gain material configured in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0023] In one embodiment, a InGaAlAs/InGaAs complementary metal oxide semiconductor (CMOS) compatible micro/nano optical gain material is provided for integration into a CMOS device. Such a gain material may be utilized in an environment with a high level of optical and electrical confinement.

[0024] The crystal structure of such a gain material provides good conversion efficiency within the small volume devices and low material absorption due to the InGaAlAs guiding and contacting structure and the low loss guiding structure combined with the highly confined Transverse Electric (TE) only optical structures has additional benefits in regards to the interaction (absorption) cross section of the optical field and quantum well and the low loss TE nature of the fabricated devices. In addition to its outstanding optical properties, this material system provides excellent ohmic contact with aluminum based CMOS metallization allowing for efficient current injection while ensuring adherence to a CMOS compatible process.

[0025] There are many advantages to the use of InGaAlAs gain material. For example, the interfaces between epitaxial layers can be tailored to be more abrupt for AlGaInAs since there is only one group V element to control. For this same reason, it is also easier to grow graded layers in this system. Interfaces between graded layers are also thermally stable which is not the case for competing GaInAsP materials. This is critical for the formation of optical structures that must endure the post processing of a CMOS process. This ability to handle high-temperature processing steps, such as plasma deposition, diffusion, and annealing are key to the development of a reliable optical gain material that can be integrated as part of the overall epic process.

[0026] The InGaAlAs quaternary alloys are also better suited to conventional Molecular Beam Epitaxy (MBE) than InGaAsP due to lack of reliable phosphorous solid or gas source. By employing MBE the user is able to better control the material composition and configuration of very thin epitaxial structures than would be possible with Metalorganic vapour phase epitaxy (MOCVD), although one skilled in the art will appreciated that this technique may be employed in some embodiments of the present invention. This level of control is important to the goal of achieving a combination of controlled gain as well as material thickness from our devices allowing us to develop uniform devices having characterizable performance.

[0027] The use of quaternaries has benefits over the simpler ternary InAlAs/InGaAs systems in that they have a larger range of lattice matched energies and can be used to maximize the conduction and valance band offsets. The larger conduction band offset of the InGaAlAs system has the following benefits:

- **[0028]** For a given emitting wavelength, larger well thickness can be used in the InGaAlAs/InGaAs system leading to a greater optical absorption;
- **[0029]** Interfaces at the well can be made very abrupt because there is only one group V element that has to be controlled at the transition; and
- **[0030]** The InGaAlAs/InGaAs system provides better confinement of the free electron gas in the wells leads to higher optical gain per well, by decreasing the gain broadening due to coupling between electron levels from well to well, and by reducing the electron spill out from the wells into the optical guiding region at high injection levels.

[0031] One embodiment of the presentation provides an approach for molecular bonding allowing the active photonic material to be combined with the existing photonic silicon and germanium devices in a single cohesive semiconductor fabrication process.

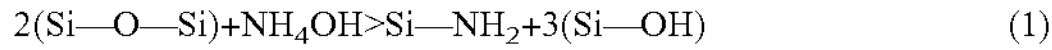
[0032] As illustrated in FIG. **1**, a flowchart of a process for the manufacture of a laser utilizing the gain material of one embodiment of the present invention. In one embodiment of the present invention, a workpiece is configured from a silicon wafer upon which is disposed CMOS and optical components and an InP wafer bearing an epitaxy **112**. The InP substrate is removed **114** mechanically, and the remaining InP is etched **116** from the epitaxy the using HCl. Oxide pads are deposited on the revealed epitaxy layer **118**. The Oxide pads act as masks during a first pattern etch removing the epitaxy to the N level **120**. Etching continues using a patterned Inductively Coupled Plasma (ICP) technique and additional pattern etching to isolate the device on the substrate (**122**-**126**). A cladding oxide is applied **128**. Contacts are patterned **130** and applied **132**, **134**, **136** and the resulting device is treated according to standard back end processing techniques **138**.

[0033] A similar embodiment is illustrated in FIGS. **2**A-**2**M, block diagrams illustrating the stages of construction of an integrated gain device. In such an embodiment, a starting structure or workpiece, in one embodiment a 6 inch Silicon CMOS and Photonics wafer **20**, is prepared, upon which an InP wafer **22** bearing an epitaxy **24** to the processed silicon wafer is performed. One skilled in the art will appreciate that depending on the devices **28** disposed on the CMOS wafer **20** planarization steps may be required before bonding of the epitaxy **24** to the wafer **20**. The workpiece having the wafer **20**, epitaxy **24** and InP layer **22** is then mechanically processed to remove substrate to a flat surface **26**, in one embodiment this involves mechanically reducing the thickness of the InP **22** layer to 20 μm. After the InP layer **22** has been mechanically thinned, wet etching with HCl of the InP is carried out to remove the layer in its entirety exposing the epitaxy layer **24** etch stop. This epitaxy **24** is then patterned and etched further to first create a desired contact **32** and then to isolate the structure **30**. The structure **30** is then metallized to create metal contacts **34** for the device **30**. The structure **30** and is then coated with cladding oxide layers **36**, in one embodiment SiO. This cladding **36** is then planarlized, vias **38** are cut filled and processed. The resulting structure is integrated in to a chip upon which may be disposed other devices **28**, and interconnections such as vias and waveguides may be made to the gain device configured according to one embodiment of the present invention.

[0034] Such an embodiment employs existing photonic processing capabilities such as oxide deposition and Chemi-Mechanical polish (CMP) to provide a clean planar bond interface and ensure that the planarization is sufficient to deflect bonded wafer or die to eliminate any gaps resulting from direct contact between two surfaces with nonzero surface bow, warp, planarity, or roughness. The typical planarization specification of (10 nm/100 μm and 0.5 nm RMS) is well known to those skilled in the art.

[0035] Known processes will be combined with a surface activation process to modify the surface of one or both of the surfaces to be bonded. This chemical process consists of a standard RCA clean including a Sulfuric acid/Hydrogen peroxide etch and oxygen/Argon plasma process to remove organics from the surface. Following this, in order to achieve a strong bond at low temperatures one embodiment of the present invention will treat the surfaces prior bonding so that they are terminated by species that produce less or no water during the required polymerization reactions that occur during the interaction at the two surfaces.

[0036] One embodiment of the present invention provides SiO_2 surfaces treated in ammonium hydroxide (NH_4OH) solution prior to room-temperature bonding which can yield a stronger bond at low temperatures than those receiving only a standard RCA clean. The treated SiO_2 surfaces are terminated mainly by NH_2 and OH groups after the treatment:

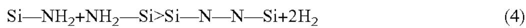


$$2(Si—O—Si)+NH_4OH>Si—NH_2+3(Si—OH) \quad (1)$$

[0037] During room-temperature bonding, clusters of two or three NH_3 or HOH molecules will bridge between NH_2 or OH groups on the two mating surfaces. We will then employ low-temperature annealing to displace the NH_3 and HOH molecules. During this thermal step the following three reactions take place:

$$Si—OH+HO—Si< >Si±O±Si+HOH \quad (2)$$

$$Si—NH_2+OH—Si>Si—O—Si+NH_3 \quad (3)$$



$$Si—NH_2+NH_2—Si>Si—N—N—Si+2H_2 \quad (4)$$

[0038] The hydrogen produced in Reaction 4 can diffuse away or dissolve in the surrounding oxide, and the strong Si—N bonds will remain. Overall, the three reactions result in a higher bonding energy of SiO_2SiO_2 bonded pairs after annealing at low temperatures (e.g., 150° C.) than for standard RCA-treated SiO_2SiO_2 bonded pairs. Once the CMOS surface has been prepared with this process, it is ready to accept placement of the epitaxy chiplet or wafer. Bonding, in one embodiment, is carried out in normal foundry ambient without need of a vacuum or inert gas environment. No applied pressure or electric field are used the surfaces are simply brought into contact. For wafer to wafer bonding from 4" to 8", the bond forms within seconds. For die to wafer applications, the bond is essentially instantaneous, enabling compatibility with conventional high-speed pick and place.

[0039] In one embodiment a laser diode is provided having an electromagnetic mode on the order of the size of the device, as such the horizontal and vertical confinement of optical and electrical field. Such features are not required in conventional laser design since such conventional lasers typically operate in a propagation mode where the operational wavelength is much smaller than the cavity.

[0040] In one embodiment of the optical gain material of the present invention, the confinement of the optical mode is provided by the use of materials having large variations not only in their index of refraction, but conductivity. This allows confinement of the electric field, allowing greater control over the interaction of electronic carriers with the active volume of our gain materials.

[0041] One embodiment of the present invention may be deployed in low power integrated micro-ring lasers that will employ a ring resonator format. Semiconductor ring resonator lasers offer a range of advantages over other geometries that require facets or other physical methods for optical feedback. These include:

[0042] Ease of integration, a lack of spatial hole burning due to traveling-wave operation and narrow line width single mode operation with high side mode rejection.

[0043] Operation with the lowest possible dimensional system enabling extremely strong confinement of the optical fields to a ridge waveguide structure with strong lateral guiding.

[0044] The continuous ring waveguide eliminates the need for any other optical feedback mechanism.

[0045] Semiconductor quantum well lasers that incorporate these low-dimensional photonic structures are far more efficient than the conventional laser structures because of a modification of the photonic density of states that enhances both the spatial and spectral coupling of spontaneous emissions into the desired lasing waveguide mode which we will control based on the high confinement nature of our optical integration scheme.

[0046] This coupling to the lasing modes is related as a constant referred to as the beta factor. The beta factor for our micro ring laser could be as large as 1, compared with 10-5 for conventional edge-emitting laser. This large beta value represents an increase in the effective gain of the cavity, making it possible to achieve lasing in a small cavity while maintaining a low lasing threshold.

[0047] For the modification of beta to be significant, the photons must be strongly confined. This can be achieved using strongly guided waveguides with cross-sectional dimensions smaller than an optical wavelength. Because of the strong guiding, very small cavities and micro-ring structures can be realized without significant bending losses. Additionally, light can be guided from one device to another evanescently, or transferred from one to another by waveguide coupling, eliminating the need for cleaved mirrors. These factors, together with their small size and low-threshold operation of micro-cavity lasers will enable the realization of ultra-high density photonic integrated circuits or VLSI photonics.

[0048] Some additional benefits of our micro-ring laser approach are:

[0049] Passive ring-resonator devices are good for wavelength filtering, routing, switching, modulation, and multiplexing/demultiplexing applications, an active stage ring would enable the compensation for losses in these structures.

[0050] Ring resonators do not require facets or gratings for optical feedback, making them particularly suited for monolithic integration with other components.

[0051] Adding gain to a ring resonator increases this scope by an order of magnitude adding massively scalar optical logic function, analog to digital conversion in the optical domain and enhanced optical signal processing.

[0052] Gain compensates for losses, increasing (multiplying) the Q of the resonator to unbelievably high numbers (millions, 10's of millions).

[0053] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

1. An optical gain material, the material comprising:

an InGaAlAs layer;

an InGaAsP layer disposed proximally to said InGaAlAs layer.

2. An integrated gain device, said device comprising;

an InGaAlAs/InGaAsP epitaxy layer;

a silicon substrate upon which said InGaAlAs/InGaAsP is disposed;

* * * * *